DATA SHEET

TDA8769
12-bit, 60/80/105 Msps Analog-to-Digital Converter (ADC) Nyquist/high IF sampling

Objective specification
Supersedes data of 2003 Apr 07

2003 Dec 09

Philips Semiconductors

PHILIPS

12-bit, 60/80/105 Msps Analog-to-Digital Converter (ADC) Nyquist/high IF sampling

TDA8769

CONTENTS

12-bit, 60/80/105 Msps Analog-to-Digital Converter (ADC) Nyquist/high IF sampling

TDA8769

1 FEATURES

- 12-bit resolution
- Optimized for both Nyquist and high IF sampling
- High-speed sampling rate up to 105 MHz
- Maximum analog input frequency of 330 MHz (see Application section)
- Only 2 clock cycles latency
- 5 V power supplies and 3.3 V output power supply
- Binary or two's-complement CMOS outputs
- Programmable Complete Conversion Signal (CCS) CMOS output
- In-range CMOS compatible output
- CMOS compatible static digital inputs
- LVTTL and LVCMOS compatible digital outputs
- Differential clock input PECL; sine wave and TTL compatible
- Integrated track-and-hold amplifier
- Differential analog input
- External amplitude range control
- Full-scale controllable from 1.5 to 1.9 V (p-p)
- Voltage controlled regulator included
- Temperature range from –40 to +85 °C.

2 APPLICATIONS

- Cellular infrastructure (2.5G, 3G, etc.)
- Base stations and "Zero-IF" or direct IF sampling subsystems
- Wireless and wired broadband communications
- Wireless Local Loop (WLL)
- Local Multipoint Distribution Service (LMDS)
- Advanced Frequency Modulation (FM) radio
- Imaging (camera scanner and medical)
- Cable modem or set top box
- Radar and satellite hub systems.

3 GENERAL DESCRIPTION

The TDA8769 is a BiCMOS 12-bit Analog-to-Digital Converter (ADC) optimized for GSM/EDGE, W-CDMA and CDMA2000 radio transceivers, high data rate radios and other applications such as advanced FM radio and professional imaging. Its main innovation is the RF sampling, based on a high-speed clock of up to 105 Msps combined with high input frequencies of up to 250 MHz. It converts the analog input signal into 12-bit binary coded digital words at a maximum sampling rate of 105 MHz.

The TDA8769 analog performances have been proven in various multi-carrier 3G radio receivers, providing the best-in-class Adjacent Channel Selectivity (ACS) up to 80 dB.

Moreover the TDA8769 offers the lowest clock cycle latency, which enables competitive and optimized feedback loops in controlled systems.

All static digital inputs (TH, CEN, OTC, DEL0 and DEL1) are CMOS compatible and all outputs are LVTTL and LVCMOS compatible. A sine wave clock input signal can also be used.

4 QUICK REFERENCE DATA

Tbf.

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8769HW/6	HTQFP48	plastic thermal enhanced thin quad flat package; 48 leads; body $7 \times 7 \times 1.0$ mm; heatsink	SOT545-2	60
TDA8769HW/8				80
TDA8769HW/10				105

6 BLOCK DIAGRAM

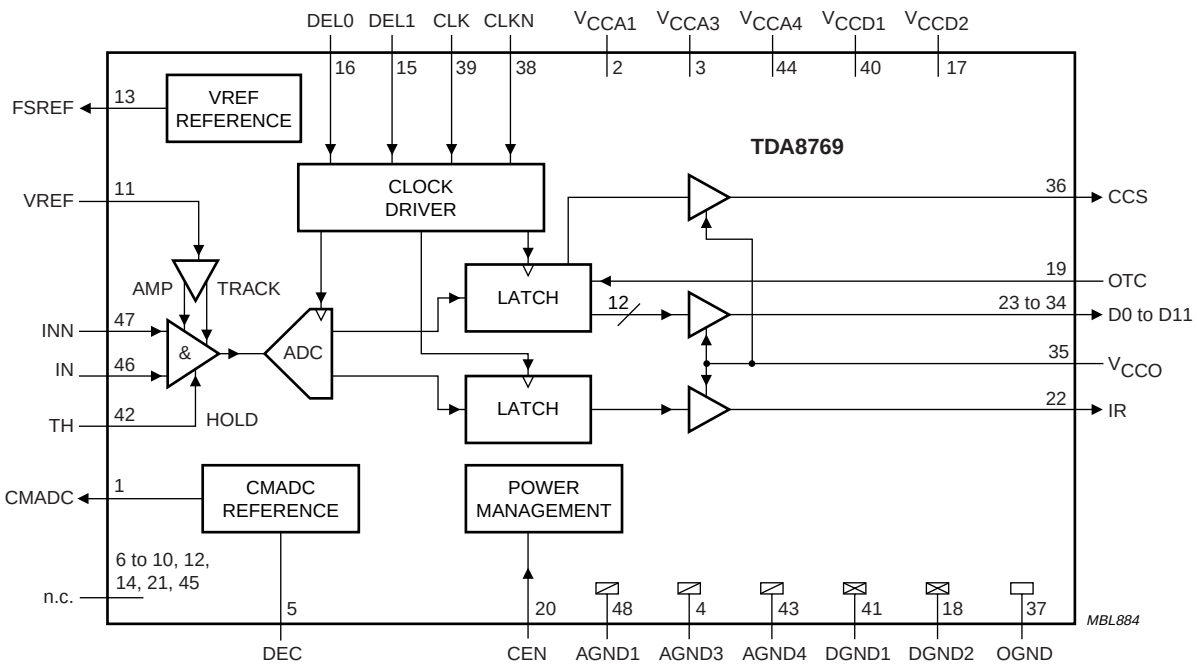


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	TYPE(1)	DESCRIPTION
CMADC	1	O	regulator output common mode ADC output
V_{CCA1}	2	P	analog supply voltage 1 (5.0 V)
V_{CCA3}	3	P	analog supply voltage 3 (5.0 V)
AGND3	4	G	analog ground 3
DEC	5	I/O	decoupling node
n.c.	6	–	not connected
n.c.	7	–	not connected
n.c.	8	–	not connected
n.c.	9	–	not connected
n.c.	10	–	not connected
VREF	11	I	reference voltage input
n.c.	12	–	not connected
FSREF	13	O	reference output
n.c.	14	–	not connected
DEL1	15	I	complete conversion sampling delay input 1
DEL0	16	I	complete conversion sampling delay input 0
V_{CCD2}	17	P	digital supply voltage 2 (5.0 V)

SYMBOL	PIN	TYPE[1]	DESCRIPTION
DGND2	18	G	digital ground 2
OTC	19	I	control input two's complement output (active HIGH)
CEN	20	I	chip enable input (CMOS level; active LOW)
n.c.	21	–	not connected
IR	22	O	in-range output
D11	23	O	data output bit 11 (MSB)
D10	24	O	data output bit 10
D9	25	O	data output bit 9
D8	26	O	data output bit 8
D7	27	O	data output bit 7
D6	28	O	data output bit 6
D5	29	O	data output bit 5
D4	30	O	data output bit 4
D3	31	O	data output bit 3
D2	32	O	data output bit 2
D1	33	O	data output bit 1
D0	34	O	data output bit 0 (LSB)
V_{CCO}	35	P	supply voltage of data output (3.3 V)
CCS	36	O	complete conversion signal output
OGND	37	G	ground of data output
CLKN	38	I	complementary clock input
CLK	39	I	clock input
V_{CCD1}	40	P	digital supply voltage 1 (5.0 V)
DGND1	41	G	digital ground 1
TH	42	I	track-and-hold enable input (CMOS level; active HIGH)
AGND4	43	G	analog ground 4
V_{CCA4}	44	P	analog supply voltage 4 (5.0 V)
n.c.	45	–	not connected
IN	46	I	analog input voltage
INN	47	I	complementary analog input voltage
AGND1	48	G	analog ground 1
AGND5	exposed die pad	G	analog ground 5

Note

1. P = power supply, G = ground, I = input and O = output.

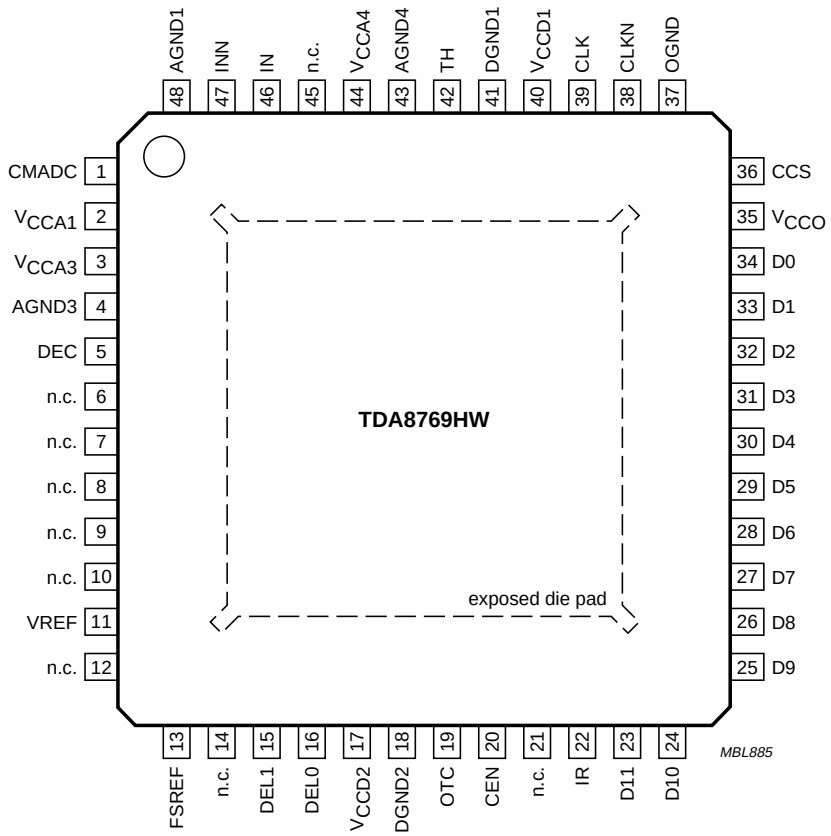


Fig.2 Pin configuration.

8 LIMITING VALUES

Tbf.

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; (tbf)	25	K/W
$R_{th(c-a)}$	thermal resistance from case to ambient	in free air; (tbf)	(tbf)	K/W

10 CHARACTERISTICS

V_{CCA} = 4.75 to 5.25 V; V_{CCD} = 4.75 to 5.25 V; V_{CCO} = 2.7 to 3.6 V; AGND connected to DGND; T_{amb} = –40 to +85 °C; $V_{IN(p-p)} - V_{INN(p-p)}$ = 1.9 V – 0.5 dBFS; $V_{VREF} = V_{CCA3} - 1.75$ V; $V_{i(CM)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V, V_{CCO} = 3.0 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TEST(1)	MIN.	TYP.	MAX.	UNIT
Supplies							
V_{CCA}	analog supply voltage			4.75	5.0	5.25	V
V_{CCD}	digital supply voltage			4.75	5.0	5.25	V
V_{CCO}	output supply voltage			2.7	3.0	3.6	V
I_{CCA}	analog supply current			–	109	(tbf)	mA
I_{CCD}	digital supply current			–	48	(tbf)	mA
I_{CCO}	output supply current	f_{CLK} = 80 Msps; f_i = 21.4 MHz		–	17.5	(tbf)	mA
P_{tot}	total power dissipation	f_{CLK} = 60 Msps; f_i = 21.4 MHz		–	825	(tbf)	mW
		f_{CLK} = 80 Msps; f_i = 21.4 MHz		–	840	(tbf)	mW
		f_{CLK} = 105 Msps; f_i = 21.4 MHz		–	855	(tbf)	mW
Clock inputs: pins CLK and CLKN; note 2							
INPUTS							
V_{IL}	LOW-level input voltage	referenced to DGND; V_{CCD} = 5 V					
		PECL mode		3.19	–	3.52	V
		TTL mode		DGND	–	0.8	V
V_{IH}	HIGH-level input voltage	referenced to DGND; V_{CCD} = 5 V					
		PECL mode		3.83	–	4.12	V
		TTL mode		2.0	–	V_{CCD}	V
I_{IL}	LOW-level input current	V_{CLK} or V_{CLKN} = 3.52 V		(tbf)	–	–	µA
		V_{CLK} or V_{CLKN} = 0.80 V		(tbf)	–	–	mA
I_{IH}	HIGH-level input current	V_{CLK} or V_{CLKN} = 3.83 V		–	–	(tbf)	µA
		V_{CLK} or V_{CLKN} = 2.00 V		–	–	(tbf)	mA
ΔV_{CLK}	differential AC input voltage for switching	$\Delta V_{CLK} = V_{CLK} - V_{CLKN}$; AC mode; DC voltage level = 2.5 V		(tbf)	1.5	(tbf)	V
R_i	input resistance	f_{CLK} = 105 Msps		–	(tbf)	–	MΩ
C_i	input capacitance	f_{CLK} = 105 Msps		–	(tbf)	–	pF

SYMBOL	PARAMETER	CONDITIONS	TEST[1]	MIN.	TYP.	MAX.	UNIT
TIMING							
$f_{clk(min)}$	minimum clock frequency	$V_{TH} = V_{CCD}$		–	–	9	Msps
$f_{clk(max)}$	maximum clock frequency TDA8769HW/6			60	–	–	MHz/ Msps
	maximum clock frequency TDA8769HW/8			80	–	–	MHz/ Msps
	maximum clock frequency TDA8769HW/10			105	–	–	MHz/ Msps
t_{CLKH}	clock HIGH pulse width	f_i = 21.4 MHz		(tbf)	–	–	ns
t_{CLKL}	clock LOW pulse width	f_i = 21.4 MHz		(tbf)	–	–	ns
Analog inputs: pins IN and INN							
I_{IL}	LOW-level input current	$V_{VREF} = V_{CCA3} - 1.75$ V; V_{TH} = HIGH		–	10	–	µA
I_{IH}	HIGH-level input current	$V_{VREF} = V_{CCA3} - 1.75$ V; V_{TH} = HIGH		–	10	–	µA
R_i	input resistance		D	–	8.4	–	MΩ
C_i	input capacitance		D	–	250	500	fF
$V_{i(CM)}$	common mode input voltage	$V_{IN} = V_{INN}$; output code = 2047	D	$V_{CCA3} - 1.2$	$V_{CCA3} - 1.6$	$V_{CCA3} - 1.7$	V
Digital inputs: pins OTC, SH, DEL1, DEL0 and CEN							
V_{IL}	LOW-level input voltage			DGND	–	$0.3V_{CCD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{CCD}$	–	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{IL} = 0.3V_{CCD}$		(tbf)	–		µA
I_{IH}	HIGH-level input current	$V_{IH} = 0.7V_{CCD}$		–	–	(tbf)	µA
Voltage controlled regulator output: pin CMADC							
$V_{o(CM)}$	common mode output voltage			–	$V_{CCA3} - 1.6$	–	V
$I_{L(CM)}$	load current			–	1	2	mA

SYMBOL	PARAMETER	CONDITIONS	TEST(1)	MIN.	TYP.	MAX.	UNIT
Reference voltage input: pin VREF; note 3							
$V_{ref(FS)}$	full-scale fixed voltage	f_i = 25 MHz; f_{CLK} = 105 Msps		–	V_{CCA3} – 1.75	–	V
$V_{i(p-p)}$	input voltage (peak-to-peak value)	$V_i = V_{IN} - V_{INN}$; $V_{VREF} = V_{CCA3}$ – 1.75 V; $V_{i(CM)} = V_{CCA3}$ – 1.6 V		–	1.9	–	V
I_{ref}	input current			–	0.3	10	µA
Full-scale voltage controlled regulator output: pin FSREF							
$V_{o(FS)}$	1.9 V full-scale output voltage			–	V_{CCA3} – 1.75	–	V
$I_{L(FS)}$	load current			–	1	2	mA
Digital outputs: pins D11 to D0 and IR							
OUTPUT LEVELS							
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA		DGND	–	DGND + 0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = –0.4 mA		V_{CCO} – 0.5	–	V_{CCO}	V
I_{OZ}	output current in 3-state	output level between 0.5 V and V_{CCO}		–20	–	+20	µA
TIMING; see Fig. 3							
$t_{d(s)}$	sampling delay	C_L = 10 pF; note 4		–	(tbf)	(tbf)	ns
$t_{h(o)}$	output hold time	C_L = 10 pF		(tbf)	3.7	–	ns
$t_{d(o)}$	output delay	C_L = 10 pF		–	4.6	(tbf)	ns
3-STATE OUTPUT DELAY							
t_{dZH}	enable to HIGH state			–	2.8	–	ns
t_{dZL}	enable to LOW state			–	7.5	–	ns
t_{dHZ}	disable from HIGH state			–	7.2	–	ns
t_{dLZ}	disable from LOW state			–	2.9	–	ns
Timing complete conversion signal: pin CCS							
$t_{d(CCS)}$	complete conversion signal delay	C_L = 10 pF; see Table 4 and Fig 4					
		DEL0 = LOW; DEL1 = HIGH		–	0	–	ns
		DEL0 = HIGH; DEL1 = LOW		–	1.2	–	ns
		DEL0 = HIGH; DEL1 = HIGH		–	2.2	–	ns

SYMBOL	PARAMETER	CONDITIONS	TEST[1]	MIN.	TYP.	MAX.	UNIT
Analog signal processing (50% clock duty factor)							
INL	integral non-linearity	f_{CLK} = 20 Msps; f_i = 400 kHz		–	±1.7	(tbf)	LSB
DNL	differential non-linearity	f_{CLK} = 20 Msps; f_i = 400 kHz; no missing code guaranteed		–	±0.4	(tbf)	LSB
E_{offset}	offset error	$V_{CCA} = V_{CCD}$ = 5 V; V_{CCO} = 3.0 V; T_{amb} = 25 °C; output code = 2047		–	–5	–	mV
E_G	gain error amplitude (spread from device to device)	$V_{CCA} = V_{CCD}$ = 5 V; V_{CCO} = 3.0 V; T_{amb} = 25 °C		(tbf)	–	(tbf)	%FS
B	analog bandwidth	f_{CLK} = 105 Msps; –3 dB; full-scale input; note 5	D	–	330	–	MHz
THD	total harmonic distortion TDA8769HW/6	B = Nyquist; note 6					
		f_i = 21.4 MHz		–	–74	–	dBc
	total harmonic distortion TDA8769HW8	B = Nyquist; note 6					
		f_i = 21.4 MHz		–	–74	–	dBc
		f_i = 50 MHz		–	–68	–	dBc
	total harmonic distortion TDA8769HW/10	B = Nyquist; note 6					
		f_i = 21.4 MHz		–	–67	–	dBc
		f_i = 78 MHz		–	–63	–	dBc
$N_{th(rms)}$	thermal noise (RMS value)	shorted input; $V_{TH} = V_{CCD}$; f_{clk} = 105 Msps		–	(tbf)	–	LSB
SNR	signal-to-noise ratio TDA8769HW/6	f_i = 21.4 MHz; note 7					
		B = Nyquist		–	66	–	dBc
	signal-to-noise ratio TDA8769HW/8	f_i = 21.4 MHz; note 7					
		B = Nyquist		–	66	–	dBc
		f_i = 50 MHz; note 7					
		B = Nyquist		–	66	–	dBc
		B = 5 MHz		–	72.4	–	dBc
	signal-to-noise ratio TDA8769HW/10	f_i = 21.4 MHz; note 7					
		B = Nyquist		–	64	–	dBc
		f_i = 78 MHz; note 7					
		B = Nyquist		–	62	–	dBc
		B = 5 MHz		–	72	–	dBc

SYMBOL	PARAMETER	CONDITIONS	TEST[1]	MIN.	TYP.	MAX.	UNIT
SFDR	spurious free dynamic range TDA8769HW/6	f_i = 21.4 MHz B = Nyquist		–	77	–	dBc
	spurious free dynamic range TDA8769HW/8	f_i = 21.4 MHz B = Nyquist		–	77	–	dBc
		f_i = 50 MHz					
		B = Nyquist		–	70	–	dBc
		B = 5 MHz		–	80.8	–	dBc
	spurious free dynamic range TDA8769HW/10	f_i = 21.4 MHz B = Nyquist		–	68	–	dBc
		f_i = 78 MHz					
		B = Nyquist		–	67	–	dBc
		B = 5 MHz		–	84	–	dBc
ENOB	effective number of bits TDA8769HW/6	f_i = 21.4 MHz; note 8 B = Nyquist		–	10.6	–	bit
	effective number of bits TDA8769HW/8	f_i = 21.4 MHz; note 8 B = Nyquist		–	10.6	–	bit
		f_i = 50 MHz; note 8					
		B = Nyquist		–	10.3	–	bit
		B = 5 MHz		–	11.7	–	bit
	effective number of bits TDA8769HW/10	f_i = 21.4 MHz; note 8 B = Nyquist		–	10	–	bit
		f_i = 78 MHz; note 8					
		B = Nyquist		–	9.6	–	bit
		B = 5 MHz		–	11.8	–	bit
IM2	second order intermodulation distortion	f_i1 = 15 MHz and f_i2 = 18 MHz; note 10 f_{clk}= 80 Msps		–	(tbf)	–	dBFS
IM3	third order intermodulation distortion	f_i1 = 15 MHz and f_i2 = 18 MHz; note 10 f_{clk}= 80 Msps		–	82	–	dBFS
BER	bit error rate	f_i = 25 MHz; V_{IN} = 16LSB at code 2047; f_{clk} = 105 Msps		–	(tbf)	–	

Notes

1. Explanation tests:
   a) D = guaranteed by design
   b) C = guaranteed by characterization
   c) I = industrially tested for 100%.

2. The circuit has two clock inputs: CLK and CLKN. There are 5 modes of operation:
   a) PECL mode 1: (DC level varies proportionally with V_{CCD}) CLK and CLKN inputs are at differential PECL levels.
   b) PECL mode 2: (DC level varies proportionally with V_{CCD}) CLK input is at PECL level and sampling is taken on the falling edge of the clock input signal. A DC level of 3.65 V has to be applied on CLKN decoupled to GND via a 100 nF capacitor.
   c) PECL mode 3: (DC level varies proportionally with V_{CCD}) CLKN input is at PECL level and sampling is taken on the rising edge of the clock input signal. A DC level of 3.65 V has to be applied on CLK decoupled to GND via a 100 nF capacitor.
   d) Differential AC driving mode 4: When driving the CLK input directly and with any AC signal of minimum 1 V (p-p) and with a DC level of 2.5 V, the sampling takes place at the falling edge of the clock signal. When driving the CLKN input with the same signal, sampling takes place at the rising edge of the clock signal. It is recommended to decouple the CLKN or CLK input to DGND via a 100 nF capacitor.
   e) TTL mode 5: CLK input is at TTL level and sampling is taken on the falling edge of the clock input signal. In that case CLKN pin has to be connected to the ground.
3. The ADC input range can be adjusted with an external reference connected to pin VREF. This voltage has to be referenced to V_{CCA}.
4. Output data acquisition: the output data is available after the maximum delay of $t_{d(s)}$.
5. The –3 dB analog bandwidth is determined by the 3 dB reduction in the reconstructed output, the input being a full-scale sine wave.
6. The total harmonic distortion is obtained with the addition of the first five harmonics.
7. The signal-to-noise ratio takes into account all harmonics above five and noise up to Nyquist frequency.
8. The effective number of bits, or ENOB, are obtained via a Fast Fourier Transform (FFT). The calculation takes into account all harmonics and noise up to half of the clock frequency (Nyquist frequency). Conversion to signal-to-noise and distortion, or SINAD, is given by SINAD = ENOB $\times$ 6.02 + 1.76 dB.
9. Intermodulation measured relative to either tone with analog input frequencies of (tbf) and (tbf) MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale input to the converter (–6 dB below full-scale for each input signal).
10. IM2 is the ratio of the RMS value of either input tone to the RMS value of the worst case second order intermodulation product. IM3 is the ratio of the RMS value of either input tone to the RMS value of the worst case third order intermodulation product.

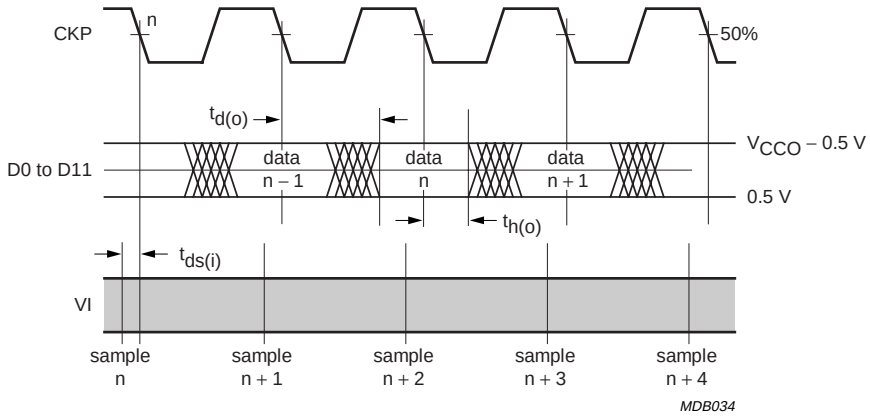


Fig.3 Output timing diagram.

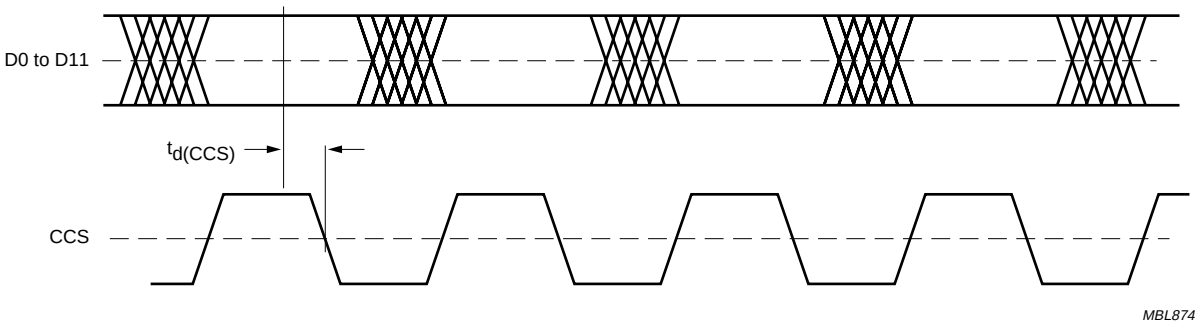


Fig.4 Complete conversion signal timing diagram.

11 APPLICATION INFORMATION

11.1 Output coding and control signals

Table 1 Output coding with differential inputs (typical values to AGND); $V_{IN(p-p)} - V_{INN(p-p)}$ = 1.9 V – 0.5 dBFS; $V_{VREF} = V_{CCA3} - 1.75$ V

CODE	$V_{IN(p-p)}$	$V_{INN(p-p)}$	IR	BINARY OUTPUTS (D11 TO D0)	TWO'S COMPLEMENT OUTPUTS (D11 TO D0)
Underflow	<2.925	>3.875	0	0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0
0	2.925	3.875	1	0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0
1	–	–		0 0 0 0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0 0 0 0 1
:	:	:		:	:
2047	3.4	3.4		0 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1
:	:	:		:	:
4094	–	–		1 1 1 1 1 1 1 1 1 1 1 0	0 1 1 1 1 1 1 1 1 1 1 0
4095	3.875	2.925		1 1 1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1 1 1
Overflow	>3.875	<2.925	0	1 1 1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1 1 1

Table 2 Mode selection

CONTROL INPUT TWO'S COMPLEMENT OUTPUT (OTC)	CHIP ENABLE NOT (CEN)	OUTPUT DATA (D0 TO D11 AND IR)
0	0	binary; active
1	0	two's complement; active
don't care	1	high impedance

Table 3 Track-and-hold selection

CONTROL INPUT TRACK-AND-HOLD (TH)	MODE
1	active
0	inactive; tracking

Table 4 Complete conversion signal selection

DEL1	DEL0	OUTPUT SIGNAL
0	0	inactive
0	1	active (for timing values, see Chapter 10)
1	0	
1	1	

11.2 TDA8769 in 3G radio receivers

TDA8769 has been proven in many 3G receivers with various operating conditions regarding input frequency, signal input frequency bandwidth and sampling frequency. TDA8769 provides a maximum analog input frequency of 250 MHz. It allows a significant cost reduction of the RF front-end, from two mixers to only one, even in multicarrier architecture. Table 5 shows possible applications with the TDA8769 in High IF sampling mode.

Table 5 Examples of possible f_i, f_{clk} and f_i bandwidth combinations supported

f_i (MHz)	f_{clk} (MHz)	f_i BW (MHz)	SNR (dB)	SFDR (dBc)
250	9.60	0.20	66.5	79.9
243.95	9.60	0.20	62.6	68.5
243.95	19.20	0.20	68.4	77.2
243.95	52.00	0.20	65.7	80.0
190	40.00	1.25	72.0	80.0
106	76.80	5.00	70.8	83.6
86	76.80	5.00	72.2	87.1
80	61.44	10.00	(tbf)	(tbf)
70	40.00	5.00	70	70
69.99	58.98	1.25	(tbf)	(tbf)
27	51.2	3.5	(tbf)	(tbf)
10.8	32.5	0.30	84.3	83.0

For a dual carrier W_CDMA receiver, the most important parameters are the sensitivity and Adjacent Channel Selectivity (ACS). In W-CDMA, it can be far below the noise floor, is defined by the Sensitivity to Noise Ratio (SENR). Its value is negative due to the gain processing. The Adjacent Channel Power Ratio (ACPR) is the difference between the peak and noise floor. It represents the ratio of the adjacent channel power and the average power of the channel. The ACS is defined by the sum of SENR and ACPR. Figure 5 illustrates the relation between these parameters.

On a typical application with the TDA8769 device, the ACS obtained is 80 dB with an ACPR of 70 dB and a SENR of 10 dB. Moreover, the Noise Figure (NF) of the TDA8769 is 31.5 dB.

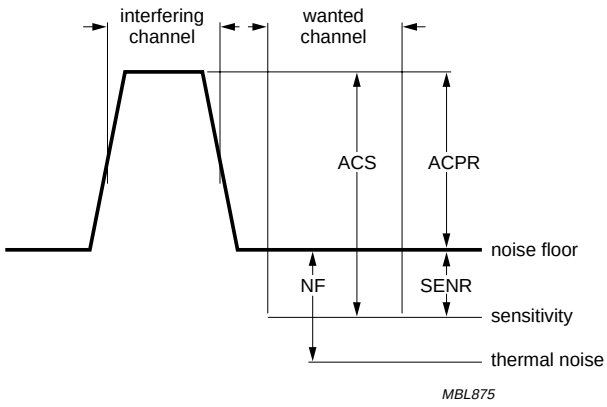


Fig.5 Adjacent channel selectivity and analog-to-digital converter sensitivity.

11.3 Application diagrams

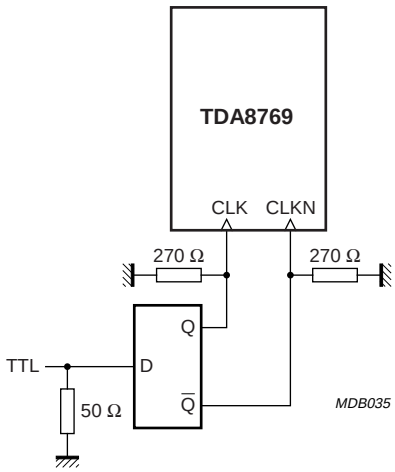


Fig.6 TTL to PECL translator application.

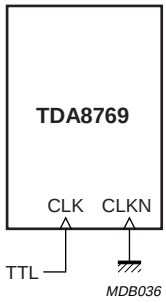


Fig.7 TTL single-ended clock application.

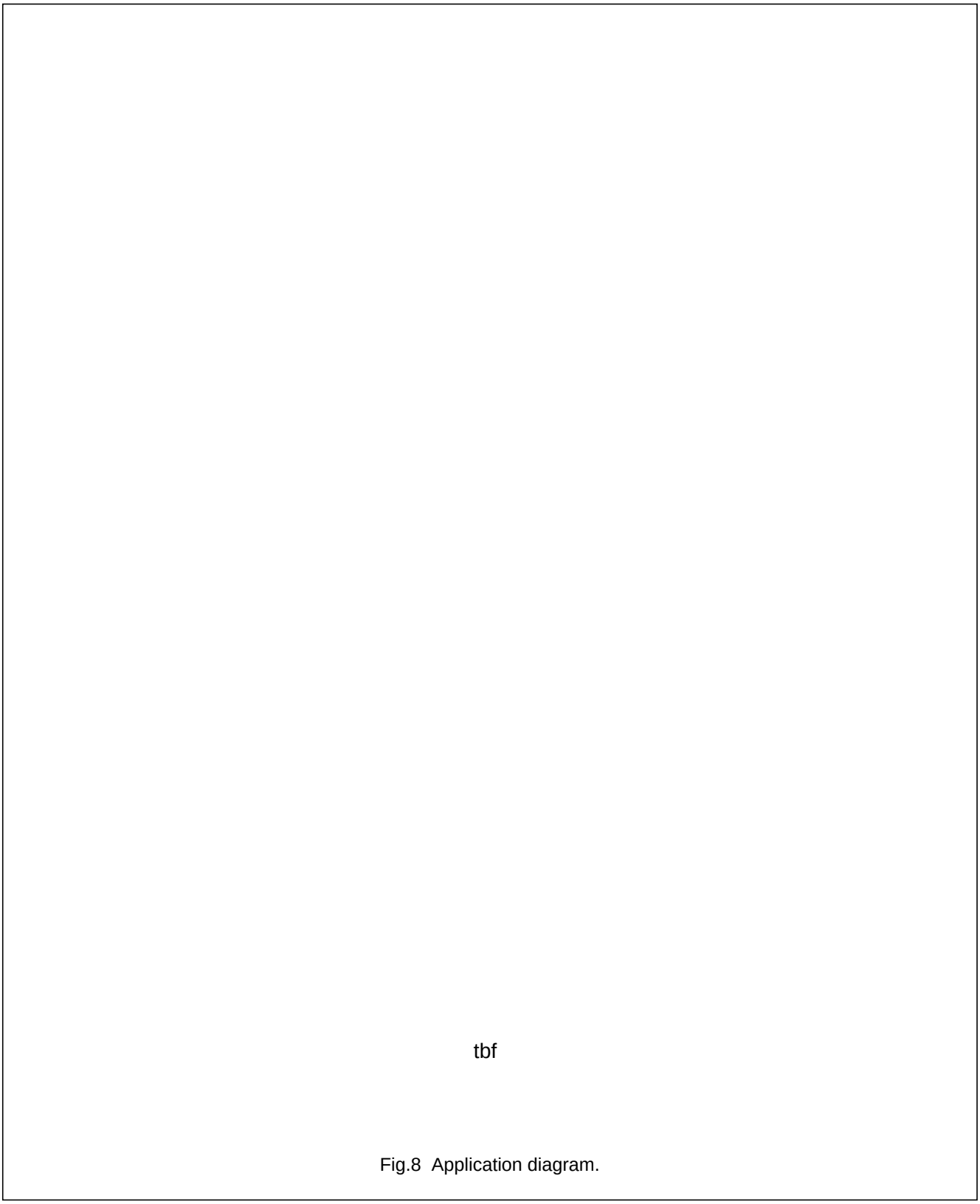


Fig.8 Application diagram.

11.4 Demonstration board

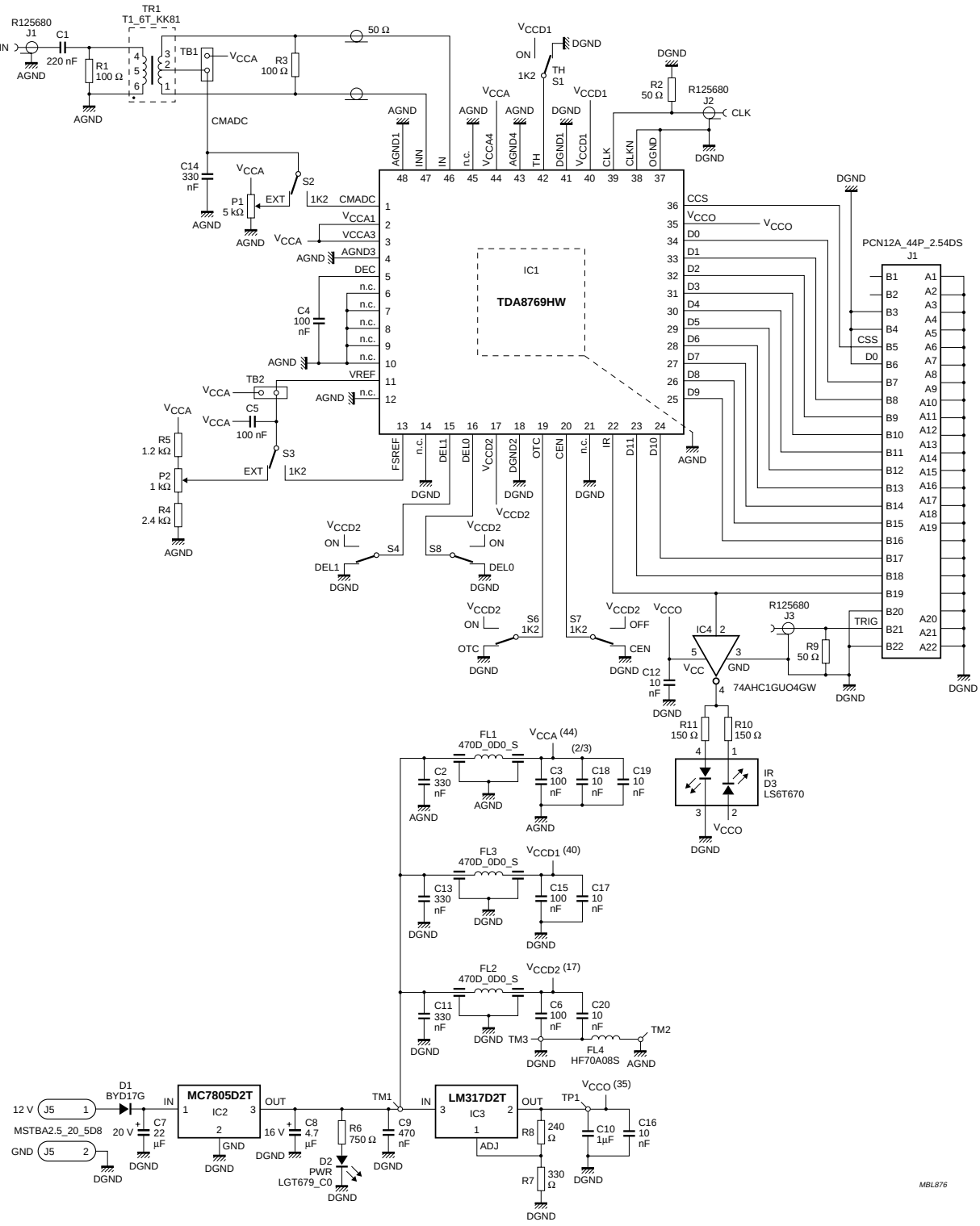


Fig.9 Demonstration board schematic.

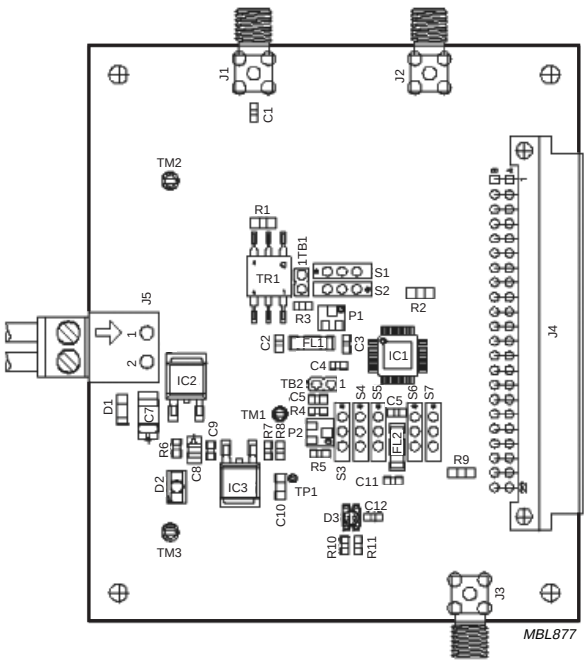


Fig.10 Component placement, top view.

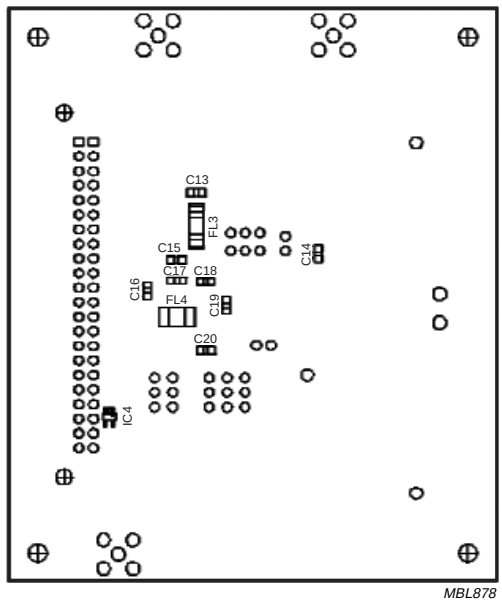


Fig.11 Component placement, bottom view.

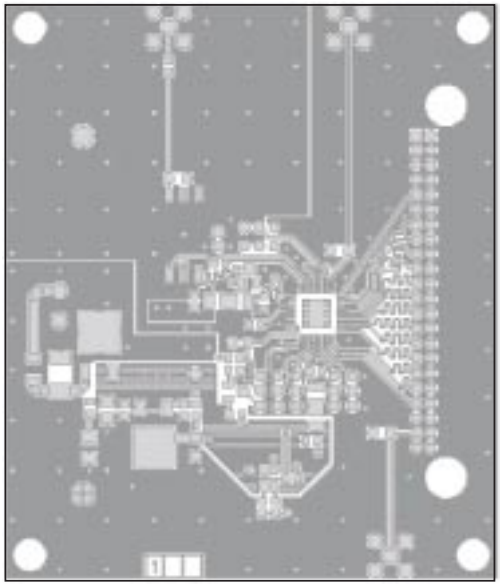


Fig.12 Printed-circuit board tracks, layout 1.

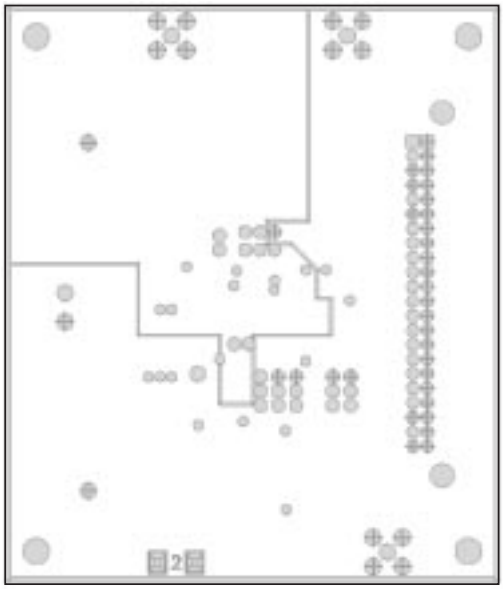


Fig.13 Printed-circuit board tracks, layout 2.

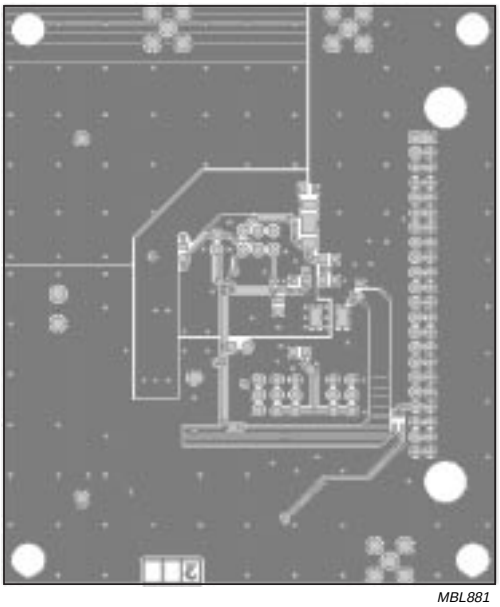


Fig.14 Printed-circuit board tracks, layout 3.

11.5 Definitions

11.5.1 STATIC PARAMETERS

11.5.1.1 Integral non-linearity (INL)

INL is defined as the deviation of the transfer function from a best fit straight line (linear regression computation). The INL of code i is obtained from the following equation:

$$INL(i) = \frac{V_{in}(i) - V_{in}(ideal)}{S}$$

where:

i = code value

V_{in} = input voltage for code i

S = slope of the ideal straight line (code width).

11.5.1.2 Differential non-linearity (DNL)

DNL is the deviation in code width from the value of one LSB. The DNL of code i is obtained from the following equation:

$$DNL(i) = \frac{V_{in}(i+1) - V_{in}(i)}{S}$$

where:

i = 0 to $2^n - 2$

V_{in} = input voltage for code i

S = slope of the ideal straight line.

11.5.2 DYNAMIC PARAMETERS

Figure 15 shows the spectrum of a single tone full-scale input sine wave with frequency f_t, conforming to coherent sampling and digitized by the ADC under test. Coherent sampling means that $\frac{f_t}{f_s} = \frac{M}{N}$, where M is the number of cycles, N the number of samples and both M and N being a relative prime.

Remark: The parameter P_{noise} used in the following equations includes the power of the random noise, non-linearities, sampling time errors and quantization noise.

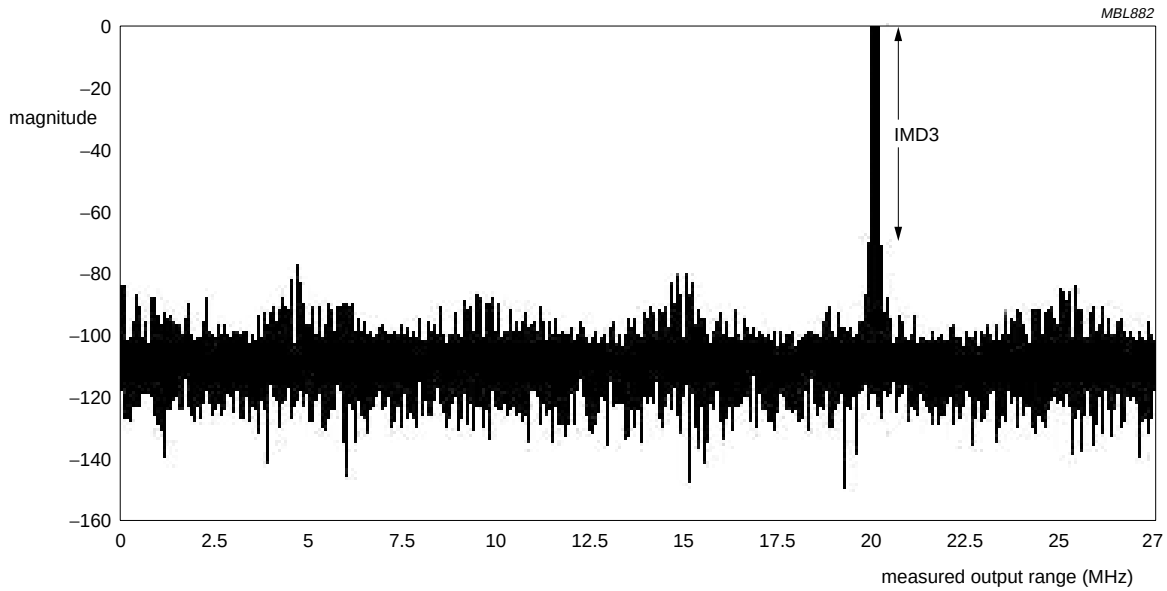


Fig.15 Spectrum of a full-scale input sine wave with frequency f_t.

11.5.2.1 Signal-to-noise and distortion (SINAD)

SINAD is the ratio of the signal power to the noise plus distortion power, excluding the DC component, at a given sample rate and input frequency:

$$SINAD = 10\log_{10}\left(\frac{P_{signal}}{P_{noise + distortion}}\right) \text{ dB.}$$

11.5.2.2 Effective number of bits (ENOB)

ENOB is derived from SINAD and gives the theoretical resolution an ideal ADC would require to obtain the same SINAD measured on the actual ADC. A good approximation is:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

11.5.2.3 Total harmonic distortion (THD)

THD is the ratio of the power of the harmonics to the power of the signal frequency. The equation for k – 1 harmonics is:

$$THD = 10\log_{10}\left(\frac{P_{harmonics}}{P_{signal}}\right) \text{ dB}$$

where:

$$P_{harmonics} = a_2^{\,2} + a_3^{\,2} + ... + a_k^{\,2}$$

$$P_{signal} = a_1^{\,2}$$

As usual the value of k = 6 (i.e. the calculation of THD is done with the first 5 harmonics).

11.5.2.4 Signal-to-noise ratio (SNR)

SNR is the ratio of the signal power to the noise power, excluding the harmonics and DC component of the signal:

$$SNR = 10\log_{10}\left(\frac{P_{signal}}{P_{noise}}\right) \text{ dB}$$

11.5.2.5 Spurious free dynamic range (SFDR)

The SFDR specifies the available signal range as the spectral distance between the amplitude of the fundamental and the amplitude of the largest spurious signal, harmonic and non-harmonic, excluding the DC component.

$$SFDR = 10\log_{10}\left(\frac{a_1}{max(s)}\right) \text{ dB}$$

11.5.2.6 Intermodulation distortion (IMD2 and IMD3)

Figure 16 shows the spectral analysis of a dual tone sine wave input, at frequencies f_{t1} and f_{t2}, meeting the coherence criterion.

The 2nd and 3rd order intermodulation distortion products, IMD2 and IMD3 respectively, are defined with a dual tone input. IMD2 is defined as the ratio of the RMS value of either tone to the RMS value of the second order intermodulation product, IMD3 with the third order intermodulation product. The IMD is given by:

$$IMD = 10\log_{10}\left(\frac{P_{intermod}}{P_{signal}}\right) \text{ dB}$$

where:

$$P_{intermod} = a^2_{im(ft1-ft2)} - a^2_{im(ft1+ft2)} + a^2_{im(ft1-2ft2)} + a^2_{im(ft1+2ft2)} + \ldots + a^2_{im(2ft1-ft2)} + a^2_{im(f2t1+ft2)}$$

$$P_{signal} = a^2_{ft1} + a^2_{ft2}.$$

$a^2_{im(ft)}$ is the power of the intermodulation component at f_t.

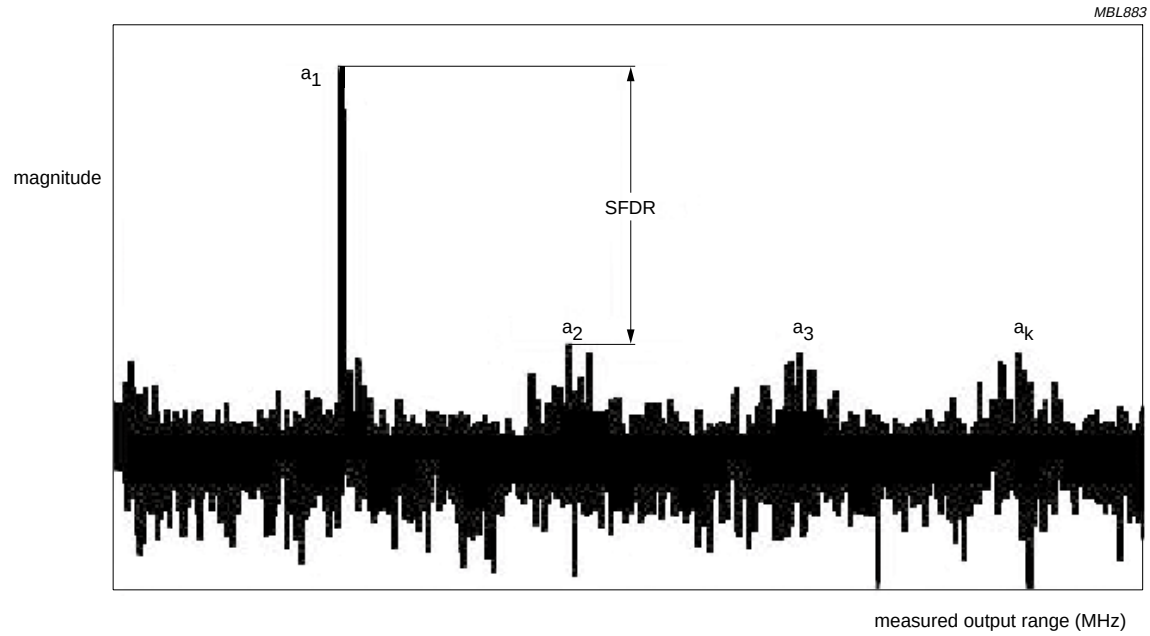
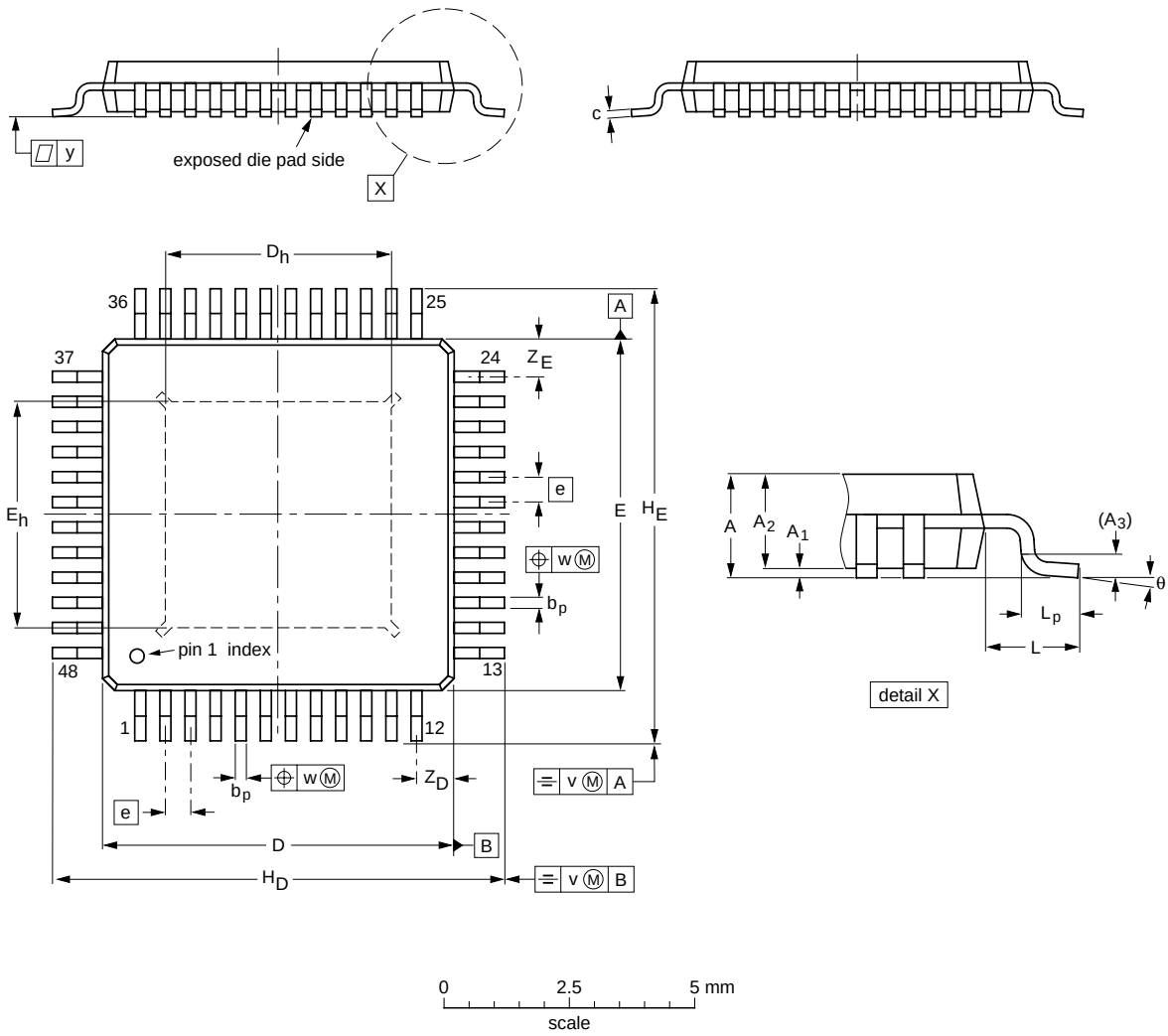


Fig.16 Spectral analysis with dual tone.

12 PACKAGE OUTLINE

HTQFP48: plastic thermal enhanced thin quad flat package; 48 leads; body 7 x 7 x 1 mm; exposed die pad **SOT545-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	7.1 6.9	4.6 4.4	7.1 6.9	4.6 4.4	0.5	9.1 8.9	9.1 8.9	1	0.75 0.45	0.2	0.08	0.08	0.89 0.61	0.89 0.61	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT545-2						~~99-08-04~~ 03-04-07

13 SOLDERING

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON-T and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
9. Hot bar or manual soldering is suitable for PMFP packages.

14 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

15 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

16 DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

Printed in The Netherlands R78/02/pp28 Date of release: 2003 Dec 09 Document order number: 9397 750 11706

Let's make things better.

Philips
Semiconductors

PHILIPS