CYPRESS SEMICONDUCTOR

CYM1621

64K x 16 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **Customer configurable**
  - **x4, x8, x16**
- **Low active power**
  - **6.8W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .270 in.**
- **Small PCB footprint**
  - **2 sq. in.**
- **2V data retention (L version)**

Functional Description

The CYM1621 is a high-performance 1-megabit static RAM module organized as 64K words by 16 bits. This module is constructed from sixteen 64K x 1 SRAMs in leadless chip carriers mounted on a ceramic substrate with pins. Four separate $\overline{CS}$ pins are used to control each 4-bit nibble of the 16-bit word. This feature permits the user to configure this module as either 256K x 4, 128K x 8 or 64K x 16 organization through external decoding and appropriate pairing of the outputs.

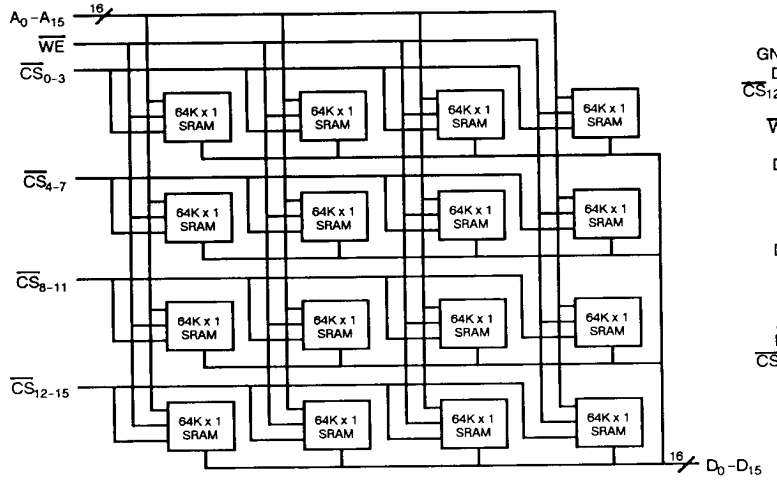
Writing to the device is accomplished when the chip select ($\overline{CS_{XX}}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the data lines (D_X) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip select ($\overline{CS_{XX}}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data lines (D_X).

The data output is in the high-impedance state when chip enable ($\overline{CS_{XX}}$) is HIGH or write enable ($\overline{WE}$) is LOW.

Power is consumed in each 4-bit nibble only when the appropriate $\overline{CS}$ is enabled, thus reducing power in the x4 or x8 mode.

Logic Block Diagram



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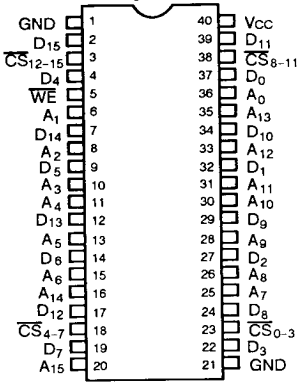
Pin Configuration

DIP
Top View



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Selection Guide

		1621HD-20	1621HD-25	1621HD-30	1621HD-35	1621HD-45
Maximum Access Time (ns)		20	25	30	35	45
Maximum Operating Current (mA)	Commercial	1250	1250	1250	1250	1250
	Military		1250	1250	1250	1250
Maximum Standby Current (mA)	Commercial	320	320	320	320	320
	Military		320	320	320	320

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -0.5V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[4]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1621HD		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		-0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	-20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	-20	+20	µA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		-350	mA
I_{CCx16}	V_{CC} Operating Supply Current by 16 mode	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_{xx}$ ≤ V_{IL}		1250	mA
I_{CCx8}	V_{CC} Operating Supply Current by 8 mode	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_{xx}$ ≤ V_{IL}		850	mA
I_{CCx4}	V_{CC} Operating Supply Current by 4 mode	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_{xx}$ ≤ V_{IL}		650	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}, $\overline{CS}_{xx}$ ≥ V_{IH} Min. Duty Cycle = 100%		320	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}, $\overline{CS}_{xx}$ ≥ V_{CC} - 0.3V, V_{IN} ≥ V_{CC} - 0.3V or V_{IN} ≤ 0.3V		320	mA

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	130	pF
C_{OUT}	Output Capacitance		15	pF

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested initially and after any design or process changes that may affect these parameters.
4. T_A is the "instant on" case temperature.

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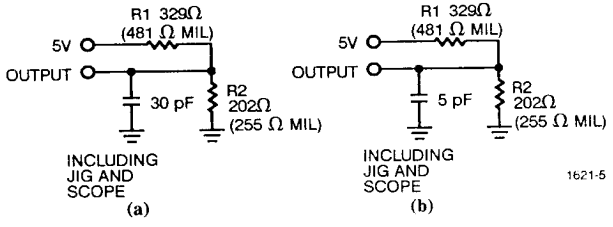
Switching Characteristics Over the Operating Range [5]

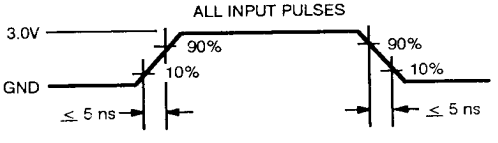
Parameters	Description	1621HD-20		1621HD-25		1621HD-30		1621HD-35		1621HD-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	20		25		30		35		45		ns
t_{AA}	Address to Data Valid		20		25		30		35		45	ns
t_{OHA}	Output Hold from Address Change	5		5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		30		35		45	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [7]	5		5		5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [6, 7]		10		20		25		30		30	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		20		25		30		35		35	ns
WRITE CYCLE [8]												
t_{WC}	Write Cycle Time	20		25		30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	15		22		25		30		40		ns
t_{AW}	Address Set-Up to Write End	15		22		25		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	2		2		3		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	16		20		20		25		30		ns
t_{SD}	Data Set-Up to Write End	10		15		20		20		25		ns
t_{HD}	Data Hold from Write End	2		3		5		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [7]	5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [6, 7]	0	20	0	20	0	25	0	25	0	25	ns

Notes:

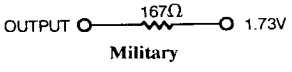
5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CS}$ = V_{IL}.
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

AC Test Loads and Waveforms

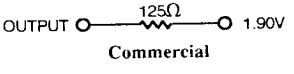




Equivalent to: THEVENIN EQUIVALENT



Military



Commercial

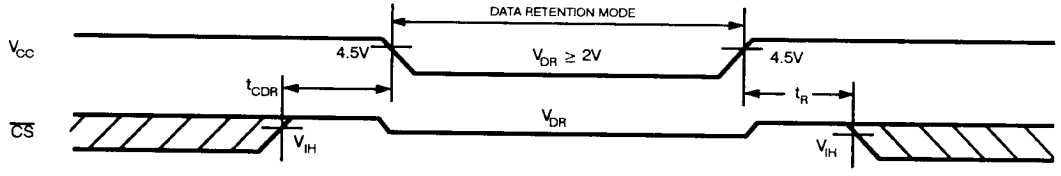
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CYM1621		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention of Data	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			16	mA
t_{CDR}	Chip Deselect to Data Retention Time		0		ns
t_R	Operation Recovery Time		t_{RC} [12]		ns
I_{LI}	Input Leakage Current			10	µA

Notes:

12. t_{RC} = Read Cycle Time.

Data Retention Waveform



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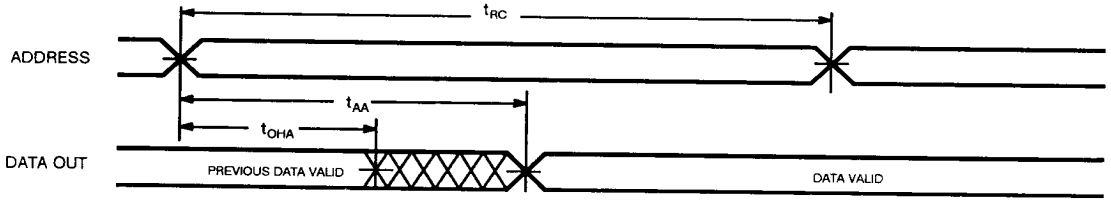
Switching Waveforms [10]

Read Cycle No. 1 [9, 10]



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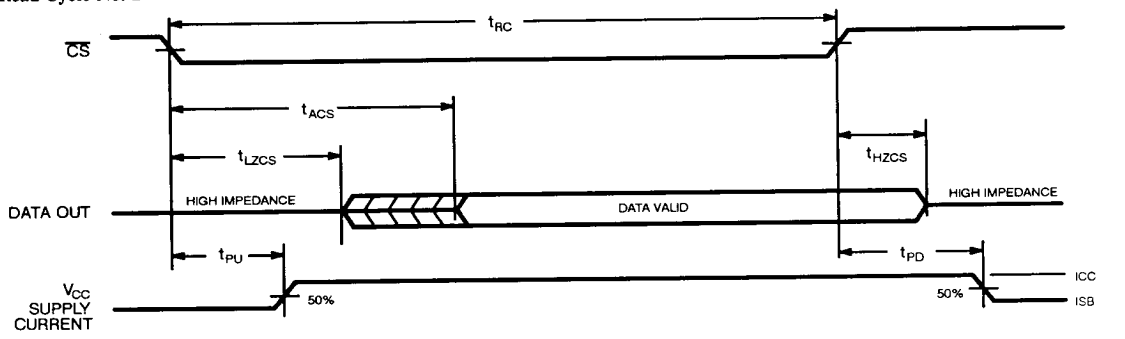
Switching Waveforms (continued)

Read Cycle No. 2[9, 10]



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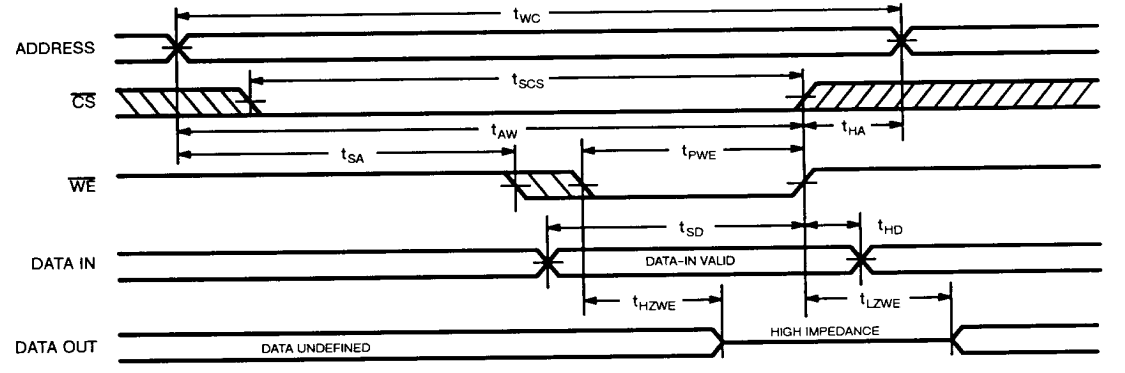
Write Cycle No. 1 ($\overline{WE}$ Controlled)[8]



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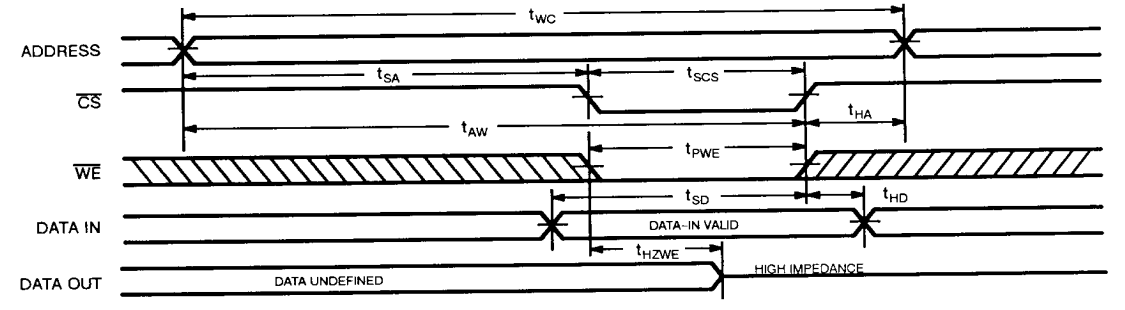
Write Cycle No. 2 ($\overline{CS}$ Controlled)[8, 11]



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Truth Table

$\overline{CS}_{xx}$	$\overline{WE}$	Input/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
20	CYM1621HD-20C	HD02	Commercial
	CYM1621LHD-20C	HD02	
25	CYM1621HD-25C	HD02	Commercial
	CYM1621LHD-25C	HD02	
	CYM1621HD-25MB	HD02	Military
	CYM1621LHD-25MB	HD02	
30	CYM1621HD-30C	HD02	Commercial
	CYM1621LHD-30C	HD02	
	CYM1621HD-30MB	HD02	Military
	CYM1621LHD-30MB	HD02	
35	CYM1621HD-35C	HD02	Commercial
	CYM1621LHD-35C	HD02	
	CYM1621HD-35MB	HD02	Military
	CYM1621LHD-35MB	HD02	
45	CYM1621HD-45C	HD02	Commercial
	CYM1621LHD-45C	HD02	
	CYM1621HD-45MB	HD02	Military
	CYM1621LHD-45MB	HD02	

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