

DESCRIPTION

The HY5116404B is the new generation and fast dynamic RAM organized 4,194,304 × 4-bit. The HY5116404B utilizes Hyundai's CMOS silicon gate process technology as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY5116404B to be packaged in standard 24/26 pin plastic SOJ, TSOP-II and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V ± 10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Low power dissipation
- Max. battery back-up 3.3mW (SL-part)
Max. CMOS standby 2.2mW (SL-part)
5.5mW

Max. TTL standby 11.0mW
Max. operating

Speed	Power
50	605mW
60	495mW
70	440mW

- Single power supply of 5V±10%
- TTL compatible inputs and outputs
- Fast access and cycle time

Speed	t _{RAC}	t _{CAC}	t _{PC}
50	50ns	13ns	20ns
60	60ns	15ns	25ns
70	70ns	18ns	30ns

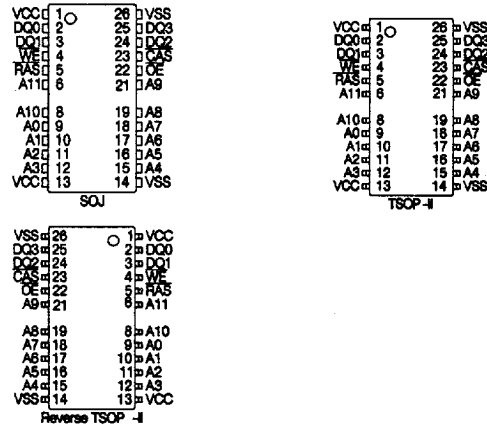
- Extended data out operation
- Multi-bit test capability
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh and Self Refresh capability
- 4096 refresh cycles / 256ms (SL-part)
4096 refresh cycles / 64ms

PIN DESCRIPTION

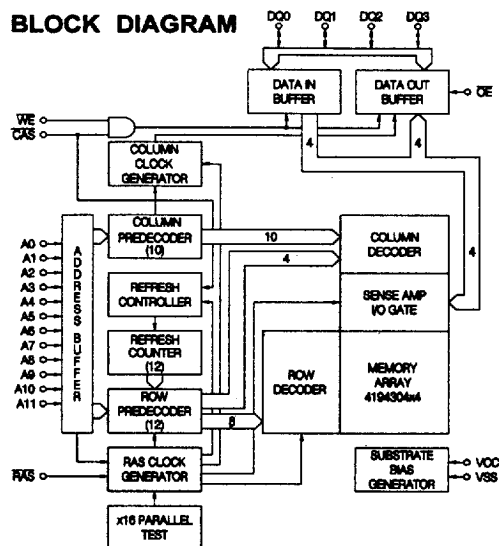
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0-A11	Address Input
DQ0-DQ3	Data Input/Output
Vcc	Power (+5V)
Vss	Ground

* A10 and A11 and applied to row address input only.

PIN CONNECTION



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 125	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to Vss	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
Pd	Power Dissipation	1.0	W
TSOLDER	Soldering Temperature • Time	260 • 10	°C • sec

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	Vcc+1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE: All voltage are referenced to Vss.

DC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	VSS ≤ VIN ≤ VCC+1.0V, All other pins not under test = VSS		-10	10	μA	
ILO	Output Leakage Current (High impedance State)	VSS ≤ VOUT ≤ VCC RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	tRC = tRC (min.)	50 60 70	- - -	110 90 80	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	2	mA	
ICC3	VCC Supply Current, RAS-only refresh	tRC = tRC (min.)	50 60 70	- - -	110 90 80	mA	1,3
ICC4	VCC Supply Current, EDO mode	tHPC = tHPC(min.)	50 60 70	- - -	130 110 90	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V	SL-part	-	1 0.4	mA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	tRC = tRC (min.)	50 60 70	- - -	110 90 80	mA	1,3
ICC7	VCC Supply Current, Battery Back up (SL-part only)	tRC = 62.5μs, CAS = CBR cycling or 0.2V, WE = VCC-0.2V, A0-A10 = VCC-0.2V or 0.2V, DQ0-DQ3 = VCC-0.2V, 0.2V or open.	tRAS ≤ 300ns tRAS ≤ 1μs	- - -	350 600	μA	1,4,5
ICC8	VCC Supply Current, Self Refresh (SL-part only)	RAS & CAS ≤ 0.2V OE & WE & A0-A10=VCC-0.2V or 0.2V, DQ0-DQ3=VCC-0.2V, 0.2V or open		-	300	μA	5
VOL	Output Low Voltage	IOL = 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH = -5.0mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1 and ICC4 and depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS=VIL and CAS=VIH.
4. tRAS(max.) = 1μs is only applied to refresh of battery backup but tRAS(max.) = 10μs is applied to normal functional operation .
5. ICC5(max.) = 0.4mA and ICC7 are applied to SL-parts only (HY5116404BSLJ, HY5116404BSLT and HY5116404BSLR).

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY5116404BJ / T / R / SLJ / SLT/SLR						UNIT	NOTE
			- 50		- 60		- 70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	84	-	104	-	124	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	113	-	137	-	160	-	ns	
3	tHPC	EDO Mode Cycle Time	20	-	25	-	30	-	ns	15
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	61	-	70	-	78	-	ns	15
5	tRAC	Access Time from RAS	-	50	-	60	-	70	ns	4,9,10
6	tCAC	Access Time from CAS	-	13	-	15	-	18	ns	4,9
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	30	-	35	-	40	ns	4
9	tCLZ	CAS to Output Low Impedance	3	-	3	-	3	-	ns	4
10	tCEZ	Output Buffer Turn-off Delay Time from CAS	3	13	3	15	3	18	ns	5
11	tT	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	3
12	tRP	RAS Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	RAS Pulse Width	50	10K	60	10K	70	10K	ns	
14	tRASP	RAS Pulse Width (EDO Mode)	50	200K	60	200K	70	200K	ns	
15	tRSH	RAS Hold Time	13	-	15	-	18	-	ns	
16	tCSH	CAS Hold Time	40	-	45	-	50	-	ns	14
17	tCAS	CAS Pulse width	8	10K	11	10K	14	10K	ns	
18	tRCD	RAS to CAS Delay	18	37	20	45	20	52	ns	9
19	tRAD	RAS to Column Address Delay Time	10	25	15	30	15	35	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	8	-	10	-	12	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold time	8	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	10	-	ns	
26	tAR	Column Address Hold Time from RAS	50	-	50	-	50	-	ns	
27	tRAL	Column Address to RAS Lead Time	25	-	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	8	-	10	-	10	-	ns	
32	tWCR	Write Command Hold Time from RAS	45	-	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	8	-	10	-	10	-	ns	
34	tRWL	Write Command to RAS Lead Time	10	-	12	-	12	-	ns	
35	tCWL	Write Command to CAS Lead Time	10	-	12	-	12	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	50	-	50	-	50	-	ns	
39	tREF	Refresh Period (4096 cycles)	-	64	-	64	-	64	ms	12
		SL-part	-	256	-	256	-	256	ms	11
40	tWCS	Write Command Set up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY5116404BJ/T/R/SLJ/SLT/SLR						UNIT	NOTE
			- 50		- 60		- 70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	30	-	34	-	40	-	ns	8
42	tRWD	RAS to WE Delay Time	67	-	79	-	92	-	ns	8
43	tAWD	Column Address to WE Delay Time	42	-	49	-	57	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	15	-	20	-	25	-	ns	
48	tROH	RAS Hold Time Reference to OE	10	-	10	-	10	-	ns	
49	tOEA	OE Access Time	-	13	-	15	-	18	ns	
50	tOED	OE to Data Delay	13	-	15	-	18	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	3	13	3	15	3	18	ns	5
52	tOEH	OE Command Hold Time	13	-	15	-	18	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	47	-	54	-	62	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	30	-	35	-	40	-	ns	
55	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
57	tWTS	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
58	tWTH	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
59	tRASS	RAS Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	ns	
60	tRPS	RAS Precharge Time (Self Refresh Cycle)	90	-	110	-	130	-	ns	
61	tCHS	CAS Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	
62	tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
63	tREZ	Output Buffer Turn Off Delay Time from RAS	3	13	3	15	3	18	ns	5
64	tWEZ	Output Buffer Turn Off Delay Time from WE	3	13	3	15	3	18	ns	5
65	tWED	WE to Data Delay Time	13	-	15	-	18	-	ns	
66	tOEP	OE Hige Pulse Width	5	-	5	-	8	-	ns	
67	tWPE	WE Pulse Width (Hyper Page Cycle)	5	-	5	-	8	-	ns	
68	tOCH	OE to CAS Hold Time	0	-	0	-	0	-	ns	
69	tCHO	CAS Hold Time to OE	5	-	5	-	8	-	ns	

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AC CHARACTERISTICS IN TEST MODE

NOTE 13

#	SYMBOL	PARAMETER	HY5116404BJC/TC/RC/SLJC/SLTC/SLR						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	95	-	115	-	135	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	140	-	160	-	185	-	ns	
3	tPC	Fast Page Mode Cycle Time	25	-	30	-	35	-	ns	
4	tHPRWC	Fast Page Mode Read-Modify-Write Cycle Time	70	-	80	-	90	-	ns	
5	tRAC	Access Time from RAS	-	55	-	65	-	75	ns	4,9,10
6	tCAC	Access Time from CAS	-	18	-	20	-	23	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	40	-	45	ns	4
13	tRAS	RAS Pulse Width	55	10K	65	10K	75	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	55	200K	65	200K	75	200K	ns	
15	tRSH	RAS Hold Time	18	-	20	-	23	-	ns	
16	tCSH	CAS Hold Time	45	-	50	-	55	-	ns	
17	tCAS	CAS Pulse Width	18	10K	20	10K	23	10K	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
41	tCWD	CAS to WE Delay Time	40	-	45	-	50	-	ns	8
42	tRWD	RAS to WE Delay Time	75	-	90	-	100	-	ns	8
43	tAWD	Column Address to WE Delay Time	50	-	60	-	65	-	ns	8
49	tOEA	OE Access Time	-	18	-	20	-	23	ns	
50	tOED	OE to Data Delay	18	-	20	-	23	-	ns	
52	tOEH	OE Command Hold Time	18	-	20	-	23	-	ns	

NOTE:

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ only $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle before proper device operation is achieved.
2. If $\overline{\text{RAS}}=\text{Vss}$ during power-up, the device could begin an active cycle. These condition results in higher current than necessary which is demanded from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current.
3. $\text{VIH}(\text{min.})$ and $\text{VIL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $\text{VIH}(\text{min.})$ and $\text{VIL}(\text{max.})$, and are assumed to be 5ns for all inputs.
4. Measured at $\text{VOH}=2.0\text{V}$ and $\text{VOL}=0.8\text{V}$ with a load equivalent to 2 TTL loads and 100pF.
5. These parameters define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either trCH or trRH must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and $\overline{\text{WE}}$ leading edge in Read-Modify-Write cycles.
8. twCS , trWD , tcWD , tAWD and tcpWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $\text{twCS} \geq \text{twCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $\text{trWD} \geq \text{trWD}(\text{min.})$, $\text{tcWD} \geq \text{tcWD}(\text{min.})$, $\text{tAWD} \geq \text{tAWD}(\text{min.})$, and $\text{tcpWD} \geq \text{tcpWD}(\text{min.})$, the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the $\text{trCD}(\text{max.})$ limit insures that $\text{trAC}(\text{max.})$ can be met. $\text{trCD}(\text{max.})$ is specified as a reference point only. If trCD is greater than the specified $\text{trCD}(\text{max.})$ limit, then access time is controlled by tcAC .
10. Operation within the $\text{trAD}(\text{max.})$ limit insures that $\text{trAC}(\text{max.})$ can be met. $\text{trAD}(\text{max.})$ is specified as a reference point only. If trAD is greater than the specified $\text{trAD}(\text{max.})$ limit, then access time is controlled by tAA .
11. $\text{tREF}(\text{max.})=256\text{ms}$ is applied to SL-Parts (HY5116404BSLJ, HY5116404BSLT and HY5116404BSLR).
12. A burst of 4096 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles must be executed within 64ms(256ms for SL-part) after exiting self refresh.
13. These specifications are applied to the test Mode.
14. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
15. $\text{tASC} \geq \text{tCP}(\text{min.})$, Assume $\text{tT}=2\text{ns}$

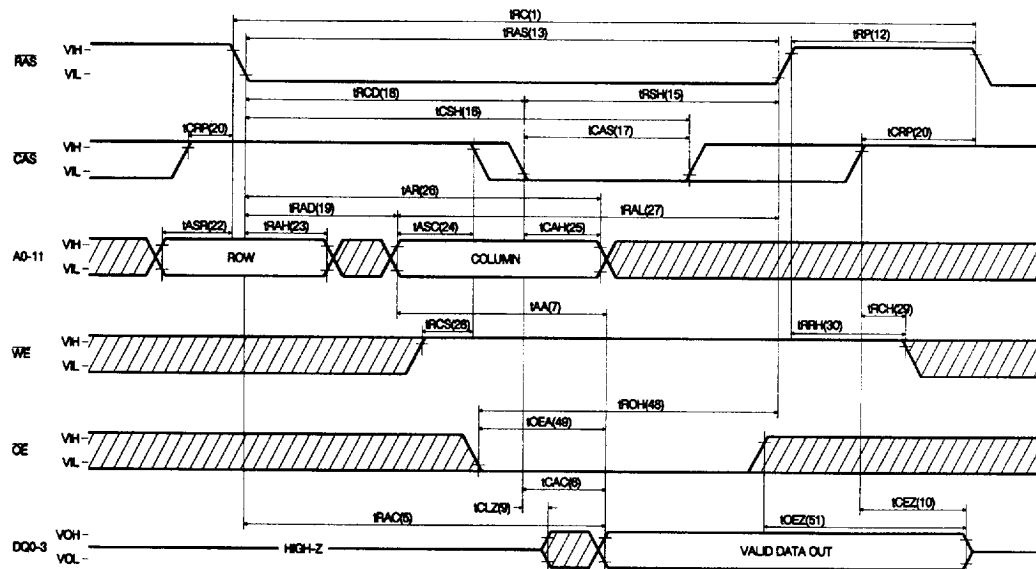
CAPACITANCE

($\text{TA}=25^\circ\text{C}$, $\text{Vcc}=5\text{V} \pm 10\%$, $\text{Vss}=0\text{V}$, $\text{f}=1\text{MHz}$, unless otherwise noted.)

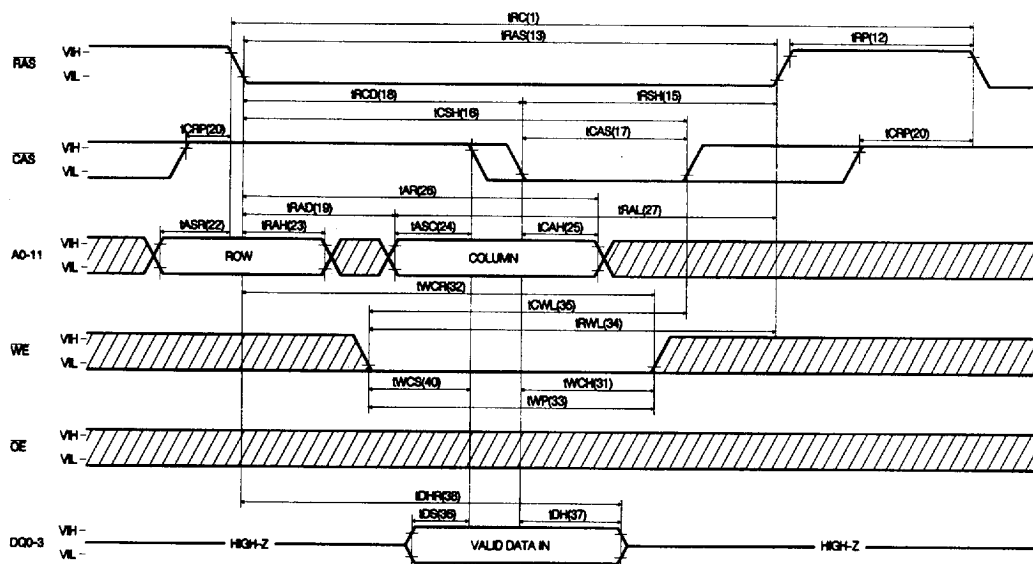
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A11)	-	5	pF
CIN2	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	-	7	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ3)	-	7	pF

TIMING DIAGRAM

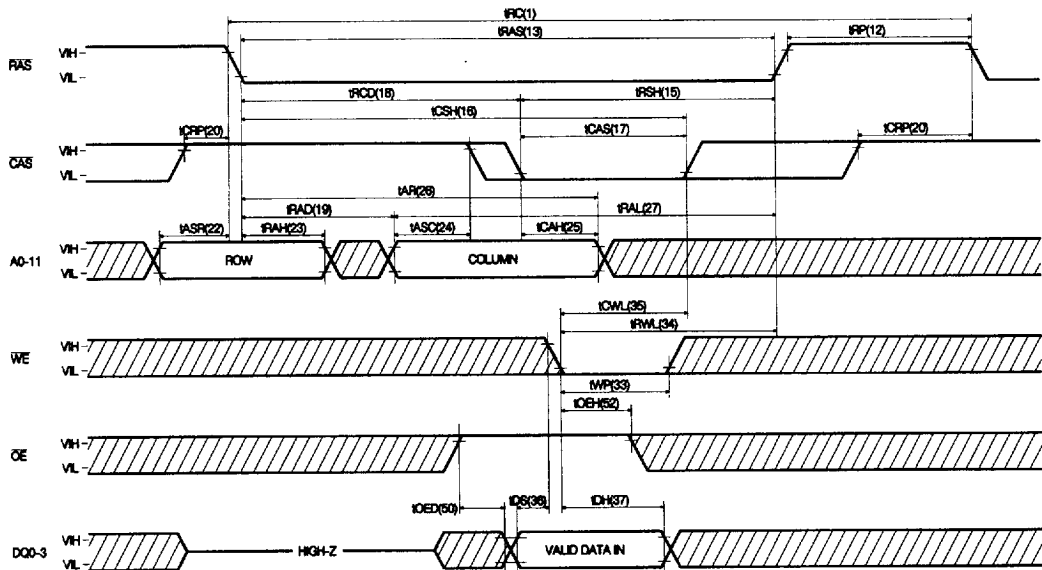
READ CYCLE



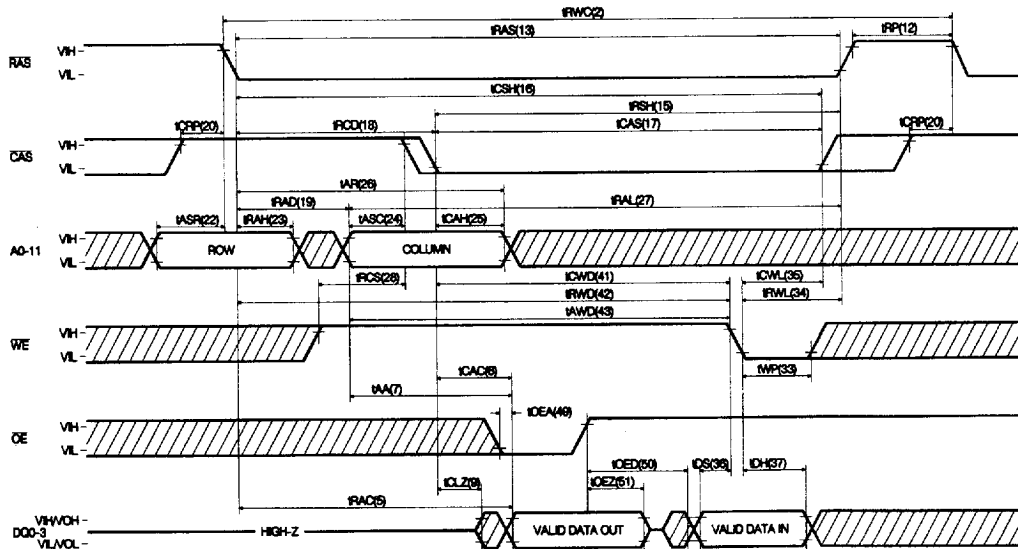
EARLY WRITE CYCLE



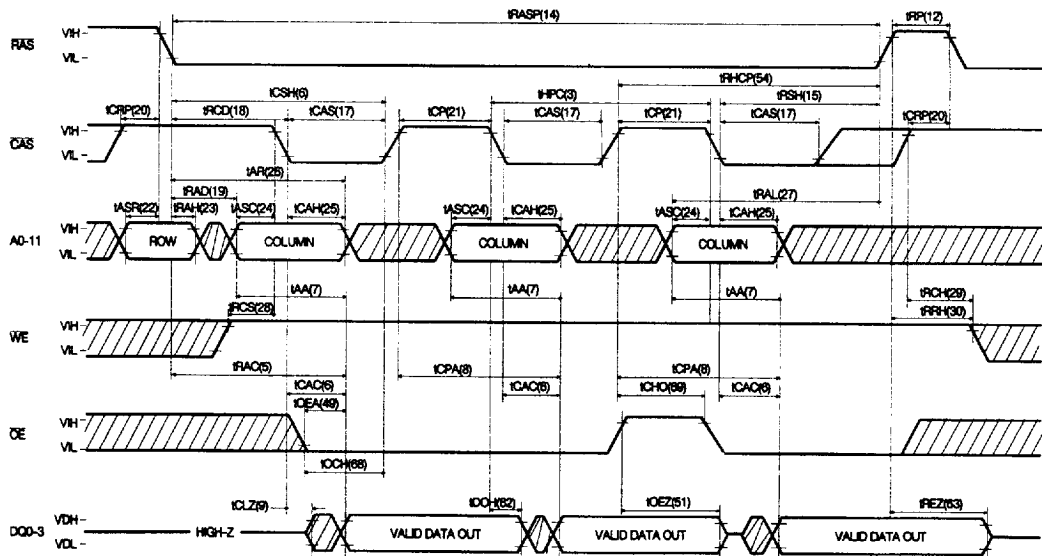
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



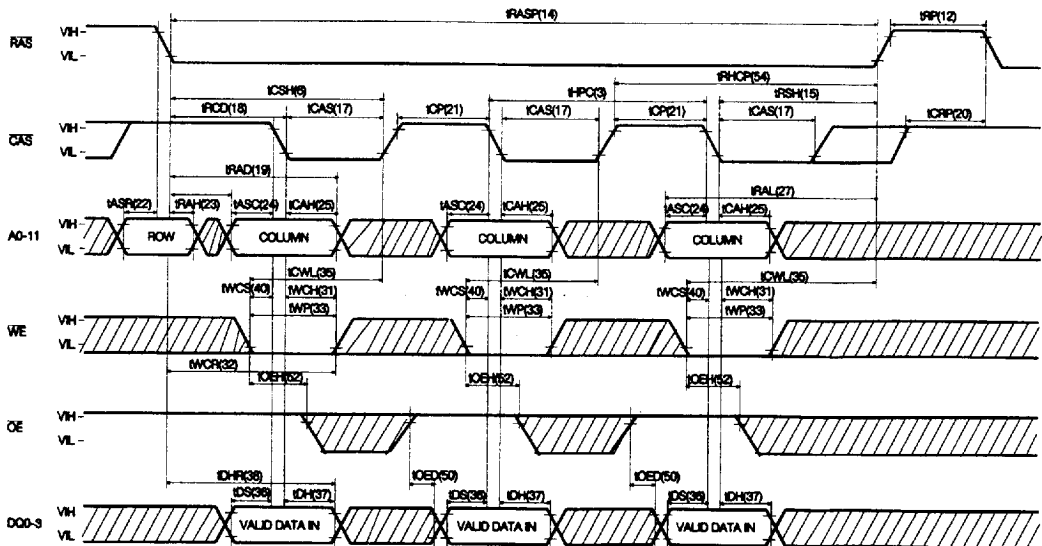
READ-MODIFY-WRITE CYCLE



EDO MODE READ CYCLE



EDO MODE EARLY WRITE CYCLE

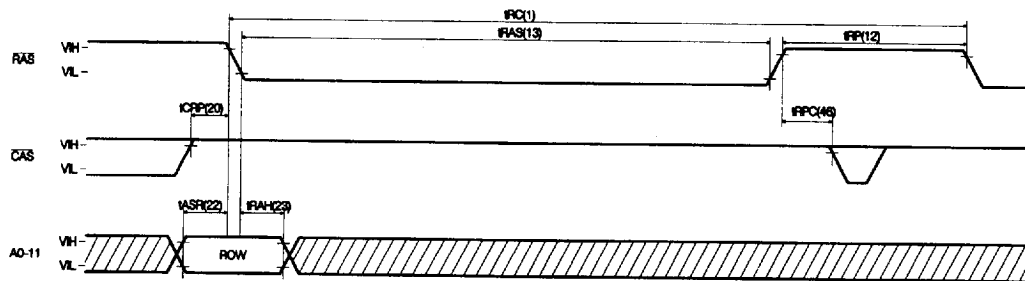


The timing diagram illustrates the relationship between several signals over time. The signals shown are:

- RAS**: Row Address Strobe. High level is labeled $t_{RAS}(14)$. A pulse is shown at the end labeled $t_{RP}(12)$.
- CAS**: Column Address Strobe. High level is labeled $t_{CAS}(17)$. Pulses are shown with intervals labeled $t_{CP}(21)$ and $t_{CA}(17)$.
- AD-11**: Address Data Bus. Shows **ROW** and **COLUMN** periods. High level is labeled $t_{AS}(22)$, $t_{AH}(25)$, $t_{AS}(24)$, and $t_{AH}(25)$.
- WE**: Write Enable. High level is labeled $t_{WC}(28)$. A pulse is shown with $t_{WE}(31)$ and $t_{WH}(31)$.
- OE**: Output Enable. High level is labeled $t_{OE}(40)$, $t_{OC}(9)$, and $t_{OA}(7)$.
- DQ0-3**: Data Bus. Shows **VALID DATA-OUT** and **VALID DATA-IN** periods. High level is labeled $t_{DQ}(32)$, $t_{WE}(24)$, $t_{DS}(38)$, $t_{AA}(7)$, and $t_{RE}(23)$.

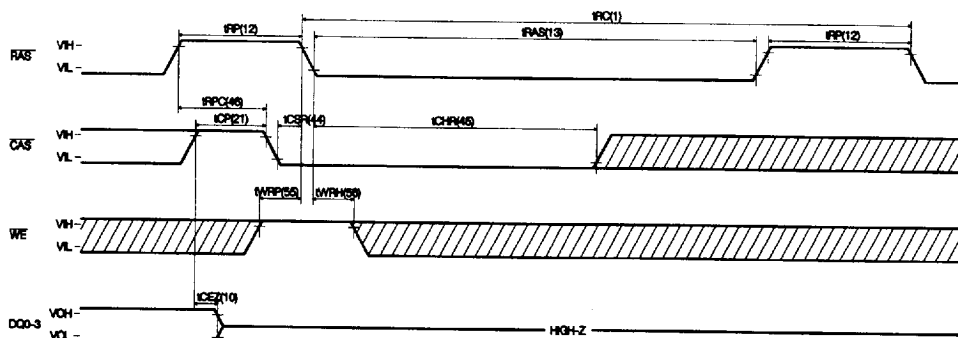
Timing parameters are indicated by dimension lines with labels such as $t_{RAS}(14)$, $t_{RCD}(17)$, $t_{RC}(21)$, $t_{RP}(12)$, $t_{AS}(22)$, $t_{AH}(25)$, $t_{AS}(24)$, $t_{AH}(25)$, $t_{WC}(28)$, $t_{WE}(31)$, $t_{WH}(31)$, $t_{OE}(40)$, $t_{OC}(9)$, $t_{OA}(7)$, $t_{DQ}(32)$, $t_{WE}(24)$, $t_{DS}(38)$, $t_{AA}(7)$, and $t_{RE}(23)$.

RAS-ONLY REFRESH CYCLE



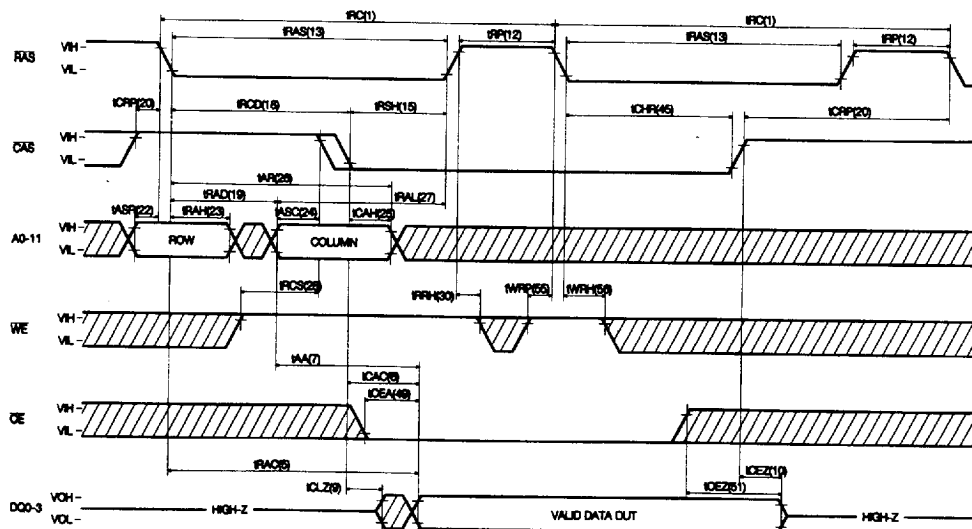
NOTE : $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

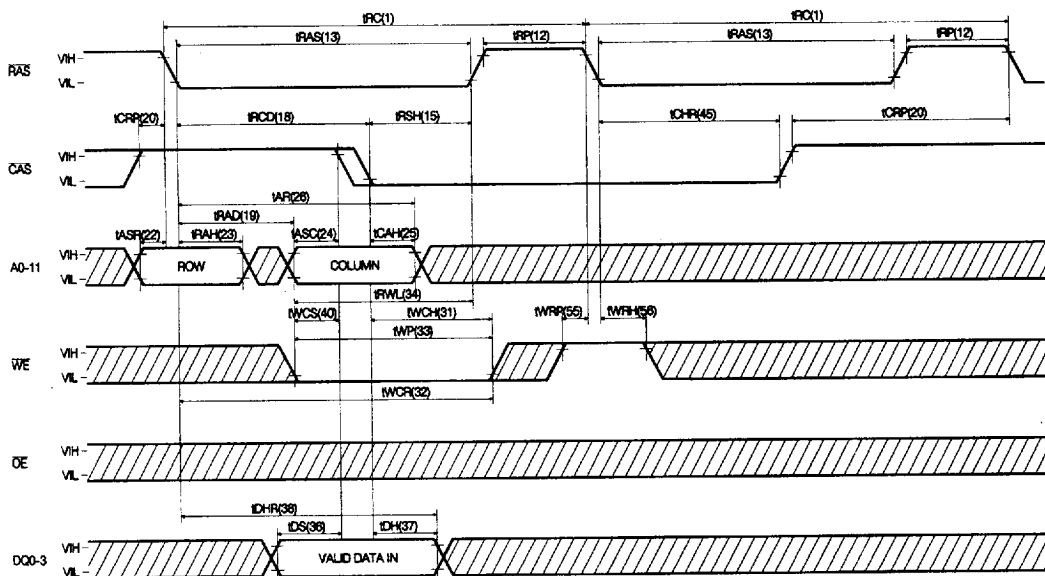


NOTE : A0-A11 and $\overline{OE}$ = "H" or "L"

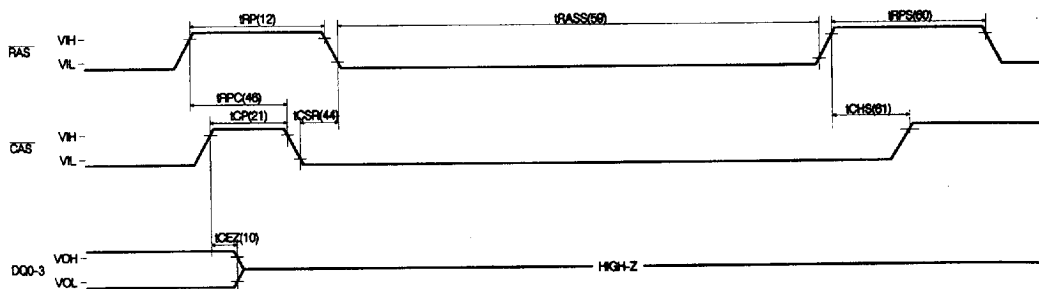
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS-BEFORE-RAS SELF REFRESH CYCLE

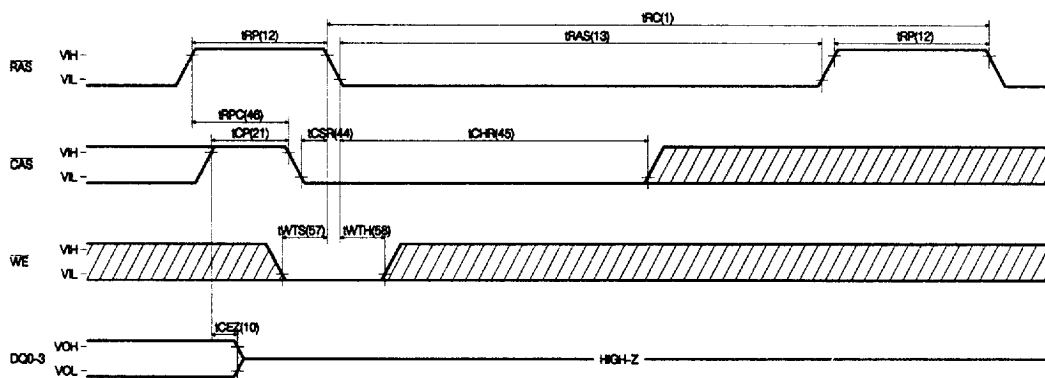


NOTE : A0-11, OE and WE = "H" or "L"

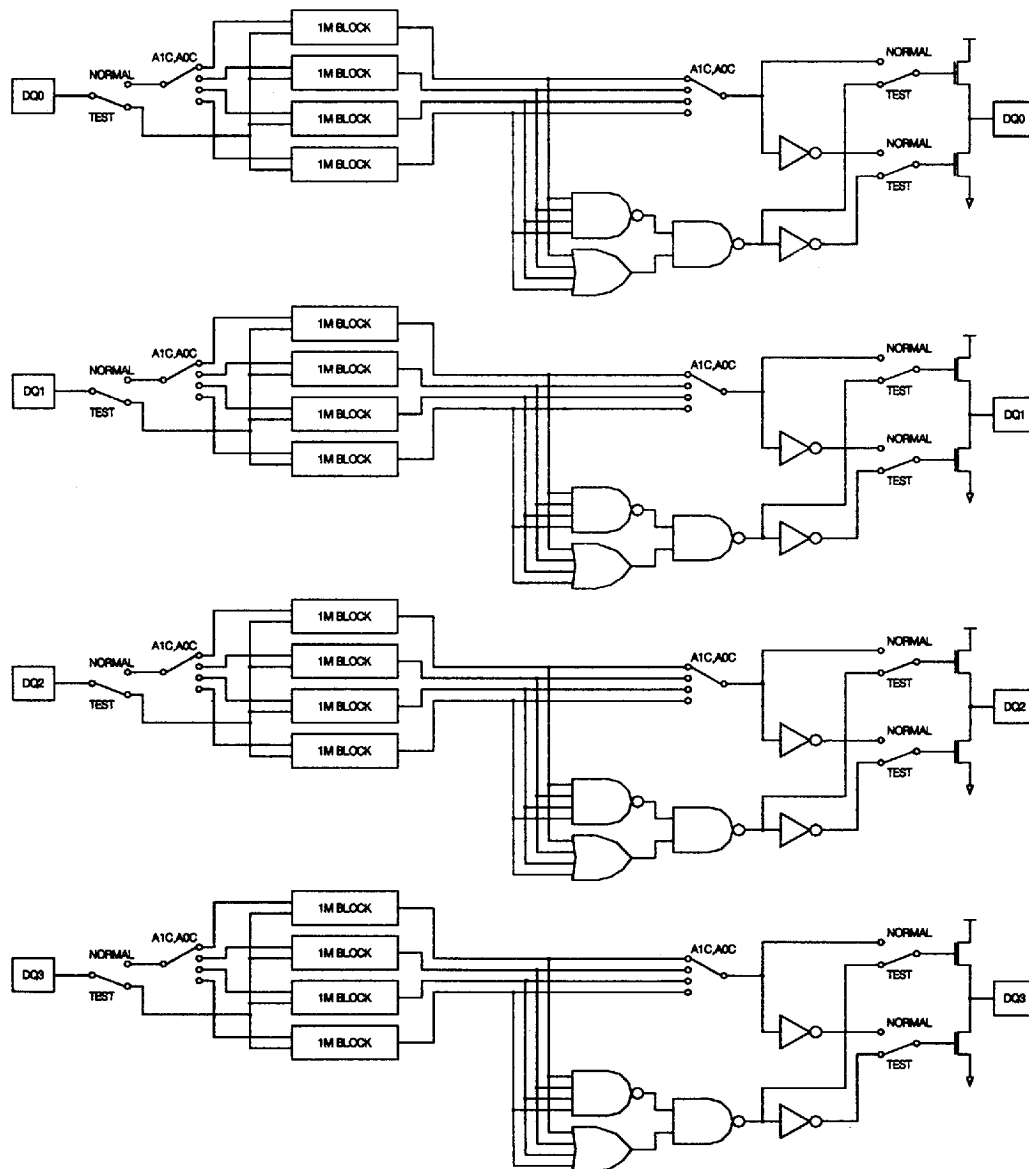
TEST MODE

The HY5116404B is a DRAM organized 4,194,304 x 4-bit. It is internally organized 1,048,576 x 16-bit. In Test Mode, data are written into 16 sectors (Each is composed of 1M bits) in parallel and retrieved the same way. Column address A0, and A1, are not used. If, upon reading, 4-bit data from 4 sectors connected to one DQ pin are equal (all "1" or "0"s), the DQ pin indicates a "1". If they are not equal, the DQ pin indicates a "0". Below shows the timing diagram of the HY5116404B to enter Test Mode. In Test Mode, the 4M x 4 DRAM can be tested as if it were a 1M x 4 DRAM. WE, CAS-before-RAS cycle (Test Mode In Cycle) puts the HY5116404B into Test Mode and CAS-before-RAS or RAS-only refresh cycle puts it back into Normal Mode. In Test Mode, WE, CAS-before-RAS cycle shall be used for the refresh operation. The Test Mode function reduces test time (1/4 in case of N test pattern).

TEST MODE IN CYCLE

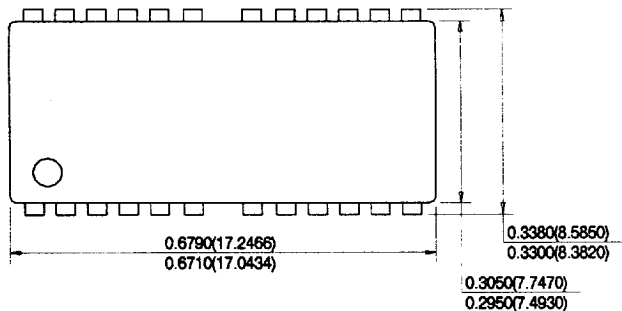


BLOCK DIAGRAM IN TEST MODE

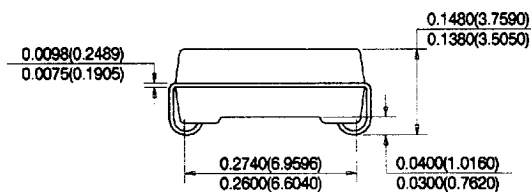
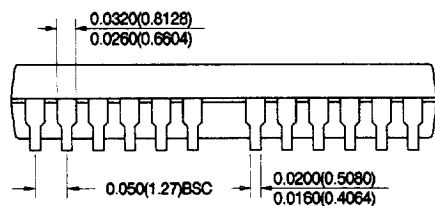


PACKAGE INFORMATION

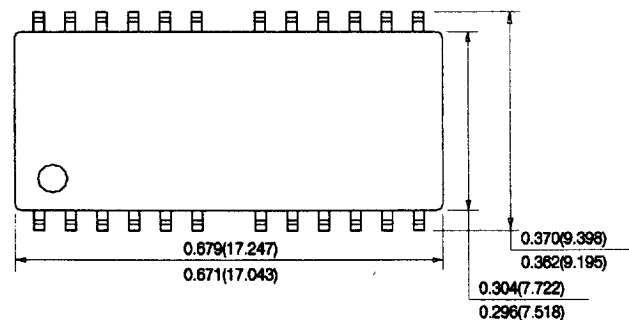
300 mil 24/26 pin Small Outline J-form Package (J)



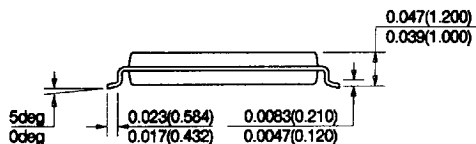
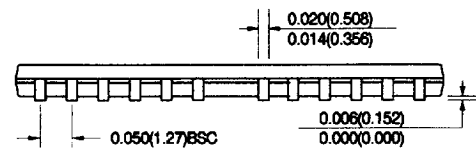
UNIT : INCH(mm)



300 mil 24/26 pin Thin Small Outline Package (T) (R)



UNIT : INCH(mm)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY5116404BJ	50/60/70		SOJ
HY5116404BSLJ	50/60/70	SL-part	SOJ
HY5116404BT	50/60/70	SL-part	TSOP-II
HY5116404BSLT	50/60/70		TSOP-II
HY5116404BR	50/60/70	SL-part	TSOP-II(R)
HY5116404BSLR	50/60/70	SL-part	TSOP-II(R)