MOTOROLA

Advance Information

6226A

Commercial Plus and Mil/Aero Applications

128K x 8 Bit Fast Static Random Access Memory

ELECTRICALLY TESTED PER:
MPG6226A

AVAILABLE AS
1) JAN: N/A
2) SMD: Pending
3) 883: 6226A - XX/BXAJC
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: DIL: X
LCC: U
FP: Y
XX = Speed in ns (25, 30, 35, 45, 55, 70, 100)
The letter "M" appears after the speed on LCC

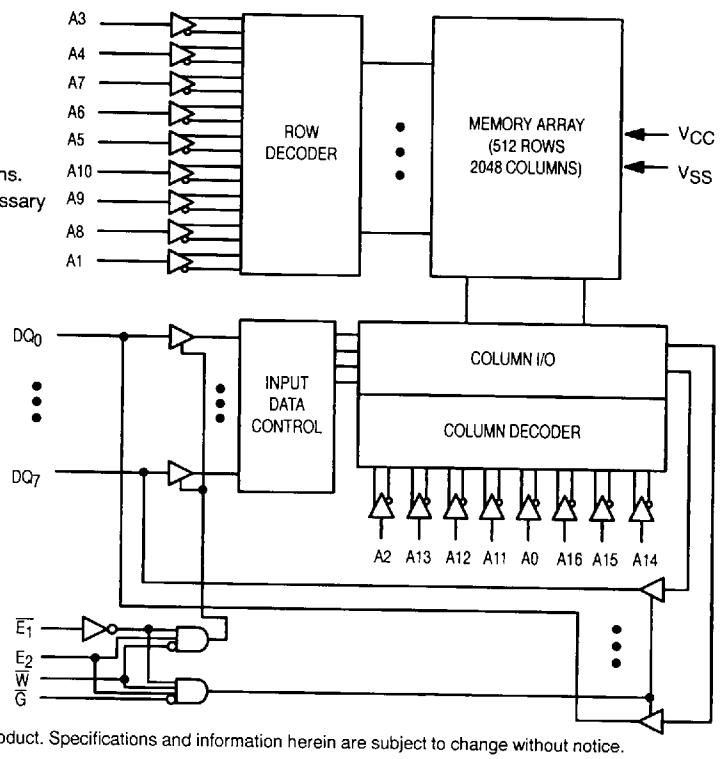
The 6226A is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits, fabricated using high performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The 6226A is equipped with 2 chip enable ($\overline{E_1}$, E_2) and 1 output enable ($\overline{G}$) inputs allowing for greater system flexibility as well as the prevention of Data Bus contention problems. Either input, when biased to disable, will force the outputs to high impedance. In case of only ($\overline{G}$) being disabled, the memory chip is not deselected, and data can be written into the memory without the problem of data bus contention.

The 6226A is available in a 600 mil ceramic DIL, 550 x 850 mil surface-mount LCC, or a 490 x 830 Flat Pack. All packages are 32 pins.

- Power Dissipation: 160/150/140/130 mA Maximum, Active AC
  - 25 ns = 160 mA
  - 30 ns = 150 mA
  - 35 ns = 140 mA
  - 45 ns = 130 mA
  - 55 ns = 120 mA
  - 70 ns = 110 mA
  - 100 ns = 90 mA
- Single 5.0 V ± 10% Power Supply
- Full Address Access Time — 25, 30, 35, 45 ns.
- Fully Static — No Clock/Timing Strobe Necessary
- Two Chip Select Controls
- One Output Enable Control
- Three State Outputs
- Fully TTL Compatible

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BURN-IN CONDITIONS:

V_{CC} = 5.0 V(min)/ 6.0 V(max), R_1 = 39.2 kΩ ± 20%, C_1 = 0.1 µF ± 20%, V_H = 3.0 V(min)/5.0 V(max), V_L = – 0.5 V(min)/0.0 V(max),

CP1:	100 kHz	CP6:	3.125 kHz	CP11:	97.66 Hz	CP16:	3.052 Hz
CP2:	50 kHz	CP7:	1.563 kHz	CP12:	48.83 Hz	CP17:	1.526 Hz
CP3:	25 kHz	CP8:	0.781 kHz	CP13:	24.41 Hz	CP18:	0.763 Hz
CP4:	12.5 kHz	CP9:	0.391 kHz	CP14:	12.21 Hz	CP19:	0.382 Hz
CP5:	6.25 kHz	CP10:	0.195 kHz	CP15:	6.104 Hz	CP20:	0.191 Hz

PIN NAME and FUNCTIONS

$A_0 - A_{16}$	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$, E	Chip Enable
$\overline{G}$	Output Enable
$DQ_0 - DQ_7$	Data Input/Outputs
V_{CC}	+ 5.0 V Power Supply
V_{SS}	Ground
N.C.	No Connection

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit.

PIN ASSIGNMENTS

Function	DIL 875-01	LCC 766C-01	FP	Burn-In (Condition-D)
N.C.	1	1	1	N.C.
A_{16}	2	2	2	CP2
A_{14}	3	3	3	CP3
A_{12}	4	4	4	CP4
A_7	5	5	5	CP5
A_6	6	6	6	CP6
A_5	7	7	7	CP7
A_4	8	8	8	CP8
A_3	9	9	9	CP9
A_2	10	10	10	CP10
A_1	11	11	11	CP11
A_0	12	12	12	CP12
DQ_0	13	13	13	CP20 to R_1
DQ_1	14	14	14	CP20 to R_1
DQ_2	15	15	15	CP20 to R_1
V_{SS}	16	16	16	GND
DQ_3	17	17	17	CP20 to R1
DQ_4	18	18	18	CP21 to R1
DQ_5	19	19	19	CP21 to R_1
DQ_6	20	20	20	CP21 to R_1
DQ_7	21	21	21	CP21 to R_1
$\overline{E}$	22	22	22	GND
A_{10}	23	23	23	CP18
$\overline{G}$	24	24	24	CP19
A_{11}	25	25	25	CP17
A_9	26	26	26	CP16
A_8	27	27	27	CP15
A_{13}	28	28	28	CP14
$\overline{W}$	29	29	29	CP1
E	30	30	30	HIGH
A_{15}	31	31	31	CP13
V_{CC}	32	32	32	V_{CC}, C_1 to GND

TRUTH TABLE

$\overline{E_1}$	E_2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	DQ Pin	Data Operation
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High Z	Don't Care
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High Z	Don't Care
L	H	H	H	Read Suppressed	I_{CCA}	High Z	Don't Care
L	H	L	H	Read	I_{CCA}	Active	D_{OUT}
L	H	X	L	Write	I_{CCA}	High Z	D_{IN}

X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)			
Rating	**Symbol**	**Value**	**Unit**
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{IN}, V_{OUT}	− 0.5 to V_{CC} + 0.5	V
Output Current	I_{OUT}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias (T_A = 25°C)	T_{bias}	− 55 to +125	°C
Storage Temperature Range	T_{stg}	− 65 to +150	°C
Operating Temperature Range	T_A	− 55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = − 55°C to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS					
Parameter	**Symbol**	**Min**	**Nominal**	**Max**	**Unit**
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	− 0.5 *	0.0	0.8	V

* V_{IL} (min) = − 0.5 Vdc; V_{IL} (min) = − 3.0 Vdc (pulse width ≤ 20 ns)

DC CHARACTERISTICS						
Parameter		**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	—	± 10	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{OUT} = 0 to V_{CC})		$I_{lkg(O)}$	—	—	± 10	µA
AC Supply Current (I_{OUT} = 0 mA)	6226A-25: t_{AVAV} = 25 ns	I_{CCA}	—	—	140	mA
	6226A-30: t_{AVAV} = 30 ns	I_{CCA}	—	—	140	mA
	6226A-35: t_{AVAV} = 35 ns	I_{CCA}	—	—	135	mA
	6226A-45: t_{AVAV} = 45 ns	I_{CCA}	—	—	125	mA
	6226A-55: t_{AVAV} = 55 ns	I_{CCA}	—	—	125	mA
	6226A-70: t_{AVAV} = 70 ns	I_{CCA}	—	—	120	mA
	6226A-100: t_{AVAV} = 100 ns	I_{CCA}	—	—	110	mA
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	—	—	25	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 2.0 V, No Restrictions on Other Inputs)		I_{SB2}	—	—	10	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = − 4.0 mA)		V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)					
Characteristic		**Symbol**	**Typ**	**Max**	**Unit**
Input Capacitance	All Inputs Except $\overline{E}$, E and DQ $\overline{E}$, E	C_{in}	4.0 5.0	6.0 7.0	pF pF
I/O Capacitance	DQ	$C_{I/O}$	5.0	7.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 55°C to +125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level	1.5 V
Input Pulse levels	0 to 3.0 V
Input Rise/Falls Time	≥ 5.0 ns
Output Timing Measurement Reference Level	1.5 V
Output Load	See Figure 1A

AC TEST LOADS OR EQUIVALENT

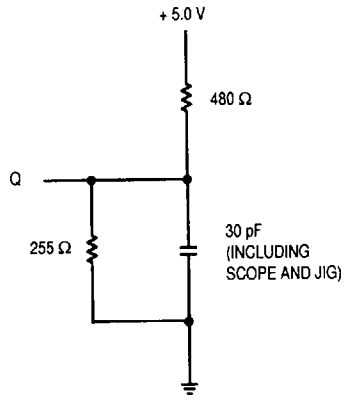


Figure 1A.

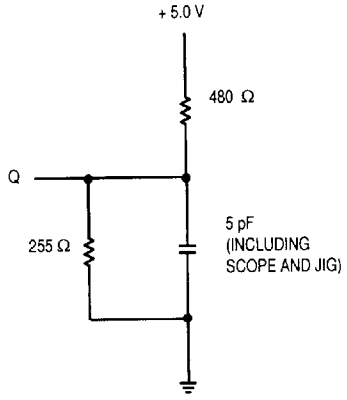
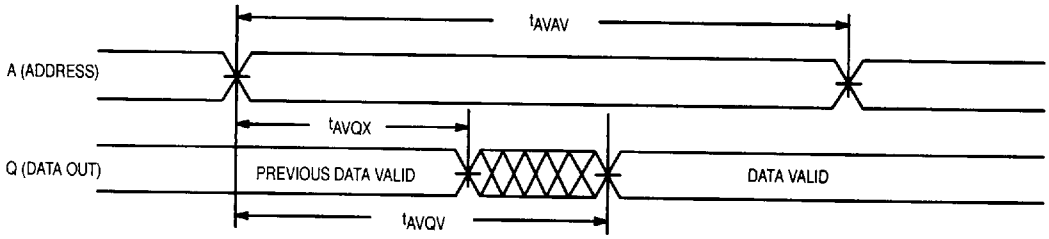


Figure 1B.

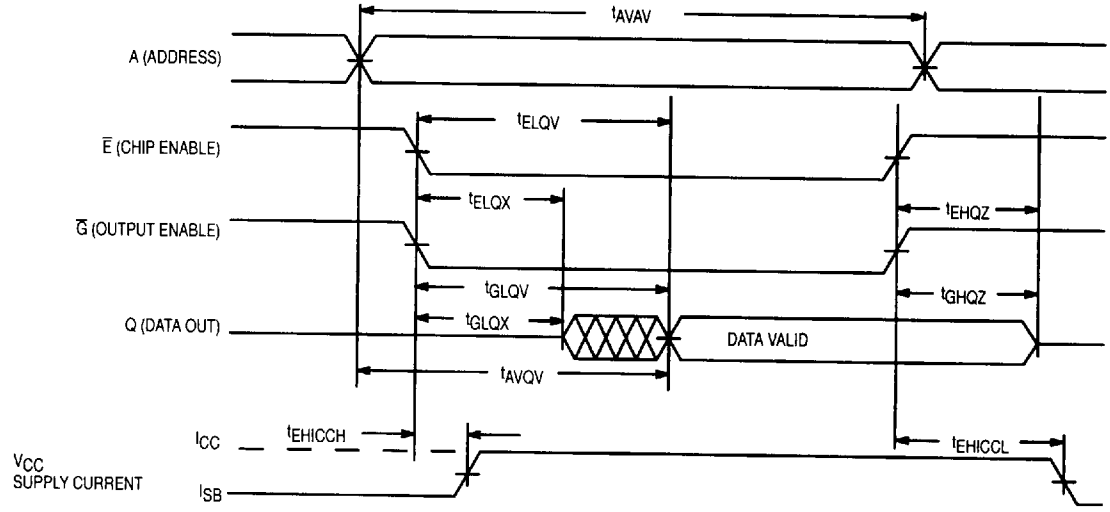
READ CYCLE (See Note 1)												
Parameter	Symbol Standard	Symbol Alternate	6226A-25		6226A-30		6226A-35		6226A-45		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	—	30	—	35	—	45	—	ns	2, 5, 7
Address Access Time	t_{AVQV}	t_{AA}	—	25	—	30	—	35	—	45	ns	5, 7
Chip Select Access Time	t_{ELQV}	t_{ACS}	—	25	—	30	—	35	—	45	ns	6
Output Enable Access Time	t_{GLQV}	t_{OE}	—	10	—	10	—	15	—	20	ns	5
Prior Output Hold Time After Address Change	t_{AVQX}	t_{OH}	3.0	—	3.0	—	3.0	—	3.0	—	ns	5, 7
Output High Z after Chip Enable	t_{ELQX}	t_{CLZ}	3.0	—	3.0	—	3.0	—	3.0	—	ns	3, 4, 6, 7
Output High Z after Chip Disable	t_{EHQZ}	t_{CHZ}	—	10	—	10	—	15	—	20	ns	3, 4, 7
Output High Z after Output Enable	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	ns	3, 4, 5
Output High Z after Output Disable	t_{GHQZ}	t_{OHZ}	0	10	0	10	0	15	0	20	ns	3, 4, 5
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	ns	4
Power Down Time	t_{EHICCL}	t_{PD}	—	25	—	30	—	35	—	45	ns	4

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
4. These parameters are periodically sampled and not 100% tested.
5. Device is continuously selected ($\overline{E_1} = V_{IL}$, $E_2 = V_{IH}$).
6. Address valid prior to coincident with $\overline{E_1}$ going low/E_2 going high.
7. Outputs are continuously enabled ($\overline{G} = V_{IL}$).

READ CYCLE 1 (See Note 5 and 7 above)



READ CYCLE 2 (See Note 6 above)



READ CYCLE (See Note 1)										
Parameter	Symbol Standard	Symbol Alternate	6226A-55		6226A-70		6226A-100		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	55	—	70	—	100	—	ns	2, 5, 7
Address Access Time	t_{AVQV}	t_{AA}	—	55	—	70	—	100	ns	5, 7
Chip Select Access Time	t_{ELQV}	t_{ACS}	—	55	—	70	—	100	ns	6
Output Enable Access Time	t_{GLQV}	t_{OE}	—	20	—	25	—	25	ns	5
Prior Output Hold Time After Address Change	t_{AVQX}	t_{OH}	3.0	—	3.0	—	3.0	—	ns	5, 7
Output High Z after Chip Enable	t_{ELQX}	t_{CLZ}	3.0	—	3.0	—	3.0	—	ns	3, 4, 6, 7
Output High Z after Chip Disable	t_{EHQZ}	t_{CHZ}	—	20	—	30	—	30	ns	3, 4, 7
Output High Z after Output Enable	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	3, 4, 5
Output High Z after Output Disable	t_{GHQZ}	t_{OHZ}	0	20	0	30	0	30	ns	3, 4, 5
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns	4
Power Down Time	t_{EHICCL}	t_{PD}	—	55	—	70	—	100	ns	4

NOTES:
1. $\overline{W}$ is high for read cycle.
2 All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
4. These parameters are periodically sampled and not 100% tested.
5. Device is continuously selected ($\overline{E_1} = V_{IL}$, $E_2 = V_{IH}$).
6. Address valid prior to coincident with $\overline{E_1}$ going low/E_2 going high.
7. Outputs are continuously enabled ($\overline{G} = V_{IL}$).

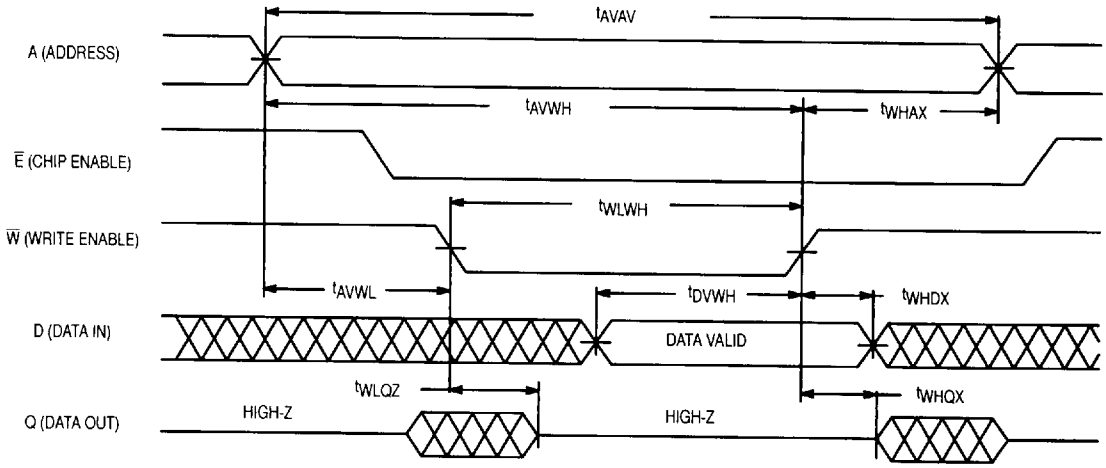
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)												
Parameter	Symbol Standard	Symbol Alternate	6226A-25		6226A-30		6226A-35		6226A-45		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	45	—	ns	2
Write Address Setup Time	t_{AVWL}	t_{WAS}	0	—	0	—	0	—	0	—	ns	—
Write Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	20	—	25	—	35	—	ns	—
Write Pulse Width	t_{WLWH}	t_{WP}	20	—	20	—	30	—	35	—	ns	—
Write Data Valid to End of Write	t_{DVWH}	t_{DWS}	15	—	15	—	20	—	25	—	ns	—
Write Data Hold Time	t_{WHDX}	t_{DWH}	0	—	0	—	0	—	0	—	ns	—
Write Enable Time	t_{WLQZ}	t_{WZ}	0	10	0	10	0	15	0	20	ns	4
Output High Z after Write Disable	t_{WHQX}	t_{WHZ}	5.0	—	5.0	—	5.0	—	5.0	—	ns	4
Write Address Hold Time	t_{WHAX}	t_{WAH}	5.0	—	5.0	—	5.0	—	5.0	—	ns	—

NOTES:
1. A write occurs during the overlap of $\overline{W}$ low while continuously $\overline{E_1}$ is low and E_2 high.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
4. Parameters is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol Standard	Symbol Alternate	6226A-55		6226A-70		6226A-100		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	55	—	70	—	100	—	ns	2
Write Address Setup Time	t_{AVWL}	t_{WAS}	0	—	0	—	0	—	ns	—
Write Address Valid to End of Write	t_{AVWH}	t_{AW}	35	—	45	—	45	—	ns	—
Write Pulse Width	t_{WLWH}	t_{WP}	35	—	40	—	40	—	ns	—
Write Data Valid to End of Write	t_{DVWH}	t_{DWS}	30	—	35	—	40	—	ns	—
Write Data Hold Time	t_{WHDX}	t_{DWH}	0	—	0	—	0	—	ns	—
Write Enable Time	t_{WLQZ}	t_{WZ}	0	20	0	35	0	35	ns	4
Output High Z after Write Disable	t_{WHQX}	t_{WHZ}	5.0	—	5.0	—	5.0	—	ns	4
Write Address Hold Time	t_{WHAX}	t_{WAH}	5.0	—	5.0	—	5.0	—	ns	—

WRITE CYCLE 1 ($\overline{W}$ Controlled)



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, response delays from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device should never provide data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)												
Parameter	Symbol Standard	Symbol Alternate	6226A-25		6226A-30		6226A-35		6226A-45		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	45	—	ns	2
Chip Select Address Setup Time	t_{AVEL}	t_{CAS}	0	—	0	—	0	—	0	—	ns	—
Chip Enable Address Valid Time	t_{AVEH}	t_{AC}	20	—	20	—	25	—	35	—	ns	—
Chip Enable Write Pulse Width	t_{ELEH}	t_{CW}	20	—	20	—	25	—	35	—	ns	3
Write Start before Chip Disable Time	t_{ELWH}	t_{CWW}	20	—	20	—	25	—	35	—	ns	—
Write Data Valid to End of Chip Enable	t_{DVEH}	t_{DCS}	15	—	15	—	20	—	25	—	ns	—
Write Data Hold Time after Chip Disable	t_{EHDX}	t_{DCH}	0	—	0	—	0	—	0	—	ns	—
Write Address Hold Time after Chip Disable	t_{EHAX}	t_{CAH}	5.0	—	5.0	—	5.0	—	5.0	—	ns	—

NOTES:
1. A write occurs during the overlap of $\overline{E}_1$ low and E_2 high while $\overline{W}$ is preconditioned low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. $\overline{W}$ remains low when chip enable pulse applies to write memory. Verify memory contents in the next upcoming Read Cycles.

Parameter	Symbol Standard	Symbol Alternate	6226A-55		6226A-70		6226A-100		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	55	—	70	—	100	—	ns	2
Chip Select Address Setup Time	t_{AVEL}	t_{CAS}	0	—	0	—	0	—	ns	—
Chip Enable Address Valid Time	t_{AVEH}	t_{AC}	35	—	45	—	45	—	ns	—
Chip Enable Write Pulse Width	t_{ELEH}	t_{CW}	35	—	40	—	40	—	ns	3
Write Start before Chip Disable Time	t_{ELWH}	t_{CWW}	35	—	45	—	45	—	ns	—
Write Data Valid to End of Chip Enable	t_{DVEH}	t_{DCS}	30	—	35	—	40	—	ns	—
Write Data Hold Time after Chip Disable	t_{EHDX}	t_{DCH}	0	—	0	—	0	—	ns	—
Write Address Hold Time after Chip Disable	t_{EHAX}	t_{CAH}	5.0	—	5.0	—	5.0	—	ns	—

WRITE CYCLE 2 ($\overline{E}$ Controlled)