National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM118-X REV 0A0

Original Creation Date: 06/30/95
Last Update Date: 03/23/00
Last Major Revision Date: 02/29/00

OPERATIONAL AMPLIFIER

General Description

The LM118 is a precision high speed operational amplifier designed for applications requiring wide bandwith and high slew rate. It features a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/uS and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1uS.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. This devices is easy to apply and offers an order of magnitude better AC performance than industry standards such as the LM709.

Industry Part Number

LM118

Prime Die

LM118

NS Part Numbers

LM118H/883
LM118J-8/883
LM118J/883
LM118WG/883

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 15 MHz small signal bandwidth
- Guaranteed 50V/uS slew rate
- Maximum bias current of 250nA
- Operates from supplies of ±5V to ±20V
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage		±20V
Power Dissipation (Note 2)		
Metal Can Pkg		750mW
J-8 Pkg		1000mW
J-14 Pkg		1250mW
CERAMIC SOIC		600mW
Differential Input Current (Note 3)		±10mA
Input Voltage (Note 4)		±15V
Output Short-Circuit Duration		Continuous
Operating Temperature Range		-55 C to +125 C
Thermal Resistance		
ThetaJA		
Metal Can Pkg	(Still Air @ 0.5W)	160 C/W
	(500LF/Min Air flow @ 0.5W)	86 C/W
J-8 Pkg	(Still Air @ 0.5W)	120 C/W
	(500LF/Min Air flow @ 0.5W)	66 C/W
J-14 Pkg	(Still Air @ 0.5W)	87 C/w
	(500LF/Min Air flow @ 0.5W)	51 C/W
CERAMIC SOIC	(Still Air @ 0.5W)	198 C/W
	(500LF/Min Air flow @ 0.5W)	124 C/W
ThetaJC		
Metal Can Pkg		48 C/W
J-8 Pkg		17 C/W
J-14 Pkg		17 C/W
CERAMIC SOIC		22 C/W
Storage Temperature Range		-65 C to +150 C
Lead Temperature (Soldering, 10 seconds)		300 C
ESD Tolerance (Note 5)		2000V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guaranteed specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 4: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 5: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Vcm = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	Vcm = ±11.5V, Rs=50 Ohms			-4	+4	mV	1
					-6	+6	mV	2, 3
		Vcc = ±20V, Rs=50 Ohms			-4	+4	mV	1
					-6	+6	mV	2, 3
		Vcc = ±20V, Vcm = ±15V, Rs=50 Ohms			-4	+4	mV	1
					-6	+6	mV	2, 3
		Vcc = ±5V, Rs=50 Ohms			-4	+4	mV	1
					-6	+6	mV	2, 3
Iio	Input Offset Current	Vcm = ±11.5V, Rs=10K Ohms			-50	+50	nA	1
					-100	+100	nA	2, 3
		Vcc = ±20V, Rs=10K Ohms			-50	+50	nA	1
					-100	+100	nA	2, 3
		Vcc = ±5V, Rs=10K Ohms			-50	+50	nA	1
					-100	+100	nA	2, 3
Iib	Input Bias Current	Vcm = ±11.5V, Rs=10K Ohms			1	250	nA	1
					1	500	nA	2, 3
		Vcc = ±20V, Rs=10K Ohms			1	250	nA	1
					1	500	nA	2, 3
		Vcc = ±5V, Rs=10K Ohms			1	250	nA	1
					1	500	nA	2, 3
PSRR	Power Supply Rejection Ratio	+Vcc = 20V to 5V, Rs=50 Ohms			70		dB	1, 2, 3
		-Vcc = -20V to -5V, Rs=50 Ohms			70		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	Vcc = ±15V, Vcm = ±11.5V, Rs=50 Ohms			80		dB	1, 2, 3
Ios+	Short Circuit Current	t<25mS			-65	-5	mA	1, 2, 3
Ios-	Short Circuit Current	t<25mS			5	65	mA	1, 2
					5	80	mA	3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Vcm = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Icc	Power Supply Current	Vcc = ±20V				8	mA	1
						7	mA	2
						11	mA	3
VioAdj	Input Offset Voltage Adjust	Vcc = ±20V			4	-4	mV	1
Rin	Input Resistance		2		1		MOhms	1
Vin	Input Voltage Range	Vcc = ±15V	1		-11.5	+11.5	V	1, 2, 3
Avs	Large Signal Voltage Gain	Rl=2K Ohms, Vo=0 to -10V	3		50		V/mV	4
			3		25		V/mV	5, 6
		Rl=2K Ohms, Vo=0 to +10V	3		50		V/mV	4
			3		25		V/mV	5, 6
Vout	Output Voltage Swing	Rl=2K Ohms			+12	-12	V	4, 5, 6

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = ±15V, Vcm = 0, Rs = 0, Rl = 2K Ohms, Cl = 33pF

Sr	Slew Rate	Vcc = ±20V, Vin = -5V to +5V, Av=1	4		50		V/uS	7
		Vcc = ±20V, Vin = +5V to -5V, Av=1	4		50		V/uS	7

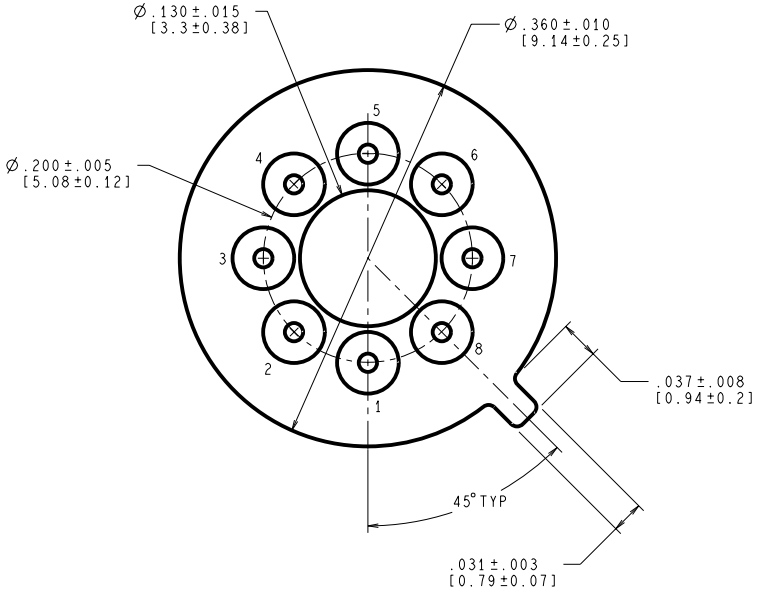
Note 1: Guaranteed by CMRR.
Note 2: Guaranteed parameter not tested.
Note 3: Datalog in K = V/mV
Note 4: Bench tested use TDN 25256223

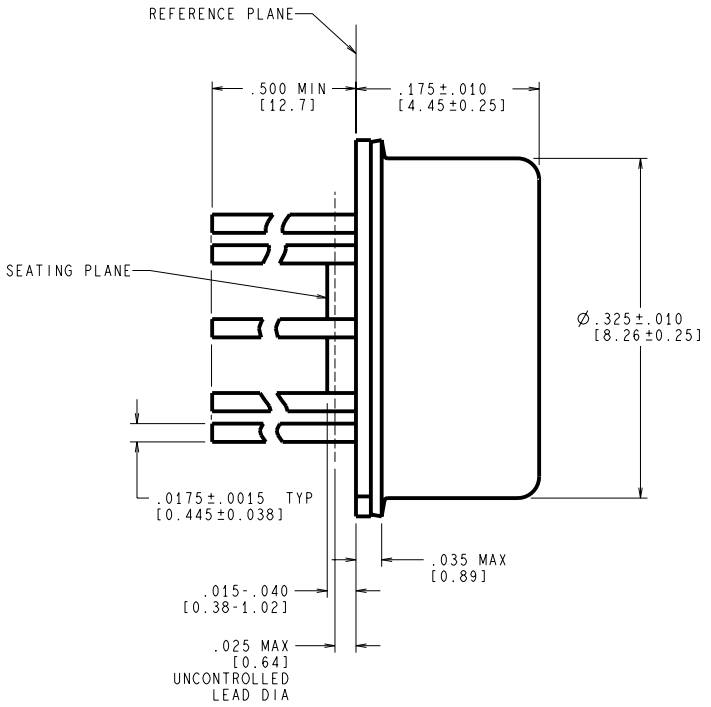
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05482HRA1	10LD CERPACK, 10LD CERAMIC SOIC (B/I CKT)
09556HR02	CERDIP (J14), CERDIP (J8) (B/I CKT)
09557HRA4	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000268A	METAL CAN (H), 8 LEAD (PINOUT)
P000315A	CERDIP (J), 8 LEAD (PINOUT)
P000316A	CERDIP (J), 14 LEAD (PINOUT)
P000459A	CERPACK, 10 LEAD (PINOUT)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

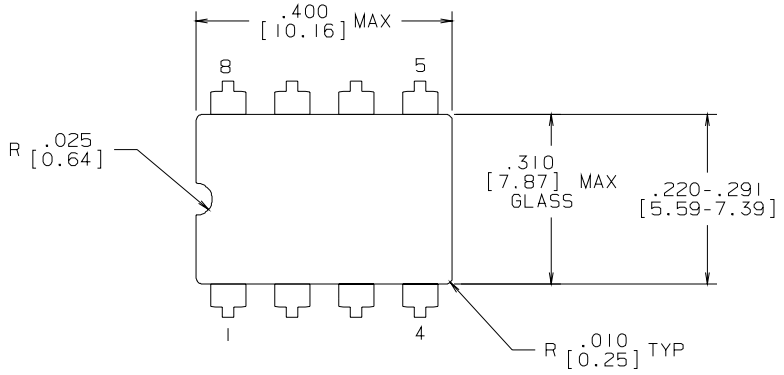
METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

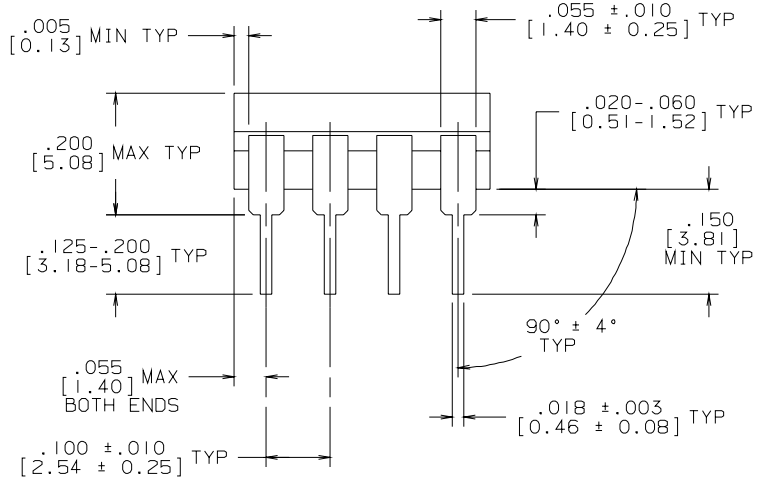
PROJECTION — INCH [MM]

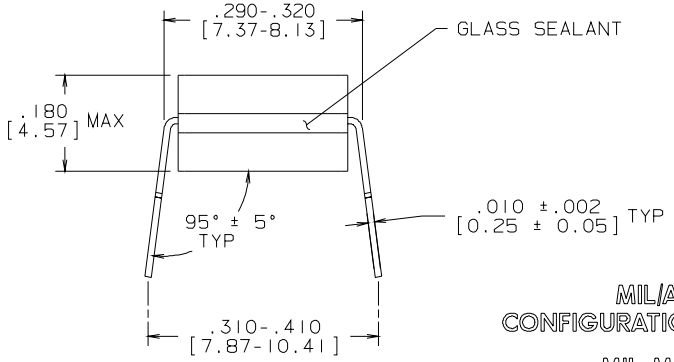
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

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CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
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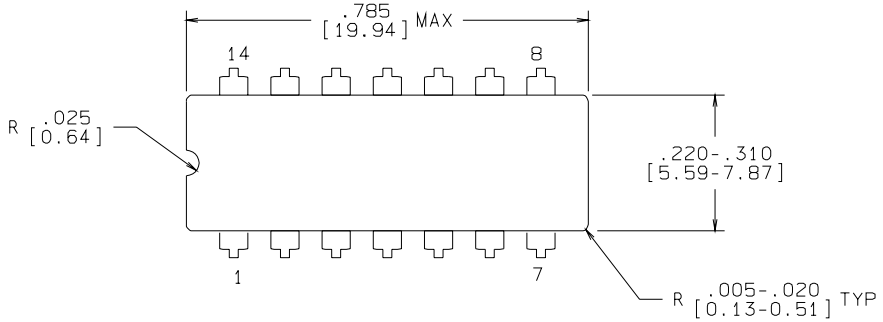

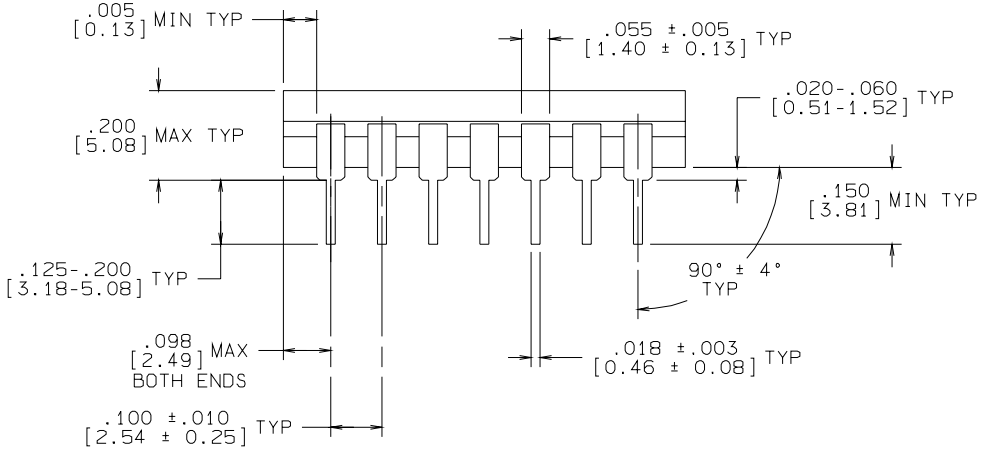

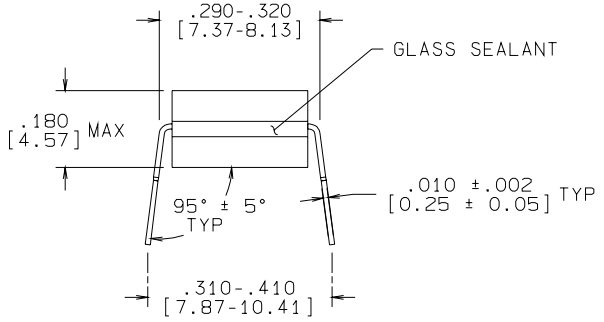

CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

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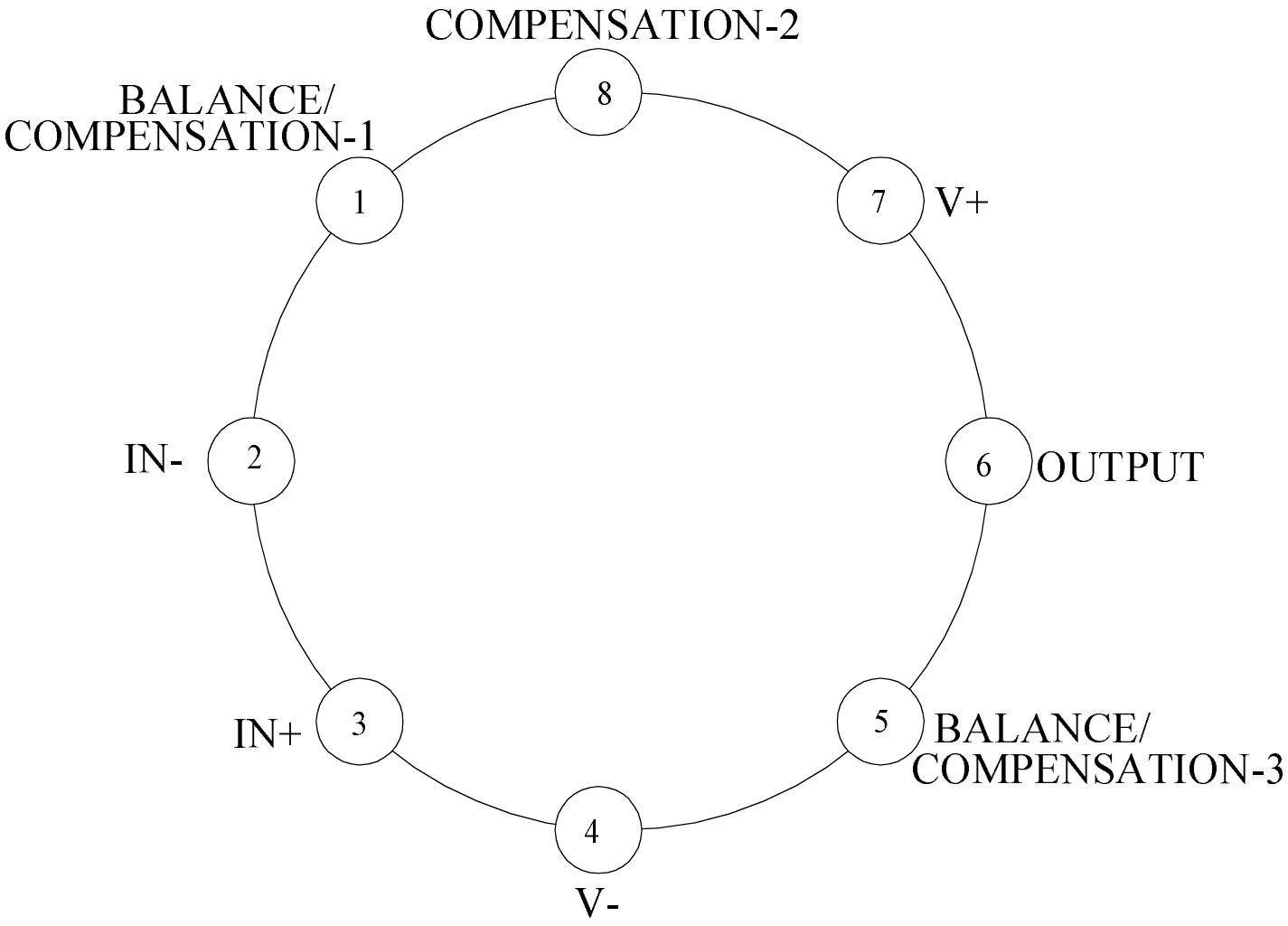
CERDIP (J), 14 LEAD,

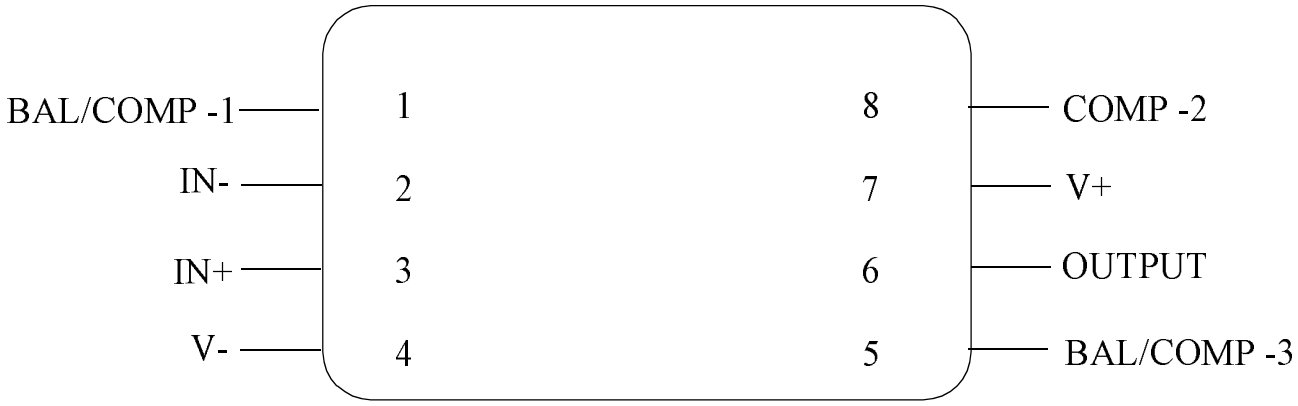
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



LM118H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000268A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM118J-8

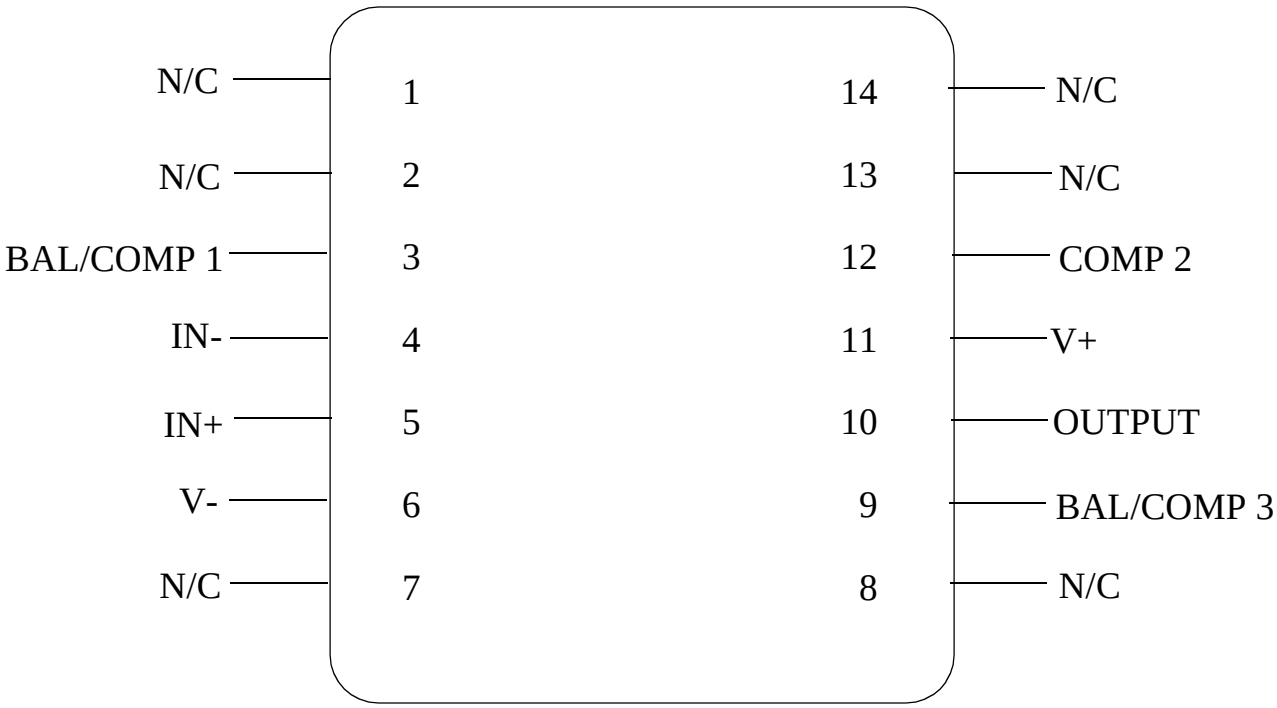
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

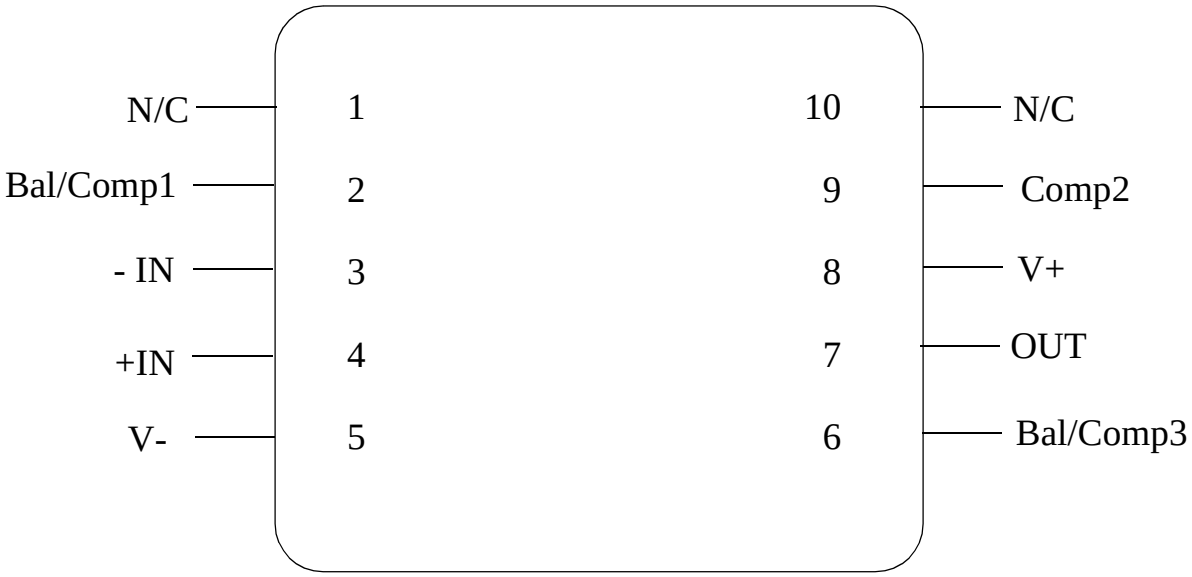
P000315A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM118J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000316A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM118WG

10 - LEAD CERAMIC SOIC

CONNECTION DIAGRAM

TOP VIEW

P000459A

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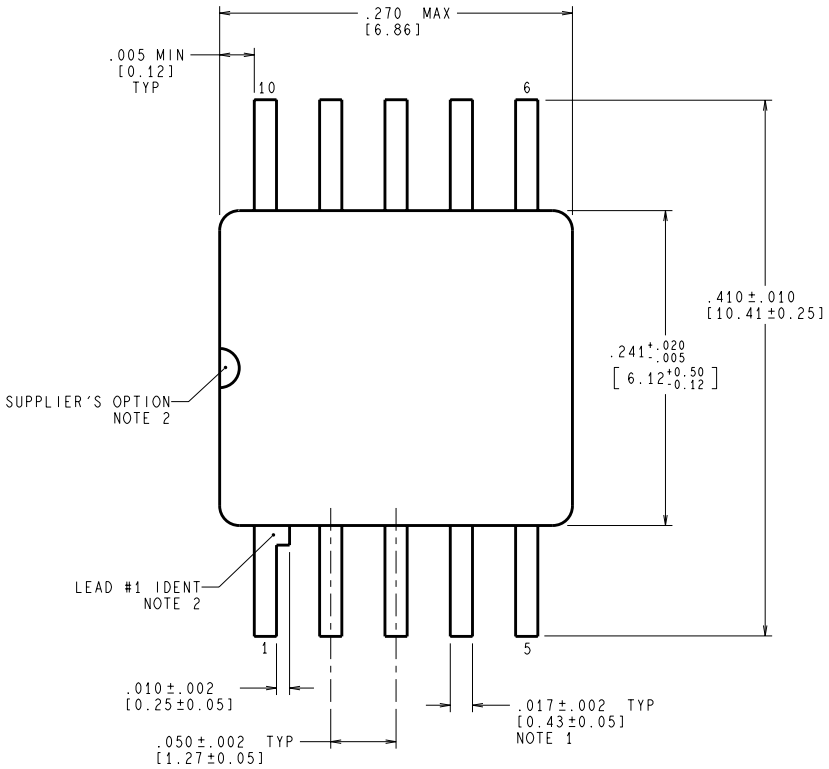
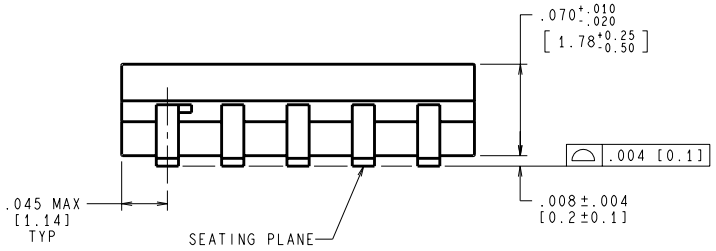
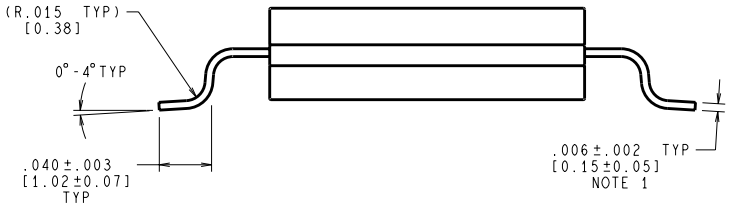
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

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2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 10 LEAD, GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG10A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003641	03/23/00	Rose Malone	Update MDS - MNLM118-X, Rev. 0AL to MNLM118-X, Rev. 0A0 Fully Released MDS. Archive/Obsolete RETS118X, Rev. AA