Features

128Kx32 bit CMOS Static
Random Access Memory

- Access Times
  BiCMOS: 10 and12ns
  CMOS: 15, 20, 25, 35, 55, 70, 85 and 100ns
- Individual Byte Selects
- Fully Static, No Clocks
- TTL Compatible I/O
- 2 Volt Data Retention Function (PLCC Package)

High Density Package

- JEDEC Standard Pinouts
- 64 Pad SIMM, No. 38 (10ns thru 35ns)
- 64 Pin ZIP, No. 39 (10ns thru 35ns)
- 68 Lead PLCC (55ns thru 100ns)
- Common Data Inputs and Outputs

Single +5V (±10%) Supply Operation

128Kx32 Static RAM
CMOS, High Speed Module

The EDI8F32128C is a high speed 4 megabit Static RAM module organized as 128K words by 32 bits. This module is constructed from four 128Kx8 Static RAMs in SOJ or TSOP packages on an epoxy laminate (FR4) board.

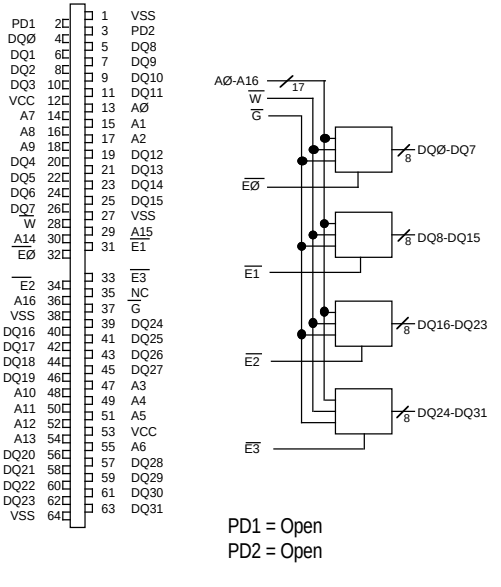
Four chip enables ($\overline{E}$Ø-$\overline{E3}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of enables.

The EDI8F32128C is offered in 64 pin ZIP, 64 Pad SIMM and 68 Lead PLCC packages, which enable four megabits of memory to be placed in less than 1.3 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

Two pins, PD1 and PD2, are used to identify module memory density in applications where alternate modules can be interchanged. (Zip and SIMM only) A low power version with 2 volt data retention functionality is also available (PLCC package only.)

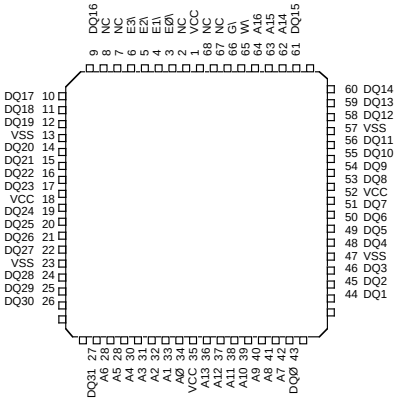
Pin Configurations and Block Diagram



PD1 = Open
PD2 = Open

Pin Names

AØ-A16	Address Inputs
$\overline{E}$Ø-$\overline{E3}$	Chip Enables
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ31	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial.	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	4 Watts
Output Current.	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load 10-35ns	1TTL, CL = 30pF
55-100ns	1 TTL, CL=100pf

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions		Min	Max 10-20ns	Max 25-35ns	Max 55-100ns	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle			680	480	360	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq$ VIH, VIN ≤ VIL or VIN ≥ VIH			120	112	80	mA
Full Standby Power	ICC3	$\overline{E} \geq$ VCC-0.2V	C		40	20	5	mA
Supply Current CMOS		VIN ≥ VCC-0.2V orVIN ≤ 0.2V	LP		--	--	400	µA
Input Leakage Current	ILI	VIN = 0V to VCC			±20	±20	±20	µA
Output Leakage Current	ILO	V I/O = 0V to VCC			±20	±20	±20	µA
Output High Voltage	VOH	IOH = -4.0mA(≤35), or -1.0mA (≥55)		2.4	--	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA(≤35), or 2.1mA (≥55)		--	0.4	0.4	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	X	Standby	HIGH Z	ICC2/ICC3
L	H	L	Read	DOUT	ICC1
L	L	X	Write	DIN	ICC1
L	H	H	Output Deselect	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	45	pF
Data Lines	CD/Q	20	pF
Chip Enable Line	CC	20	pF
Write Line	CN	45	pF

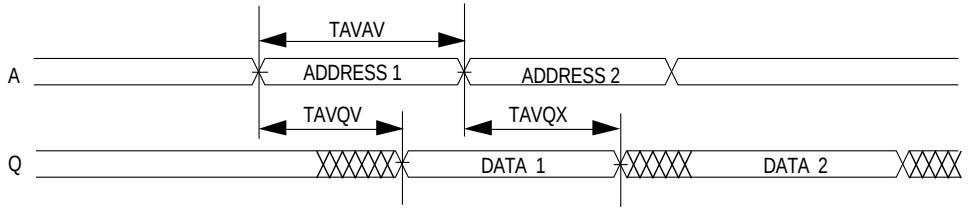
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

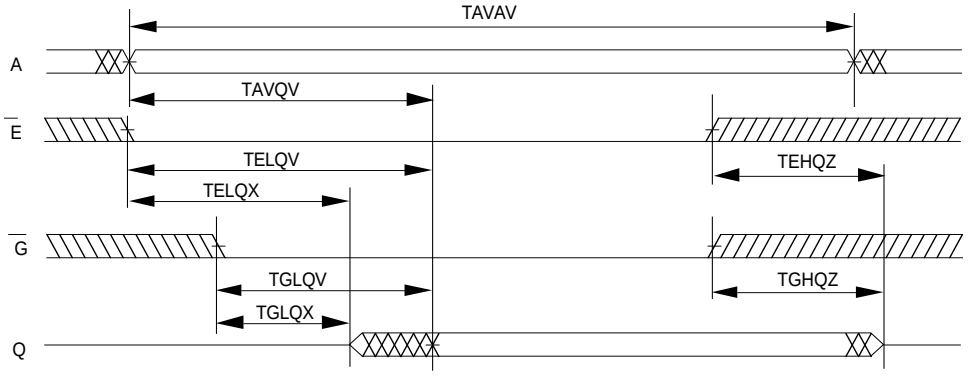
	Symbol		10ns*		12ns*		15ns		20ns		25ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	10		12		15		20		25		ns
Address Access Time	TAVQV	TAA		10		12		15		20		25	ns
Chip Enable Access	TELQV	TACS		10		12		15		20		25	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		5		6		8		10		12	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		5		5		6		13		15	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		4		4		5		8		10	ns

Note 1: Parameter guaranteed, but not tested. *BICMOS

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High



AC Characteristics Read Cycle

	Symbol		35ns		55ns		70ns		85ns		100ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	35		55		70		85		100		ns
Address Access Time	TAVQV	TAA		35		55		70		85		100	ns
Chip Enable Access	TELQV	TACS		35		55		70		85		100	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		5		5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		15		30		30		35		40	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		20		40		40		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		12		30		30		35		40	ns

Note 1: Parameter guaranteed, but not tested.

AC Characteristics Write Cycle

	Symbol		10ns*		12ns*		15ns		20ns		25ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Cycle Time	TAVAV	TWC	10		12		15		20		25		ns
Chip Enable to End of Write	TELWH	TCW	7		8		10		15		20		ns
	TWLEH	TCW	7		8		10		15		20		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	7		8		10		15		20		ns
	TAVEH	TAW	7		8		10		15		20		ns
Write Pulse Width	TWLWH	TWP	7		8		10		15		20		ns
	TELEH	TWP	7		8		10		15		20		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		0		ns
Data Hold Time	TWHDX	TDH	3		3		3		3		3		ns
	TEHDX	TDH	3		3		3		3		3		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	5	0	6	0	7	0	10	0	12	ns
Data to Write Time	TDVWH	TDW	5		6		7		12		15		ns
	TDVEH	TDW	5		6		7		12		15		ns
Output Active from End of Write (1)	TWHQX	TWLZ	2		2		2		3		3		ns

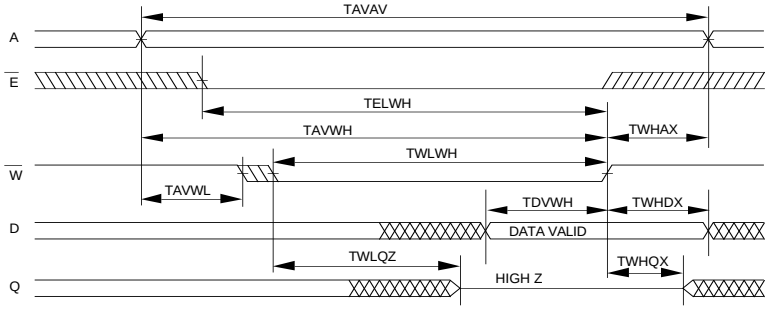
Note 1: Parameter guaranteed, but not tested. *BICMOS

AC Characteristics Write Cycle

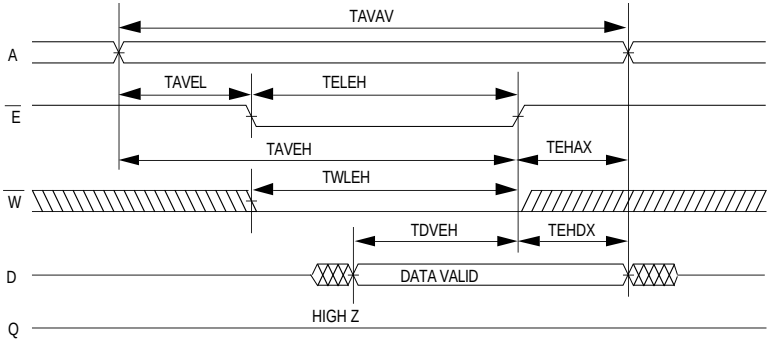
Parameter	Symbol JEDEC	Alt.	35ns Min	35ns Max	55ns Min	55ns Max	70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	Units
Write Cycle Time	TAVAV	TWC	35		55		70		85		100		ns
Chip Enable to End of Write	TELWH	TCW	30		50		65		70		80		ns
	TWLEH	TCW	30		50		65		70		80		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	30		50		65		70		80		ns
	TAVEH	TAW	30		50		65		70		80		ns
Write Pulse Width	TWLWH	TWP	25		50		65		70		80		ns
	TELEH	TWP	25		50		65		70		80		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		0		ns
Data Hold Time	TWHDX	TDH	3		0		0		0		0		ns
	TEHDX	TDH	3		0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	15	0	30	0	30	0	35	0	40	ns
Data to Write Time	TDVWH	TDW	20		30		30		35		40		ns
	TDVEH	TDW	20		30		30		35		40		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		5		5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 - $\overline{E}$ Controlled



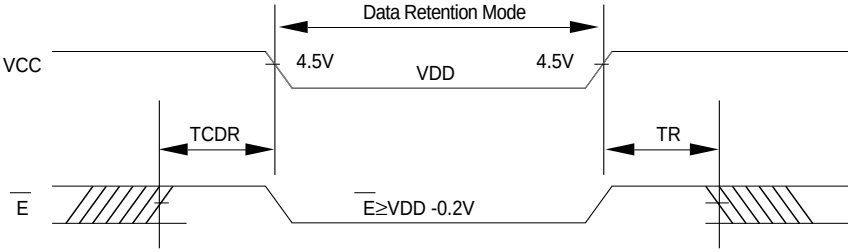
Data Retention Characteristics

EDI8F32128LP-BAC

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max		Unit
						70°C	80°C	
Data Retention Voltage	VDD	VDD = 0.2V		2	--	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E} \geq$ VDD -0.2V	2V	--	10	125	185	µA
		VIN ≥ VDD -0.2V	3V	--	20	200	250	µA
Chip Disable to Data Retention Time (1)	TCDR	or VIN ≤ 0.2V		0	--	--	--	ns
Operation Recovery Time (1)	TR			5	--	--	--	ns

Note 1: Parameter guaranteed, but not tested.

Data Retention - $\overline{E}$ Controlled



Ordering Information

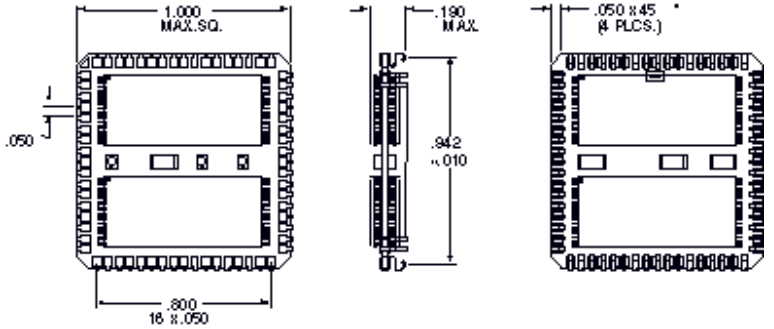
Part Number	Speed (ns)	Package No.
BiCMOS		
EDI8G32128B10MMC	10	38
EDI8G32128B12MMC	12	38
CMOS		
EDI8F32128C15MMC	15	38
EDI8F32128C20MMC	20	38
EDI8F32128C25MMC	25	38
EDI8F32128C35MMC	35	38
EDI8F32128C55BAC	55	328
EDI8F32128C70BAC	70	328
EDI8F32128C85BAC	85	328
EDI8F32128C100BAC	100	328
EDI8F32128LP55BAC	55	328
EDI8F32128LP70BAC	70	328
EDI8F32128LP85BAC	85	328
EDI8F32128LP100BAC	100	328

Part Number	Speed (ns)	Package No.
BiCMOS		
EDI8F32128B10MZC	10	39
EDI8F32128B12MZC	12	39
CMOS		
EDI8F32128C15MZC	15	39
EDI8F32128C20MZC	20	39
EDI8F32128C25MZC	25	39
EDI8F32128C35MZC	35	39

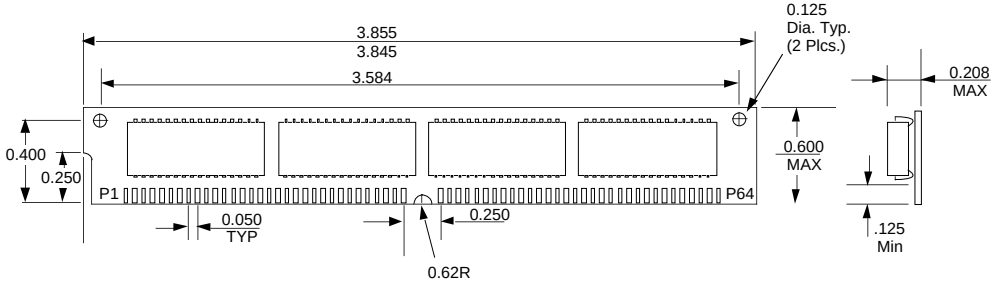
NOTE: 1. For Gold SIMM, change EDI8F to EDI8G.
2. The BICMOS 10 & 12ns SIMMs availabv2le with Gold Contacts only.

Package Description

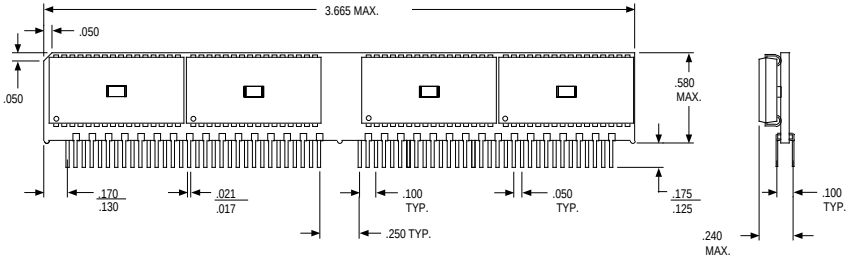
Package No. 328
64 Pin PLCC



Package No. 38
64 Lead SIMM



Package No. 39
64 Pin ZIP Plastic



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