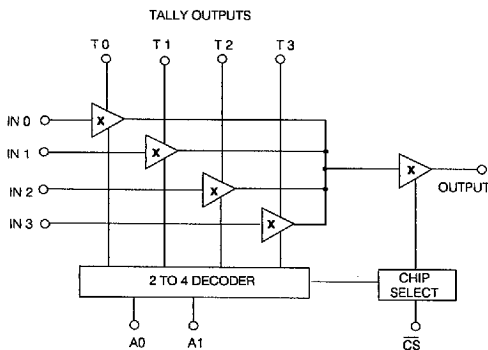




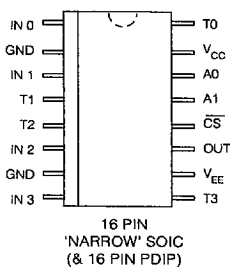
FEATURES

- low differential phase and gain
- wide bandwidth, 200 MHz at -3 dB
- small switching transient
- ± 4.5 to ± 5.5 volts supplies
- individual TALLY outputs

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



AVAILABLE PACKAGING

- 16 pin PDIP
- 16 pin SOIC
- Tape 16 pin (N) SOIC

CIRCUIT DESCRIPTION

The GX4404 is a wideband video multiplexer implemented in bipolar technology. This device is characterized by excellent differential phase and gain in the enabled state, very high off-isolation in the disabled state. Fully buffered unilateral signal paths ensure negligible output to input feedback, while delivering minimal output switching transients through make-before-break switching.

For use in NxM routing matrices, these devices feature a very high, nearly constant input impedance coupled with high output impedance in the disabled state. This allows multiple devices to be paralleled at the inputs and outputs without additional circuitry.

The chip is disabled when a logic HIGH is applied to the CS control pin. In this case, regardless of the ADDRESS data, the output of the device assumes a high impedance state. Individual PNP to V_{CC} TALLY outputs provide positive indication of crosspoint selection.

All logic inputs are TTL and 5V CMOS compatible. Supply voltages can be between ± 4.5 to ± 5.5 volts.

APPLICATIONS

- HDTV
- Very high quality video switching
- Very high density video switching
- Computer graphics
- PCM / data routing matrices

TRUTH TABLE

CS	A1	A0	OUT	TALLY O/Ps			
				T0	T1	T2	T3
0	0	0	IN 0	ON	*	*	*
0	0	1	IN 1	*	ON	*	*
0	1	0	IN 2	*	*	ON	*
0	1	1	IN 3	*	*	*	ON
1	X	X	HI - Z	*	*	*	*

X = DON'T CARE * = OFF (high impedance)

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GX4404-CDC	16 pin PDIP	0 to 70°C
GX4404-CKD	16 pin (N) SOIC	0 to 70°C
GX4404-CTD	Tape 16 pin (N) SOIC	0 to 70°C

3935783 0004275 T81

520 - 43 - 01

GX4404

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage	$\pm 7.5V$
Operating Temperature Range	$0^{\circ}C \leq T_A \leq 70^{\circ}C$
Storage Temperature Range	$-65^{\circ}C \leq T_S \leq 150^{\circ}C$
Lead Temperature (Soldering, 10 Sec)	$260^{\circ}C$

PARAMETER	VALUE
Analog Input Voltage	$(V_{EE} - 1.4) < V_A < (V_{CC} + 0.3)V$
Logic Input Voltage	$-0.5V \leq V_L \leq +5.5V$
TALLY Output Current	2 mA

ELECTRICAL CHARACTERISTICS ($V_S = \pm 5V$ DC, $0^{\circ}C \leq T_A \leq 70^{\circ}C$, $R_L = 10k\Omega$, $C_L = 30\text{ pF}$, unless otherwise shown.)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
DC SUPPLY	Supply Voltage	$\pm V_S$	Operating Range	± 4.5	-	± 5.5	V	
	Supply Current	I^+	$\overline{CS} = 0$	-	30	37	mA	
		I^-	$\overline{CS} = 0$	-	30	37	mA	
		I^+	$\overline{CS} = 1$	-	220	300	μA	
I^-		$\overline{CS} = 1$	-	220	380	μA		
STATIC	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	-2.4	-	2.6	V	
	Analog Input Bias Current	I_{BIAS}		-	12	-	μA	
	Output Offset Voltage	V_{OS}	$T_A = 25^{\circ}C$	-13	-4	7	mV	
	Output Offset Voltage Drift	ΔV_{OS}		-	35	80	$\mu V/^{\circ}C$	
LOGIC	Chip Enable Time	t_{ON}	Enable input to appearance of signal	-	200	400	ns	
	Chip Disable Time	t_{OFF}	Enable input to disappearance of signal at output.	0.6	1.2	-	μs	
	Logic Input Thresholds	V_{IH}	1		2.0	-	-	V
		V_{IL}	0		-	-	0.8	V
	Logic Input Current	I_L			-	-	4	μA
TALLY Outputs		$(V_{CC} - V_{TALLY}) I_{TALLY} = 1\text{mA}$		70	150	300	mV	
DYNAMIC	Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz	0.030	0.040	0.055	dB	
	Bandwidth (-3dB)	B.W.	small signal $C_L = 0\text{ pF}$	-	300	-	MHz	
	Input Resistance	R_{IN}	$\overline{CS} = 0$, crosspoint on	0.5	-	-	M Ω	
	Input Capacitance	C_{IN}	$\overline{CS} = 0$, crosspoint on	-	1.5	-	pF	
	Output Resistance	R_{OUT}	$\overline{CS} = 0$, crosspoint on	-	4	-	Ω	
	Output Capacitance	C_{OUT}	$\overline{CS} = 1$, chip disabled	-	3.7	-	pF	
	Differential Gain	dg	$f = 3.58\text{ MHz}$, $V_{IN} = 40\text{ IRE}$	-	-	0.05	%	
	Differential Phase	dp	$f = 3.58\text{ MHz}$, $V_{IN} = 40\text{ IRE}$	-	-	0.04	deg	
	All Hostile Crosstalk	$XTLK_{AH}$	1Vp-p on 3 inputs 4 th input has 10 Ω resistor to gnd $f=30\text{ MHz}$	-	70	-	dB	
	Chip Disabled Crosstalk	$XTLK_{CD}$	Enabled device on O/P $f=100\text{ MHz}$	-	80	-	dB	
	Slew Rate	+SR	$V_{IN} = 3V\text{ p-p}$ ($C_L = 0\text{ pF}$)		250	-	-	V/ μs
		-SR	$V_{IN} = 3V\text{ p-p}$ ($C_L = 0\text{ pF}$)		250	-	-	V/ μs
	Gain Spread at 30 MHz	ΔA_V		-	-	± 0.05	dB	
	Crosspoint Scatter		$R_S = 75\Omega$ $f = 3.58\text{ MHz}$	$T_A = 25^{\circ}C$	-	-	± 0.15	deg
$0^{\circ}C < T_A < 70^{\circ}C$				-	-	± 0.25	deg	

3935783 0004276 918

520 - 43 - 01

TYPICAL PERFORMANCE CURVES

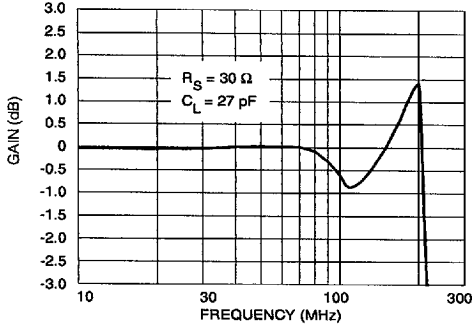


Fig. 1 Flattened Frequency Response

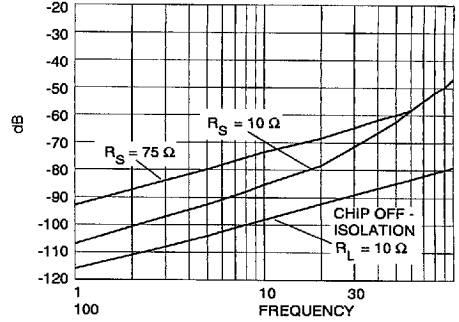


Fig. 2 All Hostile Crosstalk & Isolation

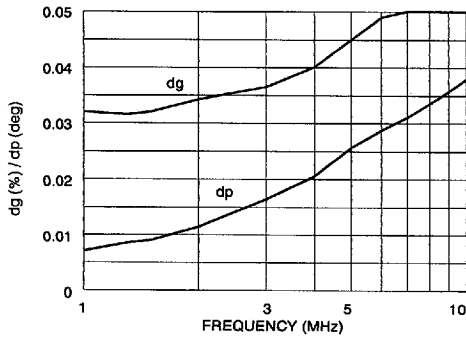


Fig. 3 Differential Gain & Phase

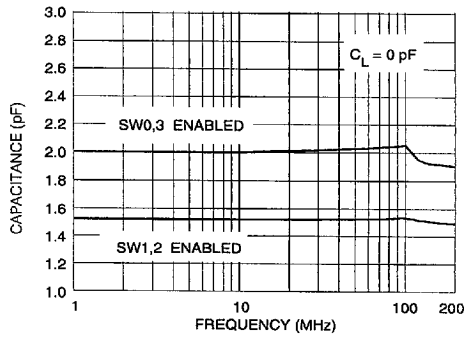
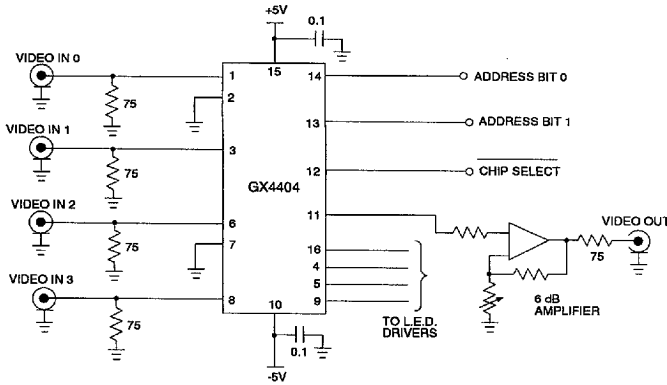
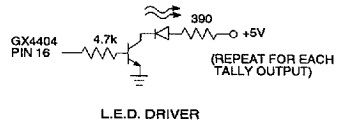


Fig. 4 Input Capacitance



All resistors in ohms, all capacitors in μF unless otherwise stated

Fig. 5 Test Circuit



CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

Gennum Corporation assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.
© Copyright July 1991 Gennum Corporation. Revision Date: January 1993. All rights reserved. Printed in Canada.