

24-Bit, 192 kHz Stereo DAC with Volume Control

Features

- Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
- 108 dB Dynamic Range
- 94 dB THD+N
- Direct Stream Digital Mode
- Low Clock Jitter Sensitivity
- +5 V to +3 V Power Supply
- ATAPI Mixing
- On-Chip Digital De-emphasis for 32, 44.1, and 48 kHz
- Volume Control with Soft Ramp
 - 119 dB Attenuation
 - 1 dB Step Size
 - Zero Crossing Click-Free Transitions
- 36 mW with 3 V supply
- Direct Interface with 5 V to 1.8 V Logic

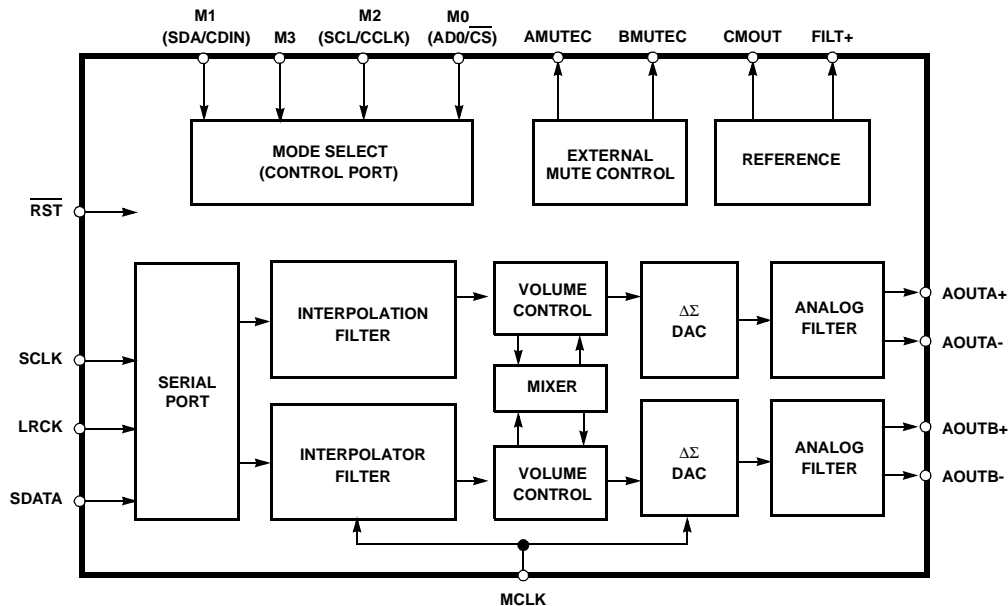
Description

The CS4391 is a complete stereo digital-to-analog system including digital interpolation, fourth-order delta-sigma digital-to-analog conversion, digital de-emphasis, volume control, channel mixing and analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

The CS4391 accepts PCM data at sample rates from 2 kHz to 192 kHz, DSD audio data, consumes very little power and operates over a wide power supply range. These features are ideal for DVD, A/V receivers, CD and set-top box systems.

ORDERING INFORMATION

| | | |
|-----------|------------------|--------------|
| CS4391-KZ | 20-pin TSSOP | -10 to 70 °C |
| CDB4391 | Evaluation Board | |



Preliminary Product Information

This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

TABLE OF CONTENTS

| | |
|--|-----------|
| 1. CHARACTERISTICS/SPECIFICATIONS | 5 |
| ANALOG CHARACTERISTICS..... | 5 |
| DIGITAL CHARACTERISTICS..... | 7 |
| ABSOLUTE MAXIMUM RATINGS..... | 7 |
| RECOMMENDED OPERATING CONDITIONS..... | 7 |
| SWITCHING CHARACTERISTICS - PCM MODES..... | 8 |
| SWITCHING CHARACTERISTICS - DSD..... | 9 |
| SWITCHING CHARACTERISTICS - I ² C CONTROL PORT..... | 10 |
| SWITCHING CHARACTERISTICS - SPI CONTROL PORT..... | 11 |
| 2. TYPICAL CONNECTION DIAGRAMS | 12 |
| 3. REGISTER QUICK REFERENCE | 14 |
| 3.1 Mode Control 1 (address 01h)..... | 14 |
| 3.2 Volume and Mixing Control (address 02h)..... | 15 |
| 3.3 Channel A Volume Control (address 03h)..... | 15 |
| 3.4 Channel B Volume Control (address 04h)..... | 15 |
| 3.5 Mode Control 2 (address 05h)..... | 16 |
| 4. REGISTER DESCRIPTION | 17 |
| 4.1 Mode Control 1 - Address 01h..... | 17 |
| 4.1.1 Auto-Mute (Bit 7)..... | 17 |
| 4.1.2 Digital Interface Formats (Bits 6:4)..... | 17 |
| 4.1.3 De-Emphasis Control (Bits 3:2)..... | 17 |
| 4.1.4 Functional Mode (Bits 1:0)..... | 17 |
| 4.2 Volume and Mixing Control (Address 02h)..... | 18 |
| 4.2.1 Channel A Volume = Channel B Volume (Bit 7)..... | 18 |
| 4.2.2 Soft Ramp or Zero Cross Enable (Bits 6:5)..... | 18 |
| 4.2.3 ATAPI Channel Mixing and Muting (Bits 4:0)..... | 18 |
| 4.3 Channel A Volume Control - Address 03h..... | 18 |
| 4.4 Channel B Volume Control - Address 04h..... | 19 |
| 4.4.1 Mute (Bit 7)..... | 19 |
| 4.4.2 Volume Control (Bits 6:0)..... | 19 |
| 4.5 Mode Control 2 - Address 05h..... | 19 |
| 4.5.1 Invert Signal Polarity (Bits 7:6)..... | 19 |
| 4.5.2 Control Port Enable (Bit 5)..... | 19 |
| 4.5.3 Power Down (Bit 4)..... | 19 |
| 4.5.4 AMUTEC = BMUTEC (Bit 3)..... | 19 |
| 4.5.5 Freeze (Bit 2)..... | 20 |
| 4.5.6 Master Clock Divide (Bit 1)..... | 20 |
| 5. PIN DESCRIPTION - PCM DATA MODE | 21 |
| Reset - RST..... | 21 |
| Interface Power - VL..... | 21 |

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| | |
|---|-----------|
| Serial Audio Data - SDATA | 21 |
| Serial Clock - SCLK | 22 |
| Left / Right Clock - LRCK | 22 |
| Master Clock - MCLK | 22 |
| Mode Select - M3, M2, M1 and M0 (Stand-alone Mode) | 22 |
| Mode Select - M3 (Control Port Mode) | 22 |
| Serial Control Interface Clock - SCL/CCLK (Control Port Mode) | 23 |
| Serial Control Data I/O - SDA/CDIN (Control Port Mode) | 23 |
| Address Bit / Chip Select - AD0 / CS (Control Port Mode) | 23 |
| Positive Voltage Reference - FILT+ | 23 |
| Common Mode Voltage - CMOUT | 23 |
| Channel A and Channel B Mute Control - AMUTEC and BMUTEC | 23 |
| Differential Analog Output - AOUTB+, AOUTB- and AOUTA+, AOUTA- | 24 |
| Analog Ground - AGND | 24 |
| Analog Power - VA | 24 |
| 6. PIN DESCRIPTION - DSD MODE | 25 |
| DSD Audio Data - DSD_A and DSD_B | 25 |
| DSD Mode - DSD_Mode | 25 |
| Master Clock - MCLK | 25 |
| DSD Serial Clock - DSD_SCLK | 25 |
| 7. APPLICATIONS | 32 |
| 7.1 Recommended Power-up Sequence for Hardware Mode | 32 |
| 7.2 Recommended Power-up Sequence and Access to Control Port Mode | 32 |
| 7.3 Analog Output and Filtering | 32 |
| 8. CONTROL PORT INTERFACE | 33 |
| 8.1 SPI Mode | 33 |
| 8.2 I2C Mode | 33 |
| 9. PARAMETER DEFINITIONS | 37 |
| Total Harmonic Distortion + Noise (THD+N) | 37 |
| Dynamic Range | 37 |
| Interchannel Isolation | 37 |
| Interchannel Gain Mismatch | 37 |
| Gain Error | 37 |
| Gain Drift | 37 |
| 10. REFERENCES | 37 |
| 11. PACKAGE DIMENSIONS | 38 |

LIST OF TABLES

| | |
|--|----|
| Figure:1. Digital Interface Formats - PCM Modes | 26 |
| Figure:2. Digital Interface Formats - DSD Mode | 26 |
| Figure:3. De-Emphasis Mode Selection | 26 |
| Figure:4. Functional Mode Selection | 26 |
| Figure:5. Soft Cross or Zero Cross Mode Selection | 26 |
| Figure:6. ATAPI Decode | 27 |
| Figure:7. Digital Volume Control | 27 |
| Figure:8. Single Speed (4 to 50 kHz sample rates) Common Clock Frequencies | 28 |
| Figure:9. Double Speed (50 to 100 kHz sample rates) Common Clock Frequencies | 28 |
| Figure:10. Quad Speed (100 to 200 kHz sample rates) Common Clock Frequencies | 28 |
| Figure:11. Single Speed (4 to 50 kHz) Digital Interface Format, Stand-Alone Mode Options | 28 |
| Figure:12. Single Speed Only (4 to 50 kHz) De-Emphasis, Stand-Alone Mode Options | 28 |
| Figure:13. Double Speed (50 to 100 kHz) Digital Interface Format, Stand-Alone Mode Options | 28 |
| Figure:14. Quad Speed (100 to 200 kHz) Digital Interface Format, Stand-Alone Mode Options | 29 |
| Figure:15. Direct Stream Digital (DSD), Stand-Alone Mode Options | 29 |
| Figure:16. Memory Address Pointer (MAP) | 34 |

LIST OF FIGURES

| | |
|---|----|
| Figure 1. Serial Mode Input Timing | 8 |
| Figure 2. Direct Stream Digital - Serial Audio Input Timing | 9 |
| Figure 3. I ² C Control Port Timing | 10 |
| Figure 4. SPI Control Port Timing | 11 |
| Figure 5. Typical Connection Diagram - PCM Mode | 12 |
| Figure 6. Typical Connection Diagram - DSD Mode | 13 |
| Figure 7. Format 0, Left Justified up to 24-Bit Data | 30 |
| Figure 8. Format 1, I2S up to 24-Bit Data | 30 |
| Figure 9. Format 2, Right Justified 16-Bit Data | 30 |
| Figure 10. Format 3, Right Justified 24-Bit Data | 30 |
| Figure 11. Format 4, Right Justified 20-Bit Data. (Available in Control Port Mode only) | 31 |
| Figure 12. Format 5, Right Justified 18-Bit Data. (Available in Control Port Mode only) | 31 |
| Figure 13. De-Emphasis Curve | 31 |
| Figure 14. ATAPI Block Diagram | 31 |
| Figure 15. CS4391 Output Filter | 32 |
| Figure 16. Control Port Timing, SPI mode | 34 |
| Figure 17. Control Port Timing, I ² C Mode | 34 |
| Figure 18. Single-Speed Frequency Response | 35 |
| Figure 19. Single-Speed Transition Band | 35 |
| Figure 20. Single-Speed Transition Band | 35 |
| Figure 21. Single-Speed Stopband Rejection | 35 |
| Figure 22. Double-Speed Frequency Response | 35 |
| Figure 23. Double-Speed Transition Band | 35 |
| Figure 24. Double-Speed Transition Band | 36 |
| Figure 25. Double-Speed Stopband Rejection | 36 |

1. CHARACTERISTICS/SPECIFICATIONS

ANALOG CHARACTERISTICS ($T_A = 25^\circ\text{C}$; Logic "1" = $V_L = V_A$; Logic "0" = AGND; Full-Scale Output Sine Wave, 997 Hz; MCLK = 12.288 MHz; SCLK = 3.072 MHz, Sample Rate = 48, 96 or 192 kHz, 24-bit data, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified. Test load $R_L = 5\text{ k}\Omega$, $C_L = 10\text{ pF}$)

| Parameter | Symbol | VA = 3 V | | | VA = 5 V | | | Unit | |
|---|------------------|-------------|-----|------|----------|-----|-----|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | | |
| Dynamic Performance | | | | | | | | | |
| Dynamic Range | (Note 17) | | | | | | | | |
| | unweighted | 97 | 102 | - | 100 | 105 | - | dB | |
| | A-Weighted | 100 | 105 | - | 103 | 108 | - | dB | |
| 40 kHz Bandwidth | A-Weighted | - | 99 | - | - | 102 | - | dB | |
| Total Harmonic Distortion + Noise | (Note 17,2) | THD+N | | | | | | | |
| | 0 dB | - | -94 | -89 | - | -94 | -89 | dB | |
| | -20 dB | - | -82 | - | - | -85 | - | dB | |
| | -60 dB | - | -42 | -37 | - | -45 | -40 | dB | |
| Idle Channel Noise / Signal-to-Noise Ratio | | | - | 105 | - | - | 108 | - | dB |
| Interchannel Isolation | (1 kHz) | | - | 100 | - | - | 100 | - | dB |
| Power Supplies | | | | | | | | | |
| Power Supply Current | normal operation | $I_A + I_L$ | - | 12 | TBD | - | 17 | TBD | mA |
| | power-down state | $I_A + I_L$ | - | 30 | - | - | 60 | - | μA |
| Power Dissipation | normal operation | | - | 36 | TBD | - | 85 | TBD | mW |
| | power-down | | - | 0.09 | - | - | 0.3 | - | mW |
| Power Supply Rejection Ratio (1 kHz) (Note 3) | (60 Hz) | PSRR | - | 60 | - | - | 60 | - | dB |
| | | | - | 40 | - | - | 40 | - | dB |

| Parameter | Symbol | Min | Typ | Max | Units |
|--|--------|-----|-------|-----|-----------------------|
| Analog Output | | | | | |
| Full Scale Differential Output Voltage | | TBD | 1.1VA | TBD | V _{pp} |
| Common Mode Voltage | CMOUT | - | 0.5VA | - | VDC |
| Interchannel Gain Mismatch | | - | 0.1 | - | dB |
| Gain Drift | | - | 100 | - | ppm/ $^\circ\text{C}$ |
| AC-Load Resistance | R_L | 5 | - | - | k Ω |
| Load Capacitance | C_L | - | - | 100 | pF |

ANALOG CHARACTERISTICS (continued)

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|---------------|-------|----------|------------|------|
| Combined Digital and On-chip Analog Filter Response - Single Speed Mode | | | | | |
| Passband (Note 3) to -0.05 dB corner to -3 dB corner | | 0 | - | .4535 | Fs |
| | | 0 | - | .4998 | Fs |
| Frequency Response 10 Hz to 20 kHz | | -.02 | - | +.035 | dB |
| StopBand | | .5465 | - | - | Fs |
| StopBand Attenuation (Note 5) | | 50 | - | - | dB |
| Group Delay | tgd | - | 9/Fs | - | s |
| Passband Group Delay Deviation 0 - 20 kHz | | - | ±0.36/Fs | - | s |
| De-emphasis Error (Relative to 1 kHz) Control Port Mode Stand-Alone Mode | Fs = 32 kHz | - | - | +.2/- .1 | dB |
| | Fs = 44.1 kHz | - | - | +.05/- .14 | dB |
| | Fs = 48 kHz | - | - | +0/.22 | dB |
| | Fs = 32 kHz | - | - | TBD | dB |
| | Fs = 44.1 kHz | - | - | +.05/- .14 | dB |
| | Fs = 48 kHz | - | - | TBD | dB |
| Combined Digital and On-chip Analog Filter Response - Double Speed Mode | | | | | |
| Passband (Note 4) to -0.1 dB corner to -3 dB corner | | 0 | - | .4621 | Fs |
| | | 0 | - | .4982 | Fs |
| Frequency Response 10 Hz to 20 kHz | | -0.1 | - | 0 | dB |
| StopBand | | .577 | - | - | Fs |
| StopBand Attenuation (Note 5) | | 55 | - | - | dB |
| Group Delay | tgd | - | 9/Fs | - | s |
| Passband Group Delay Deviation 0 - 20 kHz | | - | ±0.23/Fs | - | s |
| On-chip Analog Filter Response - Quad Speed Mode | | | | | |
| Passband (Note 4) to -3 dB corner | | 0 | - | 0.25 | Fs |
| Frequency Response 10 Hz to 20 kHz | | -0.7 | - | 0 | dB |
| On-chip Analog Filter Response - DSD Mode | | | | | |
| Passband (Note 4) to -3 dB corner | | 0 | - | 1.0 | Fs |
| Frequency Response 10 Hz to 20 kHz | | -0.7 | - | 0 | dB |

Notes: 17. Triangular PDF dithered data.

18. THD+N specifications for 48 kHz sample rates are made over a 20 kHz Bandwidth.
19. Valid with the recommended capacitor values on FILT+ and CMOUT as shown in Figure 1. Increasing the capacitance will also increase the PSRR.
20. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 17-24) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
21. For Single-Speed Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.
For Double-Speed Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.

DIGITAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

| Parameters | Symbol | Min | Typ | Max | Units |
|-----------------------------|----------|-----|-----|----------|---------------|
| High-Level Input Voltage | V_{IH} | 70% | - | - | VL |
| Low-Level Input Voltage | V_{IL} | | - | 20% | VL |
| Input Leakage Current | I_{in} | - | - | ± 10 | μA |
| Input Capacitance | | - | 8 | - | pF |
| Maximum MUTEC Drive Current | | - | 3 | - | mA |

ABSOLUTE MAXIMUM RATINGS (AGND = 0 V; all voltages with respect to ground.)

| Parameters | Symbol | Min | Max | Units |
|---|-----------|------|----------|------------------|
| DC Power Supply | VA | -0.3 | 6.0 | V |
| | VL | -0.3 | VA | V |
| Input Current, Any Pin Except Supplies | I_{in} | - | ± 10 | mA |
| Digital Input Voltage | V_{IND} | -0.3 | VL+0.4 | V |
| Ambient Operating Temperature (power applied) | T_A | -55 | 125 | $^\circ\text{C}$ |
| Storage Temperature | T_{stg} | -65 | 150 | $^\circ\text{C}$ |

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND = 0V; all voltages with respect to ground.)

| Parameters | Symbol | Min | Typ | Max | Units |
|-----------------|--------|-----|-----|-----|-------|
| DC Power Supply | VA | 2.7 | 5.0 | 5.5 | V |
| | VL | 1.8 | - | VA | V |

SWITCHING CHARACTERISTICS - PCM MODES ($T_A = -10$ to 70°C ; $V_L = 5.5$ to 1.8 Volts;
 Inputs: Logic 0 = 0 V, Logic 1 = V_L , $C_L = 20$ pF)

| Parameters | Symbol | Min | Typ | Max | Units |
|---|-------------|-----|-----|--------|-------|
| Input Sample Rate | F_s | 4 | - | 200 | kHz |
| LRCK Duty Cycle | | 45 | 50 | 55 | % |
| MCLK Duty Cycle | | 40 | 50 | 60 | % |
| SCLK Frequency | | - | - | MCLK/2 | Hz |
| SCLK Frequency Note 22 | | - | - | MCLK/4 | Hz |
| SCLK rising to LRCK edge delay | t_{slrd} | 20 | - | - | ns |
| SCLK rising to LRCK edge setup time | t_{slrs} | 20 | - | - | ns |
| SDATA valid to SCLK rising setup time | t_{sdhrs} | 20 | - | - | ns |
| SCLK rising to SDATA hold time | t_{sdh} | 20 | - | - | ns |

Notes: 22. This serial clock is available only in Control Port Mode when the MCLK Divide bit is enabled.

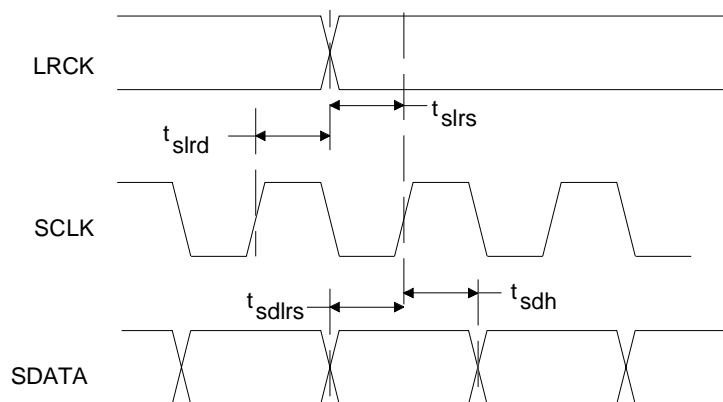


Figure 1. Serial Mode Input Timing

SWITCHING CHARACTERISTICS - DSD ($T_A = -10$ to 70°C ; Logic 0 = AGND = DGND;
Logic 1 = VL = 5.5 to 1.8 Volts; $C_L = 20\text{ pF}$)

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------------------------|--------------------|-----|-----|-----|------|
| MCLK Duty Cycle | | 40 | 50 | 60 | % |
| SCLK Pulse Width Low | t_{sckl} | TBD | - | - | ns |
| SCLK Pulse Width High | t_{sckh} | TBD | - | - | ns |
| SCLK Period | t_{sckw} | TBD | - | - | ns |
| SDIN valid to SCLK rising setup time | t_{sdlrs} | TBD | - | - | ns |
| SCLK rising to SDIN hold time | t_{sdh} | TBD | - | - | ns |

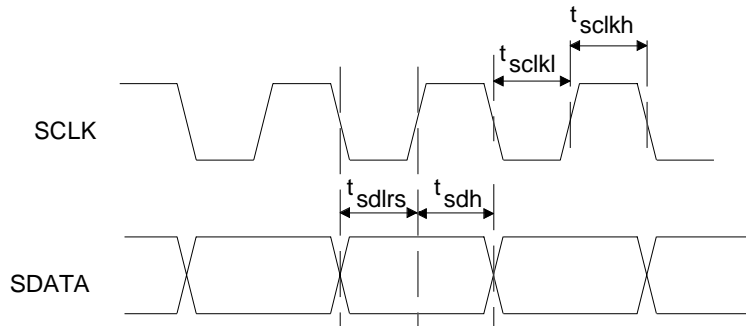


Figure 2. Direct Stream Digital - Serial Audio Input Timing

SWITCHING CHARACTERISTICS - I²C CONTROL PORT

(T_A = 25° C; V_L = 5.5 to 1.8 Volts; Inputs: logic 0 = AGND, logic 1 = V_L, C_L = 30 pF)

| Parameter | Symbol | Min | Max | Unit |
|--|-------------------|-----|-----|------|
| I²C[®] Mode | | | | |
| SCL Clock Frequency | f _{scl} | - | 100 | KHz |
| RST Rising Edge to Start | t _{irs} | 500 | - | ns |
| Bus Free Time Between Transmissions | t _{buf} | 4.7 | - | μs |
| Start Condition Hold Time (prior to first clock pulse) | t _{hdst} | 4.0 | - | μs |
| Clock Low time | t _{low} | 4.7 | - | μs |
| Clock High Time | t _{high} | 4.0 | - | μs |
| Setup Time for Repeated Start Condition | t _{sust} | 4.7 | - | μs |
| SDA Hold Time from SCL Falling (Note 23) | t _{hdd} | 0 | - | μs |
| SDA Setup time to SCL Rising | t _{sud} | 250 | - | ns |
| Rise Time of Both SDA and SCL Lines | t _r | - | 1 | μs |
| Fall Time of Both SDA and SCL Lines | t _f | - | 300 | ns |
| Setup Time for Stop Condition | t _{susp} | 4.7 | - | μs |

Notes: 23. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

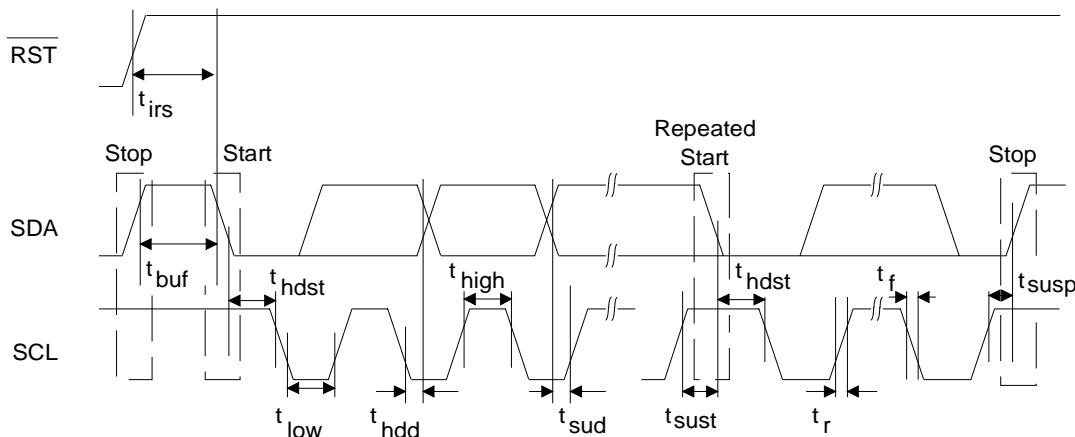


Figure 3. I²C Control Port Timing

SWITCHING CHARACTERISTICS - SPI CONTROL PORT

($T_A = 25^\circ\text{C}$; $V_L = 5.5$ to 1.8 Volts; Inputs: logic 0 = AGND, logic 1 = V_L , $C_L = 30$ pF)

| Parameter | Symbol | Min | Max | Unit |
|---|-------------------|-----|-----|---------------|
| SPI Mode | | | | |
| CCLK Clock Frequency | f_{sclk} | - | 6 | MHz |
| RST Rising Edge to CS Falling | t_{srs} | 500 | - | ns |
| CCLK Edge to CS Falling (Note 24) | t_{spi} | 500 | - | ns |
| CS High Time Between Transmissions | t_{csh} | 1.0 | - | μs |
| CS Falling to CCLK Edge | t_{css} | 20 | - | ns |
| CCLK Low Time | t_{scl} | 66 | - | ns |
| CCLK High Time | t_{sch} | 66 | - | ns |
| CDIN to CCLK Rising Setup Time | t_{dsu} | 40 | - | ns |
| CCLK Rising to DATA Hold Time (Note 25) | t_{dh} | 15 | - | ns |
| Rise Time of CCLK and CDIN (Note 26) | t_{r2} | - | 100 | ns |
| Fall Time of CCLK and CDIN (Note 26) | t_{f2} | - | 100 | ns |

Notes: 24. t_{spi} only needed before first falling edge of $\overline{\text{CS}}$ after $\overline{\text{RST}}$ rising edge. $t_{\text{spi}} = 0$ at all other times.

25. Data must be held for sufficient time to bridge the transition time of CCLK.

26. For $F_{\text{SCK}} < 1$ MHz

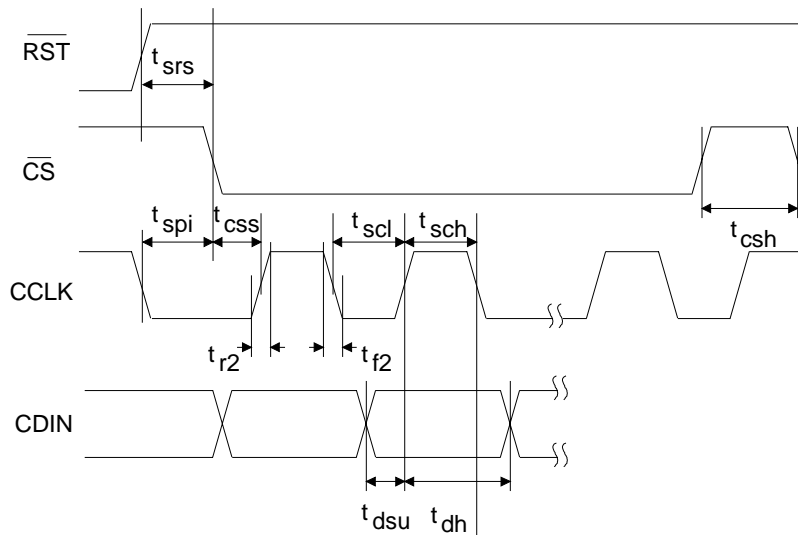


Figure 4. SPI Control Port Timing

2. TYPICAL CONNECTION DIAGRAMS

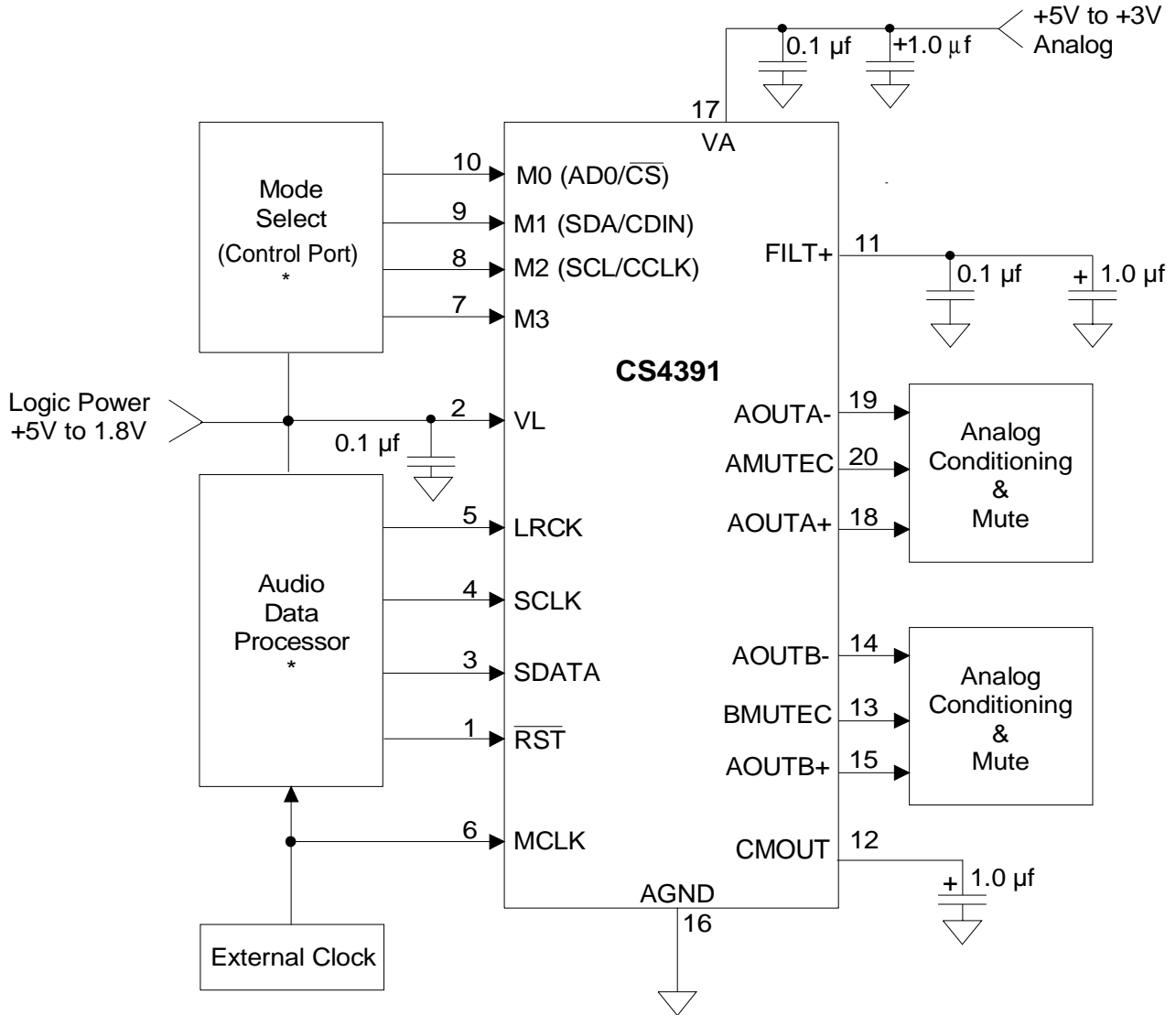


Figure 5. Typical Connection Diagram - PCM Mode

* A high logic level for all digital inputs should not exceed VL.

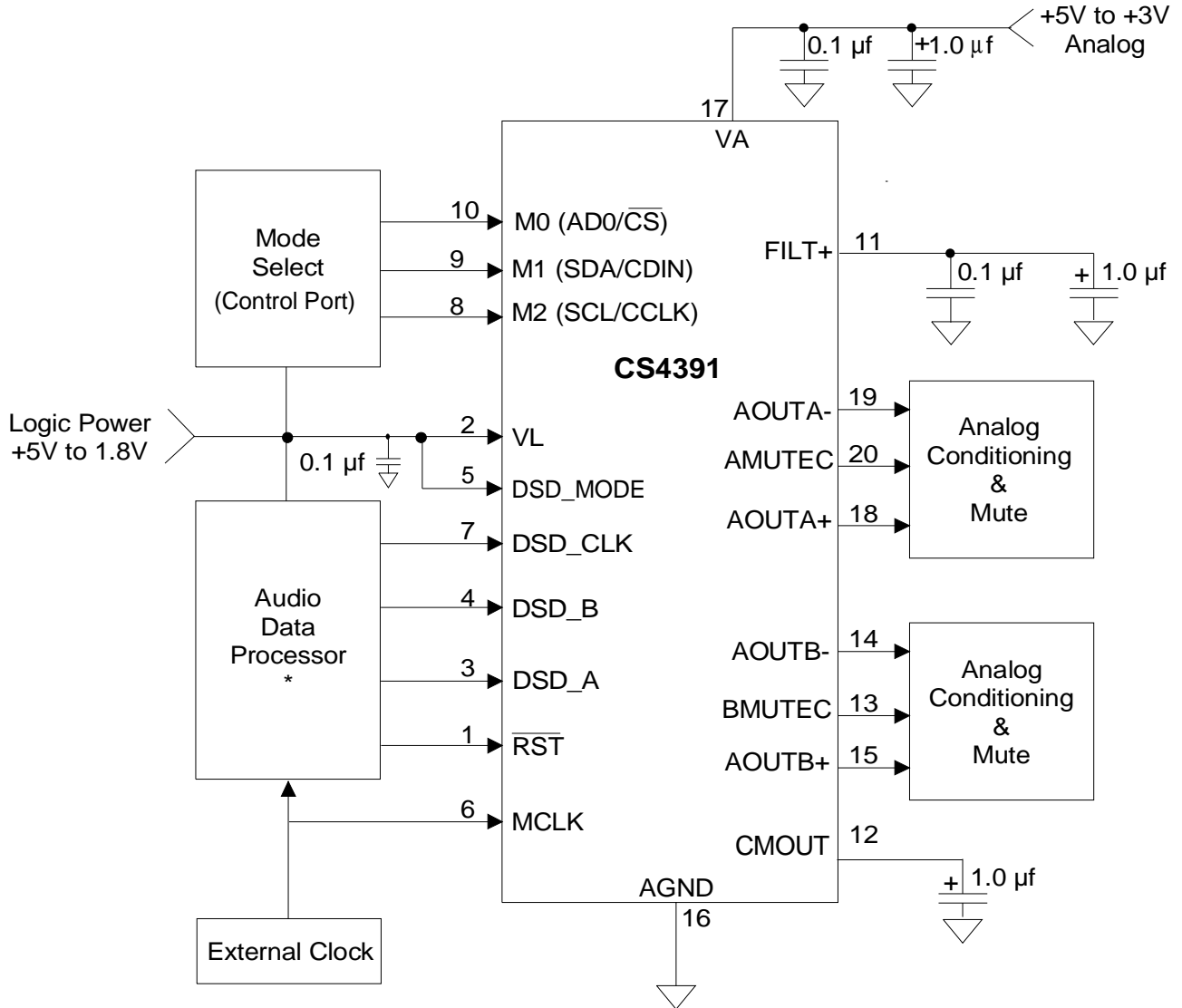


Figure 6. Typical Connection Diagram - DSD Mode
 * A high logic level for all digital inputs should not exceed VL.

3. REGISTER QUICK REFERENCE

** "default" ==> bit status after power-up-sequence or reset**

3.1 MODE CONTROL 1 (ADDRESS 01H)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|------|------|------|------|------|-----|-----|
| AMUTE | DIF2 | DIF1 | DIF0 | DEM1 | DEM0 | FM1 | FM0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

AMUTE (Auto-mute)

- Default = '1'.
- 0 - Disabled
- 1 - Enabled

DIF2, DIF1 and DIF0 (Digital Interface Format - PCM Modes). See Table 1

- Default = '0'.
- 000 - Format 0, Left Justified, up to 24-bit data
- 001 - Format 1, I²S, up to 24-bit data
- 010 - Format 2, Right Justified, 16-bit Data
- 011 - Format 3, Right Justified, 24-bit Data
- 100 - Format 4, Right Justified, 20-bit Data
- 101 - Format 5, Right Justified, 18-bit Data
- 110 - Reserved
- 111 - Reserved

DIF2, DIF1 and DIF0 (Digital Interface Format - DSD Mode Only). See Table 2

- Default = '0'.
- 000 - Format 0, 64x oversampled DSD data with a 4x MCLK to DSD data rate
- 001 - Format 1, 64x oversampled DSD data with a 6x MCLK to DSD data rate
- 010 - Format 2, 64x oversampled DSD data with a 8x MCLK to DSD data rate
- 011 - Format 3, 64x oversampled DSD data with a 12x MCLK to DSD data rate
- 100 - Format 4, 128x oversampled DSD data with a 2x MCLK to DSD data rate
- 101 - Format 5, 128x oversampled DSD data with a 3x MCLK to DSD data rate
- 110 - Format 6, 128x oversampled DSD data with a 4x MCLK to DSD data rate
- 111 - Format 7, 128x oversampled DSD data with a 6x MCLK to DSD data rate

DEM1, DEM0 (De-Emphasis Mode). See Table 3

- Default = '00'.
- 00 - No De-emphasis
- 01 - 44.1 kHz De-Emphasis
- 10 - 48 kHz De-Emphasis
- 11 - 32 kHz De-Emphasis

FM1, FM0 (Functional Mode). See Table 4

- Default = '00'.
- 00 - Single-Speed Mode (4 to 50 kHz sample rates)
- 01 - Double-Speed Mode (50 to 100 kHz sample rates)
- 10 - Quad-Speed Mode (100 to 200 kHz sample rates)
- 11 - Direct Stream Digital Mode

3.2 VOLUME AND MIXING CONTROL (ADDRESS 02H)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|------|------------|--------|--------|--------|--------|--------|
| A = B | Soft | Zero Cross | ATAPI4 | ATAPI3 | ATAPI2 | ATAPI1 | ATAPI0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |

A = B (Channel A Volume = Channel B Volume)

Default = '0'.

0 - AOUTA volume is determined by register 03h and AOUTB volume is determined by register 04h.

1 - AOUTA and AOUTB volumes are determined by register 03h and register 04h is ignored.

Soft & Zero Cross (Soft control and zero cross detection control)

Default = '10'.

SoftZero CrossMode

00 Changes take effect immediately

01 Changes take effect on zero crossings

10 Changes take effect with a soft ramp (default)

11 Changes take effect in 1/8 dB steps on each zero crossing

ATAPI 0-4 (Channel mixing and muting). See Table 6

Default = '01001', (Stereo)

AOUTA = Left Channel

AOUTB = Right Channel

3.3 CHANNEL A VOLUME CONTROL (ADDRESS 03H)

See Channel B Volume Control (address 04h)

3.4 CHANNEL B VOLUME CONTROL (ADDRESS 04H)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|------|
| MUTE | VOL6 | VOL5 | VOL4 | VOL3 | VOL2 | VOL1 | VOL0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

MUTE

Default = '0'

0 - Disabled

1 - Enabled

Volume

Default = '0'

(Refer to Table 7)

3.5 MODE CONTROL 2 (ADDRESS 05H)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|------|-----|-------------|--------|-------------|----------|
| INVERT_A | INVERT_B | CPEN | PDN | MUTEC A = B | FREEZE | MCLK Divide | Reserved |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

INVERT_A (Invert Channel A)

Default = '0'.

0 - Disabled

1 - Enabled

INVERT_B (Invert Channel B)

Default = '0'.

0 - Disabled

1 - Enabled

CPEN (Control Port Enable)

Default = '0'

0 - Disabled (Stand-Alone Mode)

1 - Enabled (Control Port Mode)

PDN (Power-Down)

Default = '1'.

0 - Disabled

1 - Enabled

MUTEC A=B

Default = '0'.

0 - Disabled

1 - Enabled

FREEZE

Default = 0.

0 - Disabled

1 - Enabled

MCLK Divide

Default = 0.

0 - Disabled

1 - Enabled

4. REGISTER DESCRIPTION

** All register access is R/W in I²C mode and write only in SPI mode **

4.1 MODE CONTROL 1 - ADDRESS 01H

| | | | | | | | |
|-------|------|------|------|------|------|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AMUTE | DIF2 | DIF1 | DIF0 | DEM1 | DEM0 | FM1 | FM0 |

4.1.1 *Auto-Mute (Bit 7)*

Function:

The Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. (However, Auto-Mute detection and muting can become dependent on either channel if the Mute A = B function is enabled.) The common mode on the output will be retained and the Mute Control pin for that channel will go active during the mute period. The muting function is effected, similar to volume control changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register.

4.1.2 *Digital Interface Formats (Bits 6:4)*

Function:

PCM Mode - The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Table 2 and Figures 6-24.

DSD Mode - The relationship between the oversampling ratio of the DSD audio data and the required Master clock to DSD data rate is defined by the Digital interface Format pins. Note that the Functional Mode registers must be set to DSD Mode.

See Table 1 (PCM Modes)

See Table 2 (DSD Mode)

4.1.3 *De-Emphasis Control (Bits 3:2)*

Function:

Implementation of the standard 15 μ s/50 μ s digital de-emphasis filter response, Figure 12, requires reconfiguration of the digital filter to maintain the proper filter response for 32, 44.1 or 48 kHz sample rates. NOTE: De-emphasis is available only in Single-Speed Mode.

See Table 3

4.1.4 *Functional Mode (Bits 1:0)*

Function:

Selects the required range of input sample rates or DSD Mode.

See Table 4

4.2 VOLUME AND MIXING CONTROL (ADDRESS 02H)

| | | | | | | | |
|-------|------|------------|--------|--------|--------|--------|--------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| A = B | Soft | Zero Cross | ATAPI4 | ATAPI3 | ATAPI2 | ATAPI1 | ATAPI0 |

4.2.1 Channel A Volume = Channel B Volume (Bit 7)

Function:

The AOUTA and AOUTB volume levels are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both AOUTA and AOUTB are determined by the A Channel Volume Control Byte and the B Channel Byte is ignored when this function is enabled.

4.2.2 Soft Ramp or Zero Cross Enable (Bits 6:5)

Function:

Soft Ramp Enable

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1dB per 8 left/right clock periods.

Zero Cross Enable

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

See Table 5

4.2.3 ATAPI Channel Mixing and Muting (Bits 4:0)

Function:

The CS4391 implements the channel mixing functions of the ATAPI CD-ROM specification.

See Table 6

4.3 CHANNEL A VOLUME CONTROL - ADDRESS 03H

See 4.4 Channel B Volume Control - Address 04h

4.4 CHANNEL B VOLUME CONTROL - ADDRESS 04H

| | | | | | | | |
|------|------|------|------|------|------|------|------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MUTE | VOL6 | VOL5 | VOL4 | VOL3 | VOL2 | VOL1 | VOL0 |

4.4.1 Mute (Bit 7)

Function:

The Digital-to-Analog converter output will mute when enabled. The common mode voltage on the output will be retained. The muting function is effected, similiar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register. The MUTE pin for that channel will go active during the mute period if the Mute function is enabled. Both the AMUTE pin and BMUTE pin will go active if either MUTE register is enabled and the MUTE A = B bit (register 5) is enabled.

4.4.2 Volume Control (Bits 6:0)

Function:

The digital volume control allows the user to attenuate the signal in 1 dB increments from 0 to -119 dB. Volume settings are decoded as shown in Table 7. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Volume and Mixing Control register. All volume settings less than -119 dB are equivalent to enabling the Mute bit.

4.5 MODE CONTROL 2 - ADDRESS 05H

| | | | | | | | |
|----------|----------|------|-----|------------|--------|-------------|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INVERT_A | INVERT_B | CPEN | PDN | MUTE A = B | FREEZE | MCLK Divide | Reserved |

4.5.1 Invert Signal Polarity (Bits 7:6)

Function:

When set, this bit inverts the signal polarity.

4.5.2 Control Port Enable (Bit 5)

Function:

This bit defaults to 0, allowing the device to power-up in Stand-Alone mode. The Control port mode can be accessed by setting this bit to 1. This will allow the operation of the device to be controlled by the registers and the pin definitions will conform to Control Port Mode. To accomplish a clean power-up, the user should write 11h to register 5 within 10 ms following the release of Reset.

4.5.3 Power Down (Bit 4)

Function:

The device will enter a low-power state whenever this function is activated. The power-down bit defaults to 'enabled' on power-up and must be disabled before normal operation will begin. The contents of the control registers are retained when the device is in power-down.

4.5.4 AMUTE = BMUTE (Bit 3)

Function:

When this function is enabled, the individual controls for AMUTE and BMUTE are internally connected through a AND gate prior to the output pins. Therefore, the external AMUTE and BMUTE pins will go active only when the requirements for both AMUTE and BMUTE are valid.

4.5.5 Freeze (Bit 2)

Function:

This function allows modifications to the registers without the changes being taking effect until Freeze is disabled. To make multiple changes in the Control port registers take effect simultaneously, set the Freeze Bit, make all register changes, then Disable the Freeze bit.

4.5.6 Master Clock Divide (Bit 1)

Function:

This function allows the user to select an internal divide by 2 of the Master Clock. This selection is required to access the higher Master Clock rates as shown in Table 9.

5. PIN DESCRIPTION - PCM DATA MODE

| | | | | | |
|------------------|-------------------------|------|------|---------------|----------------------------|
| Reset | $\overline{\text{RST}}$ | □ 1 | 20 □ | AMUTEC | Channel A Mute Control |
| Logic Voltage | VL | □ 2 | 19 □ | AOUTA- | Differential Output |
| Serial Data | SDATA | □ 3 | 18 □ | AOUTA+ | Differential Output |
| Serial Clock | SCLK | □ 4 | 17 □ | VA | Analog Power |
| Left/Right Clock | LRCK | □ 5 | 16 □ | AGND | Analog Ground |
| Master Clock | MCLK | □ 6 | 15 □ | AOUTB+ | Differential Output |
| See Description | M3 | □ 7 | 14 □ | AOUTB- | Differential Output |
| See Description | (SCL/CCLK) M2 | □ 8 | 13 □ | BMUTEC | Channel B Mute Control |
| See Description | (SDA/CDIN) M1 | □ 9 | 12 □ | CMOUT | Common Mode Voltage |
| See Description | (AD0/CS) M0 | □ 10 | 11 □ | FILT+ | Positive Voltage Reference |

Reset - $\overline{\text{RST}}$

Pin 1, Input

Function:

Hardware Mode: The device enters a low power mode and the internal state machine is reset to the default setting when low. When high, the device becomes operational.

Control Port Mode: The device enters a low power mode and all internal registers are reset to the default settings, including the control port, when low. When high, the control port becomes operational and the PDN bit must be cleared before normal operation will occur. The control port can not be accessed when reset is low. The Control Port Enable Bit must also be enabled after a device reset.

$\overline{\text{RST}}$ is required to remain low until the power supplies and clocks are applied and stable.

Interface Power - VL

Pin 2, Input

Function:

Digital interface power supply. Typically 1.8 to 5.0 VDC. The voltage on this pin determines the logic level high threshold for the digital inputs. The voltage on VL is the maximum allowable input level for all digital inputs.

Serial Audio Data - SDATA

Pin 3, Input

Function:

Two's complement MSB-first serial data is input on this pin. The data is clocked into SDATA via the serial clock and the channel is determined by the Left/Right clock. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Mode Control Byte in Control Port Mode or the Mode Pins in Hardware Mode. The options are detailed in Figures 6-24.

Serial Clock - SCLK

Pin 4, Input

Function:

Clocks the individual bits of the serial data into the SDATA pin. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Mode Control Byte in Control Port Mode or the Mode pins in Hardware Mode. The options are detailed in Figures 6-24.

Left / Right Clock - LRCK

Pin 5, Input

Function:

The Left / Right clock determines which channel is currently being input on the serial audio data input, SDATA. The frequency of the Left/Right clock must be at the input sample rate. Audio samples in Left/Right sample pairs will be simultaneously output from the digital-to-analog converter whereas Right/Left pairs will exhibit a one sample period difference. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Mode Control Byte in Control Port Mode or the Mode pins in Stand-alone Mode. The options are detailed in Figures 6-24.

Master Clock - MCLK

Pin 6, Input

Function:

The master clock frequency must be either 256x, 384x, 512x, 768x or 1024x the input sample rate in Single Speed Mode; either 128x, 192x 256x, 384x or 512x the input sample rate in Double Speed Mode; or 64x, 96x 128x, 192x or 256 x the input sample rate in Quad Speed Mode. Tables 8-10 illustrate the standard audio sample rates and the required master clock frequencies.

Note: These clocking ratios are only available in Control Port Mode when the MCLK Divide bit is enabled.

Mode Select - M3, M2, M1 and M0 (Stand-alone Mode)

Pins 7, 8, 9 and 10 Inputs

Function:

The Mode Select Pins, M0-M3, select the operational mode of the device as detailed in Tables 11-15.

Mode Select - M3 (Control Port Mode)

Pin 7, Input

Function:

The Mode Select Pin, M3, is not used in PCM Control Port mode and should be terminated to ground.

Serial Control Interface Clock - SCL/CCLK (Control Port Mode)

Pin 8, Input

Function:

Clocks the serial control data into or from SDA/CDIN.

Serial Control Data I/O - SDA/CDIN (Control Port Mode)

Pin 9, Input/Output

Function:

In I²C mode, SDA is a data I/O line. CDIN is the input data line for the control port interface in SPI mode.

Address Bit / Chip Select - AD0 / $\overline{\text{CS}}$ (Control Port Mode)

Pin 10, Input

Function:

In I²C mode, AD0 is a chip address bit. $\overline{\text{CS}}$ is used to enable the control port interface in SPI mode. The device will enter the SPI mode at anytime a high to low transition is detected on this pin. Once the device has entered the SPI mode, it will remain until either the part is reset or undergoes a power-down cycle.

Positive Voltage Reference - FILT+

Pin 11, Output

Function:

Positive reference for internal sampling circuits. External capacitors are required from FILT+ to analog ground, as shown in Figure 5 and . The recommended values will typically provide 60 dB of PSRR at 1 kHz and 40 dB of PSRR at 60 Hz. FILT+ is not intended to supply external current. FILT+ has a typical source impedance of 250 k Ω and any current drawn from this pin will alter device performance.

Common Mode Voltage - CMOOUT

Pin 12, Output

Function:

Filter connection for internal common mode reference voltage, typically 50% of V_A. Capacitors must be connected from CMOOUT to analog ground, as shown in Figure 5. CMOOUT is not intended to supply external current. CMOOUT has a typical source impedance of 250 k Ω and any current drawn from this pin will alter device performance.

Channel A and Channel B Mute Control - AMUTEC and BMUTEC

Pins 13 and 20, Outputs

Function:

The Mute Control pins go high during power-up initialization, reset, muting, master clock to left/right clock frequency ratio is incorrect or power-down. These pins are intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single supply system. Use of Mute Control is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops.

Differential Analog Output - AOUTB+, AOUTB- and AOUTA+, AOUTA-

Pins 14, 15 and 18, 19, Outputs

Function:

The full scale differential analog output level is specified in the Analog Characteristics specifications table.

Analog Ground - AGND

Pin 16, Input

Function:

Analog ground reference.

Analog Power - VA

Pin 17, Input

Function:

Analog power supply. Typically 3 to 5 VDC.

6. PIN DESCRIPTION - DSD MODE

| | | | | | |
|-------------------|-------------------------|------|------|---------------|-------------------|
| Reset | $\overline{\text{RST}}$ | □ 1 | 20 □ | AMUTEC | Refer to PCM Mode |
| Logic Voltage | VL | □ 2 | 19 □ | AOUTA- | Refer to PCM Mode |
| Channel A Data | DSD_A | □ 3 | 18 □ | AOUTA+ | Refer to PCM Mode |
| Channel B Data | DSD_B | □ 4 | 17 □ | VA | Refer to PCM Mode |
| DSD Mode Select | DSD_MODE | □ 5 | 16 □ | AGND | Refer to PCM Mode |
| Master Clock | MCLK | □ 6 | 15 □ | AOUTB+ | Refer to PCM Mode |
| DSD Serial Clock | DSD_SCLK | □ 7 | 14 □ | AOUTB- | Refer to PCM Mode |
| Refer to PCM Mode | (SCL/CCLK) M2 | □ 8 | 13 □ | BMUTEC | Refer to PCM Mode |
| Refer to PCM Mode | (SDA/CDIN) M1 | □ 9 | 12 □ | CMOUT | Refer to PCM Mode |
| Refer to PCM Mode | (AD0/CS) M0 | □ 10 | 11 □ | FILT+ | Refer to PCM Mode |

DSD Audio Data - DSD_A and DSD_B

Pins 3 and 4, Inputs

Function:

Direct Stream Digital audio data is clocked into DSD_A and DSD_B via the DSD serial clock.

DSD Mode - DSD_Mode

Pin 5, Input

Function:

This pin must be set to a logic '1' and M0-M2 must be properly set to access the DSD Mode in Hardware Mode. Refer to Table 19.

In Control Port Mode, this pin must be set to a logic '1' and the Control Registers must be properly set to access the DSD Mode. Refer to register descriptions.

Master Clock - MCLK

Pin 6, Input

Function:

The master clock frequency must be either 4x, 6x, 8x or 12x the DSD data rate for 64x oversampled DSD data or 2x, 3x, 4x or 6x the DSD data rate for 128x oversampled DSD data.

DSD Serial Clock - DSD_SCLK

Pin 7, Input

Function:

Clocks the individual bits of the DSD audio data into the DSD_A and DSD_B pins.

| DIF2 | DIF1 | DIFO | DESCRIPTION |
|------|------|------|-------------------------------------|
| 0 | 0 | 0 | Left Justified, up to 24-bit data |
| 0 | 0 | 1 | I ² S, up to 24-bit data |
| 0 | 1 | 0 | Right Justified, 16-bit Data |
| 0 | 1 | 1 | Right Justified, 24-bit Data |
| 1 | 0 | 0 | Right Justified, 20-bit Data |
| 1 | 0 | 1 | Right Justified, 18-bit Data |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

Table 1. Digital Interface Formats - PCM Modes

| DIF2 | DIF1 | DIFO | DESCRIPTION |
|------|------|------|---|
| 0 | 0 | 0 | 64x oversampled DSD data with a 4x MCLK to DSD data rate |
| 0 | 0 | 1 | 64x oversampled DSD data with a 6x MCLK to DSD data rate |
| 0 | 1 | 0 | 64x oversampled DSD data with a 8x MCLK to DSD data rate |
| 0 | 1 | 1 | 64x oversampled DSD data with a 12x MCLK to DSD data rate |
| 1 | 0 | 0 | 128x oversampled DSD data with a 2x MCLK to DSD data rate |
| 1 | 0 | 1 | 128x oversampled DSD data with a 3x MCLK to DSD data rate |
| 1 | 1 | 0 | 128x oversampled DSD data with a 4x MCLK to DSD data rate |
| 1 | 1 | 1 | 128x oversampled DSD data with a 6x MCLK to DSD data rate |

Table 2. Digital Interface Formats - DSD Mode

| DEM1 | DEMO | DESCRIPTION |
|------|------|----------------------|
| 0 | 0 | Disabled |
| 0 | 1 | 44.1 kHz de-emphasis |
| 1 | 0 | 48 kHz de-emphasis |
| 1 | 1 | 32 kHz de-emphasis |

Table 3. De-Emphasis Mode Selection

| FM1 | FM0 | MODE |
|-----|-----|--|
| 0 | 0 | Single-Speed Mode (4 to 50 kHz sample rates) |
| 0 | 1 | Double-Speed Mode (50 to 100 kHz sample rates) |
| 1 | 0 | Quad-Speed Mode (100 to 200 kHz sample rates) |
| 1 | 1 | Direct Stream Digital Mode |

Table 4. Functional Mode Selection

| SOFT | ZERO | Mode |
|------|------|----------------------------------|
| 0 | 0 | Changes to affect immediately |
| 0 | 1 | Zero Cross enabled |
| 1 | 0 | Soft Ramp enabled |
| 1 | 1 | Soft Ramp and Zero Cross enabled |

Table 5. Soft Cross or Zero Cross Mode Selection

| ATAPI4 | ATAPI3 | ATAPI2 | ATAPI1 | ATAPI0 | AOUTA | AOUTB |
|--------|--------|--------|--------|--------|---------------|---------------|
| 0 | 0 | 0 | 0 | 0 | MUTE | MUTE |
| 0 | 0 | 0 | 0 | 1 | MUTE | bR |
| 0 | 0 | 0 | 1 | 0 | MUTE | bL |
| 0 | 0 | 0 | 1 | 1 | MUTE | $b[(L+R)/2]$ |
| 0 | 0 | 1 | 0 | 0 | aR | MUTE |
| 0 | 0 | 1 | 0 | 1 | aR | bR |
| 0 | 0 | 1 | 1 | 0 | aR | bL |
| 0 | 0 | 1 | 1 | 1 | aR | $b[(L+R)/2]$ |
| 0 | 1 | 0 | 0 | 0 | aL | MUTE |
| 0 | 1 | 0 | 0 | 1 | aL | bR |
| 0 | 1 | 0 | 1 | 0 | aL | bL |
| 0 | 1 | 0 | 1 | 1 | aL | $b[(L+R)/2]$ |
| 0 | 1 | 1 | 0 | 0 | $a[(L+R)/2]$ | MUTE |
| 0 | 1 | 1 | 0 | 1 | $a[(L+R)/2]$ | bR |
| 0 | 1 | 1 | 1 | 0 | $a[(L+R)/2]$ | bL |
| 0 | 1 | 1 | 1 | 1 | $a[(L+R)/2]$ | $b[(L+R)/2]$ |
| 1 | 0 | 0 | 0 | 0 | MUTE | MUTE |
| 1 | 0 | 0 | 0 | 1 | MUTE | bR |
| 1 | 0 | 0 | 1 | 0 | MUTE | bL |
| 1 | 0 | 0 | 1 | 1 | MUTE | $[(bL+aR)/2]$ |
| 1 | 0 | 1 | 0 | 0 | aR | MUTE |
| 1 | 0 | 1 | 0 | 1 | aR | bR |
| 1 | 0 | 1 | 1 | 0 | aR | bL |
| 1 | 0 | 1 | 1 | 1 | aR | $[(aL+bR)/2]$ |
| 1 | 1 | 0 | 0 | 0 | aL | MUTE |
| 1 | 1 | 0 | 0 | 1 | aL | bR |
| 1 | 1 | 0 | 1 | 0 | aL | bL |
| 1 | 1 | 0 | 1 | 1 | aL | $[(aL+bR)/2]$ |
| 1 | 1 | 1 | 0 | 0 | $[(aL+bR)/2]$ | MUTE |
| 1 | 1 | 1 | 0 | 1 | $[(aL+bR)/2]$ | bR |
| 1 | 1 | 1 | 1 | 0 | $[(bL+aR)/2]$ | bL |
| 1 | 1 | 1 | 1 | 1 | $[(aL+bR)/2]$ | $[(aL+bR)/2]$ |

Table 6. ATAPI Decode

| Binary Code | Decimal Value | Volume Setting |
|-------------|---------------|----------------|
| 0000000 | 0 | 0 dB |
| 0010100 | 20 | -20 dB |
| 0101000 | 40 | -40 dB |
| 0111100 | 60 | -60 dB |
| 1011010 | 90 | -90 dB |

Table 7. Digital Volume Control

Note: These clocking ratios are only available in Control Port Mode when the MCLK Divide bit is enabled.

| Sample Rate (kHz) | MCLK (MHz) | | | | See Note |
|-------------------|------------|---------|---------|---------|----------|
| | 256x | 384x | 512x | 768x | 1024x |
| 32 | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 32.7680 |
| 44.1 | 11.2896 | 16.9344 | 22.5792 | 33.8688 | 45.1584 |
| 48 | 12.2880 | 18.4320 | 24.5760 | 36.8640 | 49.1520 |

Table 8. Single Speed (4 to 50 kHz sample rates) Common Clock Frequencies

| Sample Rate (kHz) | MCLK (MHz) | | | | See Note |
|-------------------|------------|---------|---------|---------|----------|
| | 128x | 192x | 256x | 384x | 512x |
| 64 | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 32.7680 |
| 88.2 | 11.2896 | 16.9344 | 22.5792 | 33.8688 | 45.1584 |
| 96 | 12.2880 | 18.4320 | 24.5760 | 36.8640 | 49.1520 |

Table 9. Double Speed (50 to 100 kHz sample rates) Common Clock Frequencies

| Sample Rate (kHz) | MCLK (MHz) | | | | See Note |
|-------------------|------------|---------|---------|---------|----------|
| | 64x | 96x | 128x | 192x | 256x |
| 176.4 | 11.2896 | 16.9344 | 22.5792 | 33.8688 | 45.1584 |
| 192 | 12.2880 | 18.4320 | 24.5760 | 36.8640 | 49.1520 |

Table 10. Quad Speed (100 to 200 kHz sample rates) Common Clock Frequencies

| M3 | M1 (DIF1) | M0 (DIF0) | DESCRIPTION | FORMAT | FIGURE |
|----|-----------|-----------|-------------------------------------|--------|--------|
| 0 | 0 | 0 | Left Justified, up to 24-bit data | 0 | 6 |
| 0 | 0 | 1 | I ² S, up to 24-bit data | 1 | 7 |
| 0 | 1 | 0 | Right Justified, 16-bit Data | 2 | 8 |
| 0 | 1 | 1 | Right Justified, 24-bit Data | 3 | 9 |

Table 11. Single Speed (4 to 50 kHz) Digital Interface Format, Stand-Alone Mode Options

| M3 | M2 (DEM) | DESCRIPTION | FIGURE |
|----|----------|---------------------|--------|
| 0 | 0 | No De-Emphasis | 12 |
| 0 | 1 | De-Emphasis Enabled | 12 |

Table 12. Single Speed Only (4 to 50 kHz) De-Emphasis, Stand-Alone Mode Options

| M3 | M2 | M1 | M0 | DESCRIPTION | FORMAT | FIGURE |
|----|----|----|----|------------------------------------|--------|--------|
| 1 | 0 | 0 | 0 | Left Justified up to 24-bit data | 0 | 6 |
| 1 | 0 | 0 | 1 | I ² S up to 24-bit data | 1 | 7 |
| 1 | 0 | 1 | 0 | Right Justified 16-bit data | 2 | 8 |
| 1 | 0 | 1 | 1 | Right Justified 24-bit data | 3 | 9 |

Table 13. Double Speed (50 to 100 kHz) Digital Interface Format, Stand-Alone Mode Options

| M3 | M2 | M1 | M0 | DESCRIPTION | FORMAT | FIGURE |
|----|----|----|----|------------------------------------|--------|--------|
| 1 | 1 | 0 | 0 | Left Justified up to 24-bit data | 0 | 6 |
| 1 | 1 | 0 | 1 | I ² S up to 24-bit data | 1 | 7 |
| 1 | 1 | 1 | 0 | Right Justified 16-bit data | 2 | 8 |
| 1 | 1 | 1 | 1 | Right Justified 24-bit data | 3 | 9 |

Table 14. Quad Speed (100 to 200 kHz) Digital Interface Format, Stand-Alone Mode Options

| DSD_Mode | M2 | M1 | M0 | DESCRIPTION |
|----------|----|----|----|---|
| 1 | 0 | 0 | 0 | 64x oversampled DSD data with a 4x MCLK to DSD data rate |
| 1 | 0 | 0 | 1 | 64x oversampled DSD data with a 6x MCLK to DSD data rate |
| 1 | 0 | 1 | 0 | 64x oversampled DSD data with a 8x MCLK to DSD data rate |
| 1 | 0 | 1 | 1 | 64x oversampled DSD data with a 12x MCLK to DSD data rate |
| 1 | 1 | 0 | 0 | 128x oversampled DSD data with a 2x MCLK to DSD data rate |
| 1 | 1 | 0 | 1 | 128x oversampled DSD data with a 3x MCLK to DSD data rate |
| 1 | 1 | 1 | 0 | 128x oversampled DSD data with a 4x MCLK to DSD data rate |
| 1 | 1 | 1 | 1 | 128x oversampled DSD data with a 6x MCLK to DSD data rate |

Table 15. Direct Stream Digital (DSD), Stand-Alone Mode Options

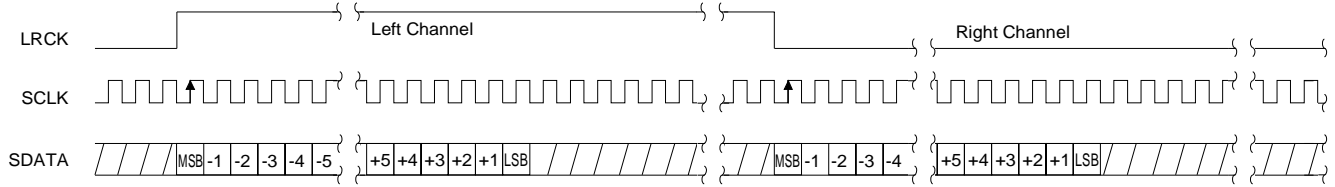


Figure 6. Format 0, Left Justified up to 24-Bit Data

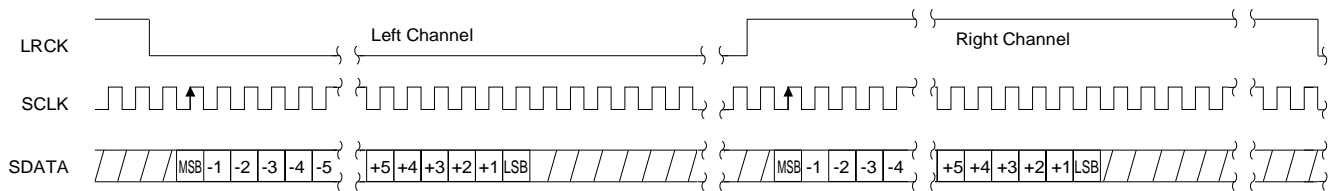


Figure 7. Format 1, I²S up to 24-Bit Data

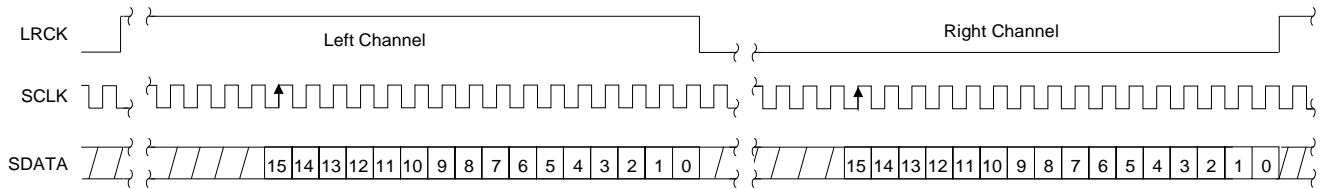


Figure 8. Format 2, Right Justified 16-Bit Data

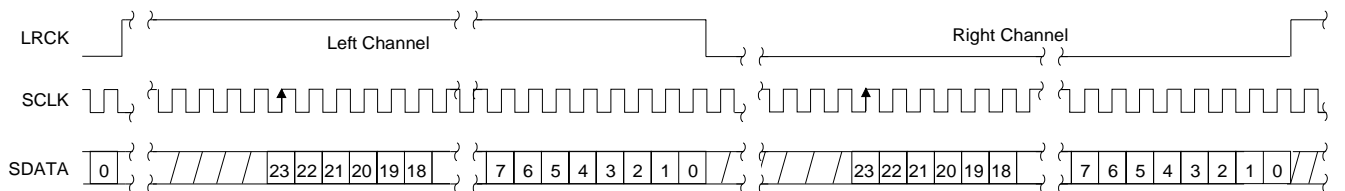


Figure 9. Format 3, Right Justified 24-Bit Data

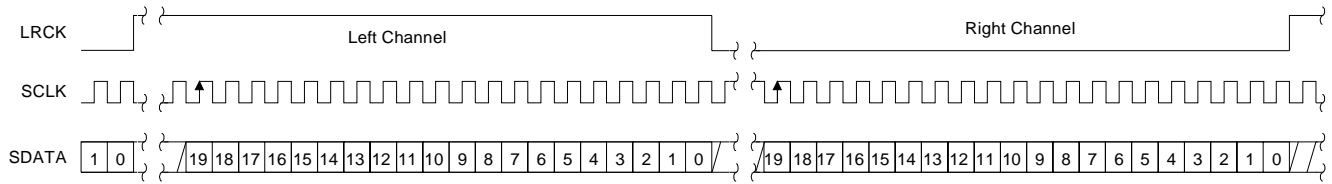


Figure 10. Format 4, Right Justified 20-Bit Data. (Available in Control Port Mode only)

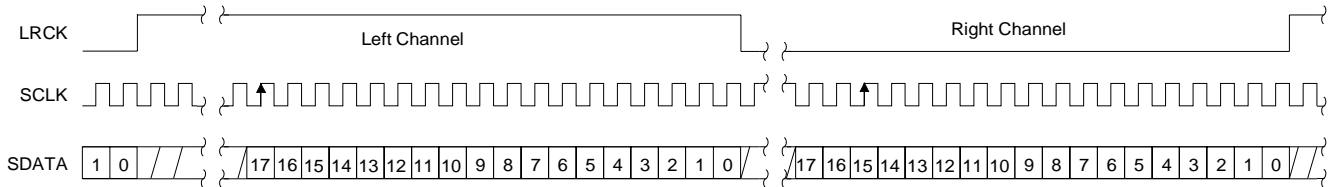


Figure 11. Format 5, Right Justified 18-Bit Data. (Available in Control Port Mode only)

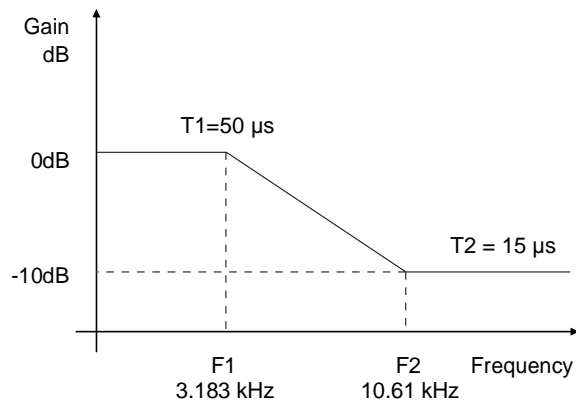


Figure 12. De-Emphasis Curve

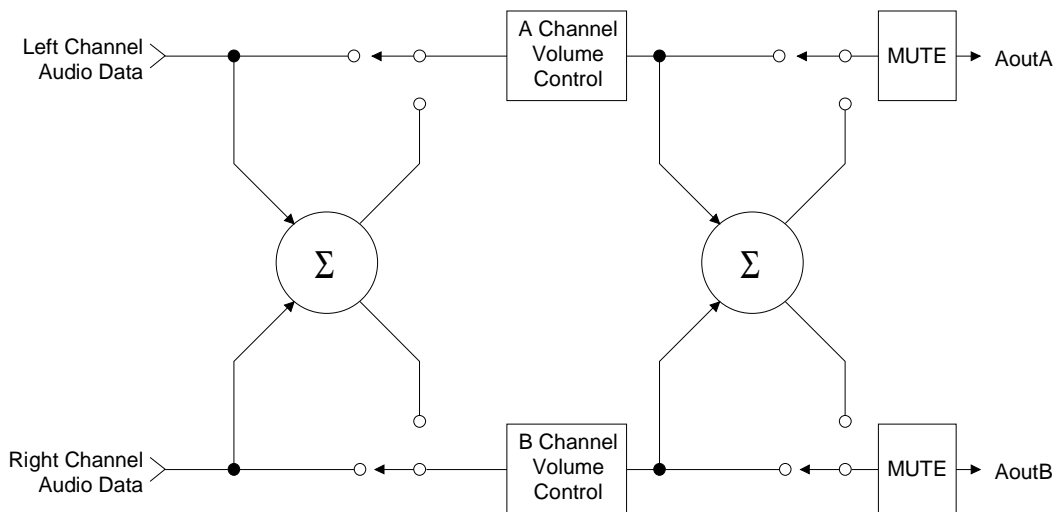


Figure 13. ATAPI Block Diagram

7. APPLICATIONS

7.1 Recommended Power-up Sequence for Hardware Mode

- 1) Hold $\overline{\text{RST}}$ low until the power supplies, master, and left/right clocks are stable.
- 2) Bring $\overline{\text{RST}}$ high.

7.2 Recommended Power-up Sequence and Access to Control Port Mode

- 1) Hold $\overline{\text{RST}}$ low until the power supply, master, and left/right clocks are stable. In this state, the control port is reset to its default settings and CMOUT will remain low.
- 2) Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with CMOUT low and the control port is accessible.
- 3) Write 11h to register 5 within 10 ms cycles following the release of $\overline{\text{RST}}$.

- 4) The desired register settings can be loaded while keeping the PDN bit set to 1.
- 5) Set the PDN bit to 0 which will initiate the power-up sequence which requires approximately 10 μs .

7.3 Analog Output and Filtering

The application note “Design Notes for a 2-Pole Filter with Differential Input” discusses the second-order Butterworth filter and differential to single-ended converter which was implemented on the CS4391 evaluation board, CDB4391. The CS4391 filter, as seen in Figure 14, is a linear phase design and does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry.

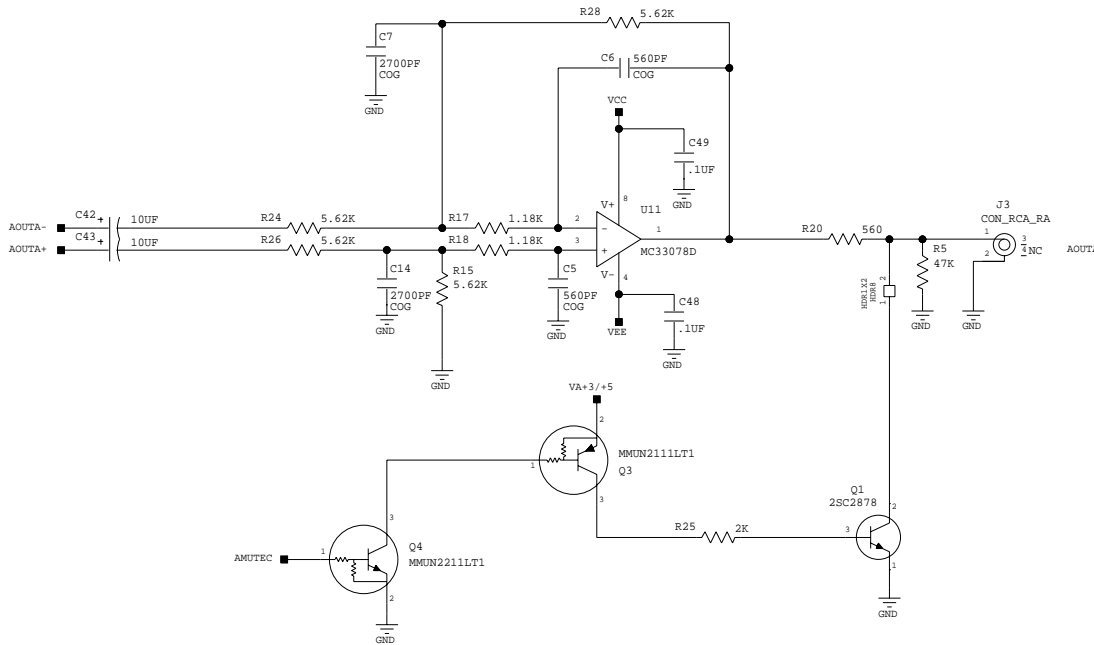


Figure 14. CS4391 Output Filter

8. CONTROL PORT INTERFACE

The control port is used to load all the internal settings of the CS4391. The operation of the control port may be completely asynchronous to the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI and I²C, with the CS4391 operating as a slave device in both modes. If I²C operation is desired, AD0/ $\overline{\text{CS}}$ should be tied to VA or AGND. If the CS4391 ever detects a high to low transition on AD0/ $\overline{\text{CS}}$ after power-up, SPI mode will be selected. The control port registers are write-only in SPI mode.

8.1 SPI Mode

In SPI mode, $\overline{\text{CS}}$ is the CS4391 chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller and the chip address is 0010000. All signals are inputs and data is clocked in on the rising edge of CCLK.

Figure 15 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{\text{CS}}$ low. The first 7 bits on CDIN form the chip address, and must be 0010000. The eighth bit is a read/write indicator ($\text{R}/\overline{\text{W}}$), which must be low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into the register designated by the MAP. See Table 16.

The CS4391 has MAP auto increment capability, enabled by the INCR bit in the MAP register. If

INCR is 0, then the MAP will stay constant for successive writes. If INCR is set to 1, then MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

8.2 I²C Mode

In I²C mode, SDA is a bi-directional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 3. There is no $\overline{\text{CS}}$ pin. Pin AD0 forms the partial chip address and should be tied to VA or AGND as required. The upper 6 bits of the 7-bit address field must be 001000. To communicate with the CS4391 the LSB of the chip address field, which is the first byte sent to the CS4391, should match the setting of the AD0 pin. The eighth bit of the address byte is the $\text{R}/\overline{\text{W}}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer, MAP, which selects the register to be read or written. The MAP is then followed by the data to be written. If the operation is a read, then the contents of the register pointed to by the MAP will be output after the chip address.

The CS4391 has MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is 0, then the MAP will stay constant for successive writes. If INCR is set to 1, then MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

For more information on I²C, please see “The I²C-Bus Specification: Version 2.0”, listed in the References section.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|----------|----------|----------|------|------|------|
| INCR | Reserved | Reserved | Reserved | Reserved | MAP2 | MAP1 | MAP0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

INCR (Auto MAP Increment Enable)

Default = '0'.

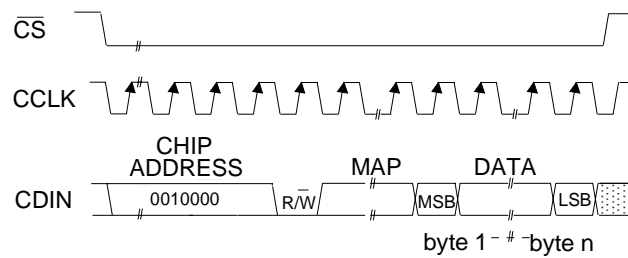
0 - Disabled

1 - Enabled

MAP0-2 (Memory Address Pointer)

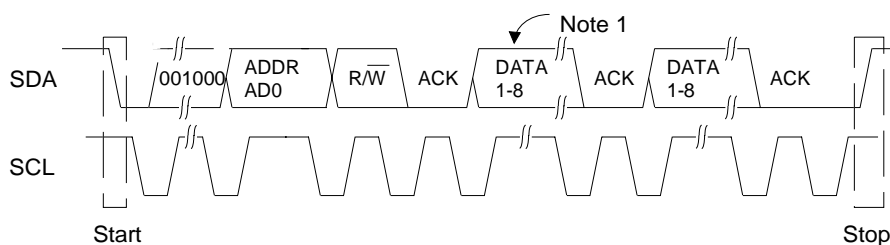
Default = '000'.

Table 16. Memory Address Pointer (MAP)



MAP = Memory Address Pointer

Figure 15. Control Port Timing, SPI mode



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 16. Control Port Timing, I²C Mode

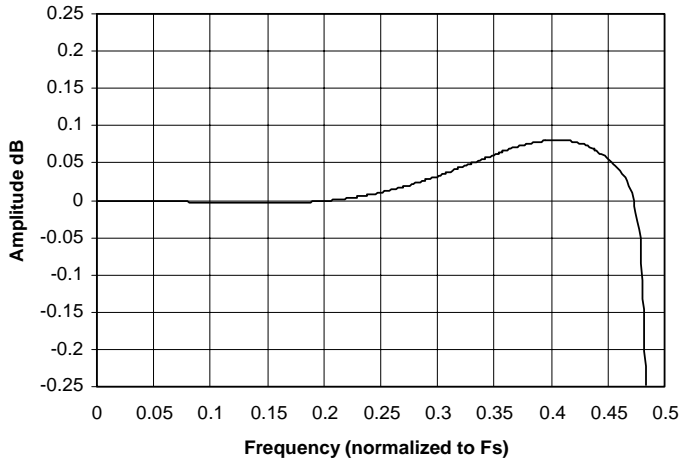


Figure 17. Single-Speed Frequency Response

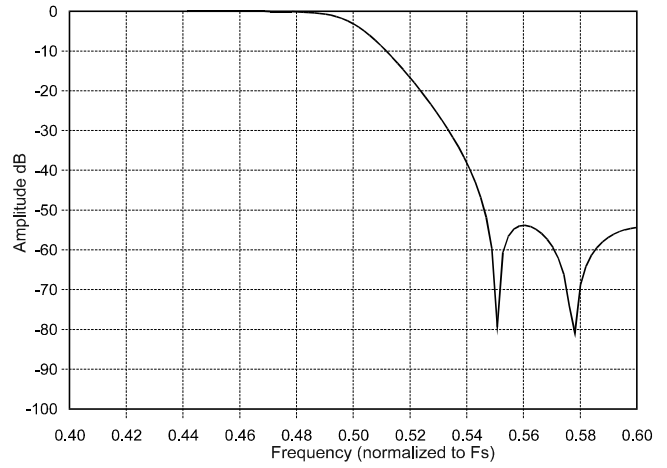


Figure 18. Single-Speed Transition Band

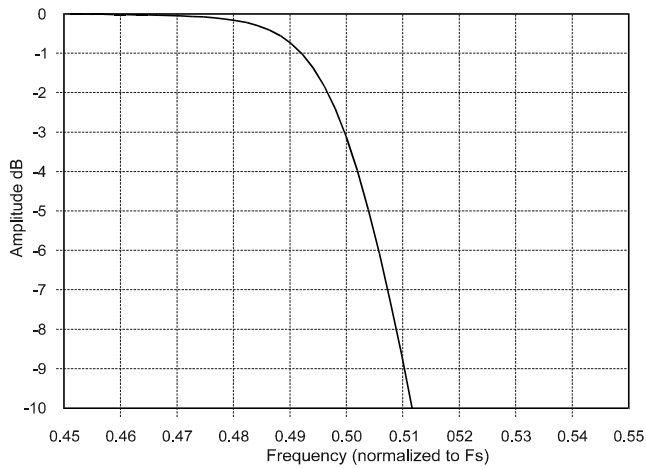


Figure 19. Single-Speed Transition Band

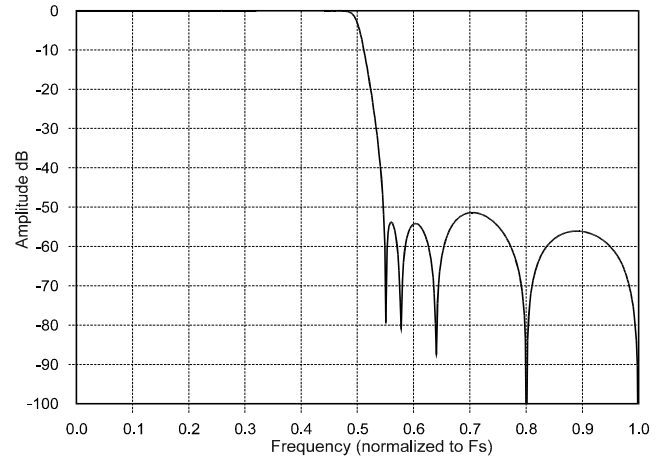


Figure 20. Single-Speed Stopband Rejection

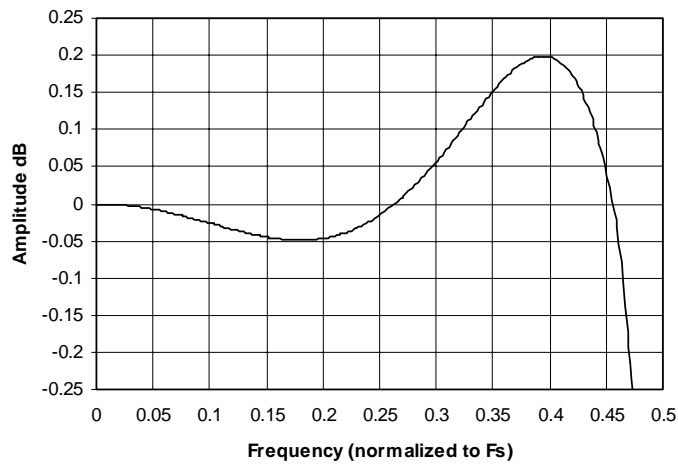


Figure 21. Double-Speed Frequency Response

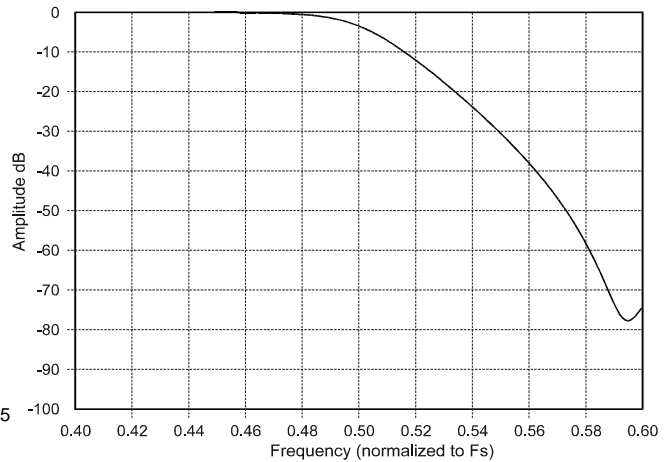
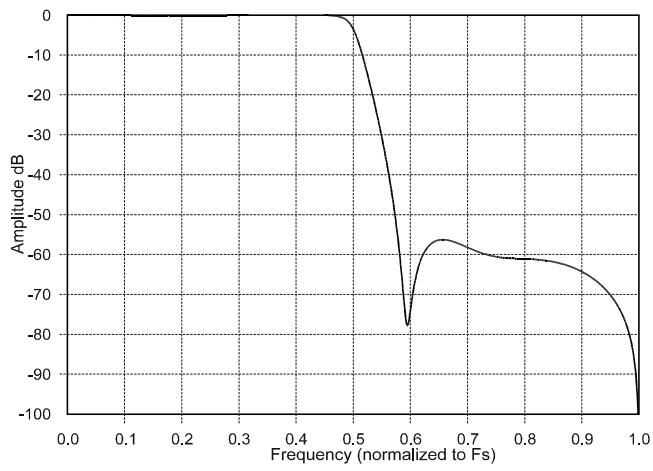
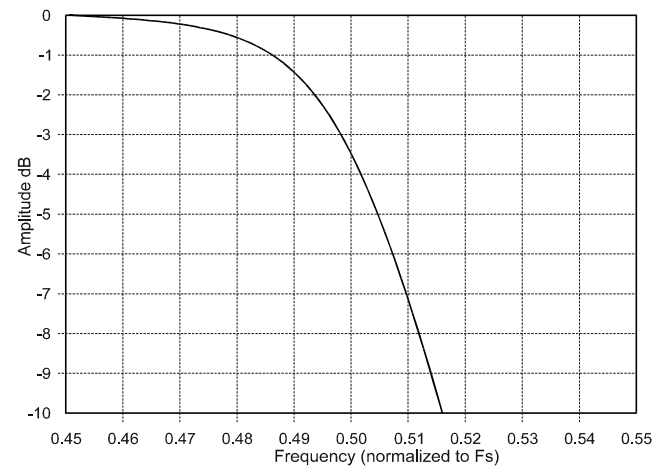


Figure 22. Double-Speed Transition Band

**Figure 23. Double-Speed Transition Band****Figure 24. Double-Speed Stopband Rejection**

9. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10Hz to 20kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

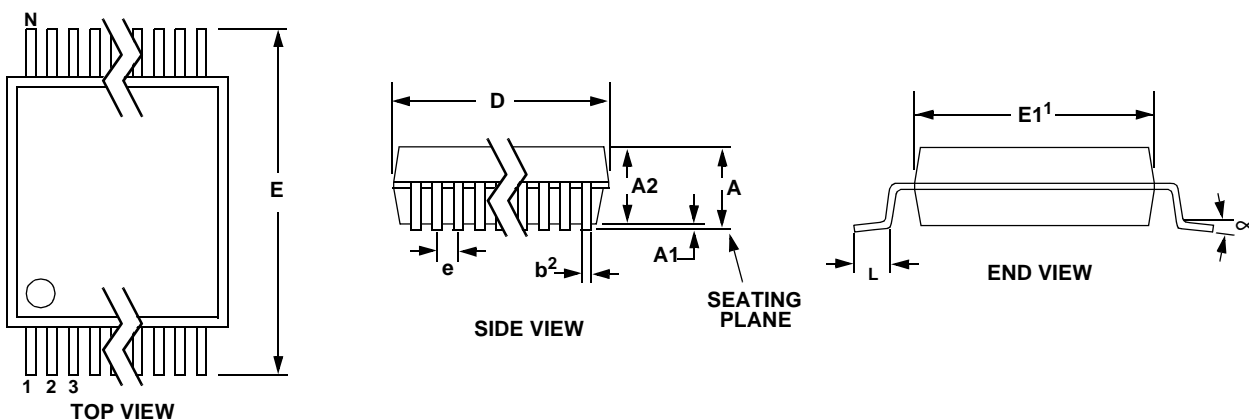
Gain Drift

The change in gain value with temperature. Units in ppm/°C.

10. REFERENCES

1. "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.
2. CDB4391 Evaluation Board Datasheet
3. "The I²C-Bus Specification: Version 2.0" Philips Semiconductors, December 1998. <http://www.semiconductors.philips.com>



11. PACKAGE DIMENSIONS
20L TSSOP (4.4 mm BODY) PACKAGE DRAWING


| DIM | INCHES | | | MILLIMETERS | | | NOT E |
|----------|---------|--------|-------|-------------|-------|------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| A | -- | -- | 0.043 | -- | -- | 1.10 | |
| A1 | 0.002 | 0.004 | 0.006 | 0.05 | -- | 0.15 | |
| A2 | 0.03346 | 0.0354 | 0.037 | 0.85 | 0.90 | 0.95 | |
| b | 0.00748 | 0.0096 | 0.012 | 0.19 | 0.245 | 0.30 | 2,3 |
| D | 0.252 | 0.256 | 0.259 | 6.40 | 6.50 | 6.60 | 1 |
| E | 0.248 | 0.2519 | 0.256 | 6.30 | 6.40 | 6.50 | |
| E1 | 0.169 | 0.1732 | 0.177 | 4.30 | 4.40 | 4.50 | 1 |
| e | -- | -- | 0.026 | -- | -- | 0.65 | |
| L | 0.020 | 0.024 | 0.028 | 0.50 | 0.60 | 0.70 | |
| ∞ | 0° | 4° | 8° | 0° | 4° | 8° | |

JEDEC #: MO-153

Controlling Dimension is Millimeters.

- Notes:
1. "D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
 2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
 3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

• **Notes** •

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