

24-Pin XOR AmPAL20XRP10 Family

24-Pin IMOX™ Programmable Array Logic (PAL) Elements

Distinctive Characteristics

- AND-OR-XOR logic structure
- AMD's superior IMOX technology
 - Guarantees $t_{PD} = 20$ ns max
- Individually programmable output polarity on each output
- Eight logical product terms per output
- Programming yields > 98% are realized via platinum-silicide fuse technology and the use of added test words
- Post Programming Functional Yield (PPFY) of 99.9%
- PRELOAD feature permits full logical verification
- Reliability assured through more than 70 billion fuse hours of life testing with no failures
- AC and DC parametric testing at the factory through on-board testing circuitry
- > 3000V ESD protection per pin
- JEDEC-Standard LCC and PLCC pinout

General Description

AMD 24-pin XOR PAL devices are high-speed, electrically programmable array logic elements. They utilize the familiar sum-of-products (AND-OR-XOR) structure allowing users to program custom logic functions to fit most applications precisely. Typically they are a replacement for low-power Schottky SSI/MSI logic circuits that require an exclusive-OR function, reducing chip count by more than 5 to 1 and greatly simplifying prototyping and board layout.

Five different devices are available, including both registered and combinatorial devices. All devices have user-programmable output polarity on all outputs. A variety of speed options allow the designer maximum flexibility in matching precise system requirements. The Product Selector Guide below shows the available speed options. The second table gives details about the functionality of the five available devices.

Please see the following pages for Block Diagrams.

Product Selector Guide

AMD PAL Speed/Power Families

| Family | t_{PD} ns (Max.) | | t_S ns (Min.) | | t_{CO} ns (Max.) | | I_{CC} mA (Max.) | I_{OL} mA (Min.) | |
|--|-----------------------|-----------|--------------------|-----------|-----------------------|-----------|-----------------------|-----------------------|-----------|
| | C Devices | M Devices | C Devices | M Devices | C Devices | M Devices | C/M Devices | C Devices | M Devices |
| Very High-Speed (-20 & -25) Versions | 20 | 25 | 20 | 25 | 13 | 15 | 210 | 24 | 12 |
| High-Speed (-30 & -35) Versions | 30 | 35 | 30 | 35 | 15 | 25 | 180 | 24 | 12 |
| High-Speed, Half-Power (-30L & -35L) Versions | 30 | 35 | 30 | 35 | 15 | 25 | 105 | 24 | 12 |
| Half-Power (-40L & -45L) Versions | 40 | 45 | 40 | 45 | 30 | 35 | 105 | 24 | 12 |

| Part Number | Array Inputs | Logic | Output Enable | Outputs/Polarity | Package Pins |
|-------------|---|-----------------------------|---------------|----------------------------|--------------|
| 22XP10 | 12 Dedicated, 10 Bidirectional | Ten (2-6)-Wide AND-OR-XOR | Programmable | Bidirectional/Programmable | 24 |
| 20XRP4 | 10 Dedicated, 4 Feedback, 6 Bidirectional | Four (2-6)-Wide AND-OR-XOR | Dedicated | Registered/Programmable | 24 |
| | | Six 8-Wide AND-OR | Programmable | Bidirectional/Programmable | |
| 20XRP6 | 10 Dedicated, 6 Feedback, 4 Bidirectional | Six (2-6)-Wide AND-OR-XOR | Dedicated | Registered/Programmable | 24 |
| | | Four 8-Wide AND-OR | Programmable | Bidirectional/Programmable | |
| 20XRP8 | 10 Dedicated, 8 Feedback, 2 Bidirectional | Eight (2-6)-Wide AND-OR-XOR | Dedicated | Registered/Programmable | 24 |
| | | Two 8-Wide AND-OR | Programmable | Bidirectional/Programmable | |
| 20XRP10 | 10 Dedicated, 10 Feedback | Ten (2-6)-Wide AND-OR-XOR | Dedicated | Registered/Programmable | 24 |

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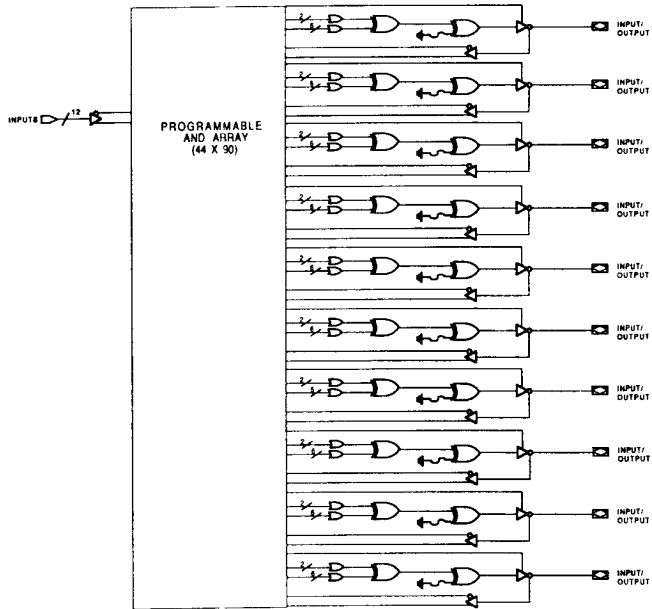


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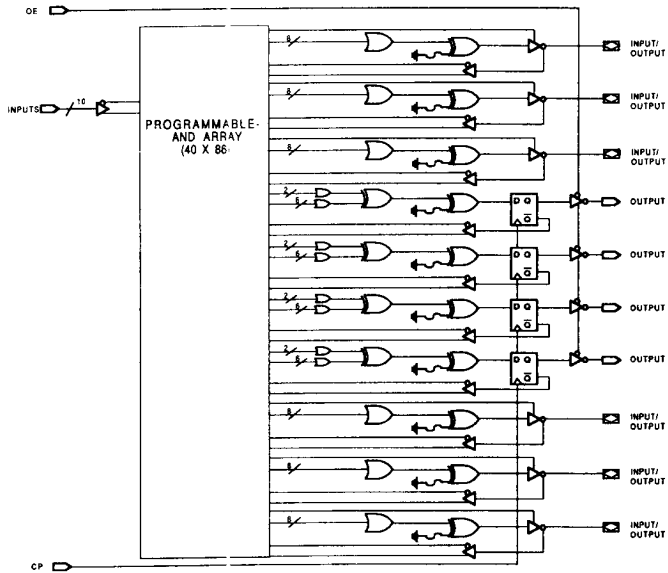
Block Diagrams

AmpPAL22XP10



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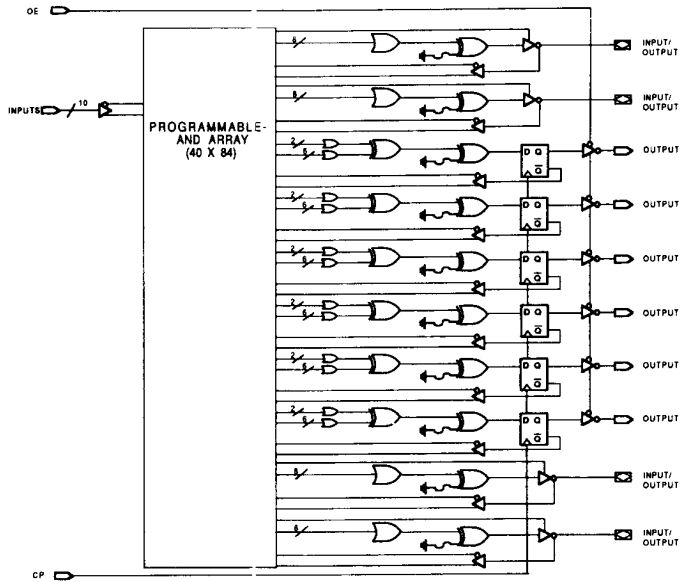
AmpPAL20XRP4



LD000940

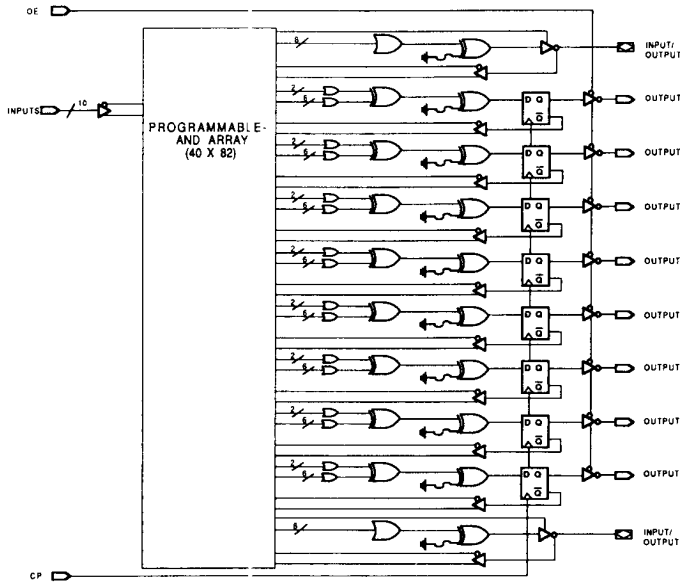
Block Diagrams (Cont'd.)

AmPAL20XRP6



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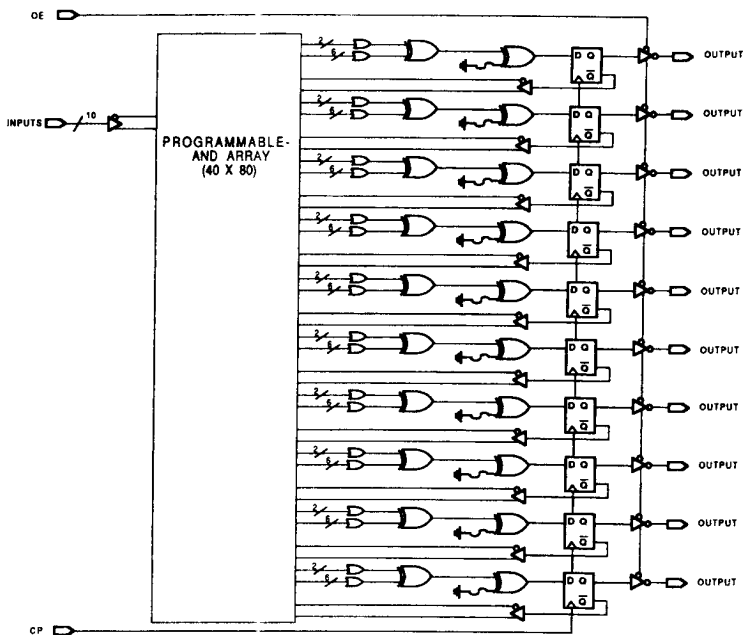
AmPAL20XRP8



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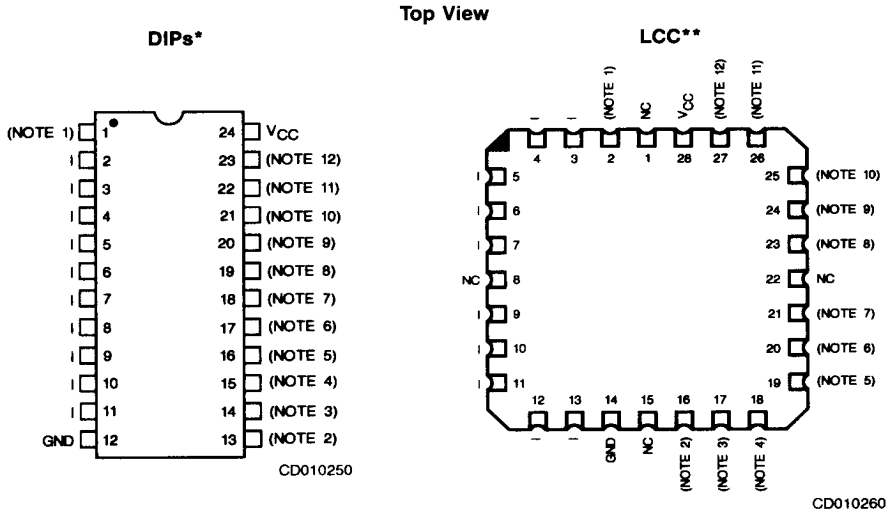
Block Diagrams (Cont'd.)

AmPAL20XRP10



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Connection Diagrams



Note: Pin 1 is marked for orientation.

Notes:

| | 22XP10 | 20XRP4 | 20XRP6 | 20XRP8 | 20XRP10 |
|----|--------|--------|--------|--------|---------|
| 1 | I | CLK | CLK | CLK | CLK |
| 2 | I | OE | OE | OE | OE |
| 3 | I/O | I/O | I/O | I/O | O |
| 4 | I/O | I/O | I/O | O | O |
| 5 | I/O | I/O | O | O | O |
| 6 | I/O | O | O | O | O |
| 7 | I/O | O | O | O | O |
| 8 | I/O | O | O | O | O |
| 9 | I/O | O | O | O | O |
| 10 | I/O | I/O | O | O | O |
| 11 | I/O | I/O | I/O | O | O |
| 12 | I/O | I/O | I/O | I/O | O |

*Also available in 24-Pin Ceramic Flatpack. Pinouts identical to DIPs.
 **Also available in 28-Pin Plastic Leaded Chip Carrier. Pinouts identical to LCC.

Pin Designations

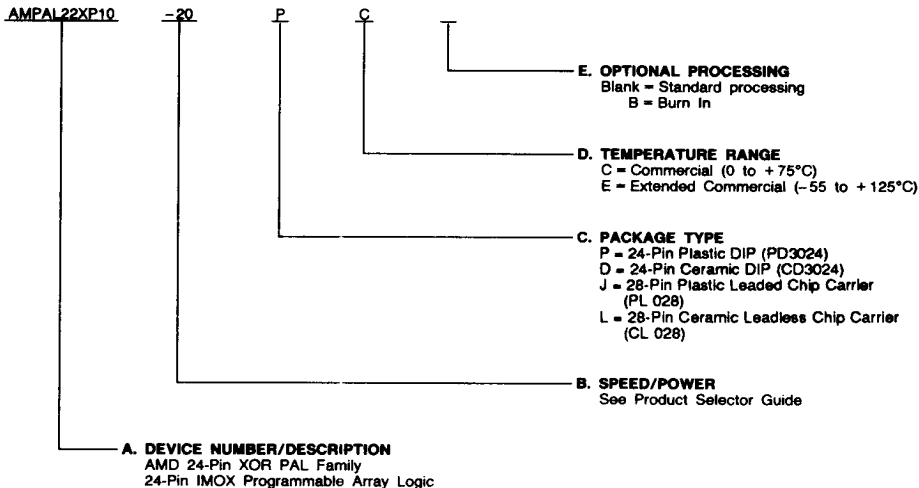
- I = Input
- I/O = Input/Output
- O = Output
- VCC = Supply Voltage
- GND = Ground
- CLK = Clock
- OE = Output Enable
- NC = No Connect

Ordering Information

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Package Type**
- D. Temperature Range**
- E. Optional Processing**



| Valid Combinations | |
|-------------------------------|-----------------------------------|
| AMPAL22XP10-20/-30/-30L/-40L | PC, DC, DCB, DE, JC, LC, LE |
| AMPAL20XRP4-20/-30/-30L/-40L | |
| AMPAL20XRP6-20/-30/-30L/-40L | |
| AMPAL20XRP8-20/-30/-30L/-40L | |
| AMPAL20XRP10-20/-30/-30L/-40L | |

Valid Combinations

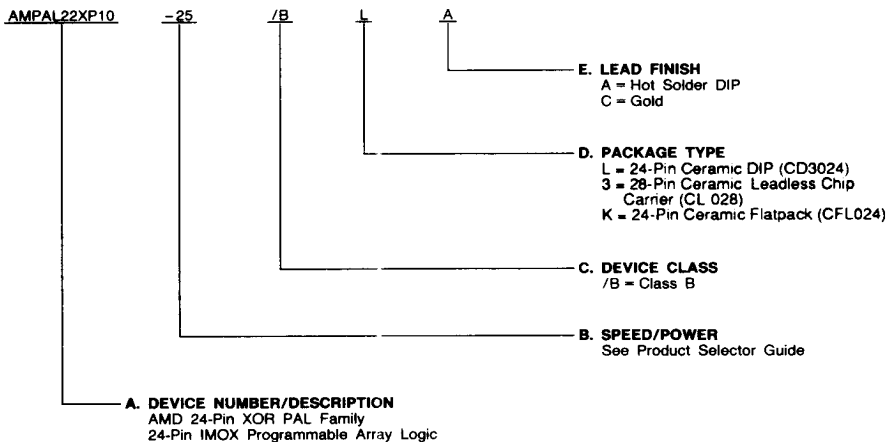
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Ordering Information (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Device Class**
- D. Package Type**
- E. Lead Finish**



| Valid Combinations | |
|-------------------------------|------------------------|
| AMPAL22XP10-25/-35/-35L/-45L | /BLA, /B3A, /BKA |
| AMPAL20XRP4-25/-35/-35L/-45L | |
| AMPAL20XRP6-25/-35/-35L/-45L | |
| AMPAL20XRP8-25/-35/-35L/-45L | |
| AMPAL20XRP10-25/-35/-35L/-45L | |

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, & 11

Functional Description

AMD 24-PIN XOR PAL20XRP10 Family Characteristics

All members of the AMD 24-Pin XOR PAL Family have common electrical characteristics and programming procedures. All parts are produced with a fusible link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit.

Initially the AND gates are connected, via fuses, to both the true and complement of each input. By selective programming of fuses the AND gates may be "connected" to only the true input (by blowing the complement fuse), to only the complement input (by blowing the true fuse), or to neither type of input (by blowing both fuses) establishing a logical "don't care." When both the true and complement fuses are left intact a logical false results on the output of the AND gate, while all fuses blown results in a logical true state. On the AmPAL22XP10 device, the AND gates are connected to fixed (2-6) OR-XOR structures whose outputs become device outputs. The remaining four (registered) devices function as follows: for combinatorial outputs, the AND gates are connected to fixed-OR gates whose outputs become device outputs. For registered outputs, the AND gates are connected to fixed (2-6) OR-XOR structures whose outputs become output register inputs.

All parts are fabricated with AMD's fast programming, highly reliable Platinum-Silicide Fuse technology. Utilizing an easily implemented programming algorithm, these products can be

rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields (> 98%), and provide extra test paths to achieve excellent parametric correlation.

Power-Up Reset

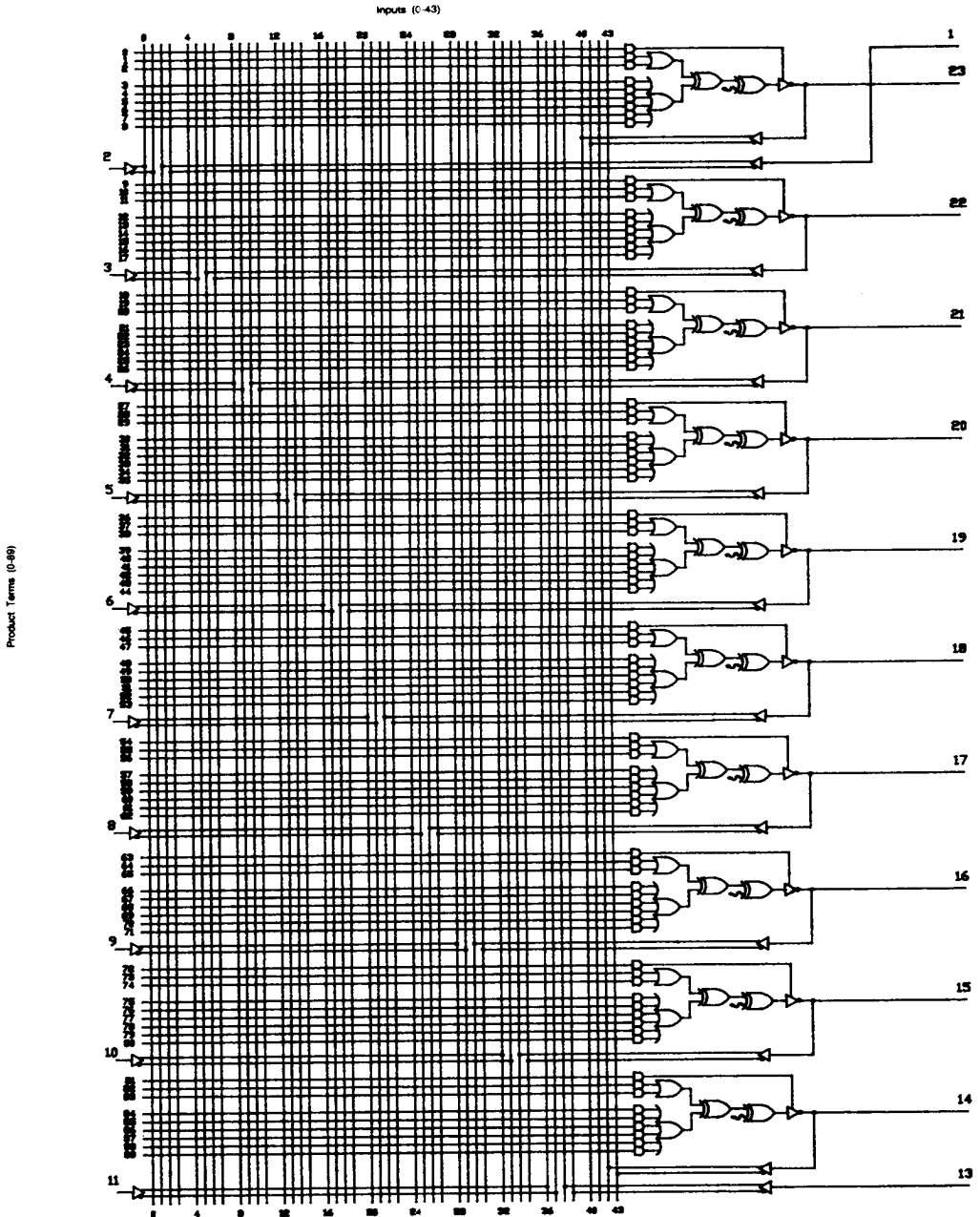
The registered devices in the AMD PAL family have been designed to reset during system power-up. Following power-up, all registers will be initialized to zero, setting all the outputs to a logic 1. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization.

PRELOAD

AMD PAL devices are designed with unique PRELOAD circuitry that provides an easy method of testing registered devices for logical functionality. PRELOAD allows any arbitrary state value to be loaded into the registered output of an AMD PAL device.

A typical functional test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the device inputs to any arbitrary "present input" value. Once this is done, the state machine is clocked into a new state or "next state." The next state is then checked to validate the transition from the present state. In this way any state transition can be checked.

24-Pin XOR AmPAL20XRP10 Family



Product Terms (0-48)

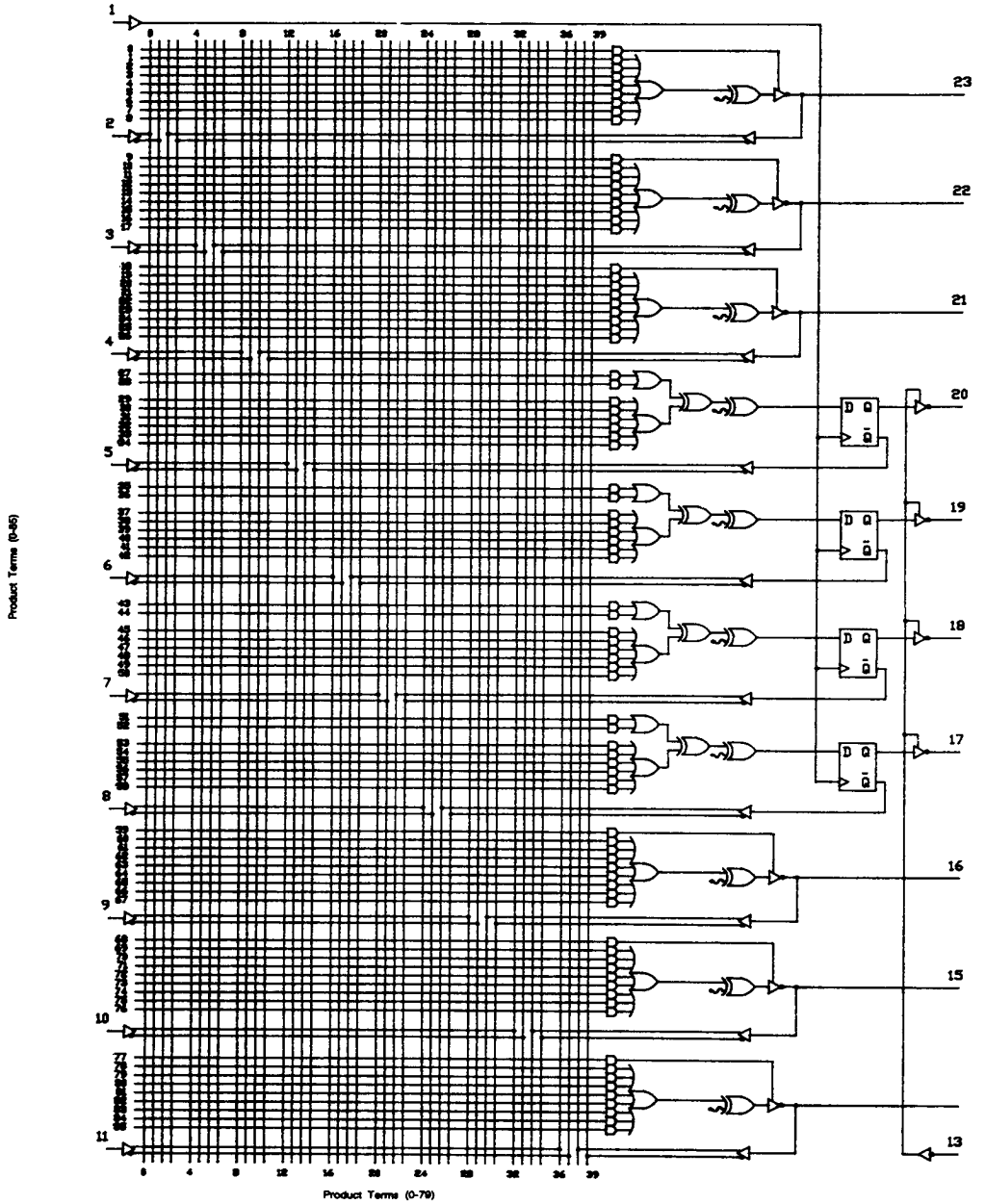
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Figure 1. AmPAL22XP10 Logic Diagram



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Figure 2. AmpAL20XRP4 Logic Diagram

24-Pin XOR AmPAL20XRP10 Family

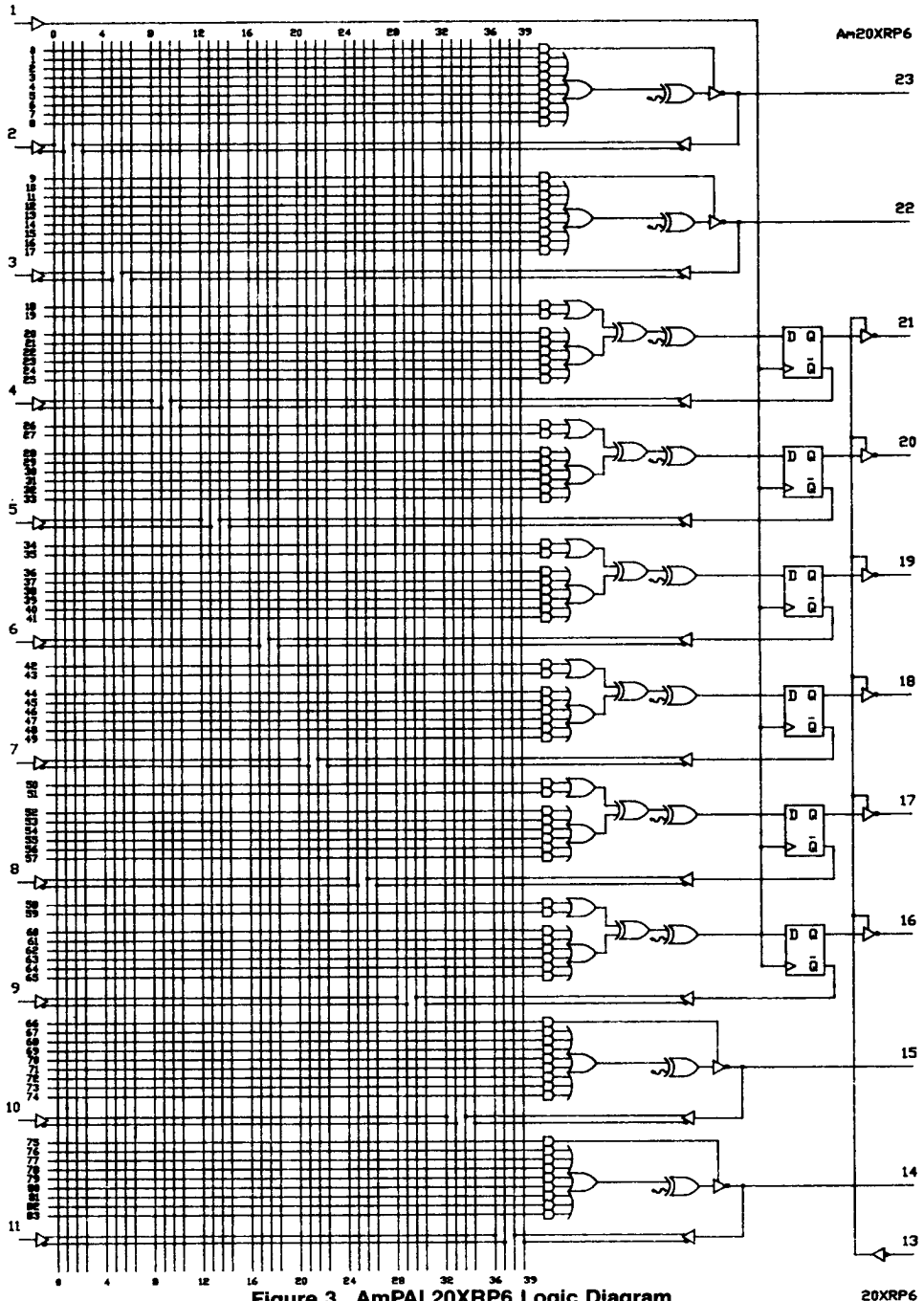
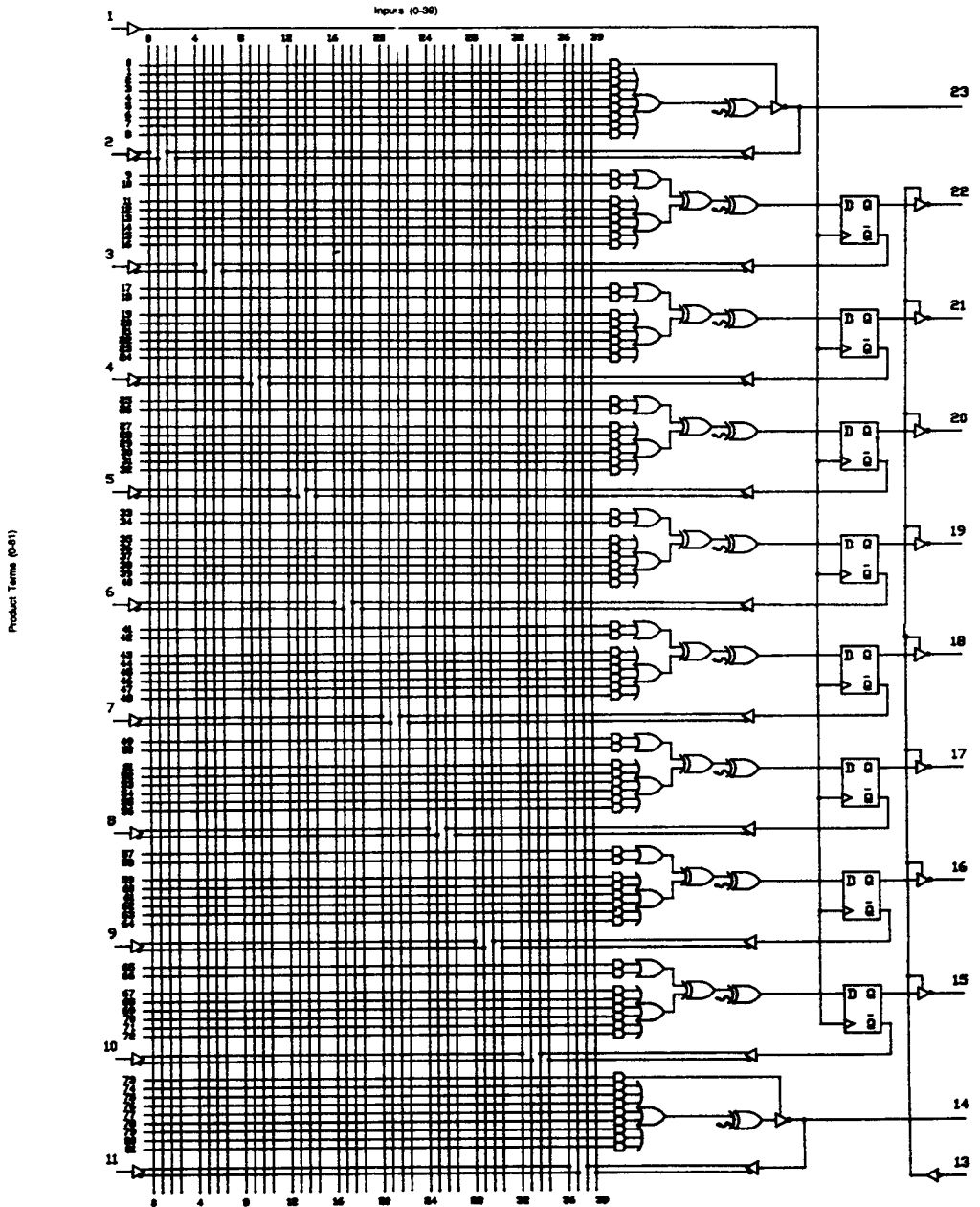


Figure 3. AmPAL20XRP6 Logic Diagram

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Figure 4. AmPAL20XRP8 Logic Diagram

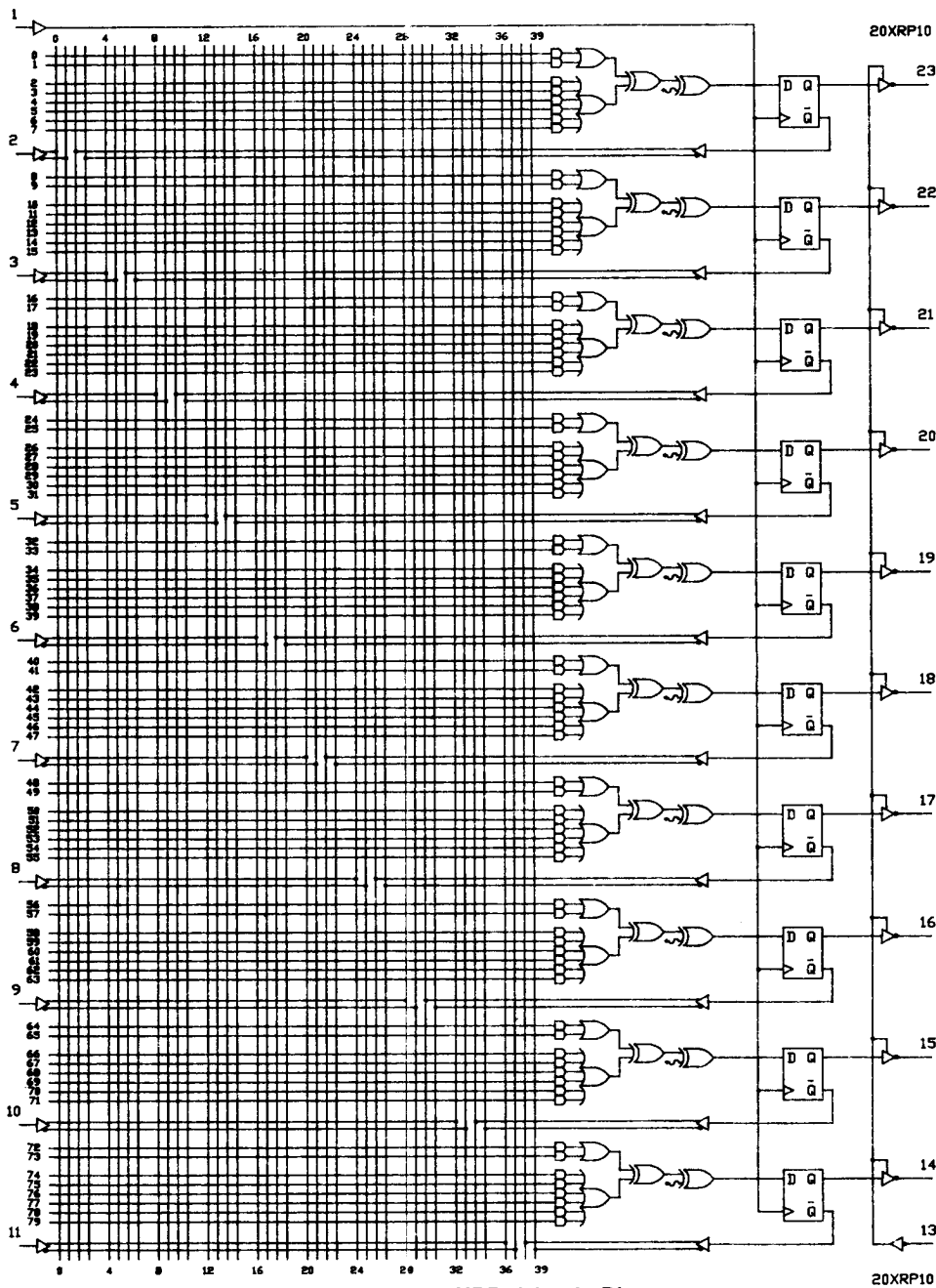


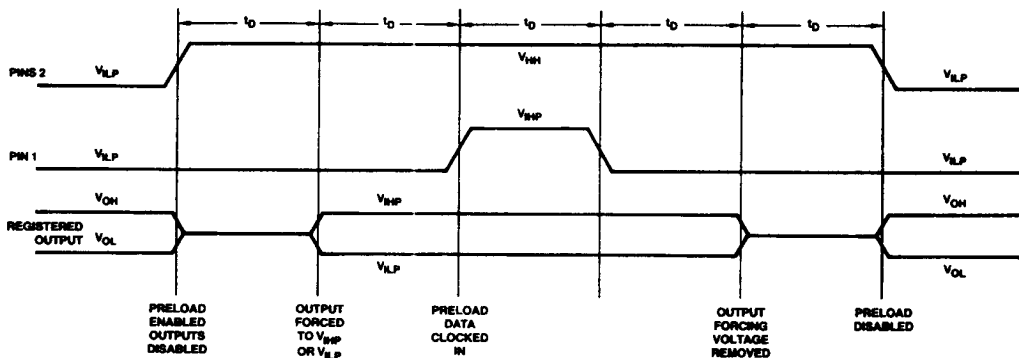
Figure 5. AmPAL20XRP10 Logic Diagram

PRELOAD of Registered Outputs

The AMD 24-pin XOR PAL devices incorporate circuitry to allow loading each register synchronously to either a HIGH or

LOW state. This feature simplifies testing since any initial state for the registers can be set to optimize test sequencing.

The pin levels and timing necessary to perform the PRELOAD function are detailed below:



| Par. | Min. | Max. |
|------------------|------|------|
| V _{HH} | 10 | 12 |
| V _{ILP} | 0 | 0.5 |
| V _{IHP} | 2.4 | 5.5 |

| Level forced on registered output pin during PRELOAD cycle | Register Q output state after cycle |
|--|-------------------------------------|
| V _{IHP} | HIGH |
| V _{ILP} | LOW |

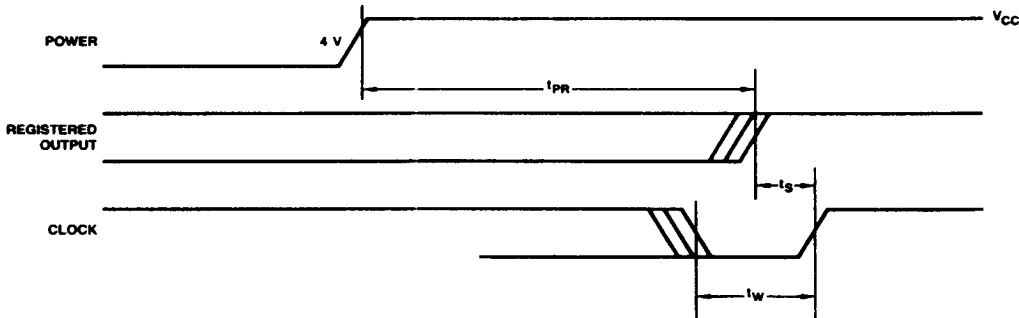
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Power-Up Reset

The registered devices in the AMD 24-Pin XOR PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will be HIGH. This feature provides flexibility to the designer and is especially valuable in simplifying state-machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation

of the power-up RESET and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up RESET. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.



WF022300

| Parameters | Description | Min. | Typ. | Max. | Units |
|-----------------|------------------------------|-------------------------------|------|------|-------|
| t _{PR} | Power-Up Reset Time | | 600 | 1000 | ns |
| t _s | Input or Feedback Setup Time | See Switching Characteristics | | | |
| t _w | Clock Width | | | | |

Absolute Maximum Ratings

Storage Temperature -65 to +150°C
 Supply Voltage to Ground Potential
 (Pin 24 to Pin 12) Continuous -0.5 to +7.0 V
 DC Voltage Applied to Outputs
 (Except During Programming) -0.5 V to +V_{CC} Max.
 DC Voltage Applied to Outputs
 During Programming 16 V
 Output Current Into Outputs During
 Programming (Max Duration of 1 sec) 200 mA
 DC Input Voltage -0.5 to +5.5 V
 DC Input Current -30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Ranges

Commercial (C) Devices
 Temperature (T_A) 0 to +75°C
 Supply Voltage (V_{CC}) +4.75 to +5.25 V
 Extended Commercial (E) Devices
 Temperature (T_A) -55°C Min.
 Temperature (T_C) +125°C Max.
 Supply Voltage (V_{CC}) +4.50 to +5.50 V
 Military (M) Devices*
 Temperature (T_A) -55°C Min.
 Temperature (T_C) +125°C Max.
 Supply Voltage (V_{CC}) +4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and -55°C.

DC Characteristics over operating range unless otherwise specified; included in Group A, Subgroup 1, 2, 3 tests unless otherwise noted

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. (Note 1) | Max. | Units | |
|--------------------------|---------------------------------|--|------------------------|---------------|------|-------|----|
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -3.2 mA COM'L I _{OH} = -2 mA MIL | 2.4 | 3.5 | | V | |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 24 mA COM'L I _{OL} = 12 mA MIL | | | 0.5 | V | |
| V _{IH} (Note 2) | Input HIGH Level | Guaranteed Input Logical HIGH Voltage for All Inputs | 2.0 | | 5.5 | V | |
| V _{IL} (Note 2) | Input LOW Level | Guaranteed Input Logical LOW Voltage for All Inputs | | | 0.8 | V | |
| I _{IL} | Input LOW Current | V _{CC} = Max., V _{IN} = 0.40 V | | -20 | -100 | μA | |
| I _{IH} | Input HIGH Current | V _{CC} = Max., V _{IN} = 2.7 V | | | 25 | μA | |
| I _I | Input HIGH Current | V _{CC} = Max., V _{IN} = 5.5 V | | | 1.0 | mA | |
| I _{SC} | Output Short-Circuit Current | V _{CC} = Max., V _{OUT} = 0.5 V (Note 3) | -30 | -60 | -90 | mA | |
| I _{CC} | Power Supply Current | V _{CC} = Max. | COM'L | | 210 | mA | |
| | | | MIL. | | | | |
| | | | -20 | -25 | | | |
| | | | -30 | -35 | | | |
| V _I | Input Clamp Voltage | V _{CC} = Min., I _{IN} = -18 mA | | | -0.9 | -1.2 | V |
| | | | | | | | |
| I _{OZH} | Output Leakage Current (Note 4) | V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} | V _O = 2.7 V | | | 100 | μA |
| I _{OZL} | | | V _O = 0.4 V | | | -100 | |

- Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
 2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
 3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
 V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
 4. I/O pin leakage is the worst case of I_{OZH} or I_{OZL} (where X = H or L).

Capacitance*

| Parameter Symbol | Parameter Description | Test Conditions | Typ. | Units |
|------------------|-----------------------|---|---------|-------|
| C _{IN} | Input Capacitance | V _{IN} = 2.0 V @ f = 1 MHz Pins 1, 13 Others | 11 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 2.0 V @ f = 1 MHz | 9 | |

*These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

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24-Pin XOR AmPAL20XRP10 Family

Switching Characteristics over operating range unless otherwise specified; included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted

Commercial Range

| No. | Parameter Symbol | Parameter Description | -20 Version | | | -30 & -30L Version | | | -40L Version | | | Units |
|-----|------------------|---|-------------|---------------|------|--------------------|---------------|------|--------------|---------------|------|-------|
| | | | Min. | Typ. (Note 1) | Max. | Min. | Typ. (Note 1) | Max. | Min. | Typ. (Note 1) | Max. | |
| 1 | t _{PD} | Input or Feedback to Non-Registered Output 22XP10, 20XRP4, 20XRP6, 20XRP8 | | | 20 | | | 30 | | | 40 | ns |
| 2 | t _{EA} | Input to Output Enable 22XP10, 20XRP4, 20XRP6, 20XRP8 | | | 20 | | | 30 | | | 40 | ns |
| 3 | t _{ER} | Input to Output Disable 22XP10, 20XRP4, 20XRP6, 20XRP8 | | | 20 | | | 30 | | | 40 | ns |
| 4 | t _{PZX} | Pin 13 to Output Enable 20XRP4, 20XRP6, 20XRP8, 20XRP10 | | | 15 | | | 20 | | | 35 | ns |
| 5 | t _{PXZ} | Pin 13 to Output Disable 20XRP4, 20XRP6, 20XRP8, 20XRP10 | | | 15 | | | 20 | | | 35 | ns |
| 6 | t _{CO} | Clock to Output 20XRP4, 20XRP6, 20XRP8, 20XRP10 | | | 13 | | | 15 | | | 30 | ns |
| 7 | t _S | Input or Feedback Setup Time 20XRP4, 20XRP6, 20XRP8, 20XRP10 | 20 | | | 30 | | | 40 | | | ns |
| 8 | t _H | Hold Time 20XRP4, 20XRP6, 20XRP8, 20XRP10 | 0 | | | 0 | | | 0 | | | ns |
| 9 | t _p | Clock Period (t _S + t _{CO}) | 33 | | | 45 | | | 70 | | | ns |
| 10 | t _w | Clock Width | 10 | | | 15 | | | 25 | | | ns |
| 11 | f _{MAX} | Maximum Frequency | | | 30.3 | | | 22.2 | | | 14.3 | MHz |

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.

2. t_{PD} is tested with switch S₁ closed and C_L = 50 pF.

3. For three-state outputs, output enable times are tested with C_L = 50 pF to the 1.5 V level; S₁ is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5 pF. HIGH to high impedance tests are made to an output voltage of V_{OH} - 0.5 V with S₁ open; LOW to high impedance tests are made to the V_{OL} + 0.5 V level with S₁ closed.

Military Range

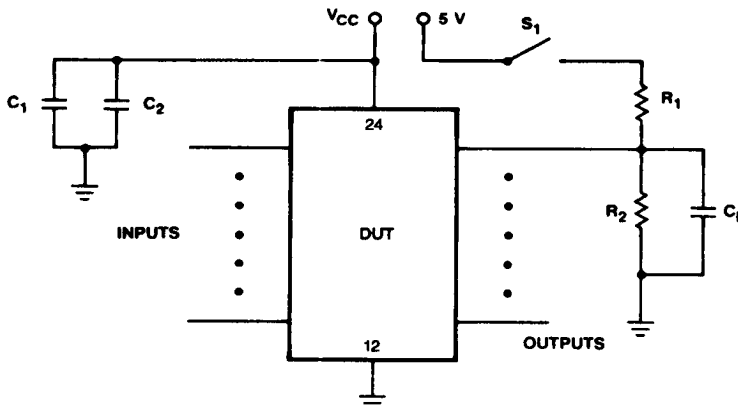
| No. | Parameter Symbol | Parameter Description | -25 Version | | | -35 & -35L Version | | | -45L Version | | | Units |
|-----|------------------|---|-------------|---------------|------|--------------------|---------------|------|--------------|---------------|------|-------|
| | | | Min. | Typ. (Note 1) | Max. | Min. | Typ. (Note 1) | Max. | Min. | Typ. (Note 1) | Max. | |
| 1 | t _{PD} | Input or Feedback to Non-Registered Output 22XP10, 20XRP4, 20XRP6, 20XRP8 | | | 25 | | | 35 | | | 45 | ns |
| 2 | t _{EA} | Input to Output Enable 22XP10, 20XRP4, 20XRP6, 20XRP8 | | | 25 | | | 35 | | | 45 | ns |
| 3 | t _{ER} | Input to Output Disable 22XP10, 20XRP4, 20XRP6, 20XRP8 | | | 25 | | | 35 | | | 45 | ns |
| 4 | t _{PZX} | Pin 13 to Output Enable 20XRP4, 20XRP6, 20XRP8, 20XRP10 | | | 20 | | | 25 | | | 40 | ns |
| 5 | t _{PXZ} | Pin 13 to Output Disable 20XRP4, 20XRP6, 20XRP8, 20XRP10 | | | 20 | | | 25 | | | 40 | ns |
| 6 | t _{CO} | Clock to Output 20XRP4, 20XRP6, 20XRP8, 20XRP10 | | | 15 | | | 25 | | | 35 | ns |
| 7 | t _S | Input or Feedback Setup Time 20XRP4, 20XRP6, 20XRP8, 20XRP10 | 25 | | | 35 | | | 45 | | | ns |
| 8 | t _H | Hold Time 20XRP4, 20XRP6, 20XRP8, 20XRP10 | 0 | | | 0 | | | 0 | | | ns |
| 9 | t _p | Clock Period (t _S + t _{CO}) | 40 | | | 60 | | | 80 | | | ns |
| 10 | t _w | Clock Width | 12 | | | 20 | | | 30 | | | ns |
| 11 | f _{MAX} | Maximum Frequency | | | 25 | | | 16.7 | | | 12.5 | MHz |

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.

2. t_{PD} is tested with switch S₁ closed and C_L = 50 pF.

3. For three-state outputs, output enable times are tested with C_L = 50 pF to the 1.5 V level; S₁ is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5 pF. HIGH to high impedance tests are made to an output voltage of V_{OH} - 0.5 V with S₁ open; LOW to high impedance tests are made to the V_{OL} + 0.5 V level with S₁ closed.

Switching Test Circuit

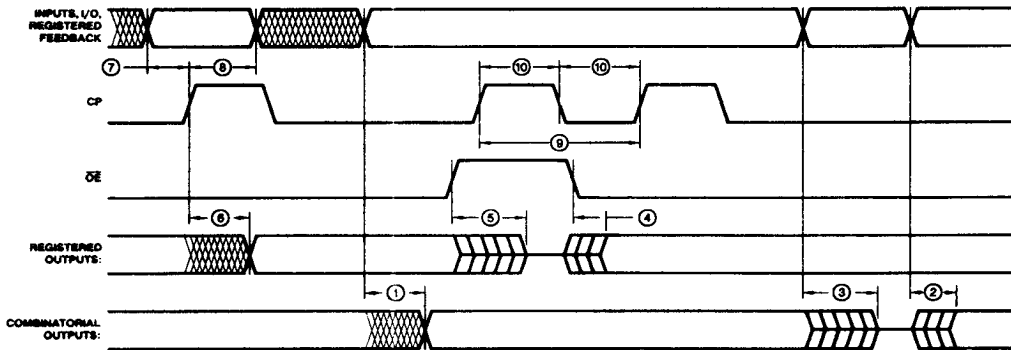


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Note: C₁ and C₂ are to bypass V_{CC} to ground.

| TEST OUTPUT LOADS | | |
|-------------------|------------|----------|
| Pin Name | Commercial | Military |
| R ₁ | 200 Ω | 390 Ω |
| R ₂ | 390 Ω | 750 Ω |
| C ₁ | 1 μF | 1 μF |
| C ₂ | 0.1 μF | 0.1 μF |
| C _L | 50 pF | 50 pF |

Switching Waveforms



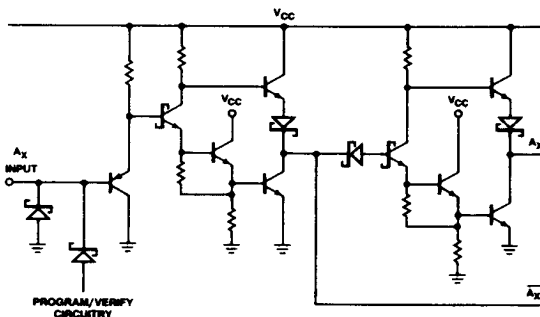
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Key to Timing Diagram

| WAVEFORM | INPUTS | OUTPUTS |
|----------|----------------------------------|---|
| | MUST BE STEADY | WILL BE STEADY |
| | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| | DON'T CARE: ANY CHANGE PERMITTED | CHANGING: STATE UNKNOWN |
| | DOES NOT APPLY | CENTER LINE IS HIGH IMPEDANCE "OFF" STATE |

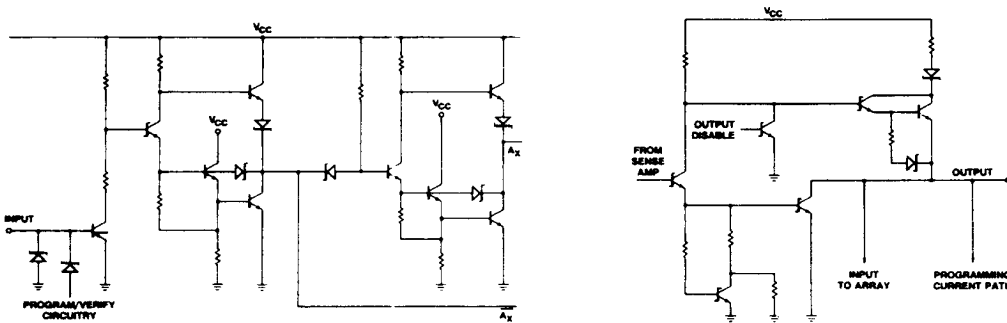
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Input Circuitry



IC000720

Output Circuitry



IC000801

Security Fuse Programming

A single fuse is provided on each device to prevent unauthorized copying of PAL fuse patterns. Once blown, the circuitry enabling fuse verification and registered output PRELOAD is permanently disabled.

Programming of the security fuse is the same as an array fuse. Verification of a blown security fuse is accomplished by verifying the whole fuse array as if every fuse is blown.

Programmers/Development Systems

(refer to Programmer Reference Guide, page 3-81)