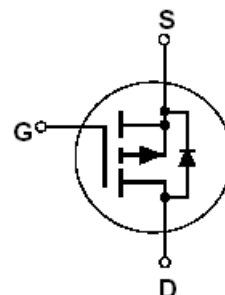
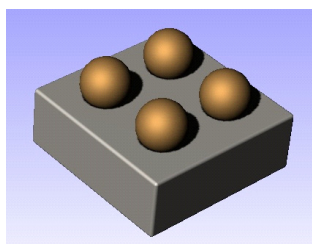


For information only

## TS8405P - Single P-Channel 1.8V Specified MicroSURF™

### General Description

Taiwan Semiconductor's new low cost, state of the art MicroSURF™ lateral MOSFET process technology in chipscale bondwireless packaging minimizes PCB space and  $R_{DS(ON)}$  plus provides an ultra-low  $Q_g \times R_{DS(ON)}$  figure of merit.

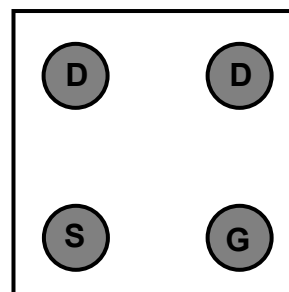


### Features

- -4.9A, -12V  $R_{DS(ON)} = 50m\Omega$  at -4.5 Volts
- -4.4A, -12V  $R_{DS(ON)} = 70m\Omega$  at -2.5 Volts
- -4.0A, -12V  $R_{DS(ON)} = 90m\Omega$  at -1.8 Volts
- Low profile package: less than 0.8mm height when mounted on PCB.
- Occupies only 2.25 mm<sup>2</sup> of PCB area. Less than 25% of the area of a SSOT-6.
- Excellent thermal characteristics.
- Lead free solder bumps available.

### MicroSURF™ for Load Switching and PA Switch

**Patent Pending**


**Bump Side View**

### Absolute Maximum Ratings

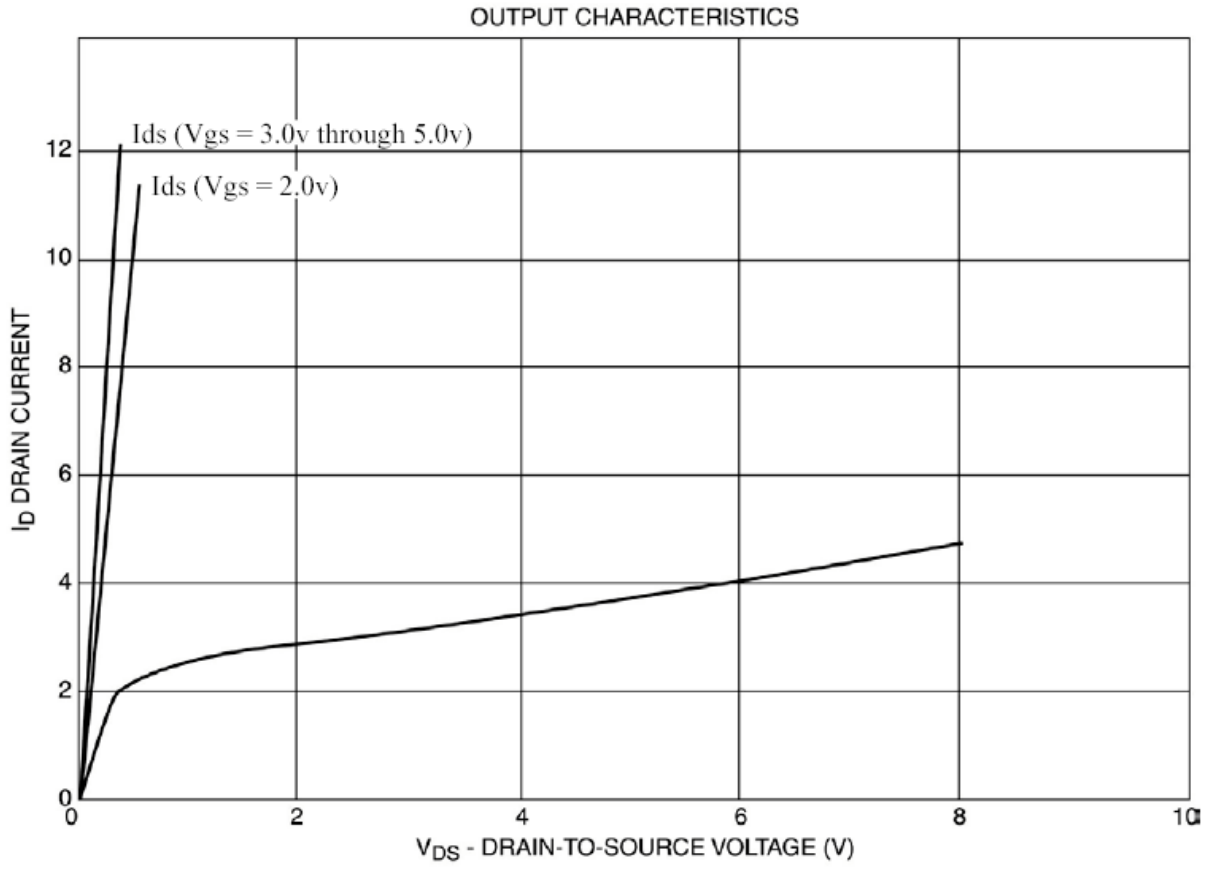
TA=25°C unless otherwise noted

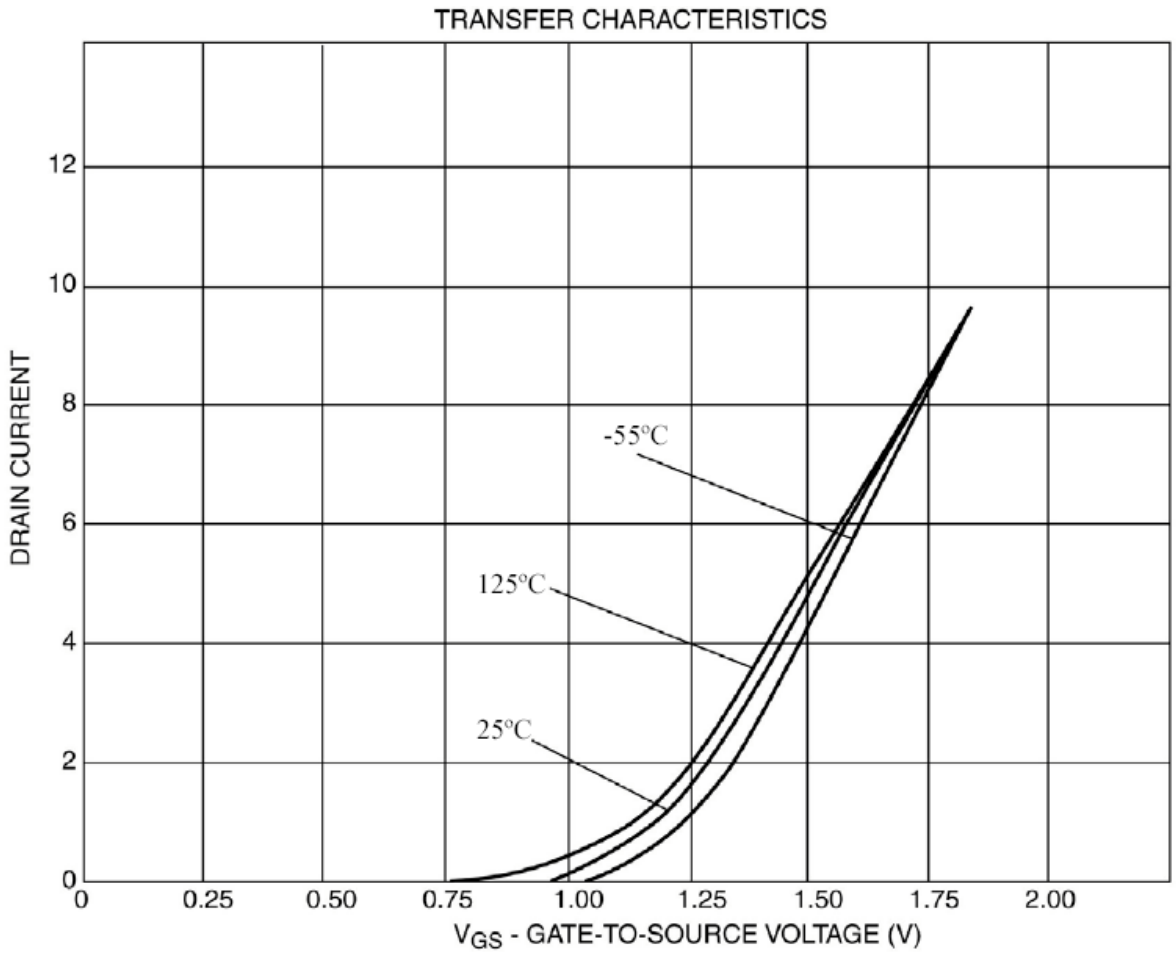
Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	-12	V
V <sub>GSS</sub>	Gate-Source Voltage	+8	V
I <sub>D</sub>	Drain Current	- Continuous	-4.9
		- Pulsed	-10
P <sub>D</sub>	Power Dissipation (Steady State)	1.5	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C
<b>Thermal Characteristics</b>			
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	85	°C/W
R <sub>θJR</sub>	Thermal Resistance, Junction-to-Balls	12	

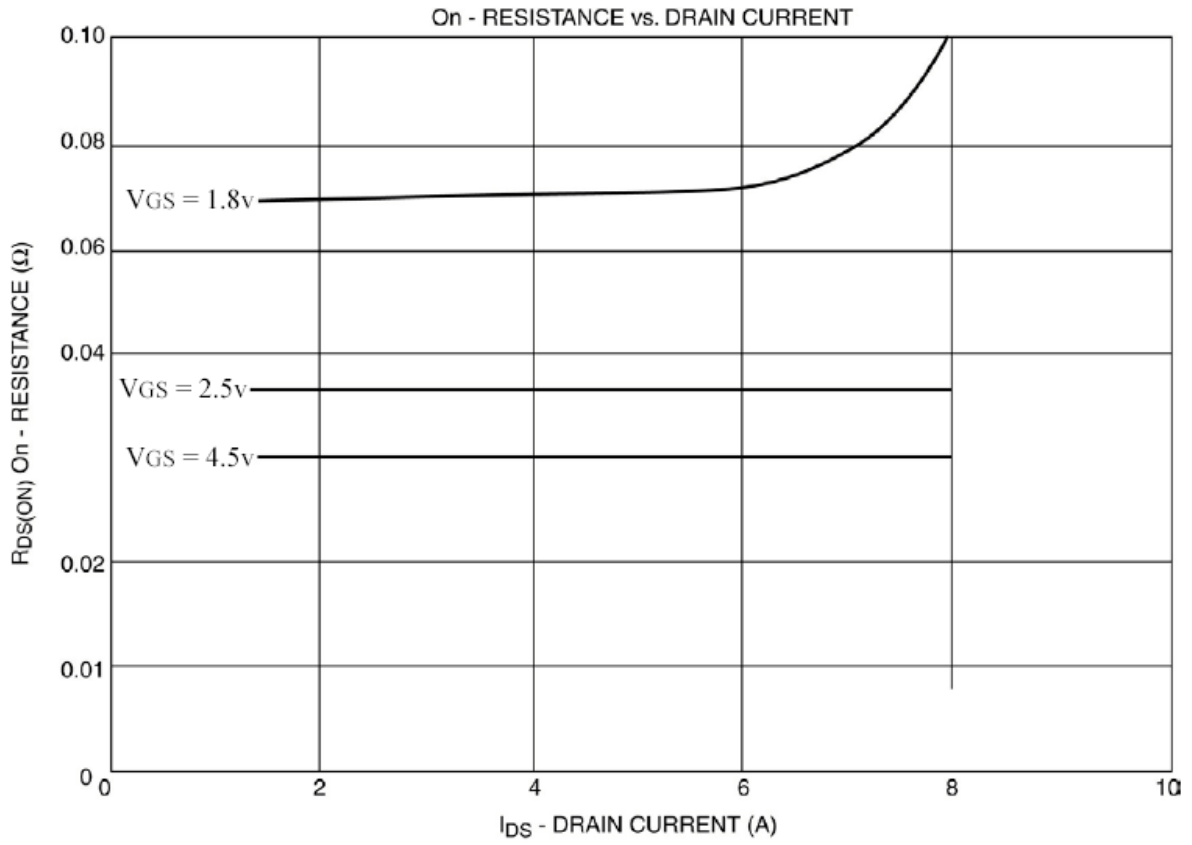
**Electrical Characteristics**
 $T_A=25^{\circ}\text{C}$  unless otherwise specified

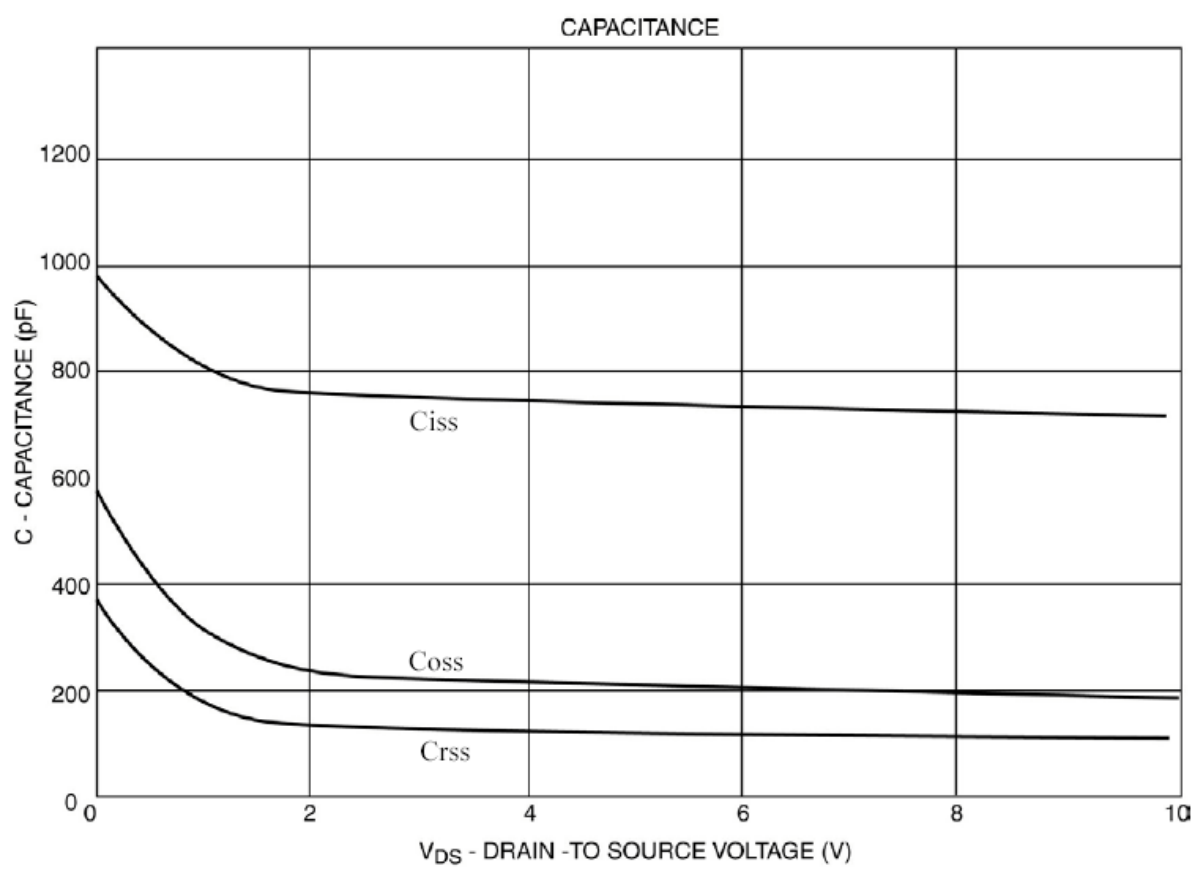
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-12\text{V}, V_{GS}=0\text{V}$			-1	$\mu\text{A}$
	Zero Gate Voltage Drain Current	$V_{DS}=-12\text{V}, V_{GS}=0\text{V}, T=70^{\circ}\text{C}$			-5	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS}=\pm 8\text{V}, V_{DS}=0\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$		-0.7		V
$r_{DS(on)}$	Drain-Source On-State Resistance	$V_{GS}=-4.5\text{V}, I_D=-1\text{A}$			50	m $\Omega$
	Drain-Source On-State Resistance	$V_{GS}=-2.5\text{V}, I_D=-1\text{A}$			70	m $\Omega$
	Drain-Source On-State Resistance	$V_{GS}=-1.8\text{V}, I_D=-1\text{A}$			90	m $\Omega$
$C_{iss}$	Input Capacitance	$V_{DS}=-12\text{V}, V_{GS}=0\text{V}, F=1\text{MHz}$		800		pF
$C_{oss}$	Output Capacitance	$V_{DS}=-12\text{V}, V_{GS}=0\text{V}, F=1\text{MHz}$		250		pF
$C_{riss}$	Reverse Transfer Capacitance	$V_{DS}=-12\text{V}, V_{GS}=0\text{V}, F=1\text{MHz}$		100		pF
$Q_g$	Total Gate Charge	$V_{GS}=-4.5\text{V}, I_D=-1\text{A}, V_{DS}=-6\text{V}$		9.0		nC
$V_{SD}$	Diode Forward Voltage	$I_S=-1\text{A}, V_{GS}=0\text{V}$		-0.71		V
$t_{tr}$	Source-Drain Reverse Recovery Time	$I_S=-1\text{A}, V_{GS}=0\text{V}, di/dt=100\text{A}/\mu\text{s}$		40		ns

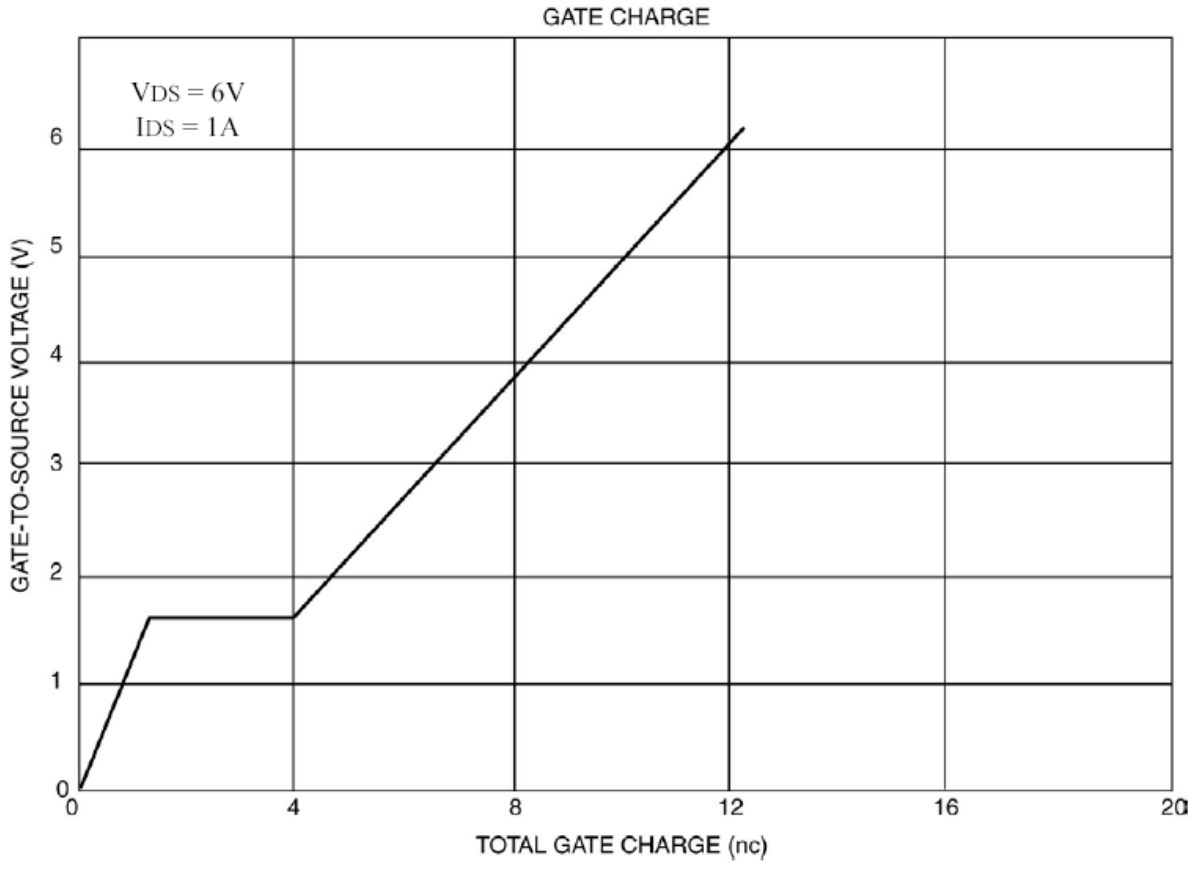
**TS8405P**

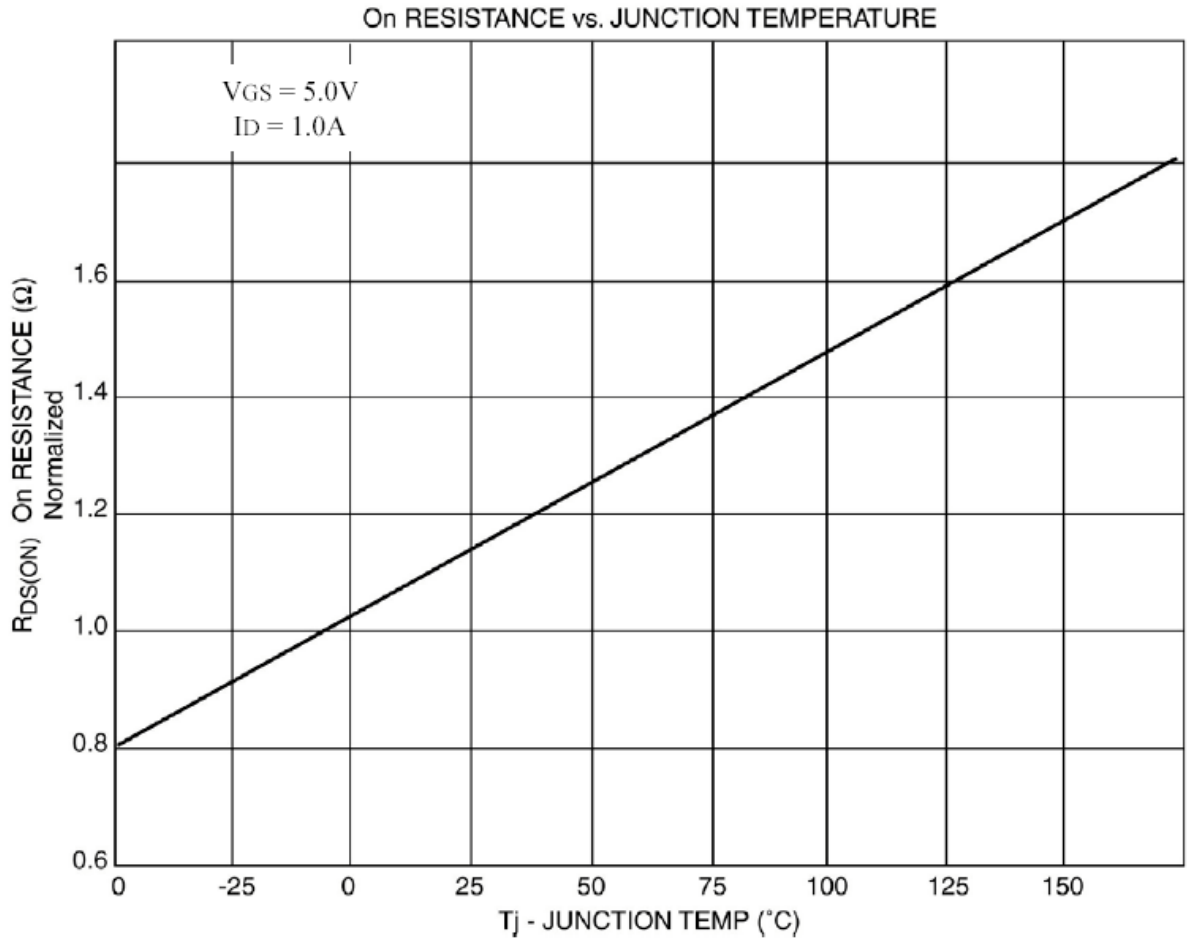


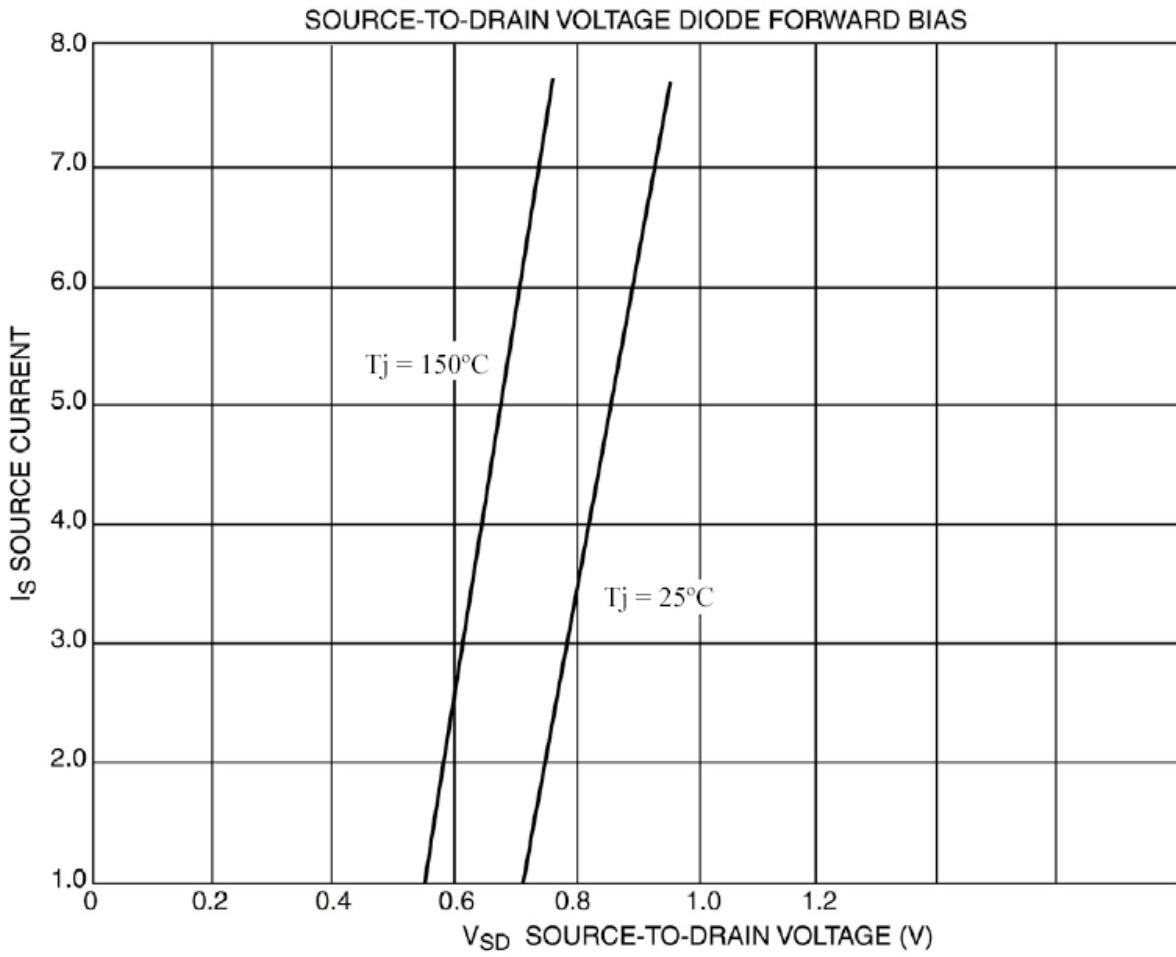


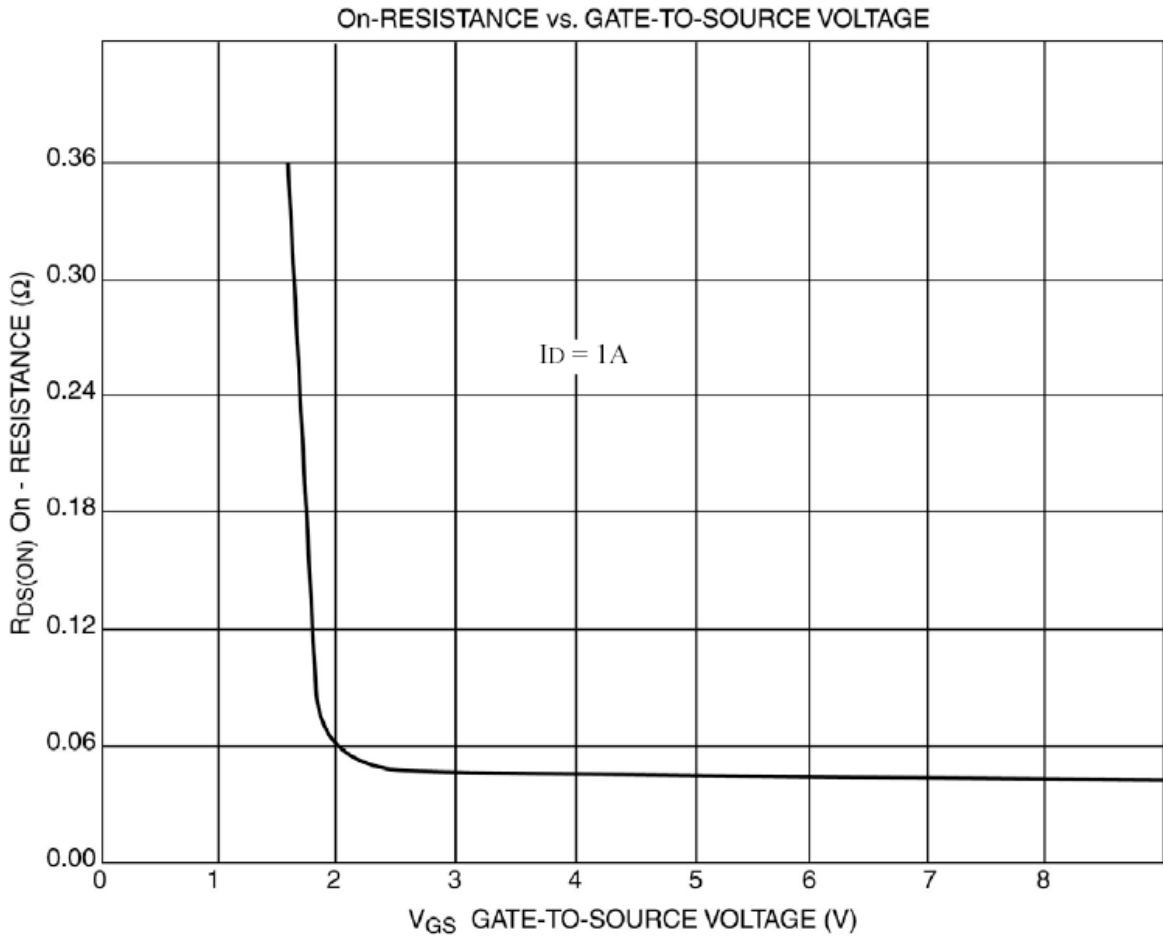


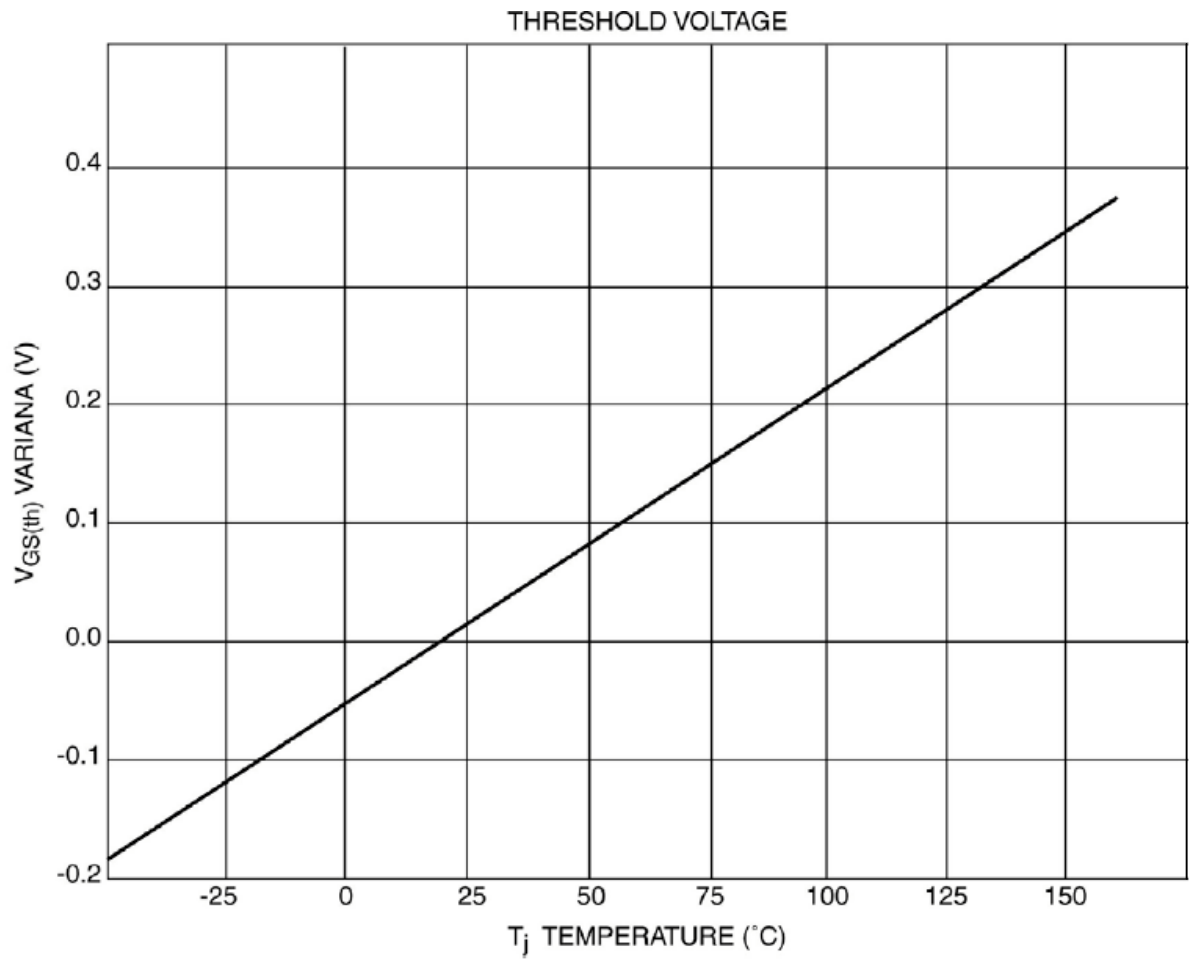






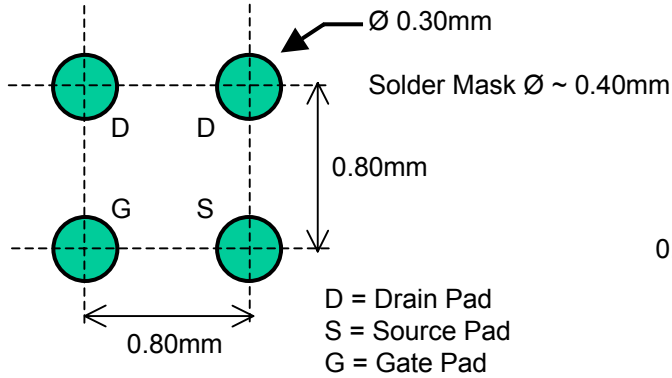




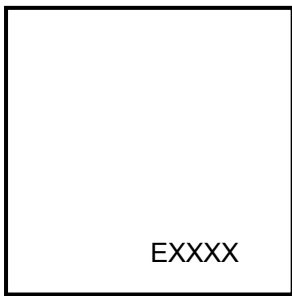
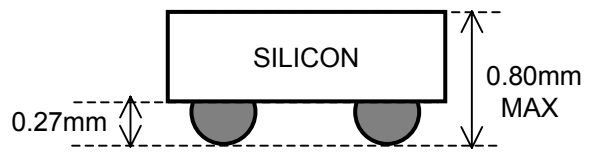




### Dimensional Outline and Pad Layout



LAND PATTERN RECOMMENDATION



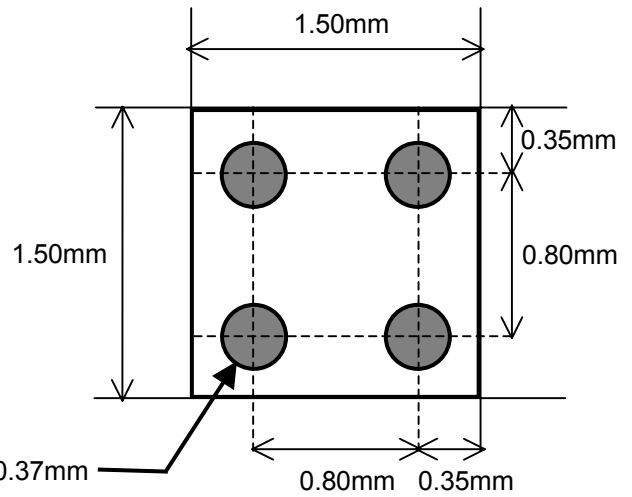
BACKSIDE VIEW (NO BUMP SIDE VIEW)

Mark on backside of die

E = 8405P Product Code

XXXX = Lot Traceability Code

Mark is located in lower right quadrant on top of Source pad. Gate pad is located in lower left quadrant.



Bumps are Eutectic solder 63/37 Sn/Pb