

NIMD6302R2

Product Preview

SMARTDISCRETES™

5 Amps, 30 Volts

Self Protected with Current Sense

N-Channel SO-8, Dual

SMARTDISCRETES devices are an advanced series of Power MOSFETs which utilize ON Semiconductor's latest MOSFET technology process to achieve the lowest possible on-resistance per silicon area while incorporating smart features. They are capable of withstanding high energy in the avalanche and commutation modes. The avalanche energy is specified to eliminate guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

This new SMARTDISCRETES device features an integrated Gate-to-Source clamp for ESD protection. Also, this device features a sense FET for current monitoring.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Current Sense FET
- ESD Protected, Main FET and SENSEFET

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

MAIN MOSFET MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	30	Vdc
Drain-to-Gate Voltage ($R_{GS} = 1.0\ \text{M}\Omega$)	V_{DGR}	30	Vdc
Gate-to-Source Voltage	V_{GS}	± 16	Vdc
Single Pulse Drain-to-Source Avalanche Energy (Note 1.) ($V_{DD} = 25\ \text{Vdc}$, $V_{GS} = 10\ \text{Vdc}$, $V_{DS} = 20\ \text{Vdc}$, $I_L = 15\ \text{Apk}$, $L = 10\ \text{mH}$, $R_G = 25\ \Omega$)	EAS	250	mJ
Drain Current			
– Continuous @ $T_A = 25^\circ\text{C}$	I_D	6.5	Adc
– Continuous @ $T_A = 100^\circ\text{C}$ (Note 1.)	I_D	4.4	Adc
– Single Pulse ($t_p \leq 10\ \mu\text{s}$)	I_{DM}	33	Apk
Maximum Power Dissipation ($T_A = 25^\circ\text{C}$)	P_D	TBD	W

1. Switching characteristics are independent of operating junction temperatures

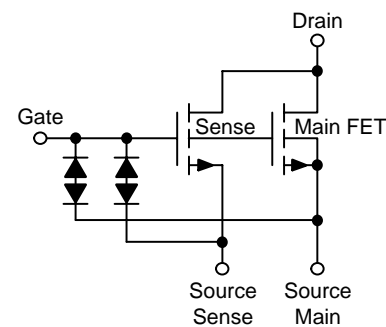
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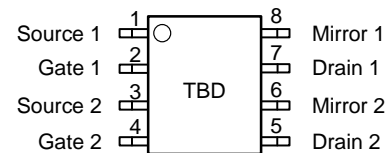
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5.0 AMPERES
30 VOLTS
 $R_{DS(on)} = 50\ \text{m}\Omega$



SOIC-8
CASE 751
STYLE 19

MARKING DIAGRAM



(Top View)

TBD = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NIMD6302R2	SOIC-8	TBD

NIMD6302R2

MAIN MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	30 –	35 30	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 30 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 30 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	– –	– –	10 100	μAdc
Gate-Body Leakage Current (V _{GS} = 12 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	22	32	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 –	– 5.0	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 2.) (V _{GS} = 10 Vdc, I _D = 3.0 Adc, T _J @ 25°C) (V _{GS} = 10 Vdc, I _D = 3.0 Adc, T _J @ 125°C)	R _{DS(on)}	– –	– –	50 TBD	mΩ
Forward Transconductance (Note 2.) (V _{DS} = 6.0 Vdc, I _D = 15 Adc) (V _{DS} = 15 Vdc, I _D = 15 Adc)	g _{FS}	– –	7.4 5.5	– –	mhos

DYNAMIC CHARACTERISTICS (Note 3.)

Input Capacitance	(V _{DS} = 6.0 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	–	380	600	pF
Output Capacitance		C _{oss}	–	272	350	
Transfer Capacitance		C _{rss}	–	93	200	

SWITCHING CHARACTERISTICS (Note 3.)

Turn-On Delay Time	(V _{DD} = 6.0 Vdc, I _D = 3.0 Adc, V _{GS} = 10 Vdc, R _G = 4.7 Ω)	t _{d(on)}	–	8.4	–	ns
Rise Time		t _r	–	24	–	
Turn-Off Delay Time		t _{d(off)}	–	18	–	
Fall Time		t _f	–	5.0	–	
Gate Charge	(V _{DS} = 6.0 Vdc, I _D = 3.0 Adc, V _{GS} = 10 Vdc)	Q _T	–	11.3	–	nC
		Q ₁	–	2.8	–	
		Q ₂	–	1.9	–	
		Q ₃	–	2.2	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage (Note 2.)	(I _S = 3.0 Adc, V _{GS} = 0 Vdc)	V _{SD}	–	0.76	–	Vdc
Forward On-Voltage (Notes 2., 3.)	(I _S = 3.0 Adc, V _{GS} = 0 Vdc, T _J = 125°C)		–	0.62	–	
Reverse Recovery Time (Note 3.)	(I _S = 3.0 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs)	t _{rr}	–	24.7	–	ns
		t _a	–	13	–	
		t _b	–	12	–	
Reverse Recovery Stored Charge (Note 3.)		Q _R	–	0.018	–	μC

MIRROR MOSFET CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Main/Mirror MOSFET Current Ratio	(V _{DS} = 6.0 Vdc, I _{Dmain} = 25 mA) (V _{DS} = 6.0 Vdc, I _{Dmain} = 25 mA, T _A = 125°C)	I _{RAT}	192 192	200 200	208 208	–
Main/Mirror Current Ratio Variation versus Current and Temperature	(V _{DS} = 6.0 Vdc, I _{Dmain} = 25 mA, T _A = 25 to 125°C)	I _{ΔRAT}	–7.5	±3.0	+7.5	%
Gate-Body Leakage Current	V _{DS} = 0 Vdc, V _{GS} = 3.0 Vdc	I _{GSS}	–	–	100	nAdc

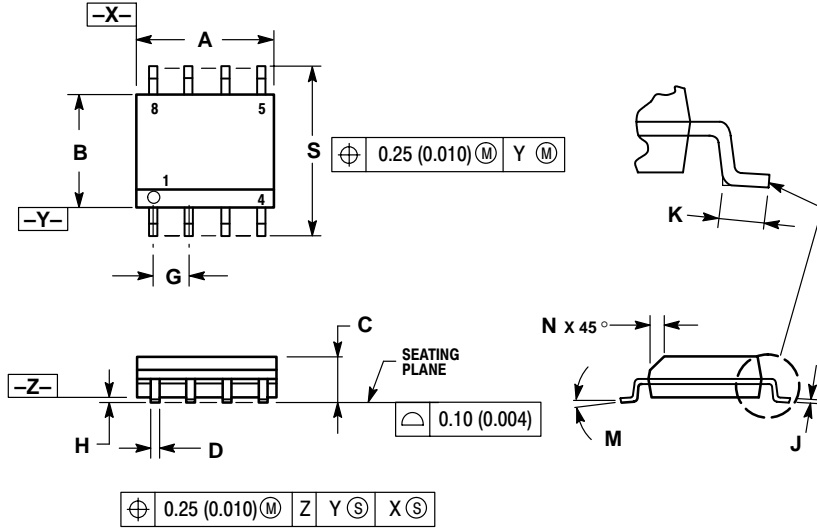
2. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

3. Switching characteristics are independent of operating junction temperatures.

NIMD6302R2

PACKAGE DIMENSIONS

SO-8
CASE 751-07
ISSUE W



NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 19:

- PIN 1: SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1

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Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

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