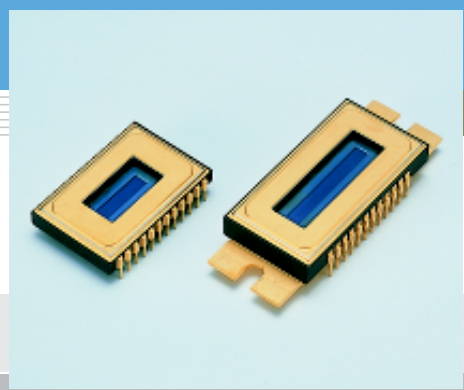


# CCD area image sensor S7033/S7034 series

## Back-thinned FFT-CCD



S7033/S7034 series are families of FFT-CCD image sensors specifically designed for low-light-level detection in scientific applications. S7033/S7034 series feature large full-well capacity in horizontal CCD register. By using the binning operation, S7033/S7034 series can be used as a linear image sensor having a long height. This makes S7033/S7034 series ideally suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit.

S7033/S7034 series have an effective pixel size of  $24 \times 24 \mu\text{m}$  and are available in image areas ranging from  $12.288 \text{ (H)} \times 2.928 \text{ (V)} \text{ mm}^2$  (S7033-0907, S7034-0907S) up to a large image area of  $24.576 \text{ (H)} \times 2.928 \text{ (V)} \text{ mm}^2$  (S7033-1007, S7034-1007S).

Either one-stage or two-stage thermoelectric cooler is built into the package (S7034/S7035 series). At room temperature operation, the device can be cooled down to  $-10 \text{ }^\circ\text{C}$  by one-stage cooler and  $-30 \text{ }^\circ\text{C}$  by two-stage cooler respectively without using any other cooling technique. In addition since both the CCD chip and the thermoelectric cooler are hermetically sealed, no dry air is required, thus allowing easy handling.

### Features

- Line, pixel binning
- Greater than 90 % quantum efficiency at peak sensitivity wavelength
- Wide spectral range
- Wide dynamic range
- MPP operation
- Built-in thermoelectric cooler

### Applications

- Fluorescence spectrometer, ICP
- Industrial inspection requiring
- Semiconductor inspection
- DNA sequencer
- Low-light-level detection

### ■ Selection guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm (V)]	Suitable multichannel detector head
S7033-0907	Non-cooled	$532 \times 128$	$512 \times 122$	$12.288 \times 2.928$	C7043
S7033-1007		$1044 \times 128$	$1024 \times 122$	$24.576 \times 2.928$	
S7034-0907S	One-stage TE-cooled	$532 \times 128$	$512 \times 122$	$12.288 \times 2.928$	C7044
S7034-1007S		$1044 \times 128$	$1024 \times 122$	$24.576 \times 2.928$	

Note) Two-stage TE-cooled type (S7035 series) is also available

### ■ General ratings

Parameter	S7033 series	S7034 series
Pixel size	$24 \text{ (H)} \times 24 \text{ (V)} \mu\text{m}$	
Vertical clock phase	2 phase	
Horizontal clock phase	2 phase	
Output circuit	One-stage MOSFET source follower	
Package	24 pin ceramic DIP (refer to dimensional outlines)	
Built-in cooler	-	One-stage
Window *1	Quartz glass	Sapphire

\*1: Window-less is available upon request.

## CCD area image sensor S7033/S7034 series

### ■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+30	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	VOD	-0.5	-	+25	V
RD voltage	VRD	-0.5	-	+18	V
ISV voltage	VISV	-0.5	-	+18	V
ISH voltage	VISH	-0.5	-	+18	V
IGV voltage	VIG1V, VIG2V	-10	-	+15	V
IGH voltage	VIG1H, VIG2H	-10	-	+15	V
SG voltage	VSG	-10	-	+15	V
OG voltage	VOG	-10	-	+15	V
RG voltage	VRG	-10	-	+15	V
TG voltage	VTG	-10	-	+15	V
Vertical clock voltage	VP1V, VP2V	-10	-	+15	V
Horizontal clock voltage	VP1H, VP2H	-10	-	+15	V

### ■ Operating conditions (MPP mode, Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Output transistor drain voltage	VOD	18	20	22	V	
Reset drain voltage	VRD	11.5	12	12.5	V	
Output gate voltage	VOG	1	3	5	V	
Substrate voltage	VSS	-	0	-	V	
Test point (vertical input source)	VISV	-	VRD	-	V	
Test point (horizontal input source)	VISH	-	VRD	-	V	
Test point (vertical input gate)	VIG1V, VIG2V	-8	0	-	V	
Test point (horizontal input gate)	VIG1H, VIG2H	-8	0	-	V	
Vertical shift register clock voltage	High	VP1VH, VP2VH	4	6	8	V
	Low	VP1VL, VP2VL	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	4	6	8	V
	Low	VP1HL, VP2HL	-9	-8	-7	
Summing gate voltage	High	VSGH	4	6	8	V
	Low	VSGL	-9	-8	-7	
Reset gate voltage	High	VRGH	4	6	8	V
	Low	VRGL	-9	-8	-7	
Transfer gate voltage	High	VTGH	4	6	8	V
	Low	VTGL	-9	-8	-7	

### ■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	1	MHz
Charge transfer efficiency *2	CTE	0.99995	0.99999	-	-
DC output level *3	Vout	12	15	18	V
Output impedance *3	Zo	-	3	-	kΩ
Power consumption *3 *4	P	-	15	-	mW

\*2: Charge transfer efficiency per pixel, measured at half of the full well capacity.

\*3: The values depend on the load resistance. (Typical, VOD=20 V, Load resistance=22 kΩ)

\*4: Power consumption of the on-chip amplifier.

### ■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage	Vsat	-	Fw × Sv	-	V
Full well capacity	Vertical	150,000	300,000	-	e <sup>-</sup>
	Horizontal	1,350,000	2,700,000	-	
CCD node sensitivity	Sv	0.5	0.6	-	μV/e <sup>-</sup>
Dark current *5 (MPP mode)	25 °C	-	4,000	12,000	e <sup>-</sup> /pixel/s
	0 °C	-	200	600	
Readout noise *6	Nr	-	30	-	e <sup>-</sup> rms
Dynamic range *7	Line binning	22,500	90,000	-	-
	Area scanning	2,500	10,000	-	
Photo response non-uniformity *8	PRNU	-	±3	±10	%
Spectral response range	λ	-	200 to 1100	-	nm

\*5: Dark current nearly doubles for every 5 to 7 °C increase in temperature.

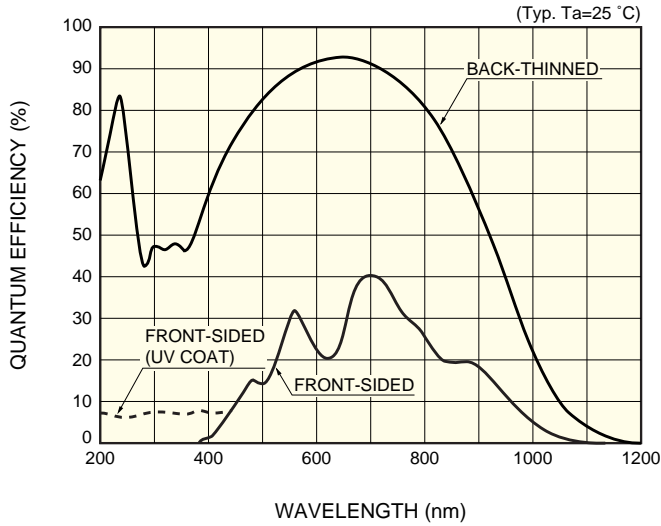
\*6: Operating frequency is 150 kHz.

\*7: Dynamic range (DR)=Full well/Readout noise.

\*8: Measured at the half of the full well capacity output.

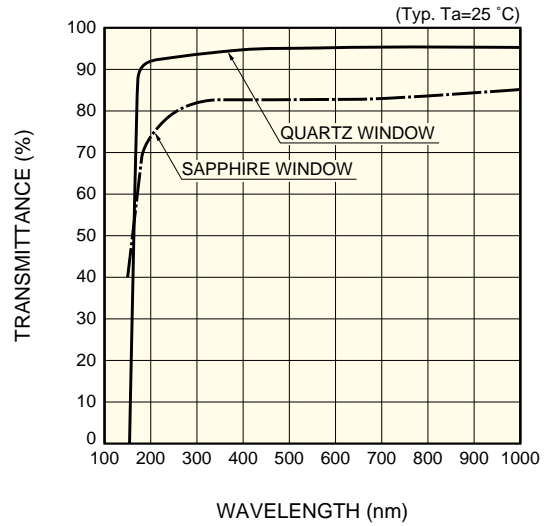
$$\text{Photo response non-uniformity (PRNU) [\%]} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

## ■ Spectral response (without window) <sup>\*9</sup>



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## ■ Spectral transmittance characteristics of window material



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\*9: Spectral response with quartz glass or sapphire are decreased by the transmittance.

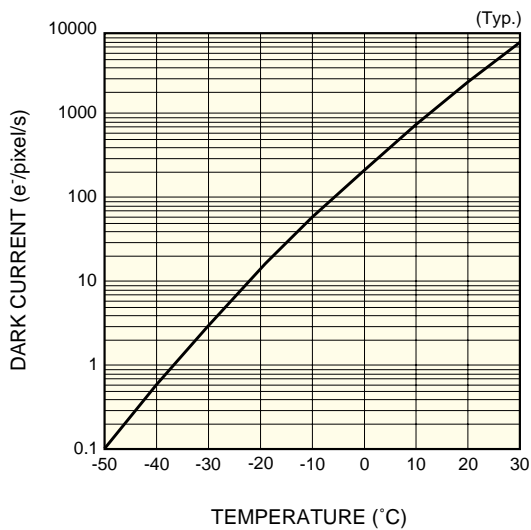
## ● Window material

Type No.	Window material
S7033 series	Quartz glass <sup>*10</sup> (option: window-less.)
S7034 series	Sapphire <sup>*11</sup> (option: window-less)
S7035 series (two-stage TE-cooled type)	Sapphire <sup>*11</sup> (option: window-less)

\*10: Resin sealing

\*11: Hermetic sealing

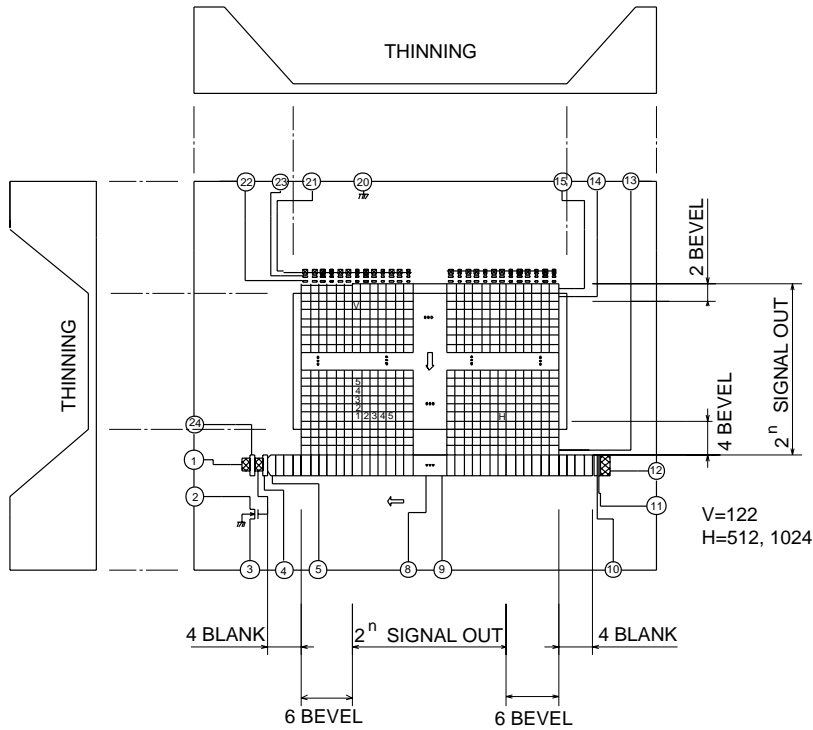
## ■ Dark current vs. temperature



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# CCD area image sensor S7033/S7034 series

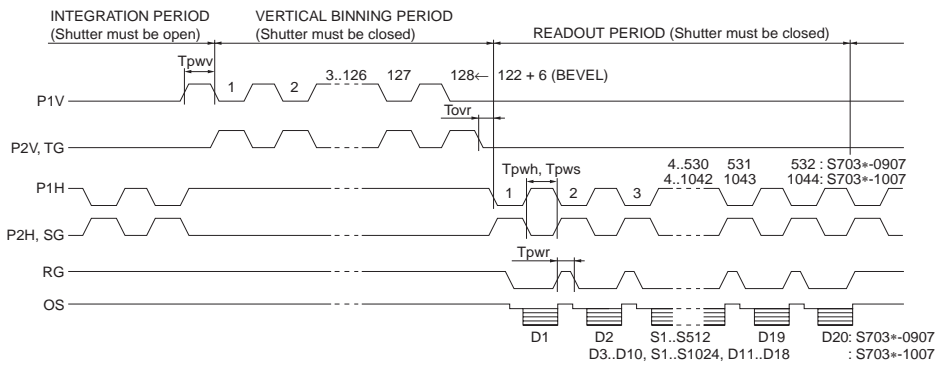
## ■ Device structure (Conceptual drawing of top view)



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## ■ Timing chart

### Line binning



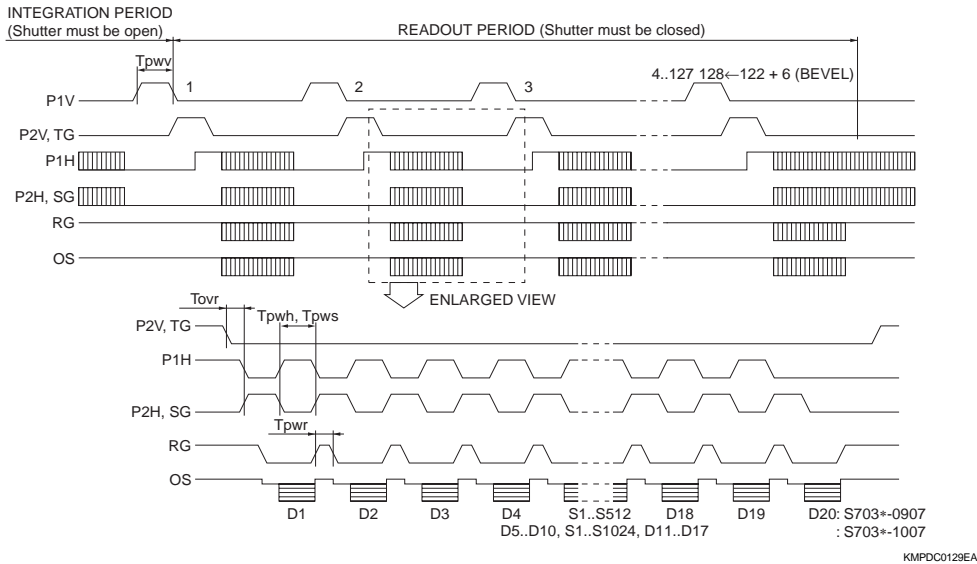
KMPDC0128EA

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpww	*12	6 *13	-	-	μs
	Rise and fall time	Tprv, Tprf		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*12	500	-	-	ns
	Rise and fall time	Tprh, Tprf		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	-	-	ns
	Rise and fall time	Tprs, Tprf		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	-	-	ns
	Rise and fall time	Tpr, Tprf		5	-	-	ns
TG - P1H	Overlap time	Tovr	-	3	-	-	μs

\*12: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

\*13: In case of S7033-1007, S7034-1007S

## Area scanning 1: low dark current mode

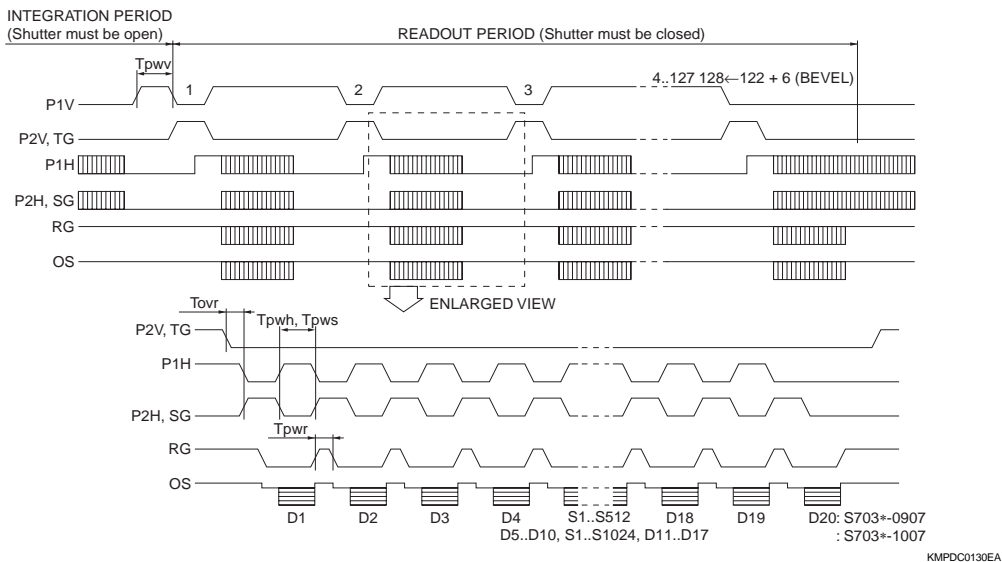


Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	$T_{pww}$	*14	6 <sup>*15</sup>	-	-	$\mu$ s
	Rise and fall time	$T_{prv}$ , $T_{pfv}$		200	-	-	ns
P1H, P2H	Pulse width	$T_{pwh}$	*14	500	-	-	ns
	Rise and fall time	$T_{prh}$ , $p_{fh}$		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	$T_{pws}$	-	500	-	-	ns
	Rise and fall time	$T_{prs}$ , $T_{pfs}$	-	10	-	-	ns
	Duty ratio	-	-	-	50	-	%
RG	Pulse width	$T_{pwr}$	-	100	-	-	ns
	Rise and fall time	$T_{prr}$ , $T_{pfr}$	-	5	-	-	ns
TG - P1H	Overlap time	$T_{ovr}$	-	3	-	-	$\mu$ s

\*14: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

\*15: In case of S7033-1007, S7034-1007S

## Area scanning 2: large full well mode



# CCD area image sensor S7033/S7034 series

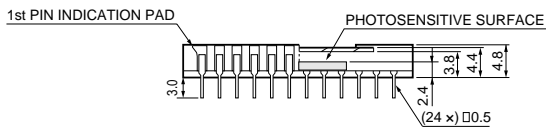
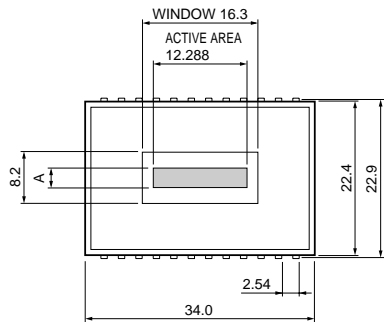
Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit	
P1V, P2V, TG	Pulse width	Tpww	*16	6 *17	-	-	μs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*16	500	-	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	-	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	-	-	ns
	Rise and fall time	Tpr, Tpr		5	-	-	ns
TG - P1H	Overlap time	Tovr	-	3	-	μs	

\*16: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

\*17: In case of S7033-1007, S7034-1007S

## ■ Dimensional outlines (unit: mm)

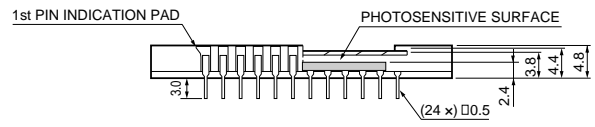
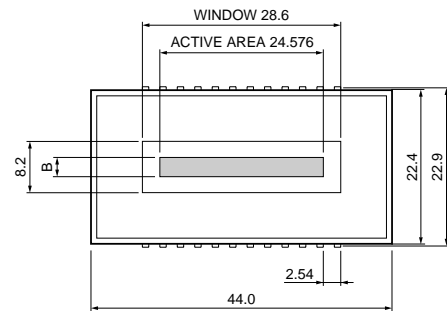
### S7033-0907



S7033-0907: A=2.928

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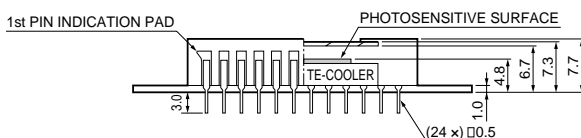
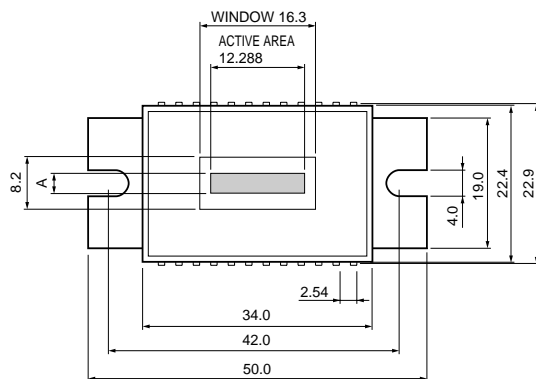
### S7033-1007



S7033-1007: B=2.928

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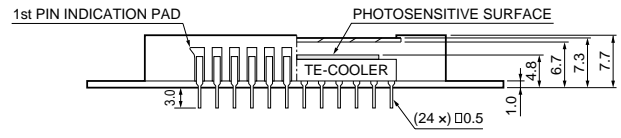
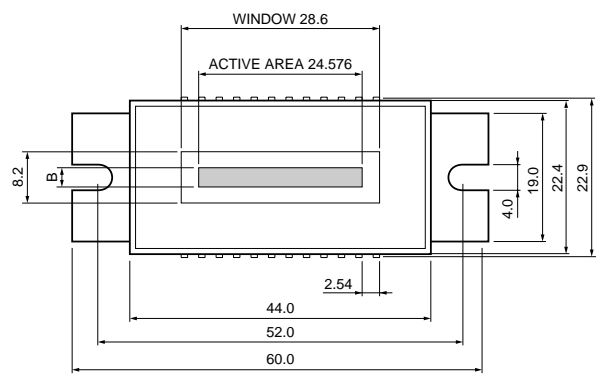
### S7034-0907S



S7034-0907S: A=2.928

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### S7034-1007S



S7034-1007S: B=2.928

KMPDA0083EC

# CCD area image sensor S7033/S7034 series

## ■ Pin connections

Pin No.	S7033 series		S7034 series		Remark (standard operation)
	Symbol	Function	Symbol	Function	
1	RD	Reset drain	RD	Reset drain	+12 V
2	OS	Output transistor source	OS	Output transistor source	RL=10 k to 100 kΩ
3	OD	Output transistor drain	OD	Output transistor drain	+20 V
4	OG	Output gate	OG	Output gate	+3 V
5	SG	Summing gate	SG	Summing gate	Same pulse as P2H
6	-		-		
7	-		-		
8	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	0 V
11	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	0 V
12	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Connect to RD
13	TG *18	Transfer gate	TG *15	Transfer gate	Same pulse as P2V
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	-		Th1	Thermistor	
17	-		Th2	Thermistor	
18	-		P-	TE-cooler-	
19	-		P+	TE-cooler+	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	Connect to RD
22	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	0 V
23	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	0 V
24	RG	Reset gate	RG	Reset gate	

\*18: Isolation gate between vertical register and horizontal register.

In standard operation, TG should be applied the same pulse as P2V.

## ■ Specifications of built-in TE-cooler (Typ.)

Parameter	Symbol	Condition	S7034-0907S	S7034-1007S	Unit
Internal resistance	Rint	Ta=25 °C	2.5	1.2	Ω
Maximum current *19	I <sub>max</sub>	T <sub>c</sub> *20=Th *21=25 °C	1.5	3.0	A
Maximum voltage	V <sub>max</sub>	T <sub>c</sub> *20=Th *21=25 °C	3.8	3.6	V
Maximum heat absorption *22	Q <sub>max</sub>		3.4	5.1	W
Maximum temperature of heat radiating side	-		70	70	°C

\*19: Maximum current I<sub>max</sub>:

If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.

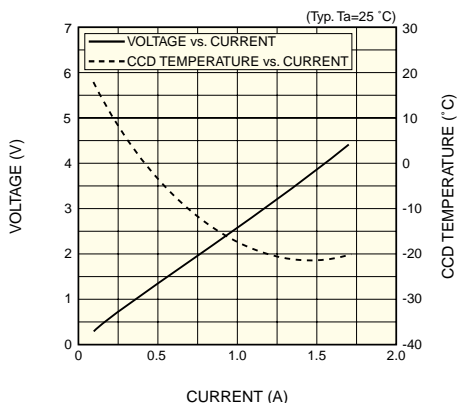
\*20: Temperature of the cooling side of thermoelectric cooler

\*21: Temperature of the heat radiating side of thermoelectric cooler

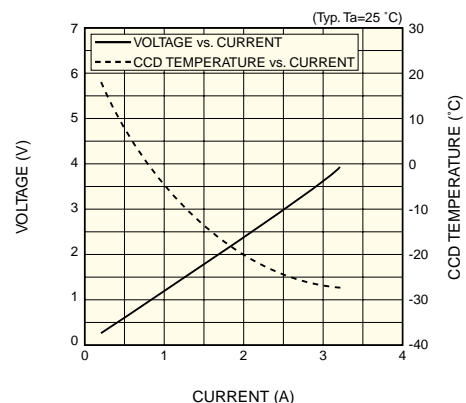
\*22: Maximum heat absorption Q<sub>max</sub>.

This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.

S7034-0907S



S7034-1007S



**■ Specifications of built-in temperature sensor**

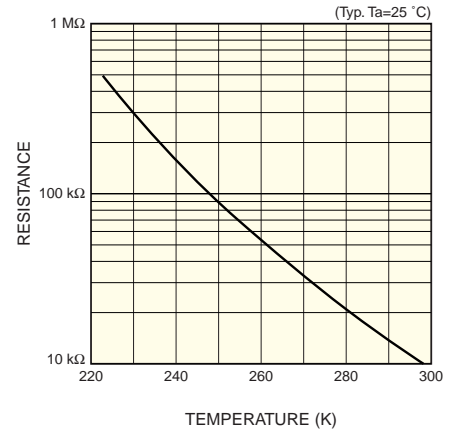
A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$$R1 = R2 \times \exp B (1 / T1 - 1 / T2)$$

where R1 is the resistance at absolute temperature T1 (K)  
 R2 is the resistance at absolute temperature T2 (K)  
 B is so-called the B constant (K)

The characteristics of the thermistor used are as follows.

- R (298K) = 10 kΩ
- B (298K / 323K) = 3450 K



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**■ Precaution for use (Electrostatic countermeasures)**

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

**■ Element cooling/heating temperature incline rate**

Element cooling/heating temperature incline rate should be set at less than 5 K/min.

**Multichannel detector head C7043/C7044**

**Features**

- C7043: for S7033 series  
C7044: for S7034 series
- Area scanning or full line-binning operation
- Readout frequency: 250 kHz
- Readout noise: 60 e<sup>-</sup>rms
- ΔT=50 °C (ΔT changes by cooling method.)

Input	Symbol	Value
Supply voltage	VD1	+5 Vdc, 200 mA
	VA1+	+15 Vdc, +100 mA
	VA1-	-15 Vdc, -100 mA
	VA2	+24 Vdc, 30 mA
	VD2	+5 Vdc, 30 mA (C7044)
	Vp	+5 Vdc, 2.5 A (C7044)
	VF	+12 Vdc, 100 mA (C7044)
Master start	φms	HCMOS logic compatible
Master clock	φmc	HCMOS logic compatible, 1 MHz

