512K×8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM48C512/L/SL-7	70ns	20ns	130ns
KM48C512/L/SL-8	80ns	20ns	150ns
KM48C512/L/SL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Dual +5V±10% power supply**
- **Refresh Cycle**
  - **— 1024 cycle/16ms (Normal)**
  - **— 1024 cycle/128ms (L-version)**
  - **— 1024 cycle/256ms (SL-version)**
- **Power Dissipation**
  - **— Standby: 11mW (Normal)**
    1.1mW (L-version)
    0.55mW (SL-version)
  - **— Active (70/80/100): 578/495/413mW**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ, ZIP and TSOP II**

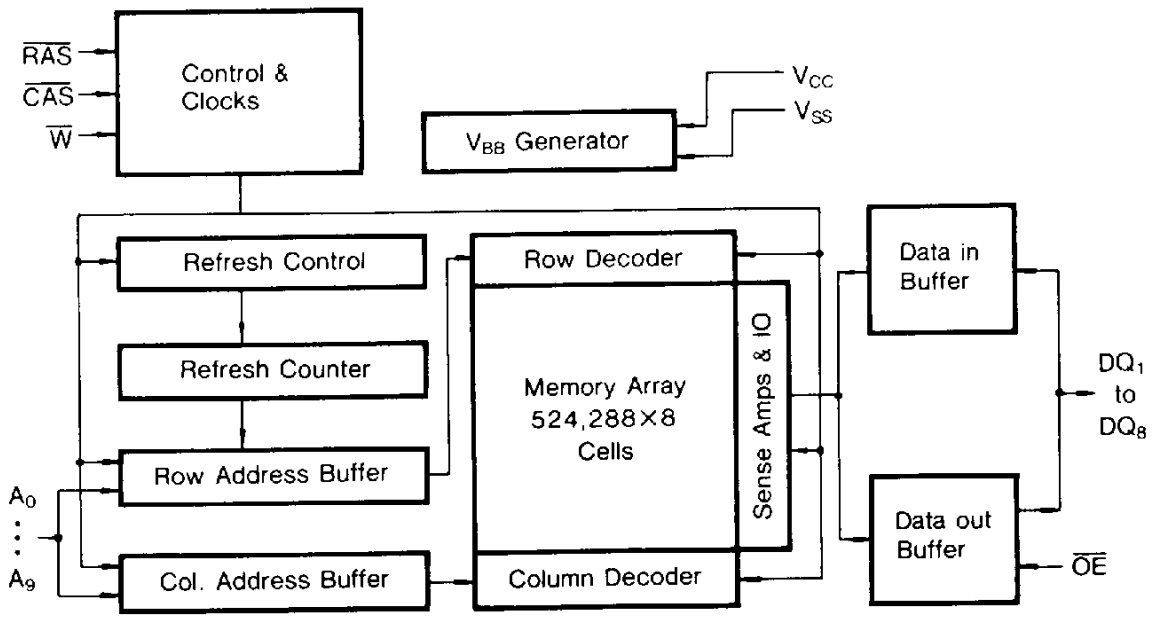
GENERAL DESCRIPTION

The Samsung KM48C512/L/SL is a CMOS high speed 524,288 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM48C512/L/SL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

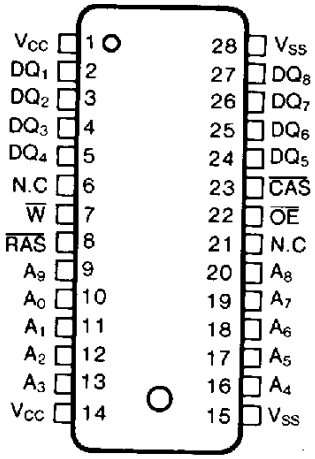
The KM48C512/L/SL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



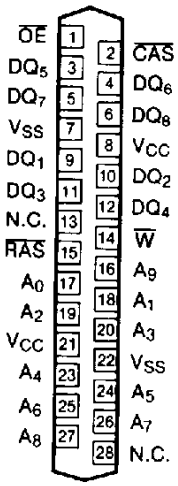
PIN CONFIGURATION (Top Views)

• KM48C512J/LJ/SLJ



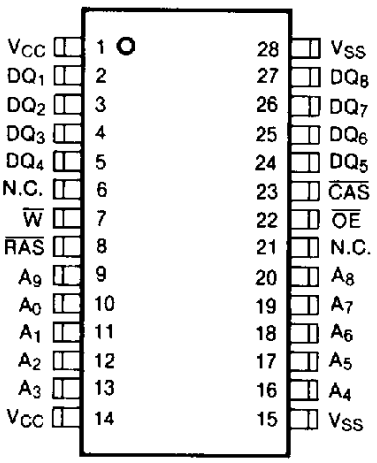
(SOJ)

• KM48C512Z/LZ/SLZ



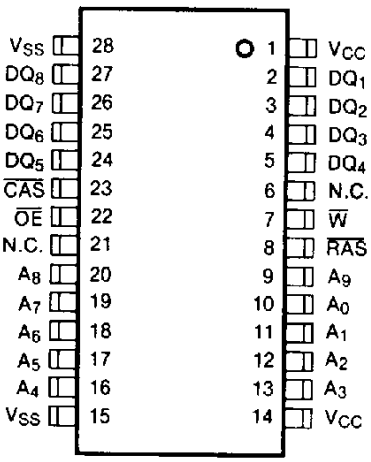
(ZIP)

• KM48C512T/LT/SLT



(TSOP(II)-Forward Type)

• KM48C512TR/LTR/SLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A_0-A_9	Address Input
DQ_{1-8}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe

Pin Name	Pin Function
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM48C512/L/SL-7	I_{CC1}	—	105	mA
	KM48C512/L/SL-8		—	90	mA
	KM48C512/L/SL-10		—	75	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM48C512/L/SL-7	I_{CC3}	—	105	mA
	KM48C512/L/SL-8		—	90	mA
	KM48C512/L/SL-10		—	75	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM48C512/L/SL-7	I_{CC4}	—	85	mA
	KM48C512/L/SL-8		—	75	mA
	KM48C512/L/SL-10		—	65	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)	KM48C512	I_{CC5}	—	1	mA
	KM48C512L		—	200	μA
	KM48C512SL		—	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM48C512/L/SL-7	I_{CC6}	—	105	mA
	KM48C512/L/SL-8		—	90	mA
	KM48C512/L/SL-10		—	75	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode Input High Voltage (V_{IH}) = V_{CC}-0.2V Input Low Voltage (V_{IL}) = 0.2V $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V D_{IN} = Don't Care T_{RC}=125 μS(L-ver), T_{RC}=250 μS(SL-ver), T_{RAS}=T_{RAS}min.~1μS.	KM48C512L	I_{CC7}	—	300	μA
	KM48C512SL		—	150	μA

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any Input $0 \le V_{IN} \le 6.5V$, all other pins not under test=0V)	I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le 5.5V$)	I_{OL}	−10	10	μA
Output High Voltage Level(I_{OH}=−5mA)	V_{OH}	2.4	—	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4}, Address can be changed maximum once while $\overline{CAS} = V_{IH}$.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_8)	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM48C512/L/SL-7		KM48C512/L/SL-8		KM48C512/L/SL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	180		200		240		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to CAS delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	11
$\overline{CAS}$ to RAS precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC}=5.0V \pm 10\%$, See notes 1,2)

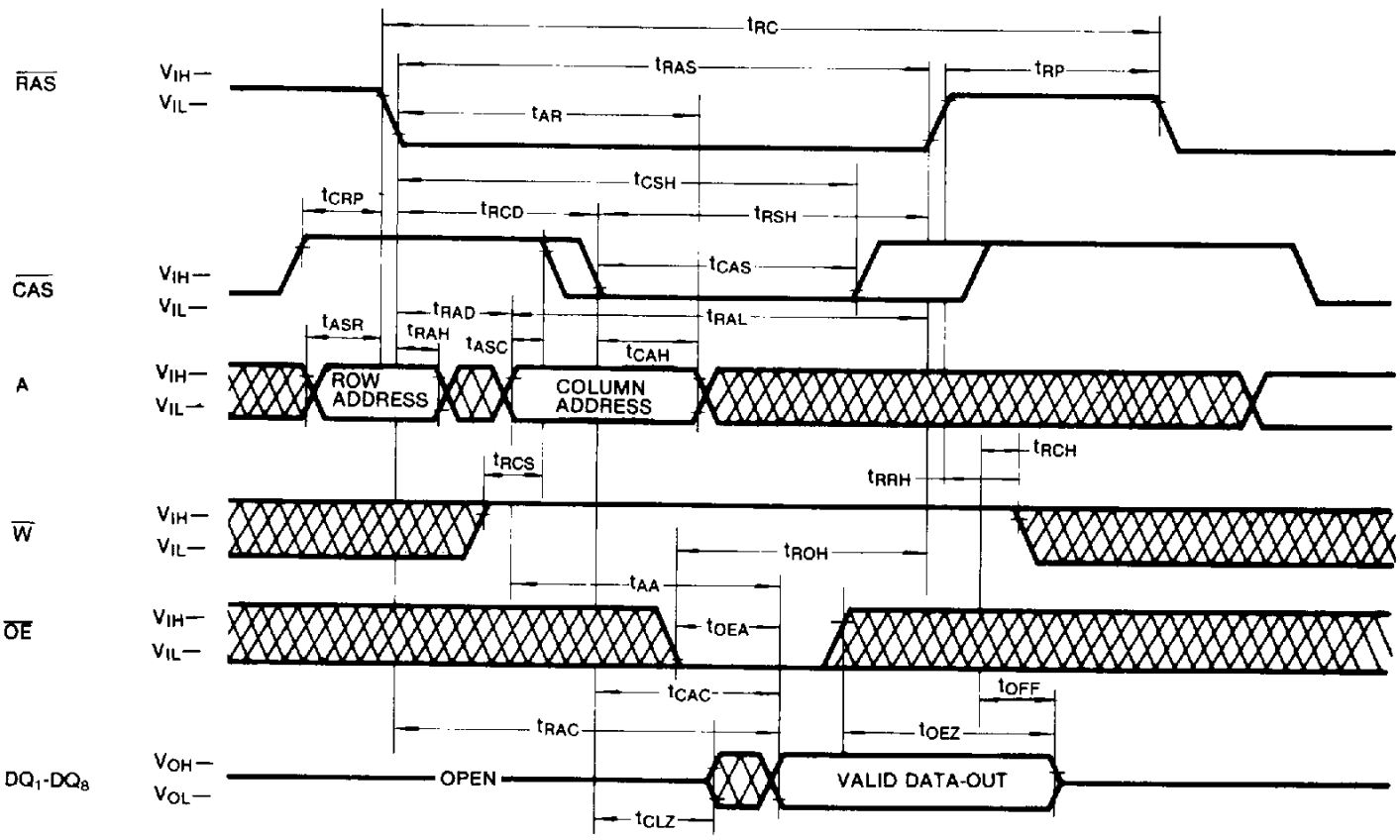
Parameter	Symbol	KM48C512/L/SL-7		KM48C512/L/SL-8		KM48C512/L/SL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Refresh period (L-version)	t_{REF}		128		128		128	ms	
Refresh period (SL-version)	t_{REF}		256		256		256	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	45		45		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	95		105		130		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		65		75		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
Fast page mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	95		100		115		ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data-in delay time	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or r_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point ony. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

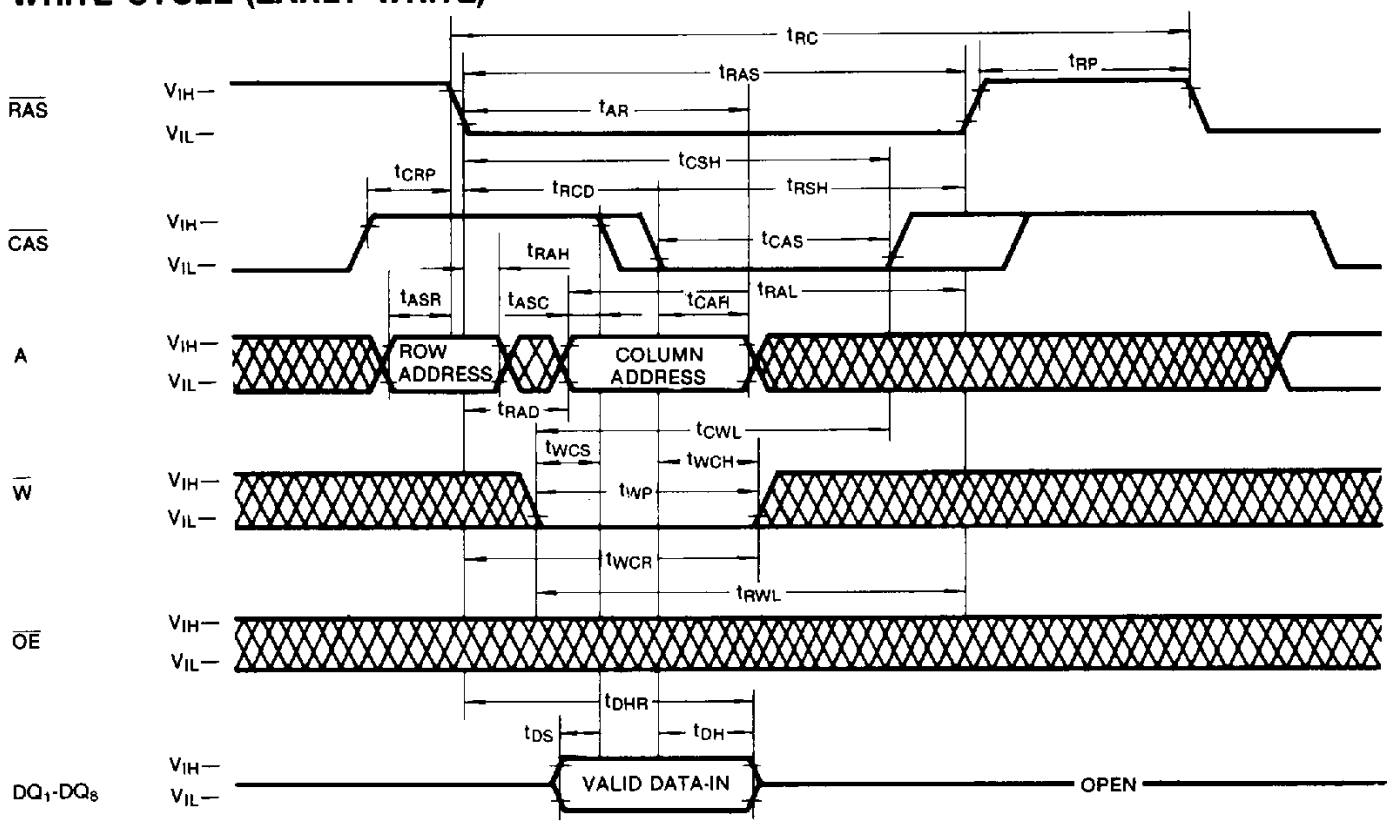
TIMING DIAGRAMS

READ CYCLE

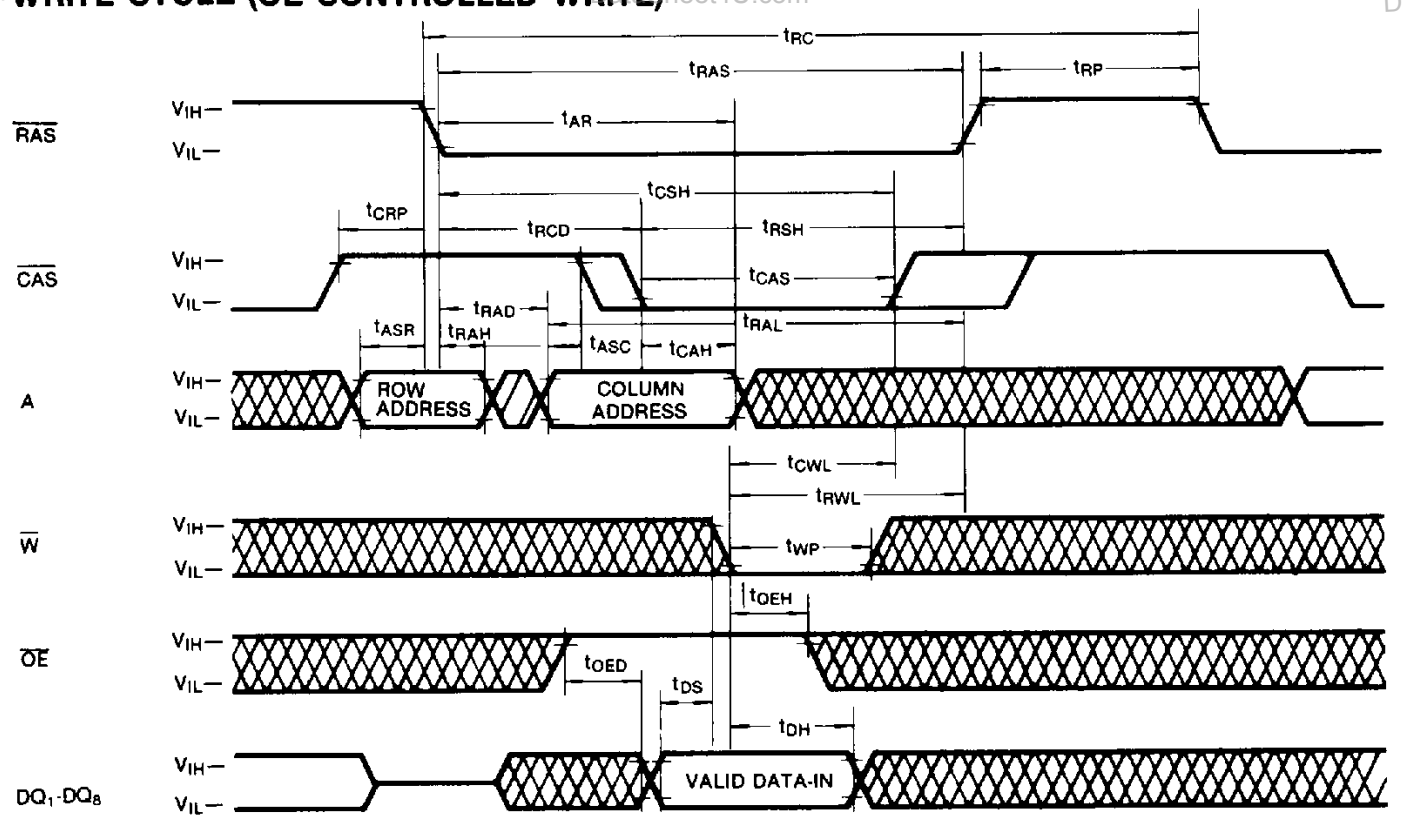


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



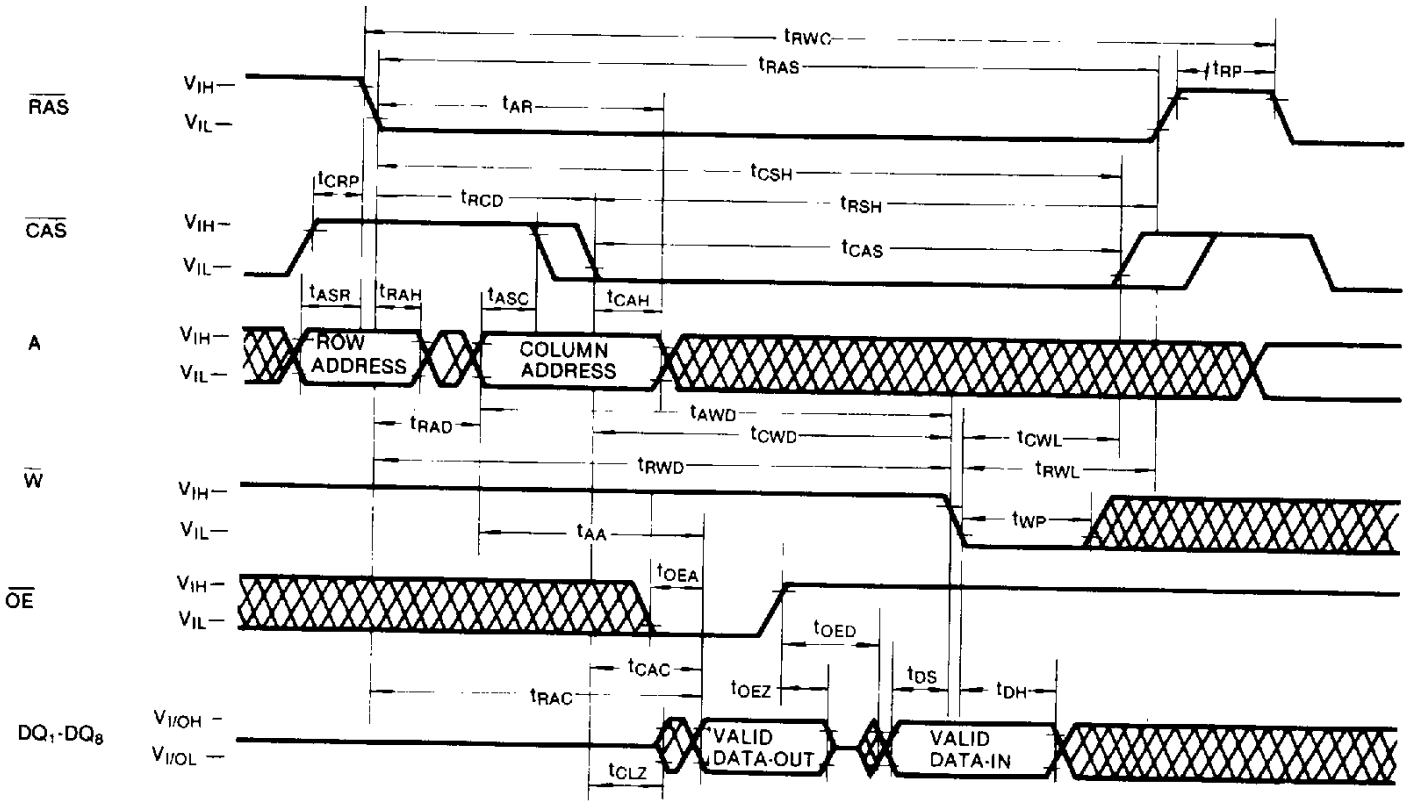
WRITE CYCLE (OE CONTROLLED WRITE)



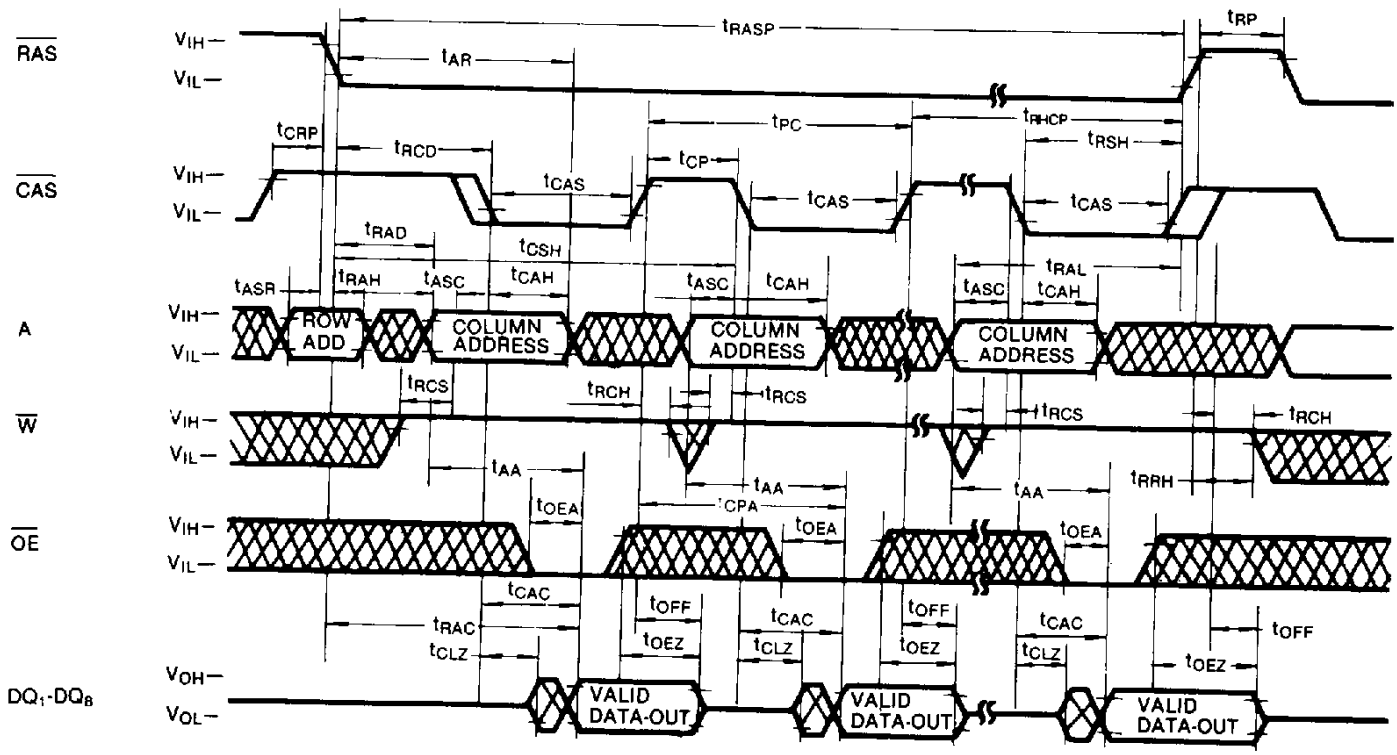
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



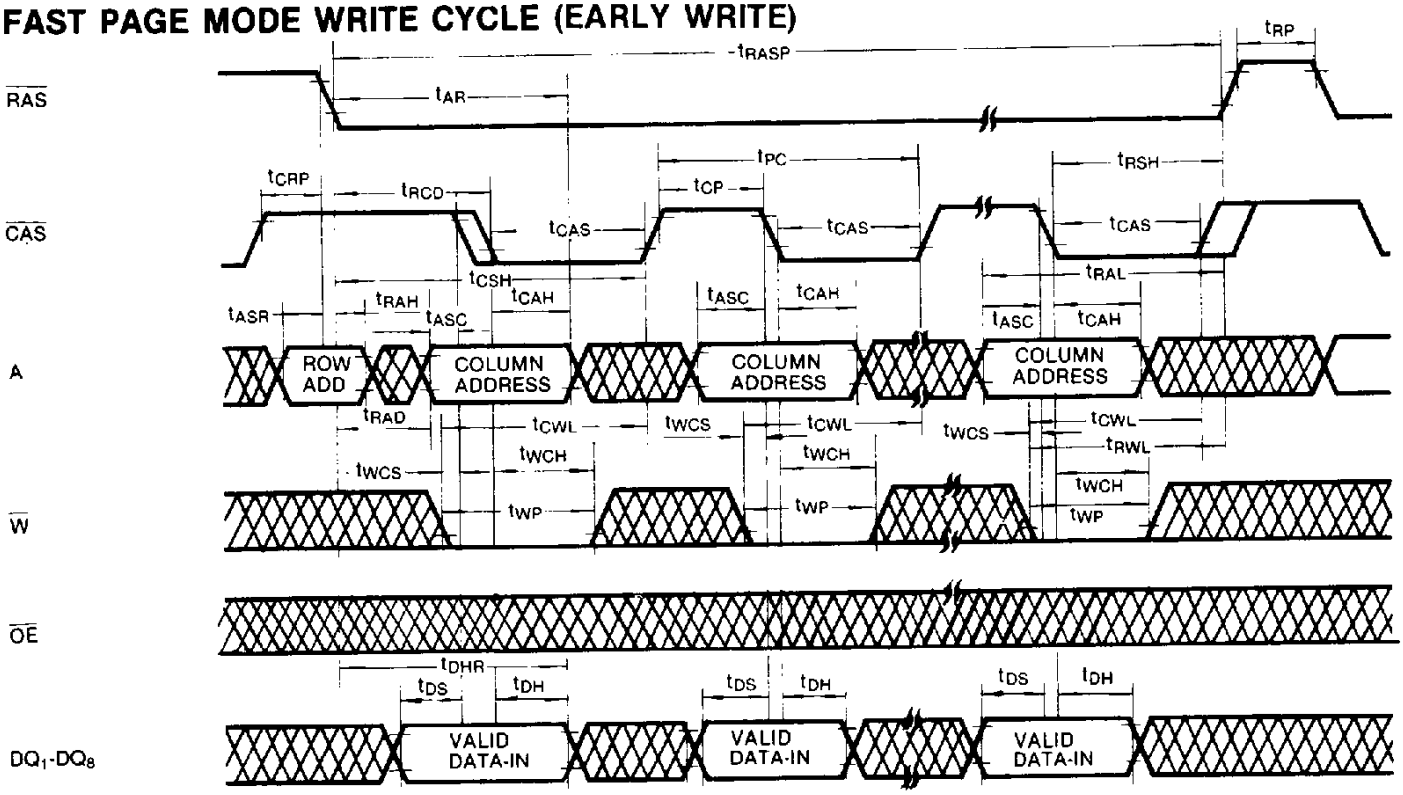
FAST PAGE MODE READ CYCLE



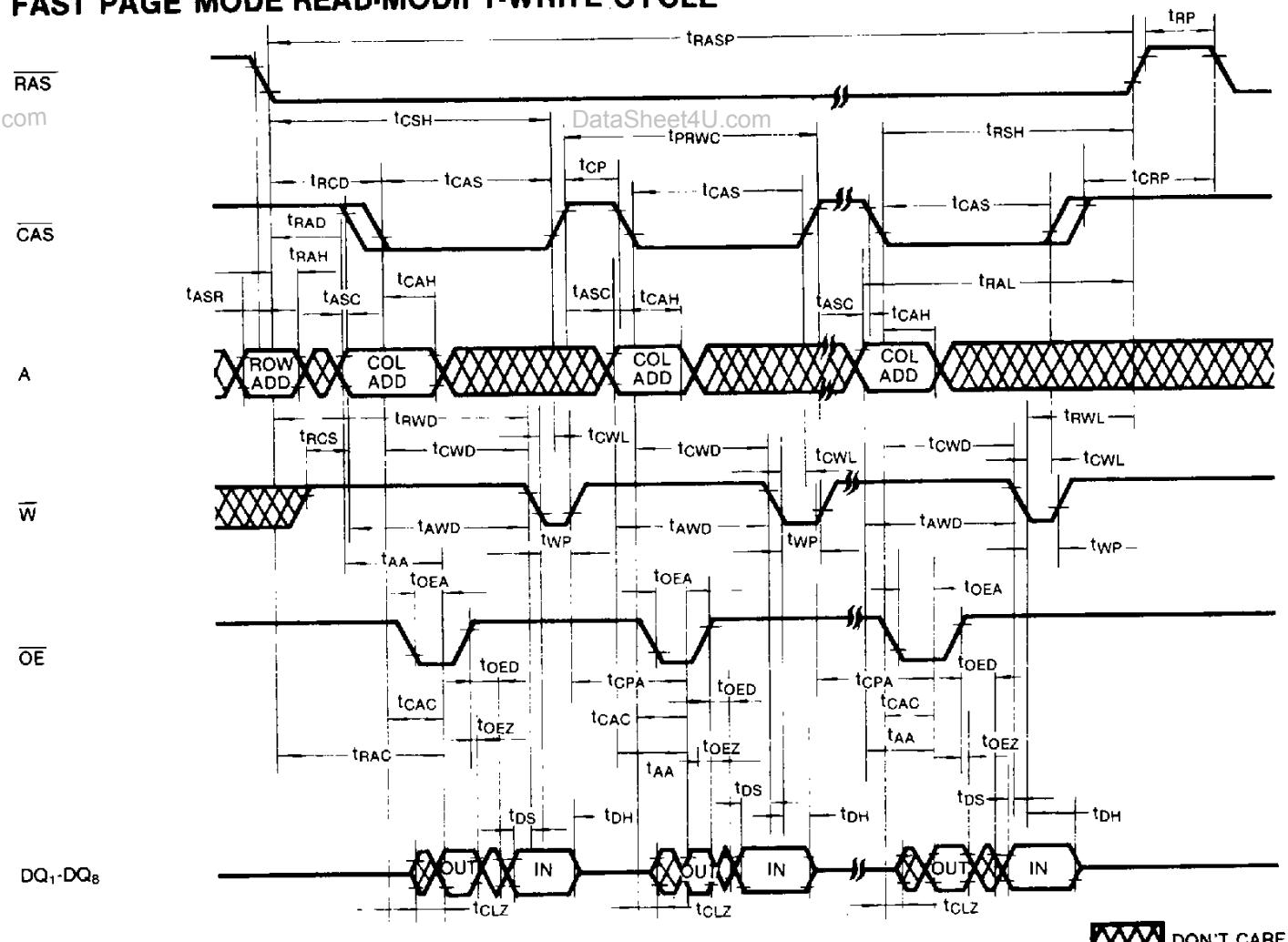
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



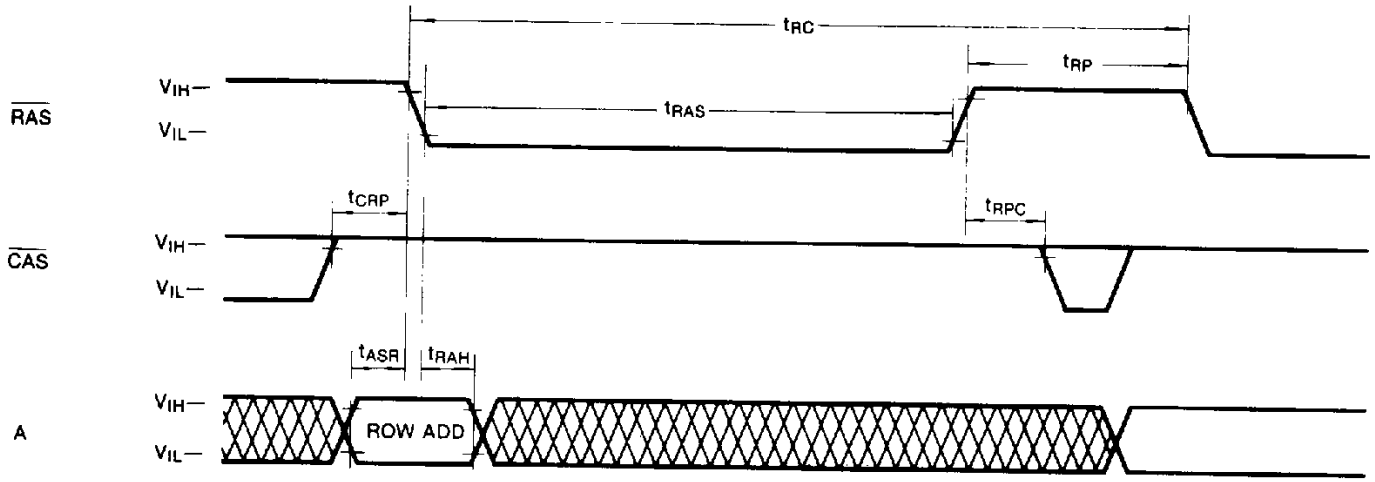
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

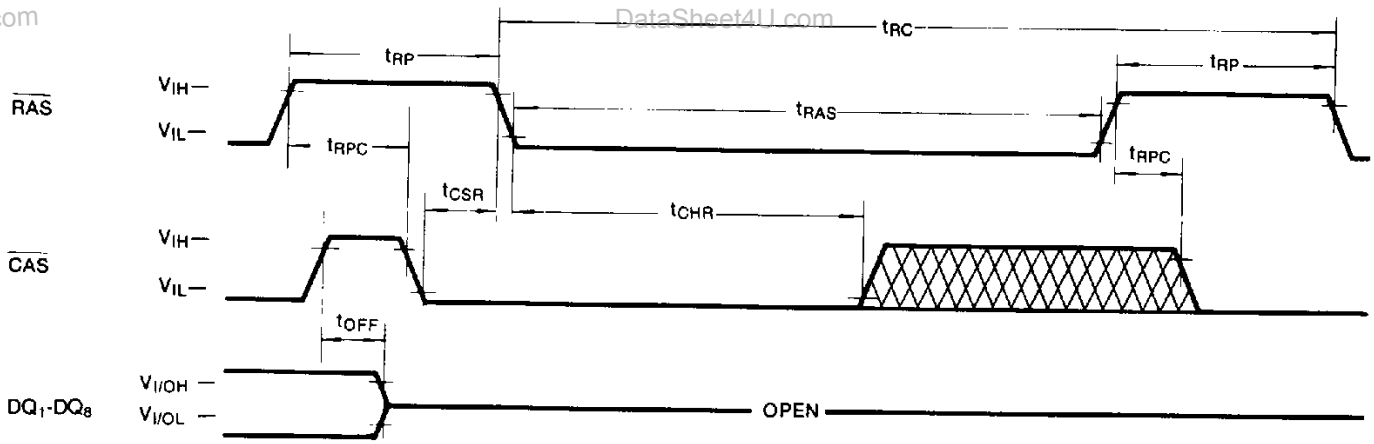
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

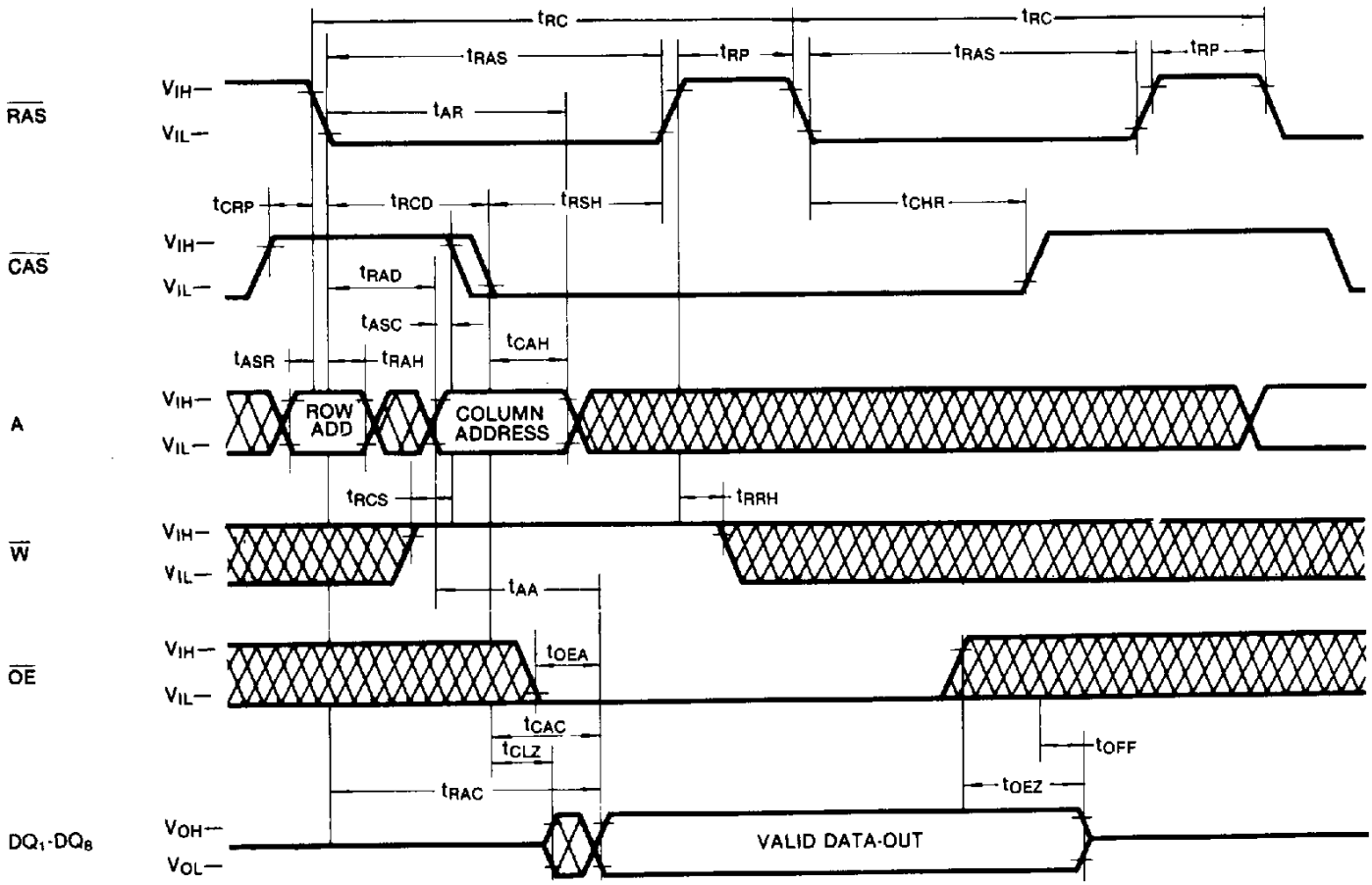
NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care



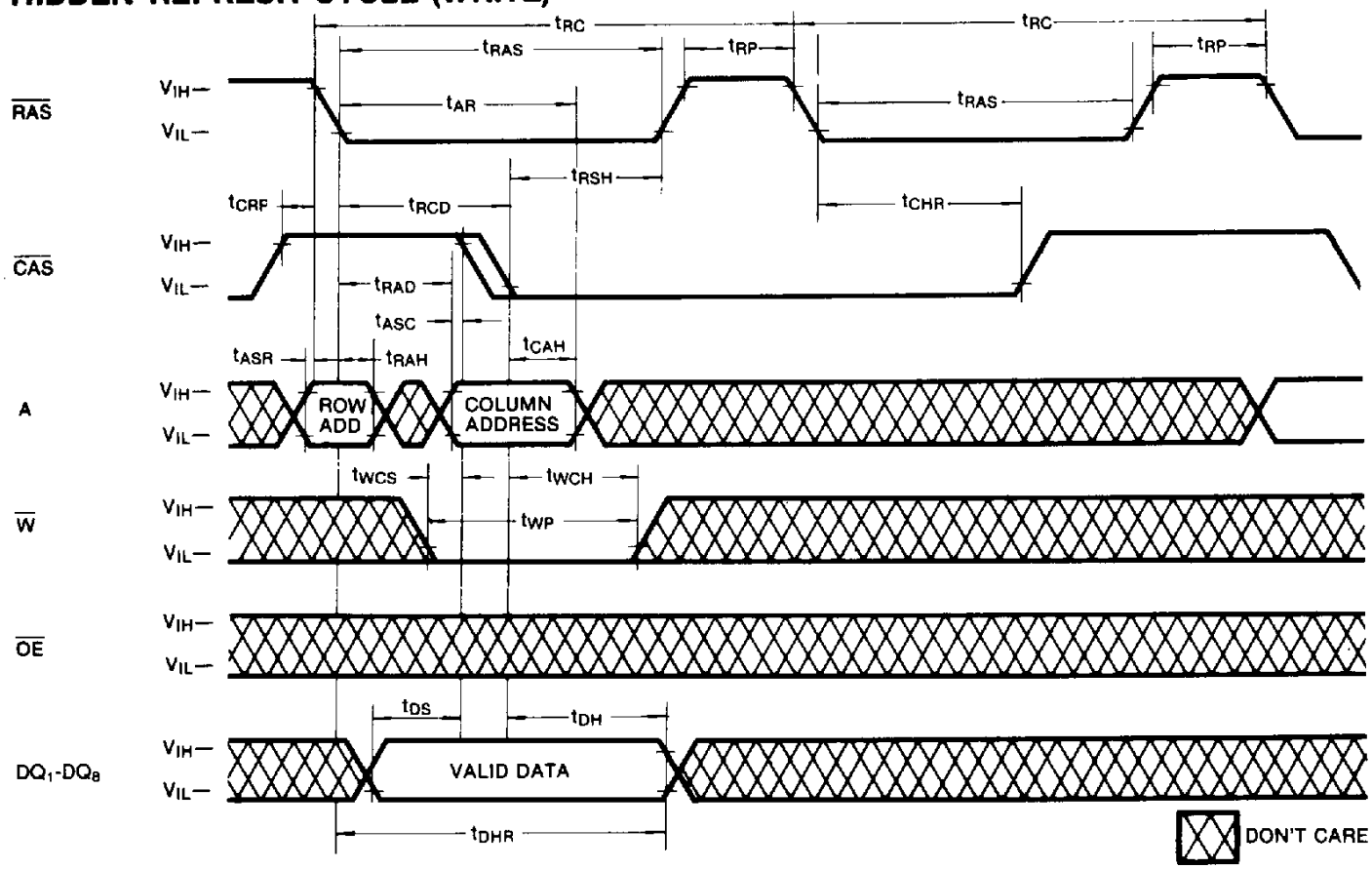
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

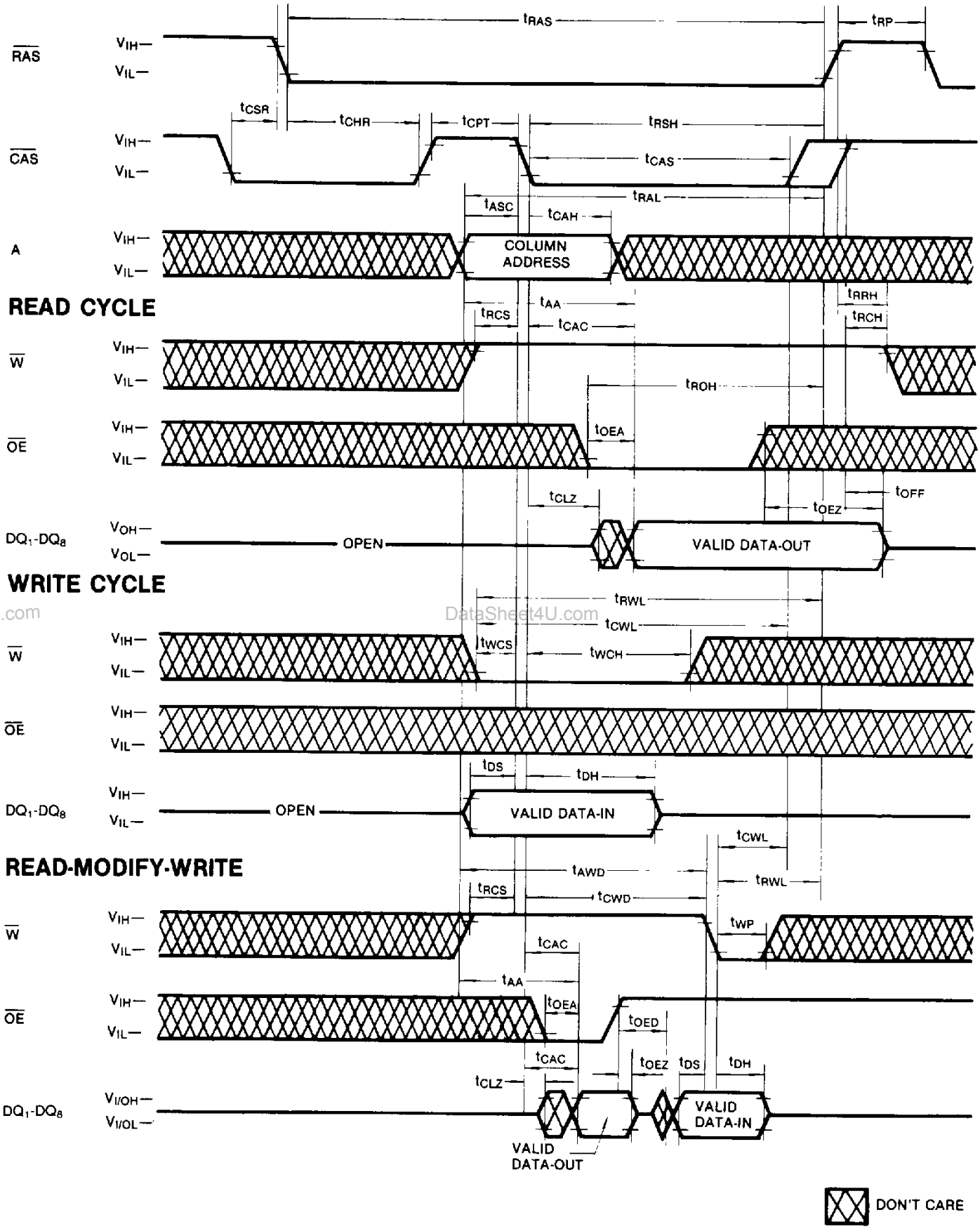


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM48C512/L/SL contains 4,194,304 memory locations arranged in 8 groups of 524,288 × 1 bit each. Ninteen address bits are required to address a particular memory location. Since the KM48C512/L/SL has only 10 address input pins, time multiplexed addressing is used to input 10 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM48C512/L/SL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM48C512/L/SL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM48C512/L/SL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM48C512/L/SL can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 8-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM48C512/L/SL DQ pins.

Data Output

The KM48C512/L/SL has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM48C512/L/SL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM48C512/L/SL is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will affect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) off within 16ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 1024 row address (A0-A9).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM48C512/L/SL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM48C512/L/SL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM48C512/L/SL has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A9 are supplied by on chip refresh counter.

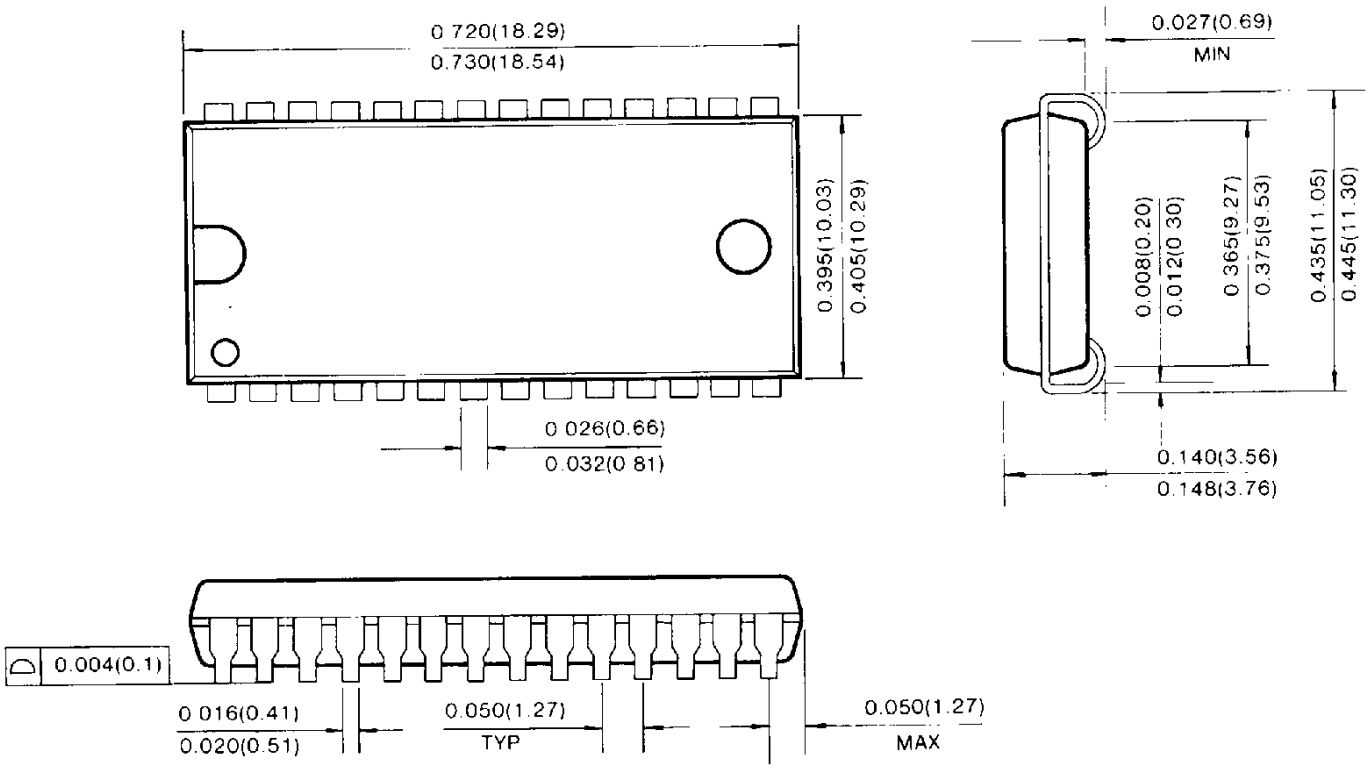
Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM48C512/L/SL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize the power-up current.

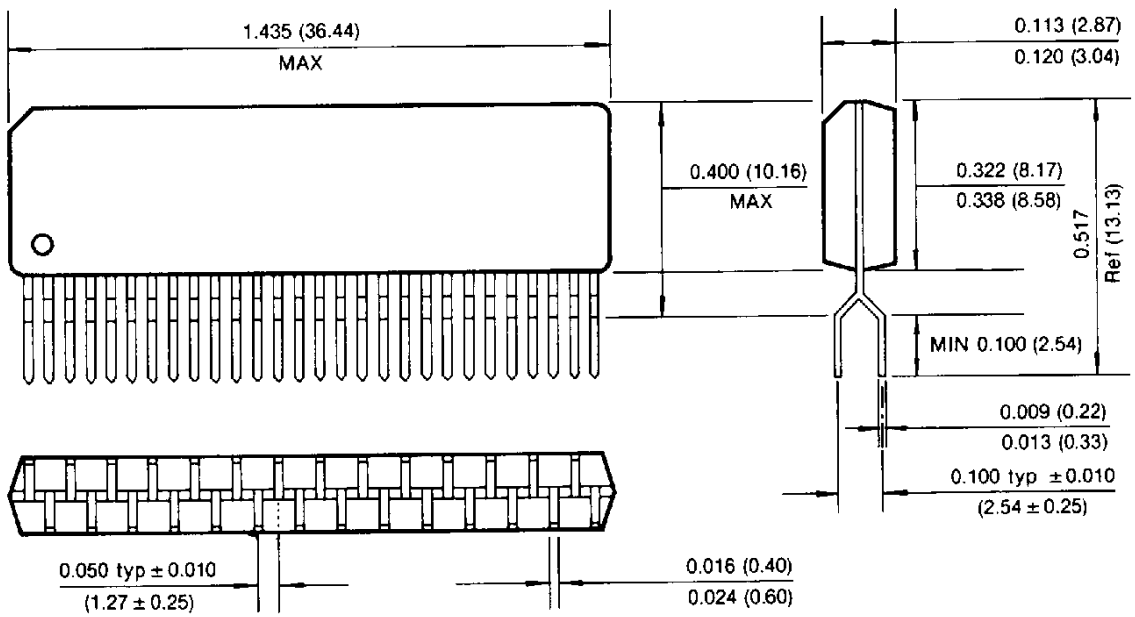
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)