HD404818/HD404814/HD4074818/ HD40L4818/HD40L4814/HD407L4818

Description

The HD404818/HD404814/HD4074818/ HD40L4818/HD40L4814/HD407L4818 is a 4-bit single-chip HMCS400 series microcomputer providing high program productivity. It incorporates a large size memory, LCD driver/controller, voltage comparator, and 32-kHz watch oscillator circuit.

The HD4074818/HD407L4818, containing a PROM, is a ZTAT™ microcomputer which can dramatically shorten system development time and smoothly proceed from debugging to mass production.

Features

- 8192-word × 10-bit ROM (HD404818, HD4074818, HD40L4818, HD407L4818)
- 4096-word × 10-bit ROM (HD404814, HD40L4814)
- 1184-digit × 4-bit RAM
- 30 I/O pins, including 10 high-current output pins, all CMOS and programmable as I/O pull-up MOS
- 16-digit LCD driver
- Three timer/counters
- Clock-synchronous 8-bit serial interface
- Six interrupt sources
  - — Two by external sources
  - — Four by internal sources
- Subroutine stack up to 16 levels, including interrupts
- Instruction cycle time:
  - — 1 µs (f_{OSC} = 4 MHz for HD404818/HD404814/HD4074818)
  - — 5 µs (f_{OSC} = 800 kHz for HD40L4818/HD40L4814/HD407L4818)
- Four low-power dissipation modes
  - — Standby mode
  - — Stop mode
  - — Watch mode
  - — Subactive mode
- Internal oscillator:
  - — Crystal or ceramic filter
  - — External clock is available
- Voltage comparator (2 channels)
- Package
  - — 80-pin plastic flat package (FP-80B) (FP-80A)
  - — 80-pin plastic thin flat package (TFP-80)*

* Under development

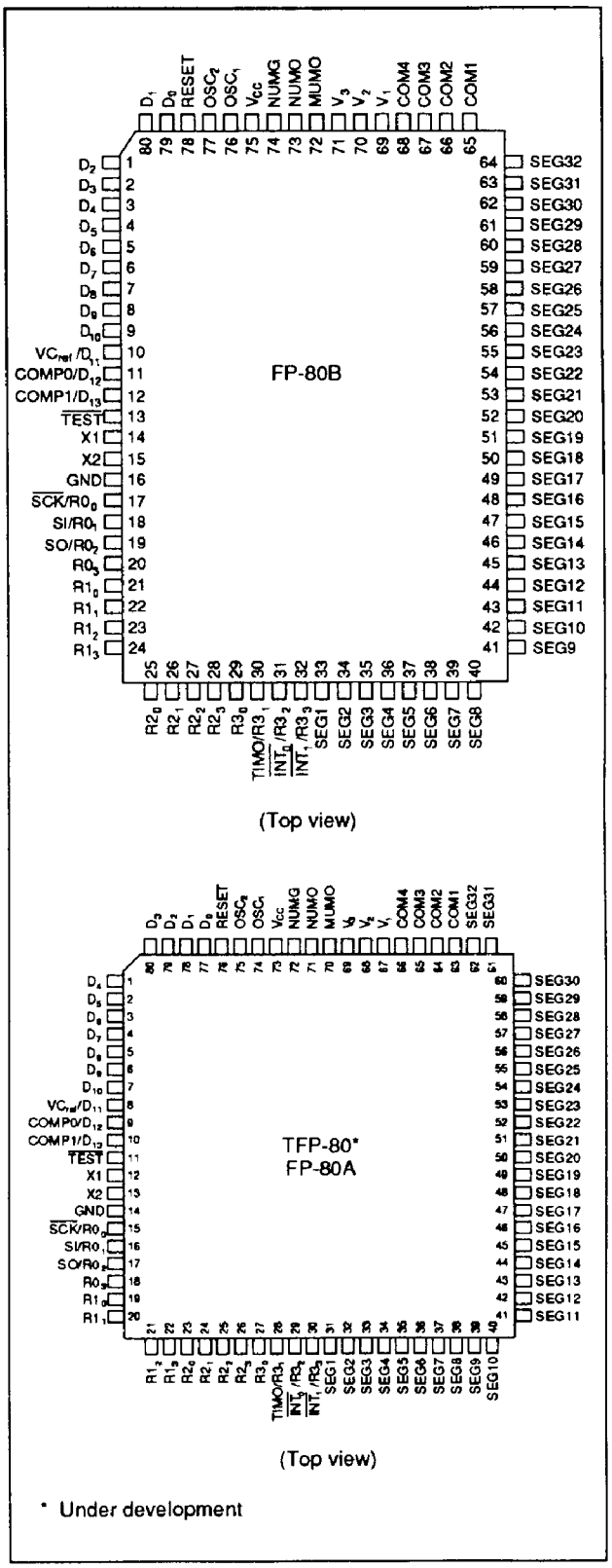
Ordering Information

Mask ROM Type

Type	Product Number	Clock Frequency	Package
Mask ROM	HD404818FS HD404814FS	4	FP-80B
	HD404818H HD404814H		FP-80A
	HD404818TF HD404814TF		TFP-80Note
	HD40L4818FS HD40L4814FS	0.8	FP-80B
	HD40L4818H HD40L4814H		FP-80A
	HD40L4818TF HD40L4814TF		TFP-80Note
ZTAT™	HD4074818FS	4	FP-80B
	HD4074818H		FP-80A
	HD4074818TF		TFP-80Note
	HD407L4818FS	0.8	FP-80B
	HD407L4818H		FP-80A
	HD407L4818TF		TFP-80Note

Note: Under development.

Pin Arrangement



Pin Description

Pin Number				Pin Number			
FP-80B	FP-80A, TFP-80	Pin Name	I/O	FP-80B	FP-80A, TFP-80	Pin Name	I/O
1	79	D_2	I/O	41	39	SEG9	O
2	80	D_3	I/O	42	40	SEG10	O
3	1	D_4	I/O	43	41	SEG11	O
4	2	D_5	I/O	44	42	SEG12	O
5	3	D_6	I/O	45	43	SEG13	O
6	4	D_7	I/O	46	44	SEG14	O
7	5	D_8	I/O	47	45	SEG15	O
8	6	D_9	I/O	48	46	SEG16	O
9	7	D_{10}	I	49	47	SEG17	O
10	8	D_{11}/VC_{ref}	I	50	48	SEG18	O
11	9	D_{12}/COMP0	I	51	49	SEG19	O
12	10	D_{13}/COMP1	I	52	50	SEG20	O
13	11	$\overline{TEST}$	I	53	51	SEG21	O
14	12	X1	I	54	52	SEG22	O
15	13	X2	O	55	53	SEG23	O
16	14	GND		56	54	SEG24	O
17	15	$R0_0/\overline{SCK}$	I/O	57	55	SEG25	O
18	16	$R0_1$/SI	I/O	58	56	SEG26	O
19	17	$R0_2$/SO	I/O	59	57	SEG27	O
20	18	$R0_3$	I/O	60	58	SEG28	O
21	19	$R1_0$	I/O	61	59	SEG29	O
22	20	$R1_1$	I/O	62	60	SEG30	O
23	21	$R1_2$	I/O	63	61	SEG31	O
24	22	$R1_3$	I/O	64	62	SEG32	O
25	23	$R2_0$	I/O	65	63	COM1	O
26	24	$R2_1$	I/O	66	64	COM2	O
27	25	$R2_2$	I/O	67	65	COM3	O
28	26	$R2_3$	I/O	68	66	COM4	O
29	27	$R3_0$	I/O	69	67	V_1	
30	28	$R3_1$/TIMO	I/O	70	68	V_2	
31	29	$R3_2/\overline{INT_0}$	I/O	71	69	V_3	
32	30	$R3_3/\overline{INT_1}$	I/O	72	70	NUMO	
33	31	SEG1	O	73	71	NUMO	
34	32	SEG2	O	74	72	NUMG	
35	33	SEG3	O	75	73	V_{CC}	
36	34	SEG4	O	76	74	OSC_1	I
37	35	SEG5	O	77	75	OSC_2	O
38	36	SEG6	O	78	76	RESET	I
39	37	SEG7	O	79	77	D_0	I/O
40	38	SEG8	O	80	78	D_1	I/O

Note: I/O: Input/output pin, I: Input pin, O: Output pin, NUMO: Open, NUMG: GND

Pin Functions

Power Supply

V_{CC}: Apply the V_{CC} power supply voltage to this pin.

GND: Connect to ground.

$\overline{TEST}$: For test purposes only. Connect it to V_{CC}.

RESET: MCU reset pin. Refer to the Reset section for details.

NUMG: Non-user pin. Connect it to GND.

NUMO: Non-user pin. Do not connect it to any lines.

Oscillators

OSC_1, OSC_2: Internal oscillator input pins. They both can be connected to a crystal, ceramic filter resonator, or external oscillator circuit. Refer to the Internal Oscillator Circuit section for details.

X1, X2: Watch oscillator 32-kHz crystal pins.

Ports

D_0–D_{13} (D Port): 14 1-bit I/O ports. D_0 to D_9 are I/O ports and D_{10} to D_{13} are input ports. D_0–D_9 are high current output ports (15 mA max.). D_{11}–D_{13} are also available as voltage comparators. Refer to the Input/Output section for details.

R0–R3 (R Ports): 4-bit I/O ports. $R0_0$, $R0_1$, $R0_2$, $R3_1$, $R3_2$, and $R3_3$ are multiplexed with $\overline{SCK}$, SI, SO, TIMO, $\overline{INT_0}$, and $\overline{INT_1}$, respectively.

Interrupts

$\overline{INT_0}$, $\overline{INT_1}$: External interrupt pins. $\overline{INT_1}$ can be used as an external event input pin for timer B. $\overline{INT_0}$ and $\overline{INT_1}$ are multiplexed with $R3_2$ and $R3_3$, respectively. For details, see the Interrupts section.

Serial Communications Interface

$\overline{SCK}$, SI, SO: The transmit clock I/O pin ($\overline{SCK}$), serial data input pin (SI), and serial data output pin (SO) are used for serial interface. $\overline{SCK}$, SI, and SO are multiplexed with $R0_0$, $R0_1$, and $R0_2$, respectively. For details, see the Serial Interface section.

Timer

TIMO: Variable duty-cycle pulse waveform output pin. See the Timer C section for details.

LCD Driver/Controller

V_1, V_2, V_3: Power supply pins for the LCD driver. Since the LCD driving resistors are provided internally, no lines should be connected to these pins. The voltage on each pin is $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$. See the Liquid Crystal Display section for details.

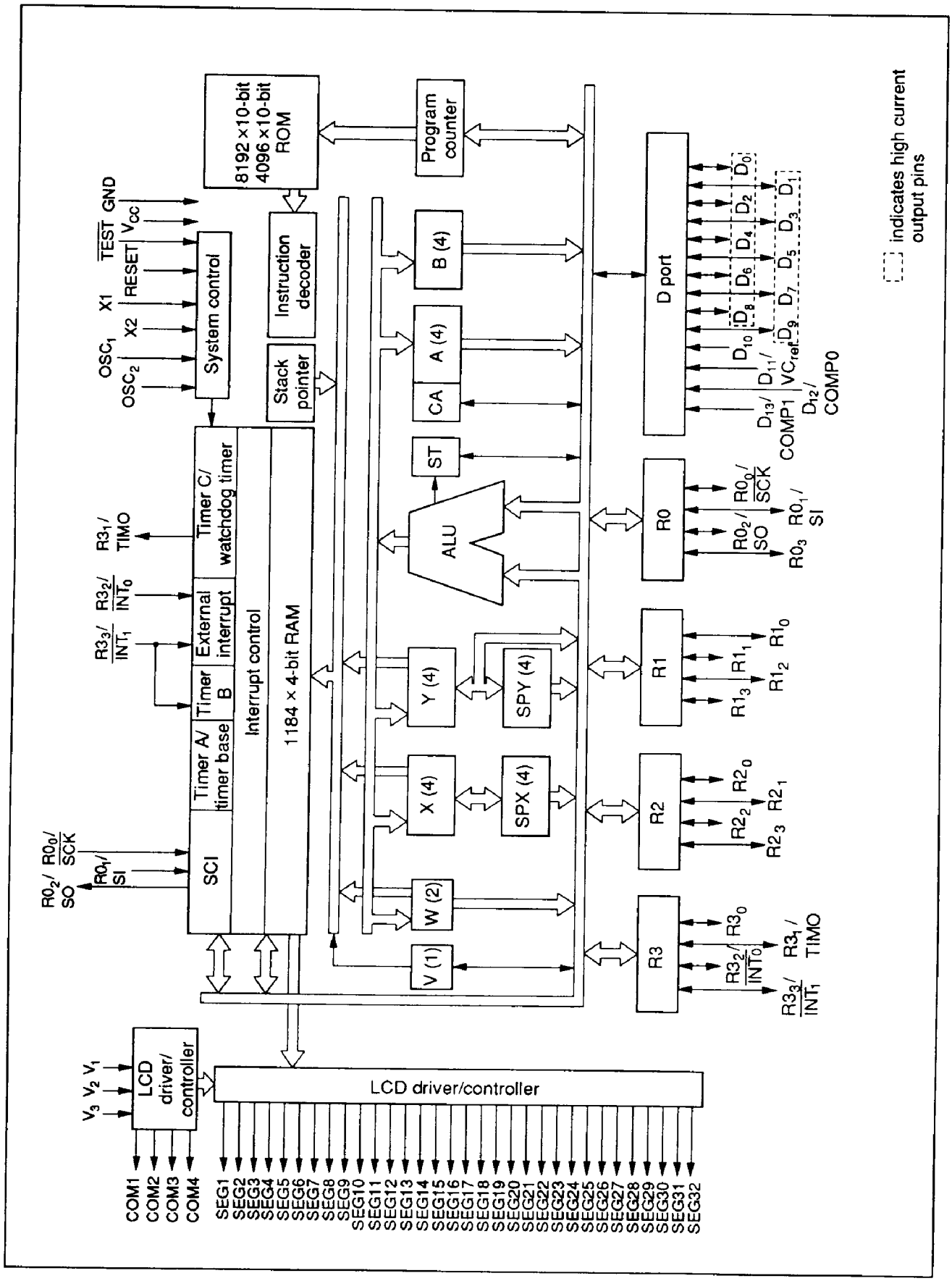
COM1 to COM4: Common signal output pins for the LCD display. See the Liquid Crystal Display section for details.

SEG1 to SEG32: Segment signals output pins for the LCD display. See the Liquid Crystal Display section for details.

Voltage Comparator

COMP0, COMP1, VC_{ref}: Analog input pins for the voltage comparator. VC_{ref} is used as a reference voltage pin to input the threshold voltage of the analog input pin.

Block Diagram



Memory Map

ROM Memory Map

The ROM is described in the following paragraphs with the ROM memory map in figure 1.

Vector Address Area ($0000 to $000F): Locations $0000 through $000F are reserved for JMPL instructions to branch to the starting address of the initialization program and of the interrupt programs. After reset or an interrupt routine, the program is executed from the vector address.

Zero-Page Subroutine Area ($0000 to $003F): Locations $0000 through $003F are reserved for subroutines. The program sequence branches to subroutines by the CAL instruction.

Pattern Area ($0000 to $0FFF): Locations $0000 through $0FFF are reserved for ROM data. The P instruction allows the MCU to reference ROM data as a pattern.

Program Area ($0000 to $1FFF: HD404818, HD4074818, HD40L4818, HD407L4818; $0000 to $0FFF: HD404814, HD40L4814): Used for program coding.

RAM Memory Map

The MCU also contains a 1,184-digit × 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bits Area ($000 to $003): The interrupt control bits area (figure 3) is used for interrupt control. It is accessible only by RAM bit manipulation instructions. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area ($004 to $01F, $024 to $03F): The special function registers are the mode or data registers for the serial interface, timer/counters, LCD, and the data control registers for the I/O ports. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2.

The SEM/REM and SEMD/REMD instructions are available for the LCD control register (LCR).

Other registers cannot be accessed by RAM bit manipulation instructions.

Register Flag Area ($020 to $023): Consist of the LSON, WDON, TGSP, and DTON flags which are bit registers accessible by the RAM bit manipulation instruction.

The WDON flag can only be set, and only by the SEM/SEMD instruction.

The DTON flag can be set, reset, and tested by the SEM/SEMD, REM/REMD, and TMD instructions. Note that the DTON flag is active only in subactive mode, and is normally reset in active mode.

LCD Data Area ($050 to $06F): Locations $050 to $06F store the LCD data which is automatically transmitted to the segment driver as display data. The LCD is illuminated with 1s and faded with 0s. This area can be used as a data area.

Data Area ($040 to $2CF, $100 to $2CF; Bank 0/1): The 16 digits of $040 through $04F are called memory registers (MR) and are accessible by the LAMR and XMRA instructions (figure 4). 464 digits of $100 through $2CF are selected as bank 0 or 1 depending on the value of the V register.

Stack Area ($3C0 to $3FF): Locations $3C0 through $3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status flag (ST), and carry flag (CA) when subroutine calls (CAL or CALL instruction) and interrupts are processed. This area can be used as a 16-level nesting stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by the RTN and RTNI instructions. The status and carry flags are restored only by the RTNI instruction. This area, when not used as a stack, is available as a data area.

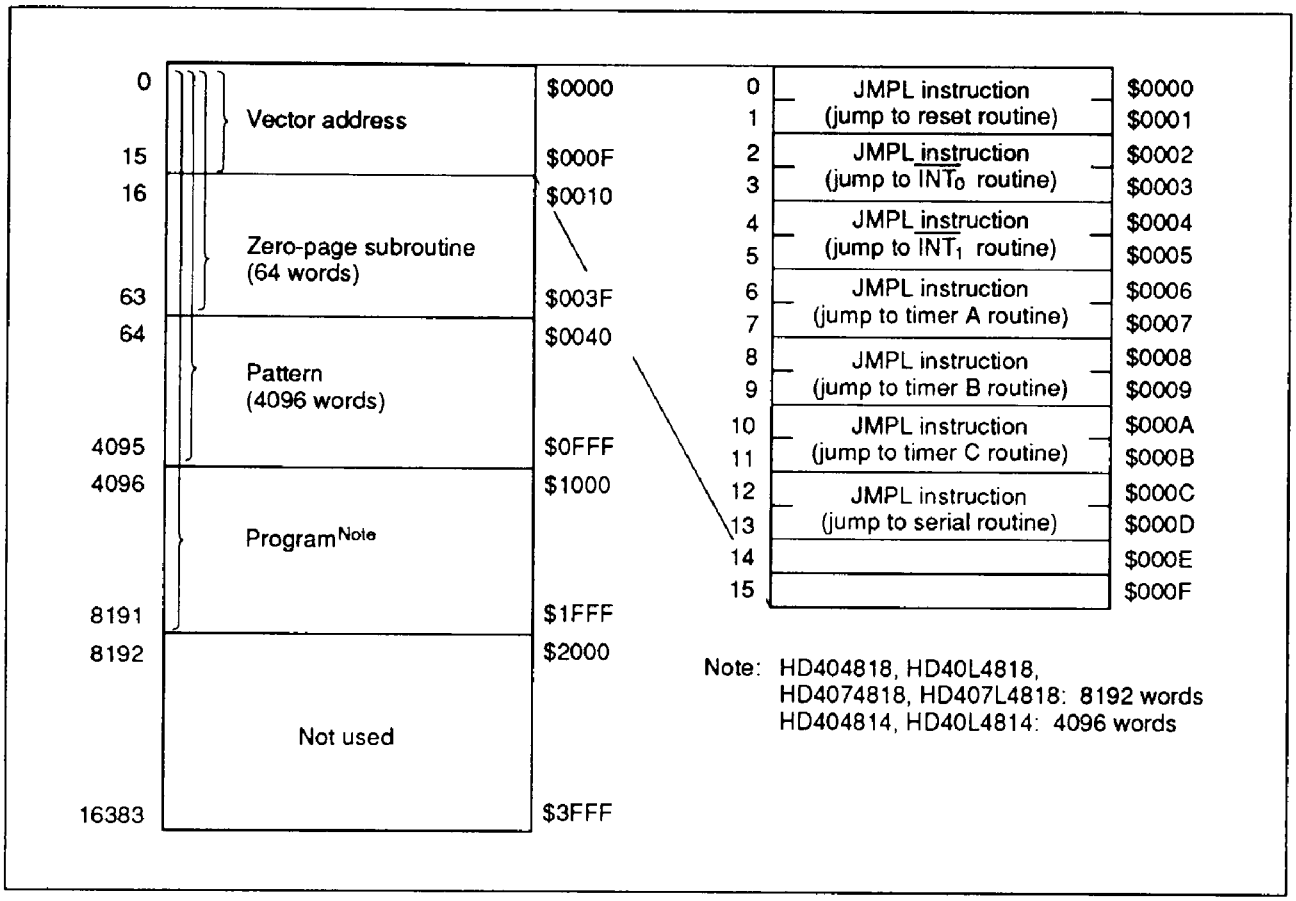


Figure 1 ROM Memory Map

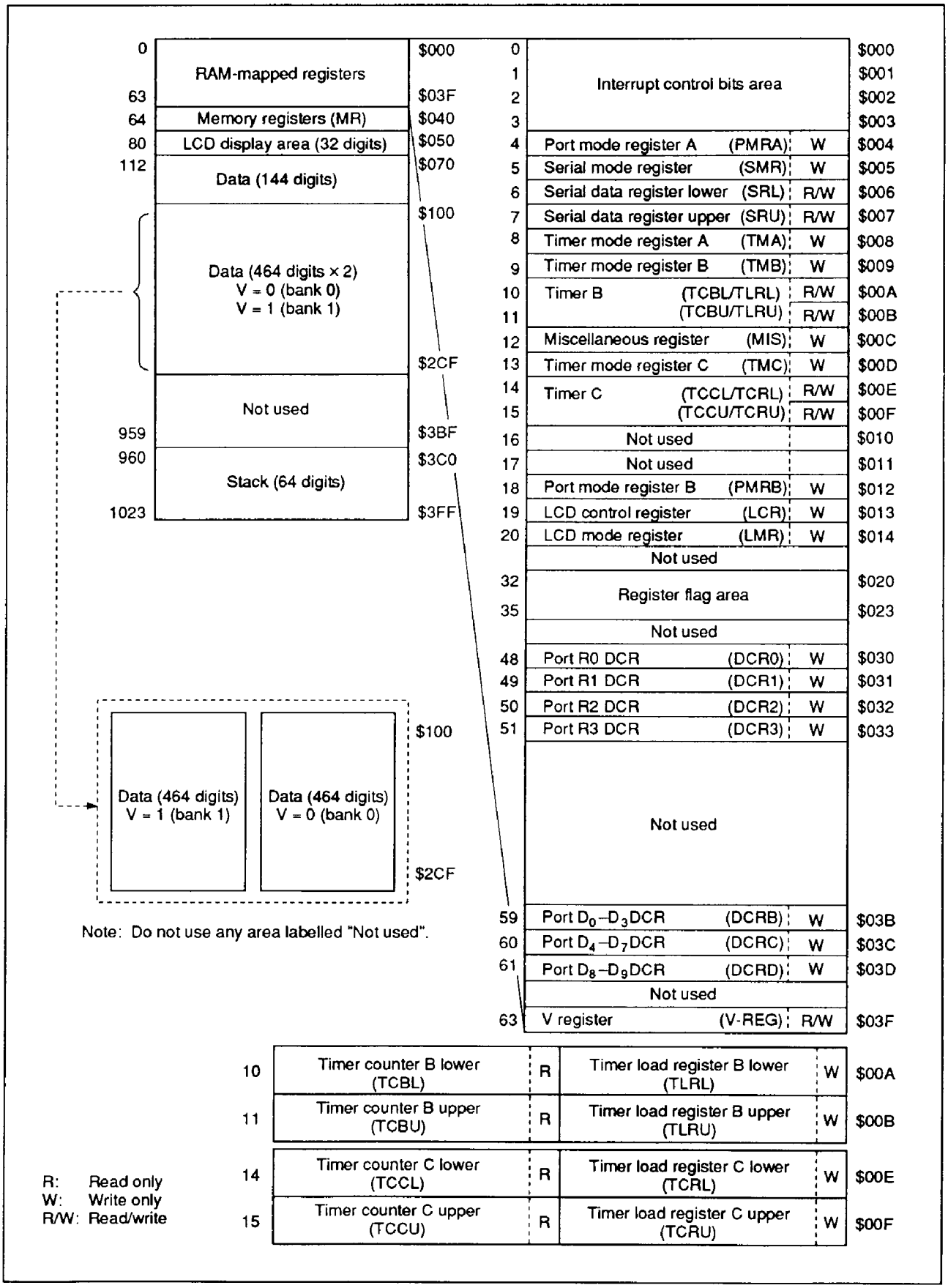


Figure 2 RAM Memory Map

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	IMTC (IM of timer C)	IFTC (IF of timer C)	IMTB (IM of timer B)	IFTB (IF of timer B)	$002
3	Not used	Not used	IMS (IM of serial)	IFS (IF of serial)	$003
32	DTON Direct transfer on flag	Not used	WDON (Watchdog on flag)	LSON (Low speed on flag)	$020
	Reserved				$021 to $023

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Bits in the interrupt control bits area and register flag area are set by the SEM or SEMD instruction, reset by the REM or REMD instruction, and tested by the TM or TMD instruction. Other instructions have no effect.
Note that the interrupt request flag cannot be set by the SEM or SEMD instruction.
If the RSP bit or a non-existent bit is tested by the TM or TMD instruction, its status is undefined.
The WDON flag can only be used by the SEM or SEMD instruction .
(It is reset only by MCU reset).

Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas

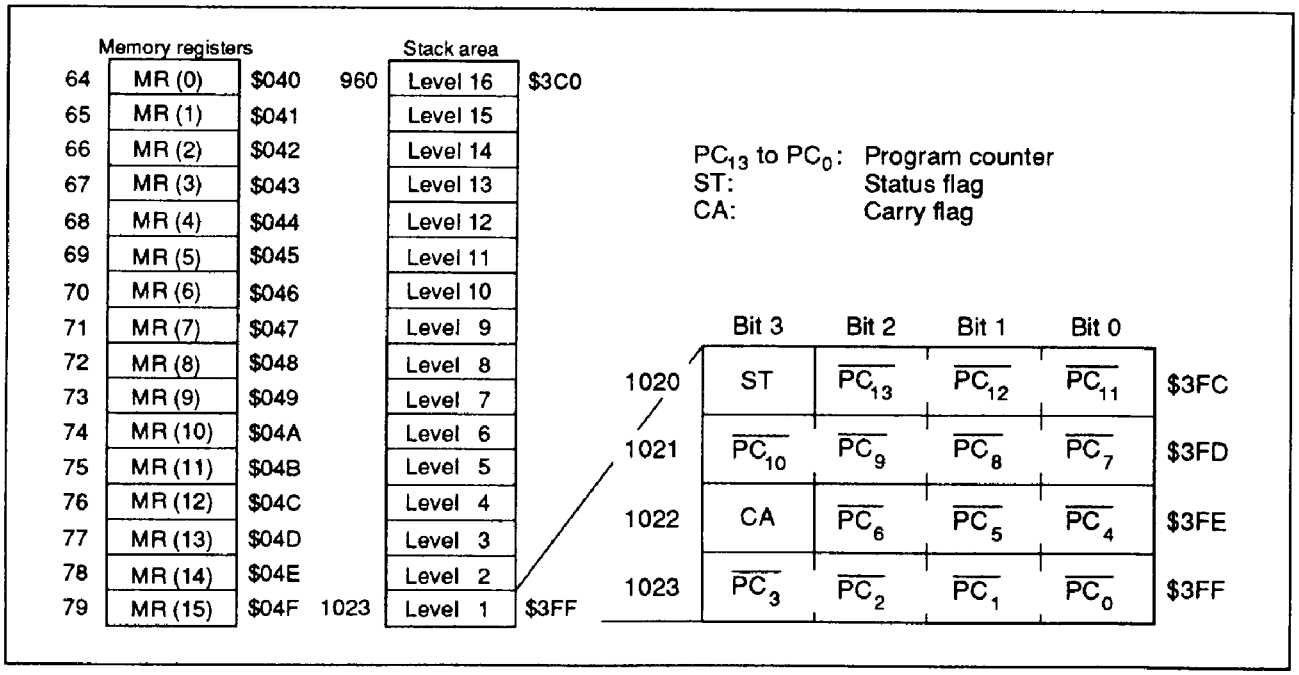


Figure 4 Configuration of Memory Registers, Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU provides ten registers and two flags for CPU operations. They are illustrated in figure 5 and described in the following paragraphs.

Accumulator (A), B Register (B): The accumulator and B register are 4-bit registers which hold the results of the arithmetic logic unit (ALU), and exchange data between memory, I/O, and other registers.

V Register (V): The V register, available for RAM address expansion, selects the bank of locations $100–$2CF on the RAM address (464 digits) depending on its value. Therefore, when accessing locations $100–$2CF on the RAM address, specify the value of the V register (V = $0: bank 0; V = $1: bank 1). Locations $000–$0FF and $300–$3FF can be accessed independently of the V register. The V register is located at $03F of the RAM address area.

W Register (W), X Register (X), Y Register (Y): The 2-bit W register and 4-bit X and Y registers address RAM indirectly. The Y register is also available for addressing port D.

SPX Register (SPX), SPY Register (SPY): The 4-bit SPX and SPY registers are available for assisting the X and Y registers, respectively.

Carry Flag (CA): The carry flag holds the ALU overflow generated by an arithmetic operation. It is also affected by the SEC, REC, ROTL, and ROTR instructions. During an interrupt, the carry flag is pushed onto the stack and restored back from the stack by the RTNI instruction. (It is unaffected by the RTN instruction.)

Status Flag (ST): The status flag holds the ALU overflow, ALU non-zero, and the results of a bit test instruction for arithmetic or compare instructions. The status flag is a branch condition of the BR, BRL, CAL, or CALL instruction. The value of the status flag remains unchanged until an instruction which affects the next status is executed. The status flag becomes a 1 after the BR, BRL, CAL, or CALL instruction is either executed or skipped. During an interrupt, the status flag is pushed onto the stack and restored back from the stack by the RTNI instruction, not by the RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter for holding the ROM address.

Stack Pointer (SP): The stack pointer is a 10-bit register to indicate the next stacking area up to 16 levels. The stack pointer is initialized to RAM address $3FF at MCU reset. It is decremented by 4 as data is pushed onto the stack, and incremented by 4 as data is restored back from the stack. The stack pointer is initialized to $3FF either by MCU reset or by the RSP bit reset from the REM/REMD instruction.

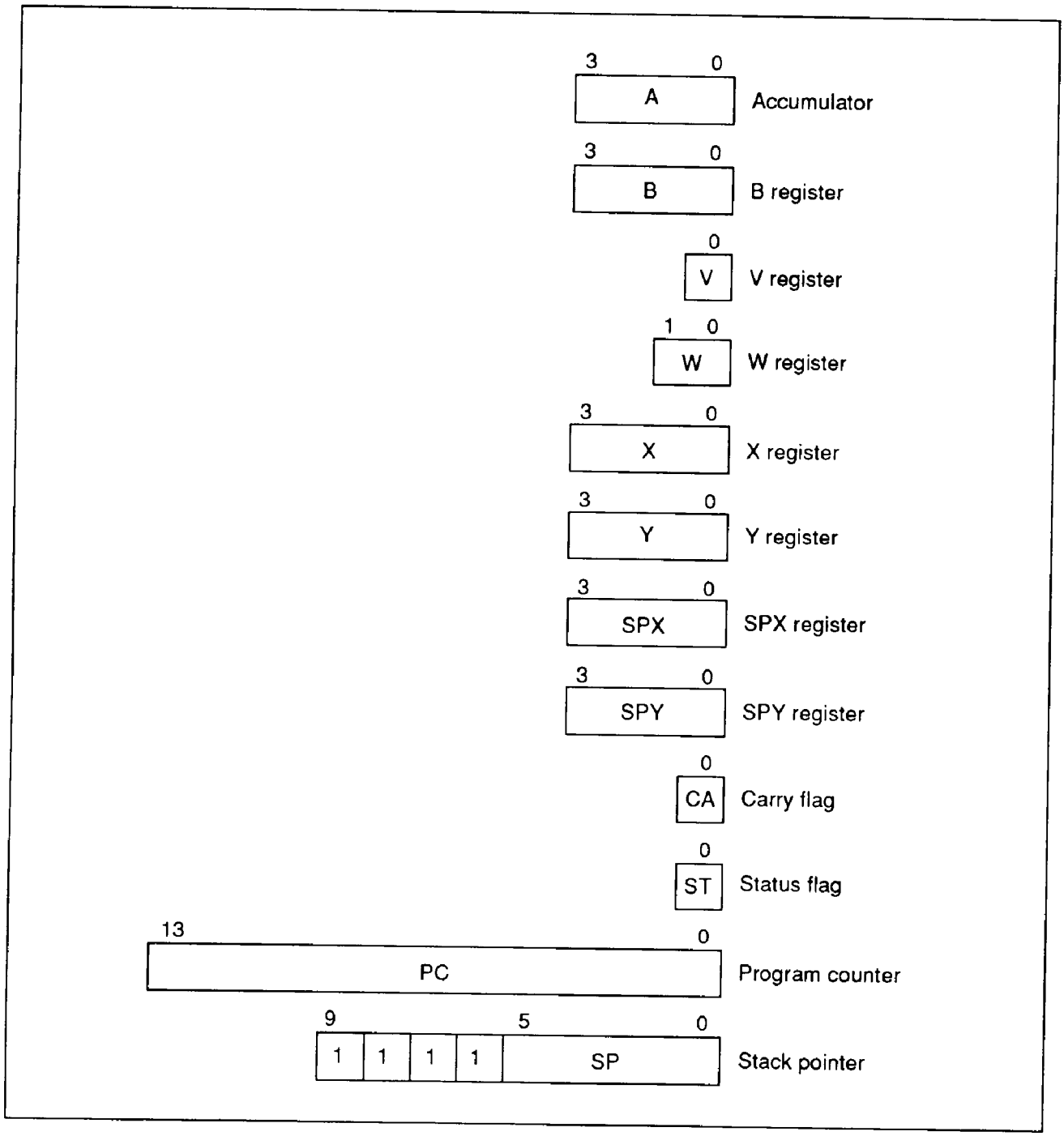


Figure 5 Registers and Flags

Interrupts

Six interrupt sources are available on the MCU: external requests ($\overline{INT_0}$, $\overline{INT_1}$), timer/counters (timers A, B, and C), and the serial interface. For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control interrupt operations.

Interrupt Control Bits and Interrupt Servicing: The interrupt control bits are mapped on $000 through $003 by the RAM space. They are accessible by RAM bit manipulations instructions, although the interrupt request flag (IF) cannot be set by software. The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 after MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

The interrupt request is generated when IF is set to 1 and IM is 0. If IE is 1 at this time, the interrupt will be activated and vector addresses will be

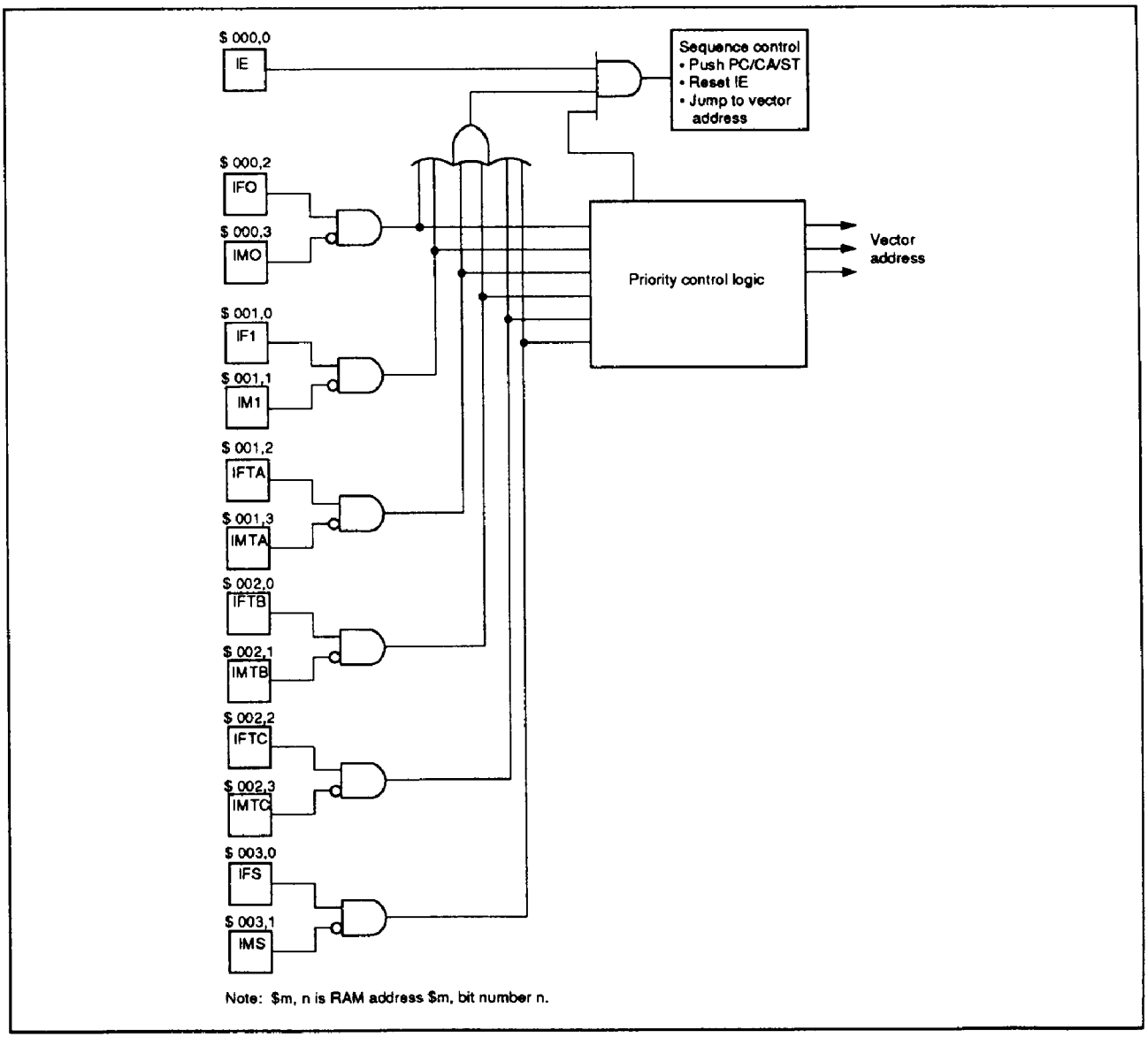


Figure 6 Interrupt Control Circuit Block Diagram

generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt processing sequence, and figure 8 shows the interrupt processing flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry flag, status flag, and program counter are pushed onto the stack. In the third cycle, the instruction is executed after jumping to the vector address.

In each vector address, program the JMPL instruction to branch to the starting address of the interrupt program. The IF, which caused the interrupt, must be reset by software in the interrupt program.

Interrupt Enable Flag (IE: $000, Bit 0): The interrupt enable flag enables/disables interrupt requests (table 3). It is reset by an interrupt and set by the RTNI instruction.

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): The external interrupt request inputs ($\overline{INT_0}$, $\overline{INT_1}$) can be selected by port mode register A (PMRA: $004).

The external interrupt request flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$ and $\overline{INT_1}$ inputs, respectively (table 4).

The $\overline{INT_1}$ input can be used as a clock signal input to timer B, in which timer B counts up at each falling edge of the $\overline{INT_1}$ input. When using $\overline{INT_1}$ as the timer B external event input, the external interrupt mask (IM1) has to be set so that the interrupt request by $\overline{INT_1}$ will not be accepted (table 5).

Table 1 Vector Addresses and Interrupt Priority

Reset/Interrupt	Priority	Vector Addresses
RESET	—	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
Timer C	5	$000A
Serial	6	$000C

Table 2 Interrupt Conditions

	Interrupt Source					
Interrupt Control Bit	$\overline{INT_0}$	$\overline{INT_1}$	Timer A	Timer B	Timer C	Serial
IE	1	1	1	1	1	1
IF0 • $\overline{IM0}$	1	0	0	0	0	0
IF1 • $\overline{IM1}$	*	1	0	0	0	0
IFTA • $\overline{IMTA}$	*	*	1	0	0	0
IFTB • $\overline{IMTB}$	*	*	*	1	0	0
IFTC • $\overline{IMTC}$	*	*	*	*	1	0
IFS • $\overline{IMS}$	*	*	*	*	*	1

Note: *Don't care.

More than two instruction cycle times ($2t_{cyc}/2t_{SUBcyc}$) are needed to detect the edge of $\overline{INT_0}$ or $\overline{INT_1}$.

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the $\overline{INT_0}$ and $\overline{INT_1}$ inputs, respectively (table 4).

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1): The external interrupt masks mask the external interrupt requests (table 5).

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): The timer A interrupt request flag is set by the overflow output of timer A (table 6).

Timer A Interrupt Mask (IMTA: $001, Bit 3): The timer A interrupt mask prevents an interrupt request from being generated by the timer A interrupt request flag (table 7).

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 8).

Timer B Interrupt Mask (IMTB: $002, Bit 1): The timer B interrupt mask prevents an interrupt request from being generated by the timer B interrupt request flag (table 9).

Timer C Interrupt Request Flag (IFTC: $002, Bit 2): The timer C interrupt request flag is set by the overflow output of timer C (table 10).

Timer C Interrupt Mask (IMTC: $002, Bit 3): The timer C interrupt mask prevents the interrupt from being generated by the timer C interrupt request flag (table 11).

Serial Interrupt Request Flag (IFS: $003, Bit 0): The serial interrupt request flag will be set when the octal counter counts eight transmit clock signals, or when data transfer is discontinued by resetting the octal counter (table 12).

Serial Interrupt Mask (IMS: $003, Bit 1): The serial interrupt mask masks the interrupt request (table 13).

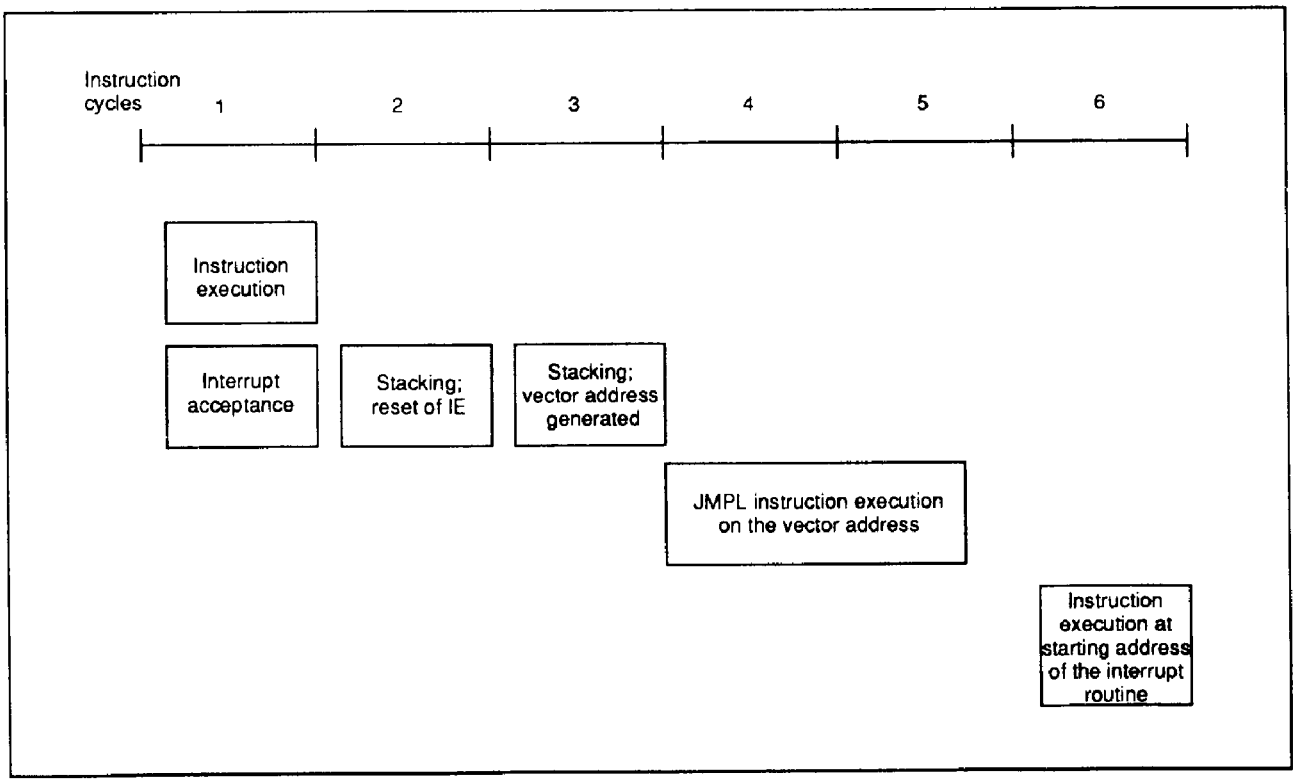


Figure 7 Interrupt Processing Sequence

Table 3 Interrupt Enable Flag

IE	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4 External Interrupt Request Flags

IF0, IF1	Interrupt Request
0	No
1	Yes

Table 5 External Interrupt Masks

IM0, IM1	Interrupt Request
0	Enable
1	Disable (Mask)

Table 6 Timer A Interrupt Request Flag

IFTA	Interrupt Request
0	No
1	Yes

Table 7 Timer A Interrupt Mask

IMTA	Interrupt Request
0	Enable
1	Disable (Mask)

Table 8 Timer B Interrupt Request Flag

IFTB	Interrupt Request
0	No
1	Yes

Table 9 Timer B Interrupt Mask

IMTB	Interrupt Request
0	Enable
1	Disable (Mask)

Table 10 Timer C Interrupt Request Flag

IFTC	Interrupt Request
0	No
1	Yes

Table 11 Timer C Interrupt Mask

IMTC	Interrupt Request
0	Enable
1	Disable (Mask)

Table 12 Serial Interrupt Request Flag

IFS	Interrupt Request
0	No
1	Yes

Table 13 Serial Interrupt Mask

IMS	Interrupt Request
0	Enable
1	Disable (Mask)

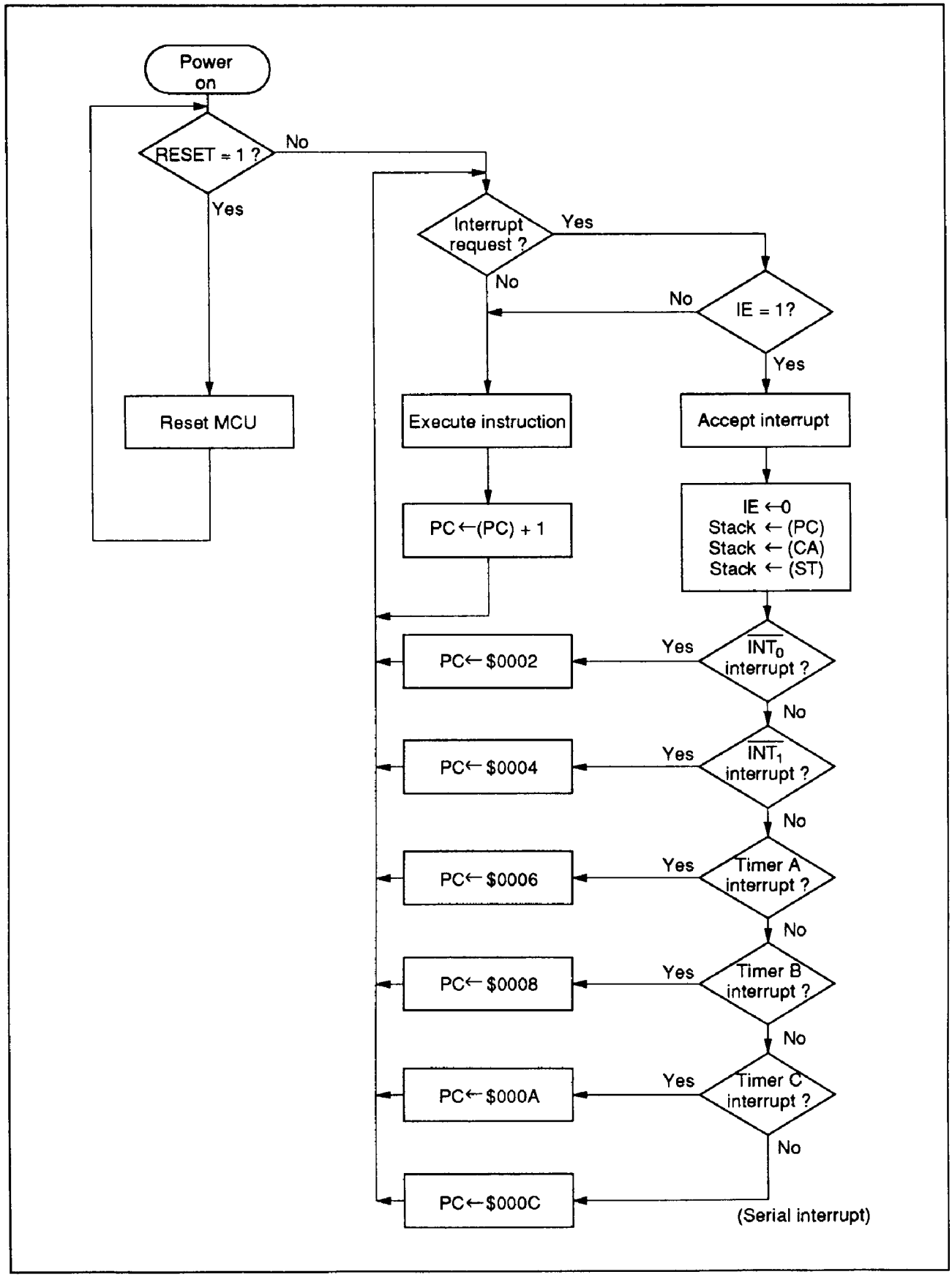


Figure 8 Interrupt Processing Flowchart

Serial Interface

The serial interface transmits/receives 8-bit data serially. It consists of the serial data register, the serial mode register, port mode register A, the octal counter, and the multiplexer (figure 9). Pin $R0_0/\overline{SCK}$ and the transmit clock signal are controlled by the serial mode register. The data of the serial data register can be written in or read out by software. The data in the serial data register can be shifted synchronously with the transmit clock signal.

The STS instruction starts serial interface operations and resets the octal counter to $0. The octal counter starts to count at the falling edge of the transmit clock signal ($\overline{SCK}$) and increments by one at the rising edge of the $\overline{SCK}$. When the octal counter is reset to $0 after eight transmit clock signals, or when a transmit/receive operation is discontinued by resetting the octal counter, the serial interrupt request flag will be set.

Serial Mode Register (SMR: $005): The 4-bit write-only serial mode register controls the $R0_0/\overline{SCK}$, prescaler divide ratio, and transmit clock source (table 14).

The write signal to the serial mode register controls the internal state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from applying the transmit clock, and it also resets the octal counter to $0 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transfer and to set the serial interrupt request flag.

Data of the serial mode register will be changed at the second instruction after a write instruction to the serial mode register. Therefore, it is required to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register will be reset to $0 by MCU reset.

Serial Data Register (SRL: $006, SRU: $007): The 8-bit read/write serial data register consists of low-order digits (SRL: $006) and high-order digits (SRU: $007).

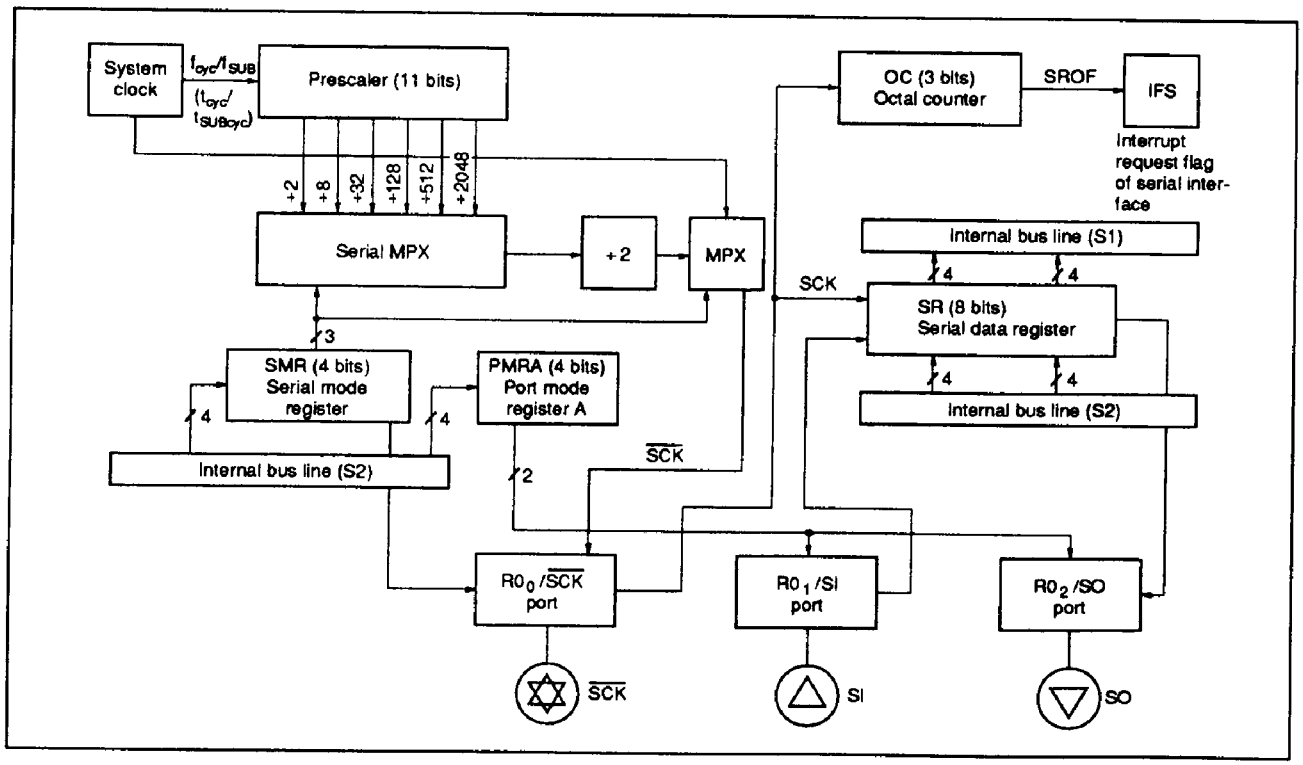


Figure 9 Serial Interface Block Diagram

The data in the serial data register will be output from the SO pin LSB first synchronously with the falling edge of the transmit clock signal. At the same time, external data will be input from the SI pin to the serial data register synchronously with the rising edge of the transmit clock. Figure 11 shows the I/O timing chart for the transmit clock signal and the data.

The read/write operation of the serial data register should be performed after the completion of data transmit/receive. Otherwise, the data may not be guaranteed.

Selection and Change of the Operation Mode: Table 15 shows the serial interface operation modes which are determined by a combination of the value in the port mode register and in the serial mode register.

Initialize the serial interface by the write signal to the serial mode register in order to change the operation mode of the serial interface.

Operating State of Serial Interface: The serial interface has three operating states: the STS waiting state, transmit clock wait state, and transfer state (figure 12).

The STS waiting state is the initialization state of the serial interface internal state. The serial interface enters this state in one of two ways: either by changing the operation mode through a change in the data in the port mode register, or by writing data into the serial mode register. In this state, the serial interface does not operate even if the transmit clock is applied. If the STS instruction is executed then, the serial interface shifts to the transmit clock wait state.

Table 14 Serial Mode Register

SMR3	$R0_0/\overline{SCK}$
0	Used as $R0_0$ port input/output pin
1	Used as $\overline{SCK}$ input/output pin

				Transmit Clock		
SMR2	SMR1	SMR0	$R0_0/\overline{SCK}$ Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	$\overline{SCK}$/output	Prescaler	÷ 2048	÷ 4096
0	0	1	$\overline{SCK}$/output	Prescaler	÷ 512	÷ 1024
0	1	0	$\overline{SCK}$/output	Prescaler	÷ 128	÷ 256
0	1	1	$\overline{SCK}$/output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$/output	Prescaler	÷ 8	÷ 16
1	0	1	$\overline{SCK}$/output	Prescaler	÷ 2	÷ 4
1	1	0	$\overline{SCK}$/output	System clock		÷ 1
1	1	1	$\overline{SCK}$/input	External clock		

In the transmit clock wait state, the falling edge of the first transmit clock causes the serial interface to shift to the transfer state, while the octal counter counts up and the serial data register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in transmit clock wait state while the transmit clock outputs continuously. The octal counter becomes 000 again after 8 external transmit clocks or by the execution of the STS instruction, so that the serial interface returns to the transmit clock wait state, and the serial interrupt request flag is set simultaneously. In the transfer state the octal counter becomes 000 after 8 internal transmit clocks, so that the serial interface enters the STS instruction waiting state, and the serial interrupt request flag is set simultaneously.

When the internal transmit clock is selected, the transmit clock output is triggered by the execution of the STS instruction, and stops after 8 clocks.

Table 15 Serial Interface Operation Mode

SMR3	PMRA1	PMRA0	Serial Interface Operating Mode
1	0	0	Clock continuous output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/receive mode

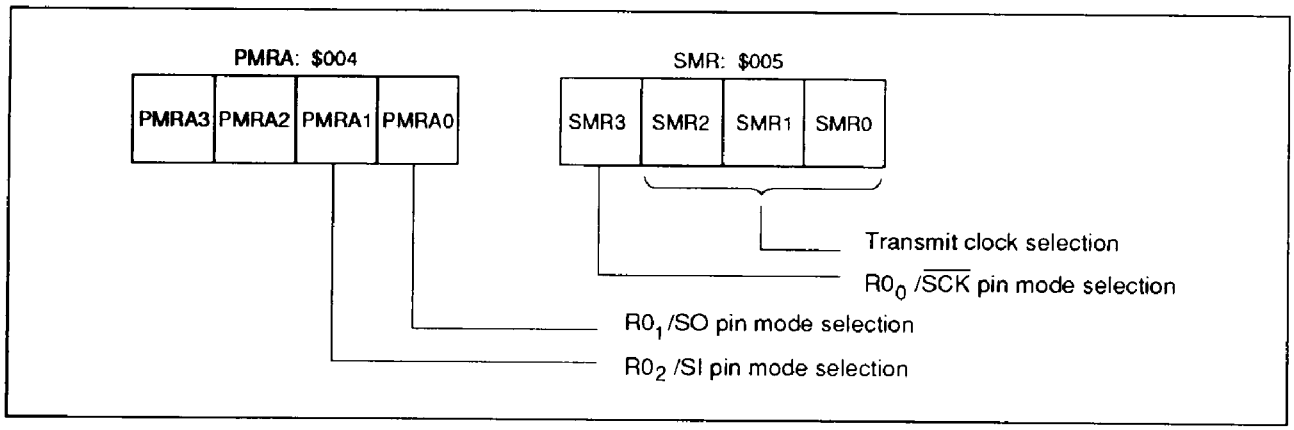


Figure 10 Configurations and the Functions of the Mode Registers

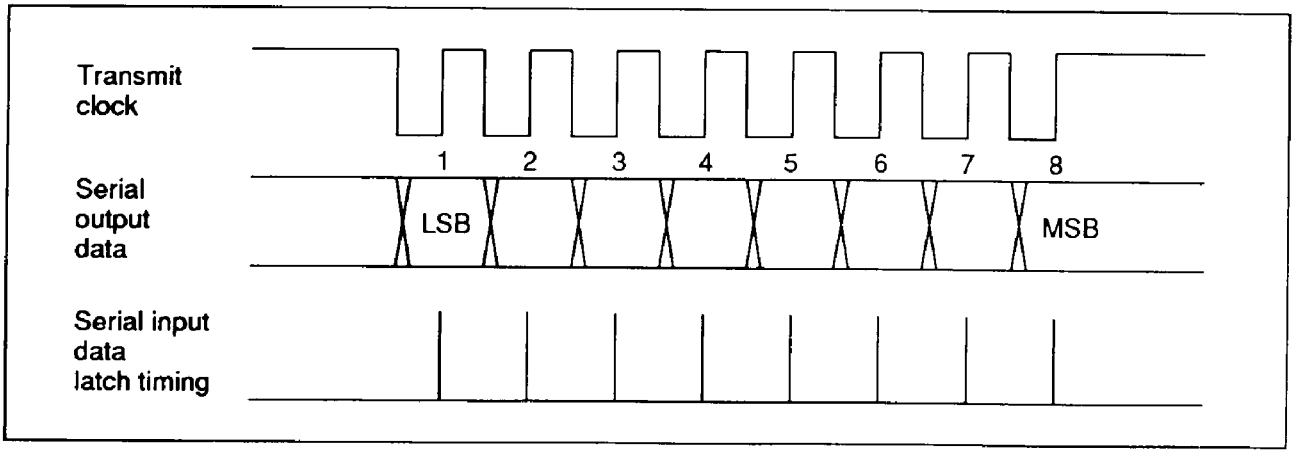


Figure 11 Serial Interface I/O Timing

Program the SMR again to initialize the internal state of the serial interface when the PMRA is programmed in the transfer state or in the transmit clock wait state. Then the serial interface goes into the STS waiting state.

Example of Transmit Clock Error Detection: The serial interface malfunctions when the transmit clock is disturbed by external noise. In this case, transmit clock errors can be detected by the procedure shown in figure 13.

If more than 8 transmit clocks are applied in the transmit clock wait state, the state of the serial interface shifts in the following sequence: transfer state, transmit clock wait state, and transfer state again. The serial interrupt request flag should be reset before entering into the STS waiting state by writing data to SMR. This procedure causes the serial interface request flag to be set again.

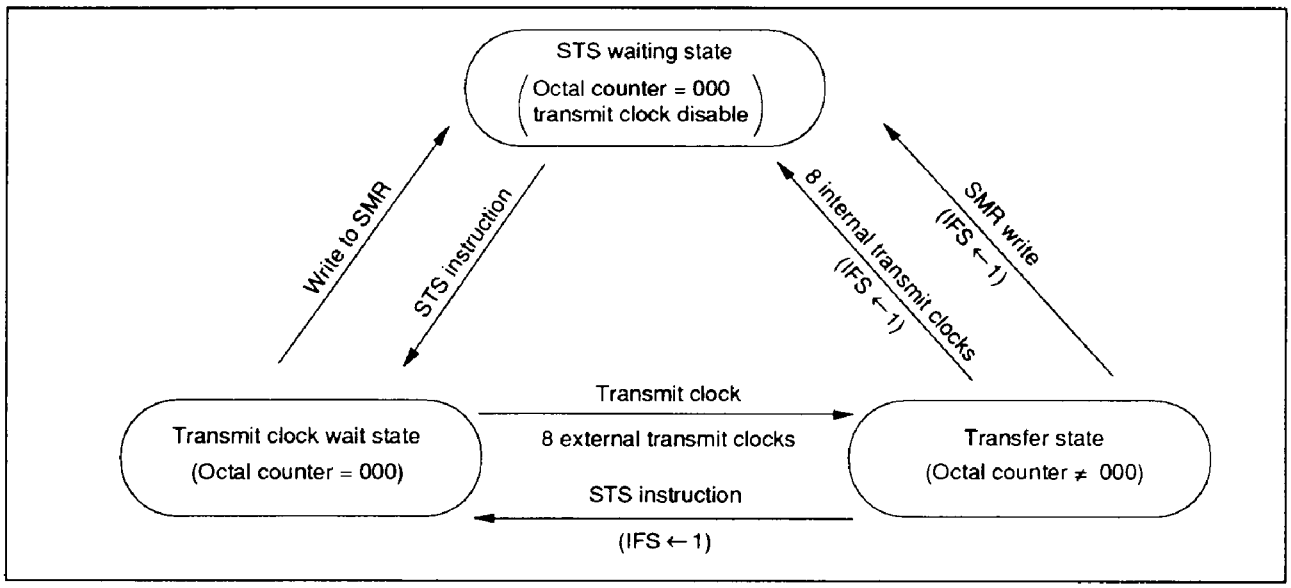


Figure 12 Serial Interface Operation States

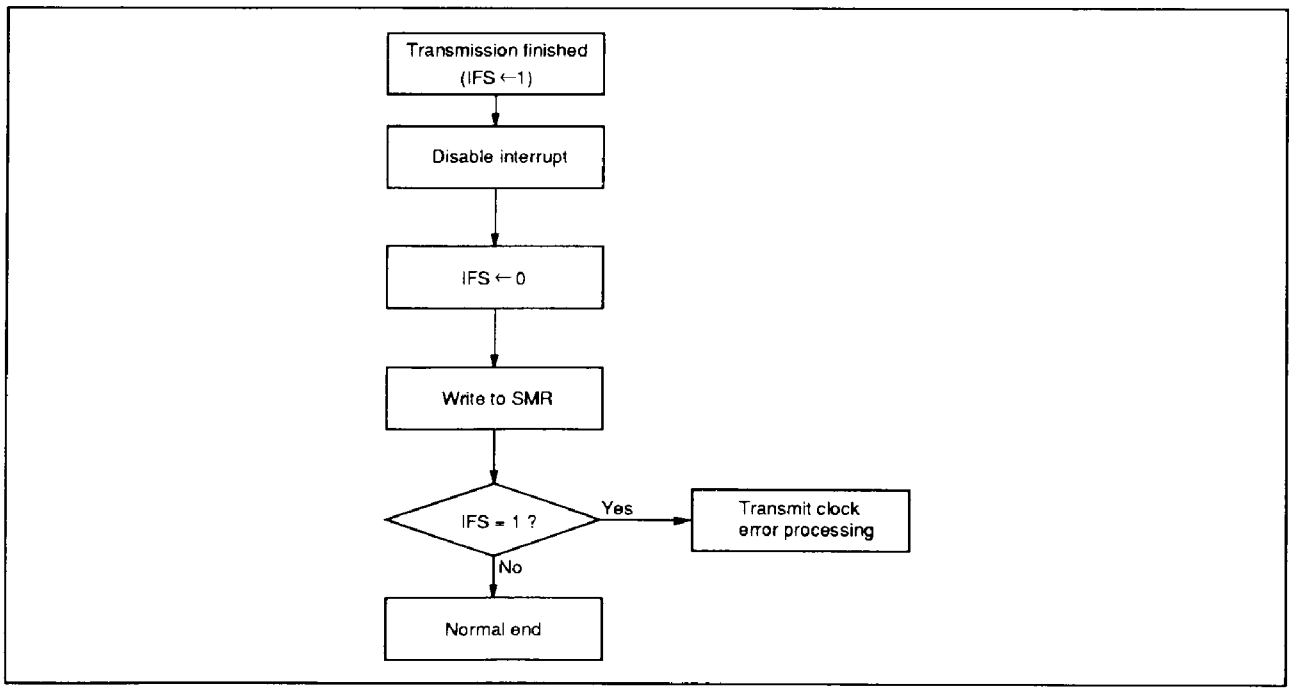


Figure 13 Transmit Clock Error Detection

Timers

The MCU provides prescalers S and W (each with a different input clock source), and 3 timer/counters (timers A, B, and C). Figures 14 and 15 show their diagrams.

Prescaler S: The input to prescaler S is the system clock signal. The prescaler is initialized to $000 by MCU reset, and starts to count up the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except at MCU reset and in the stop and watch modes. The prescaler provides input clock signals to timers A to C and the transmit clock of the serial interface. They can be selected by timer mode registers A (TMA), B (TMB), C (TMC), and the serial mode register (SMR), respectively.

Prescaler W: The input to prescaler W is a clock which divides the X1 input clock by 8. The output of prescaler W is available as an input clock for timer A by controlling timer mode register A (TMA).

Timer A Operation: After timer A is initialized to $00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after timer A has counted up to $FF, timer A is set to $00 again, and an overflow output is generated. This leads to setting the timer A interrupt request flag (IFTA: $001, bit 2) to 1. Therefore, timer A can function as an interval timer periodically generating overflow output at every 256th clock signal input.

To use timer A as a watch time base, set TMA3 to 1. Timer counter A receives prescaler W output, and timer A generates interrupts with accurate timing (reference clock = 32-kHz crystal oscillator). When using timer A as a watch time base, prescaler W and the timer counter can be initialized to $0 by setting timer mode register A.

The clock input signals to timer A are selected by timer mode register A (TMA: $008).

Timer B Operation: Timer mode register B (TMB: $009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select $R3_3/\overline{INT_1}$ as $\overline{INT_1}$ by port mode register A (PMRA: $004) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into timer load register B by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set

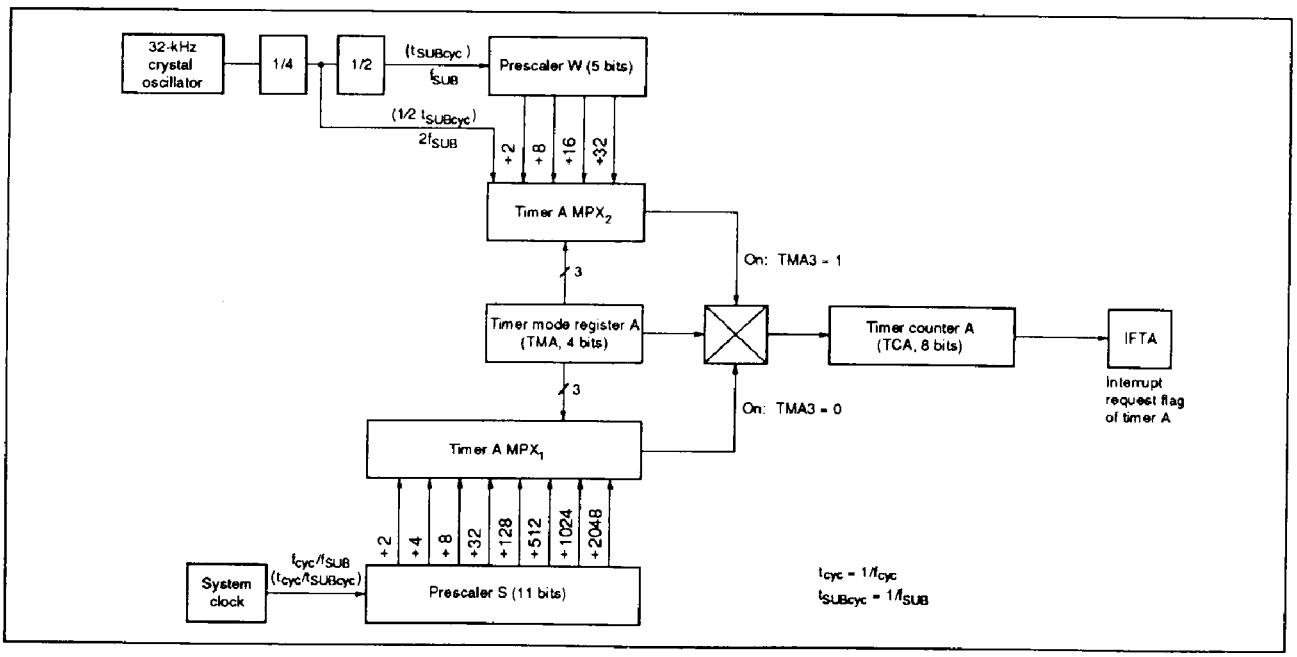


Figure 14 Block Diagram of Timer A

to $FF, it will generate an overflow output. In this case, if the auto-reload function is selected, timer B is initialized according to the value of timer load register B. If it is not selected, timer B goes to $00. The timer B interrupt request flag (IFTB: $002, bit 0) will be set as this overflow is output.

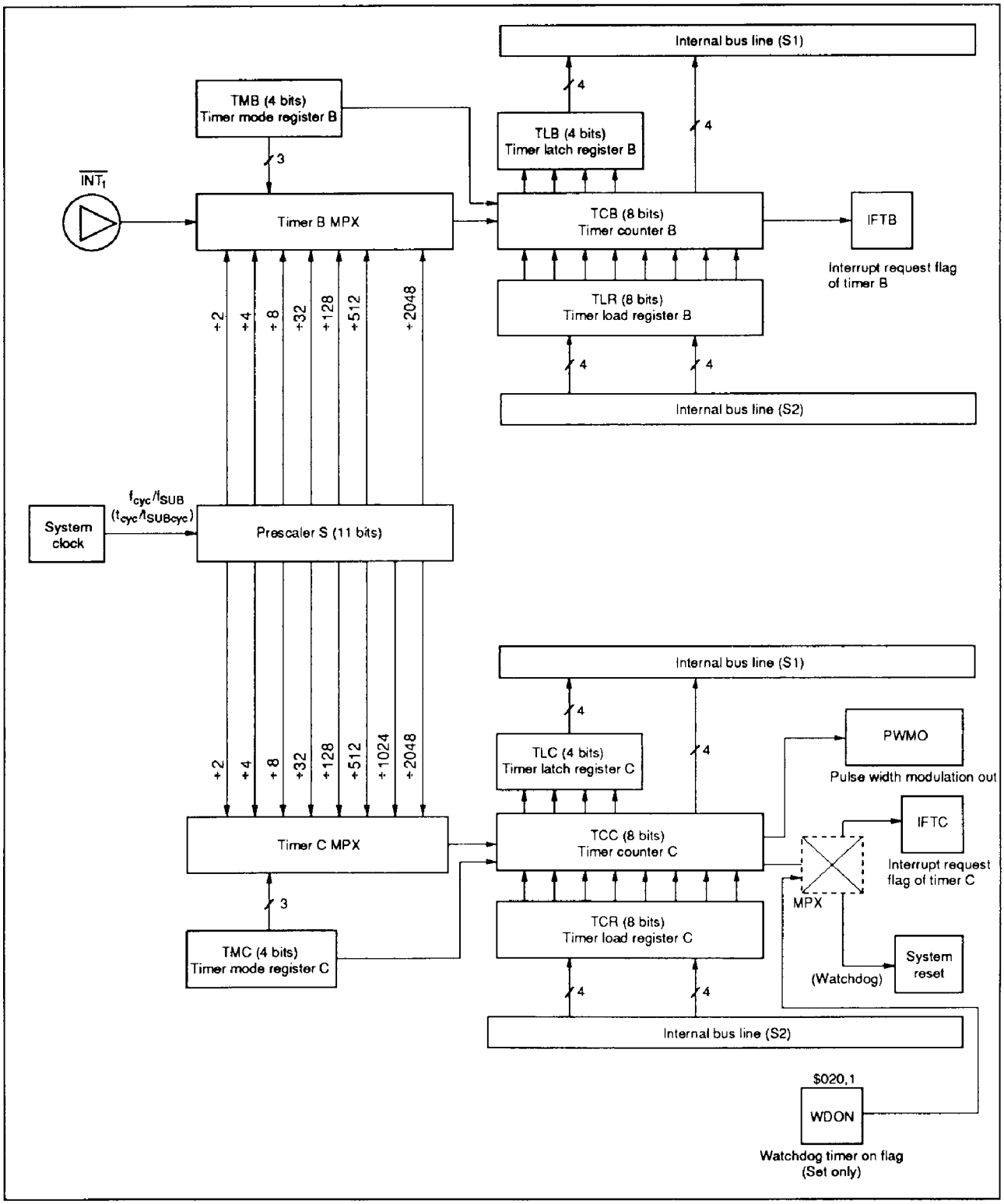


Figure 15 Timers B and C Block Diagram

Timer C Operation: Timer mode register C (TMC: $00D) selects the auto-reload function and the prescaler divide ratio for timer C.

Timer C is initialized according to the data written into timer load register C by software. Timer C counts up at every clock input signal. When the next clock signal is applied to timer C after it is set to $FF, it will generate an overflow output. In this case, if the auto-reload function is selected, timer C is initialized according to the value of timer load register C. If it is not selected, timer C goes to $00. The timer C interrupt request flag (IFTC: $002, bit 2) will be set as this overflow is output.

Timer C is also available as a watchdog timer for detecting a program out of sequence. MCU reset occurs when the watchdog on flag (WDON) is 1 and the counter overflow output is generated by the program going out of sequence. If timer C stops, the watchdog timer function also stops. In the standby mode, this function is enabled.

Timer C provides a variable duty-cycle pulse output function (PWMO). The output waveform differs depending on the contents of the timer mode register and timer load register C (figure 16). When selecting the pulse output function, set $R3_1$/TIMO to TIMO by controlling port mode register B.

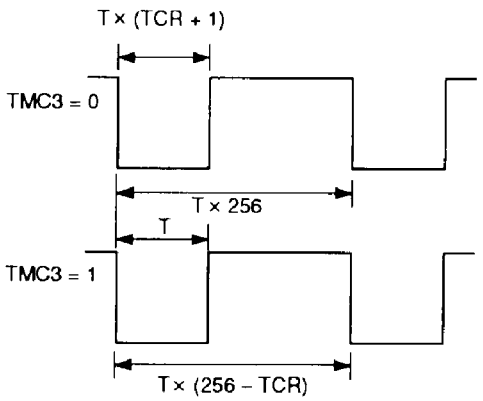
When timer C stops, this functions also stops.

Timer Mode Register A (TMA: $008): Timer mode register A is a 4-bit write-only register which controls the timer A operation as table 16 shows. Timer mode register A is initialized to $0 at MCU reset.

Timer Mode Register B (TMB: $009): Timer mode register B (TMB) is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 17. Timer mode register B is initialized to $0 by MCU reset.

The data of timer B changes at the second instruction cycle of a write instruction. Initialization of timer B by writing data into timer load register B should be performed after the contents of TMB are changed.

Timer Mode Register C (TMC: $00D): Timer mode register C is a 4-bit write-only register which selects the auto-reload function, input clock source, and prescaler divide ratio, as table 18 shows. Timer mode register C is initialized to $0 at MCU reset.



T: Input clock period to counter (see table 18)
TCR: The value of the timer load register

Note: When TCR = $FF, this waveform is always fixed low.

Figure 16 Variable Duty-Cycle Pulse Output Waveform

Table 16 Timer Mode Register A

TMA				Source Prescaler, Input Clock Period, Operating Mode	
Bit 3	Bit 2	Bit 1	Bit 0		
0	0	0	0	PSS, 2048 t_{cyc}	Timer A mode
			1	PSS, 1024 t_{cyc}	
		1	0	PSS, 512 t_{cyc}	
			1	PSS, 128 t_{cyc}	
	1	0	0	PSS, 32 t_{cyc}	
			1	PSS, 8 t_{cyc}	
		1	0	PSS, 4 t_{cyc}	
			1	PSS, 2 t_{cyc}	
1	0	0	0	PSW, 32 t_{SUBcyc}	Time-base mode
			1	PSW, 16 t_{SUBcyc}	
		1	0	PSW, 8 t_{SUBcyc}	
			1	PSW, 2 t_{SUBcyc}	
	1	0	0	PSW, 1/2 t_{SUBcyc}	
			1	Do not use	
		1	0	PSW, TCA reset	
			1		

Notes: 1. t_{SUBcyc} = 244.14 µs (when a 32.768-kHz crystal oscillator is used)
2. Timer counter overflow output period (s) = input clock period (s) × 256
3. If PSW or TCA reset is selected while the LCD is operating, LCD operation halts (power switch goes off).
   When the LCD is connected for display, the PSW and TCA reset periods must be set in the program to the minimum.
4. In time base mode, the timer counter overflow output cycle must be greater than half of the interrupt frame period (T/2 = t_{RC}).
   If 1/2 t_{SUBcyc} is selected, t_{RC} must be 7.8125 ms ((MIS1, MIS0) = (0, 1), see figure 34).

The contents of timer mode register C can be changed at the second instruction cycle of a write instruction. Therefore, it is required to initialize timer C after the contents of timer mode register C have been changed completely.

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit read-only timer counter. Each of them has low-order digits (TCBL: $00A, TLRL: $00A) and high-order digits (TCBU: $00B, TLRU: $00B). (Refer to figure 15.)

Timer counter B can be initialized by writing data into timer load register B. In this case, write the low-order digits first, and then the high-order digits. The timer counter is initialized when the high-order digit is written. The timer load register is initialized to $00 by MCU reset.

The counter value of timer B can be obtained by reading timer counter B. In this case, read the high-order digits first, and then the low-order digits. The count value of the low-order digit is obtained when the high-order digit is read.

Timer C (TCCL: $00E, TCCU: $00F, TCRL: $00E, TCRU: $00F): Timer C consists of the 8-bit write-only timer load register and the 8-bit read-only timer counter. These individually consist of low-order digits (TCCL: $00E, TCRL: $00E) and high-order digits (TCCU: $00F, TCRU: $00F). The operation mode of timer C is the same as that of timer B.

Table 17 Timer Mode Register B

TMB3	Auto-Reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{INT_1}$ (External event input)

Table 18 Timer Mode Register C

TMC3	Auto-Reload Function
0	No
1	Yes

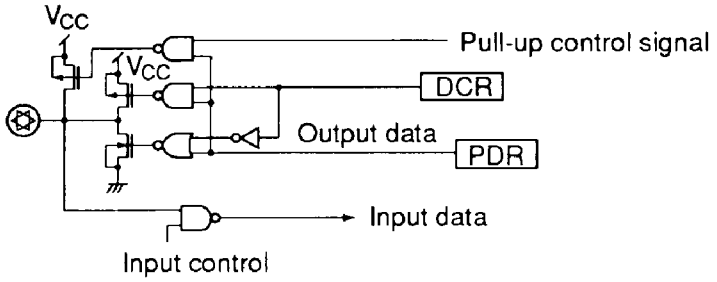
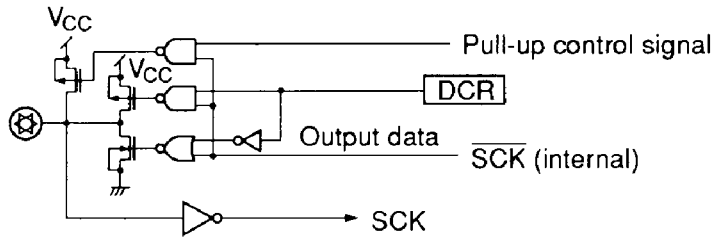
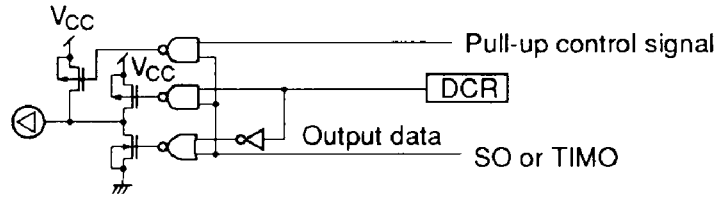
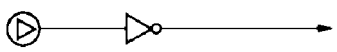
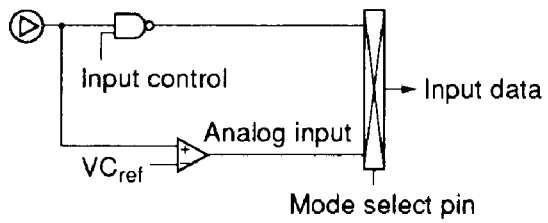
TMC2	TMC1	TMC0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Input/Output

The MCU provides 26 I/O pins and 4 input-only pins including 10 high-current pins (15 mA max.). 26 I/O pins contain pull-up MOS controllable by the program. When each I/O pin is used as an input, the data control register (DCR) controls the output buffer. Table 19 shows the I/O pin circuit types.

The configuration of the I/O buffers are shown in table 19.

Table 19 I/O Pin Circuit Types

I/O Pins	Circuit	Pin Name
I/O common pins (with pull-up MOS)		D_0–D_9 $R0_0$–$R0_3$ $R1_0$–$R1_3$ $R2_0$–$R2_3$ $R3_0$–$R3_3$
		$\overline{SCK}$
Output pins (with pull-up MOS)		SO TIMO
Input pins		$\overline{INT_0}$ $\overline{INT_1}$ SI
		D_{10} D_{11}/VC_{ref}
		D_{12}/COMP0 D_{13}/COMP1 (Multiplexed with analog inputs)

Note: For $R0_2$/SO, refer to table 20, note 3.

Port D: Port D consists of 10 1-bit I/O ports and 4 input ports. Pins D_0 to D_9 are high-current I/O pins (15 mA max.). The sum of the current for all D-port pins is up to 100 mA. Port D can be set/reset by the SED/RED and SEDD/REDD instructions, and can be tested by the TD/TDD instruction. Output data is stored in the port data register. The on/off of the output buffer for port D can be controlled by the data control register for port D (DCRB, DCRC, DCRD). The DCR is located in the memory address area. Pins D_{10} to D_{13} are input-only pins.

Two operation modes are available for pins D_{12} and D_{13}: digital input mode and analog input mode. The operation modes can be selected by port mode register B (PMRB; bits 1, 0). In the digital input mode, these pins can be used as input with the same characteristics as other I/O pins. In the analog input mode, users can read the result of the comparison between the reference voltage as input data. The reference voltage is input through D_{11}/VC_{ref}.

Port R: Port R, consisting of four 4-bit I/O ports, can receive/transmit data by the LAR/LRA and LBR/LRB instructions. Output data is stored in the port data register (PDR) of each pin.

The on/off of the output buffer for port R can be controlled by the data control registers for port R (DCR0–DCR3).

The DCR is located in the memory address area.

Pins $R0_0$, $R0_1$, and $R0_2$ are multiplexed with $\overline{SCK}$, SI, and SO, respectively.

Pins $R3_1$, $R3_2$, and $R3_3$ are multiplexed with TIMO, $\overline{INT_0}$, and $\overline{INT_1}$, respectively. Refer to figure 18.

Controlling the Pull-Up MOS: All I/O ports, except for pins D_{10}–D_{13}, contain pull-up MOS which can be controlled by the program.

Bit 3 of port mode register B (PMRB3) controls the activation of all pull-up MOS simultaneously. Pull-up MOS is controlled by the port data register (PDR) of each pin. Therefore, each bit of pull-up MOS can be individually on or off. Refer to table 20.

Unused I/O Pins: If unused pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent this: pull-up with V_{CC} through internal pull-up MOS, or pull-up with V_{CC} through a resistor of approximately 100 kΩ.

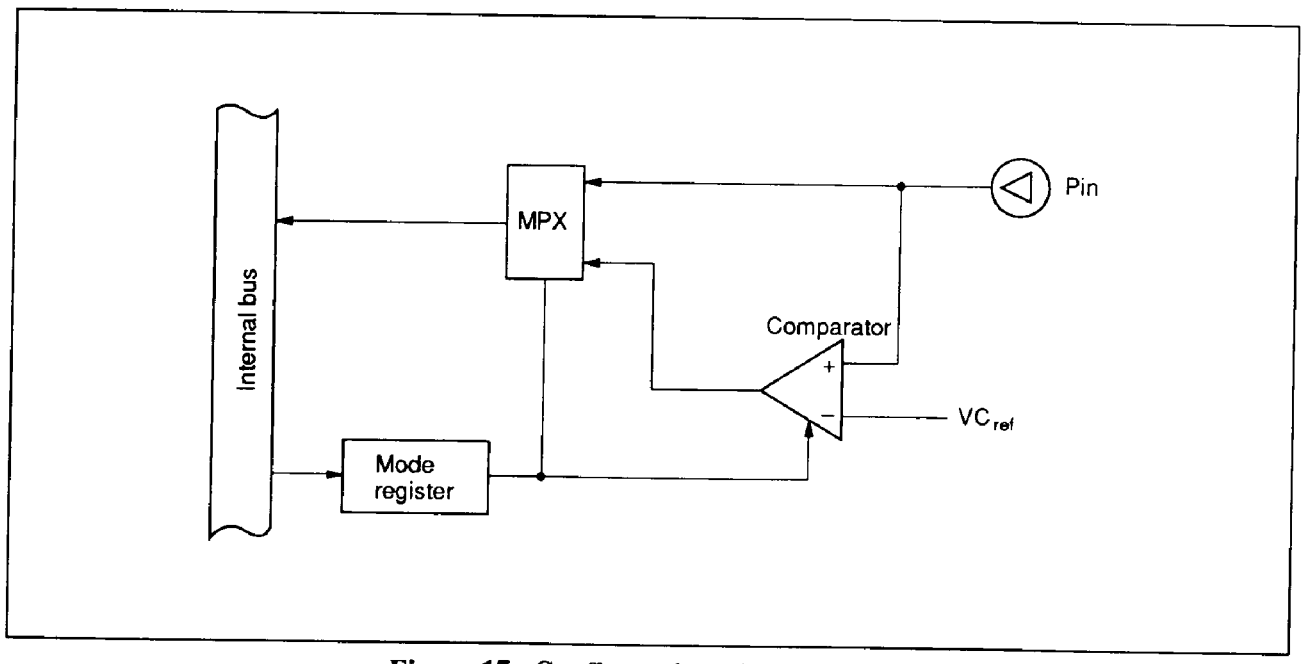
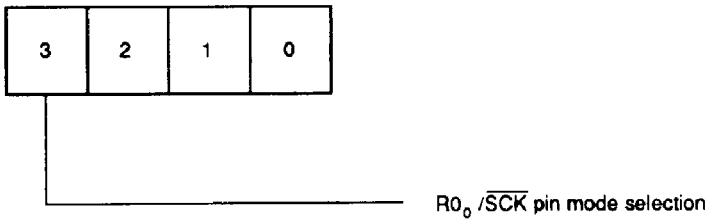
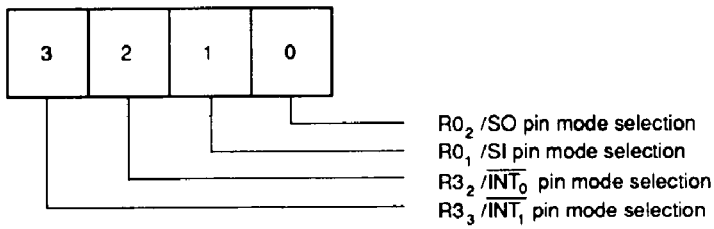


Figure 17 Configuration of D_{12} and D_{13}

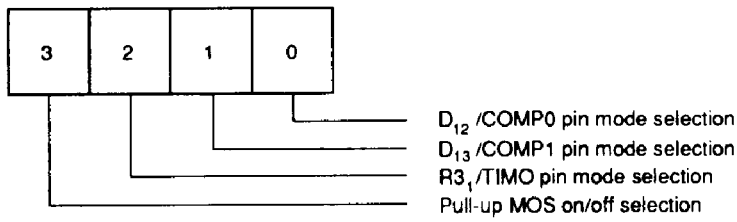
SMR (Serial mode register) ADR: $005



PMRA (Port mode register A) ADR: $004



PMRB (Port mode register B) ADR: $012



SMR Bit 3	Port select
0	R0$_0$
1	$\overline{SCK}$

PMRA Bit 3	Port select	PMRA Bit 2	Port select	PMRA Bit 1	Port select	PMRA Bit 0	Port select
0	R3$_3$	0	R3$_1$	0	R0$_1$	0	R0$_2$
1	$\overline{INT_1}$	1	$\overline{INT_0}$	1	SI	1	SO

PMRB Bit 3	Pull-up MOS on/off	PMRB Bit 2	Port select	PMRB Bit 1	Port select	PMRB Bit 0	Port select
0	Off	0	R3$_1$	0	D$_{13}$	0	D$_{12}$
1	On	1	TIMO	1	COMP1	1	COMP0

Figure 18 I/O Select Mode Registers

Table 20 Input/Output by Program Control

PRMB: Bit 3	0				1			
DCR	0		1		0		1	
PDR	0	1	0	1	0	1	0	1
PMOS (A)	Off	Off	Off	On	Off	Off	Off	On
NMOS (B)	Off	Off	On	Off	Off	Off	On	Off
Pull-up MOS	Off	Off	Off	Off	Off	On	Off	On

Notes: 1. Combine the values of the above mode registers (PMRB3, DCR, and PDR) to select the input/output for PMOS (A), NMOS (B), and the pull-up MOS, individually.
The DCR and PDR control each pin. Also, the PMRB3 controls the on/off of all pull-up MOSs.

2. The second bit of the miscellaneous register (MIS2) controls $R0_2$/SO. When MIS2 is 1, PMOS (A) is off.

MIS2	$R0_2$/SO PMOS (A)
0	On
1	Off

3. Each bit of DCR corresponds to each port as follows:

DCR	Bit 3	Bit 2	Bit 1	Bit 0
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_2$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCRB	D_3	D_2	D_1	D_0
DCRC	D_7	D_6	D_5	D_4
DCRD	—	—	D_9	D_8

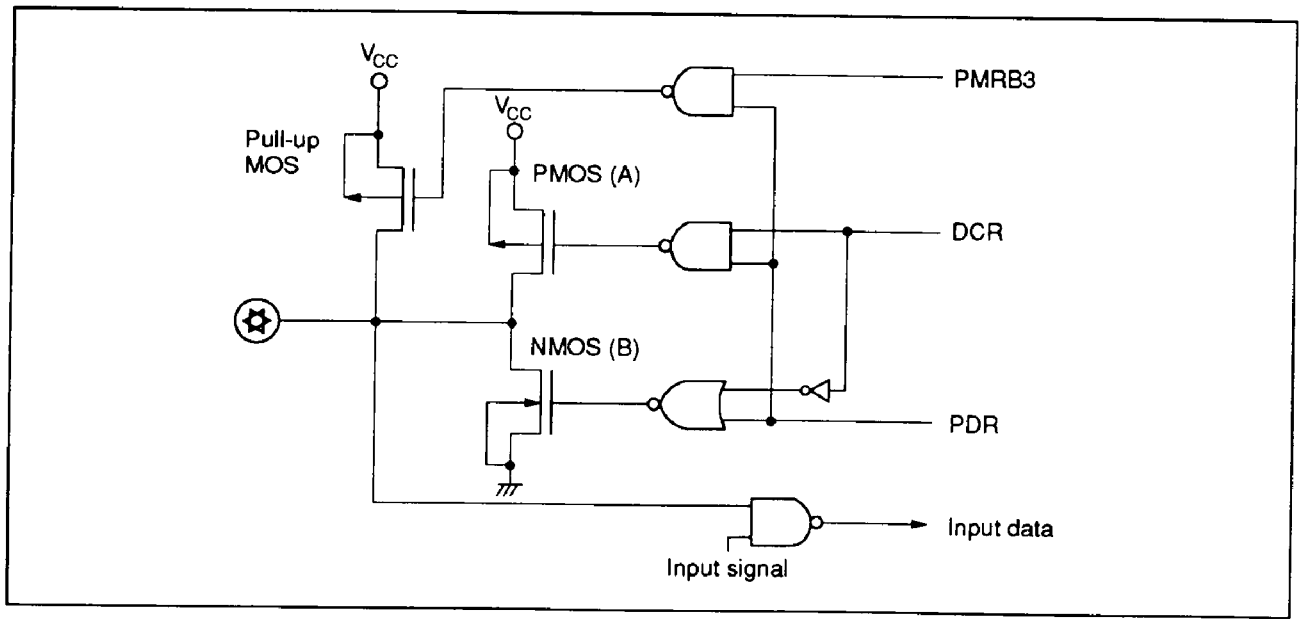


Figure 19 Configuration of the Input/Output Buffer

Reset

Setting the RESET pin high resets the MCU. At power-on or when cancelling the stop mode for the oscillator, apply the reset input for at least t_{RC} for the oscillator to stabilize. In all other cases, at least two instruction cycles of reset input are required for the MCU reset.

Table 21 shows the components initialized by MCU reset, and each of its status.

Table 21 Initial Values after MCU Reset

Items		Initial Value	Contents
Program counter (PC)		$0000	Execute program from the top of the ROM address
Status flag (ST)		1	Enable branching with conditional branch instructions
Stack pointer (SP)		$3FF	Stack level is 0
V register (Bank register) (V)		0	Bank 0 (memory)
Interrupt flags/mask	Interrupt enable flag (IE)	0	Inhibit all interrupts
	Interrupt request flag (IF)	0	No interrupt request
	Interrupt mask (IM)	1	Masks interrupt request
I/O	Port data register (PDR)	All bits are 1	Enable to transmit high
	Data control register (DCR)	All bits are 0	Output buffer is off (high impedance)
	Port mode register A (PMRA)	0000	See Port Mode Register A section
	Port mode register B (PMRB)	0000	See Port Mode Register B section
Timer/counters, serial interface	Timer mode register A (TMA)	0000	See Timer Mode Register A section
	Timer mode register B (TMB)	0000	See Timer Mode Register B section
	Timer mode register C (TMC)	0000	See Timer Mode Register C section
	Serial mode register (SMR)	0000	See Serial Mode Register section
	Prescaler S	$000	
	Prescaler W	$00	
	Timer counter A (TCA)	$00	
	Timer counter B (TCB)	$00	
	Timer counter C (TCC)	$00	
	Timer load register B (TLR)	$00	
	Timer load register C (TCR)	$00	
	Octal counter	000	

Table 21 Initial Values after MCU Reset (cont)

Items		Initial Value	Contents
LCD	LCD control register (LCR)	000	Refer to description of LCD Control Register
	LCD mode register (LMR)	0000	Refer to description of LCD Duty/Clock Control
Bit register	Low speed on flag (LSON)	0	Refer to description of Low-Power Dissipation Mode
	Watchdog timer on flag (WDON)	0	Refer to description of Timer C
	Direct transfer on flag (DTON)	0	Refer to description of Low-Power Dissipation Mode
Miscellaneous register	(MIS)	000	—

Item	After MCU Reset to Recover from Stop Mode	After MCU Reset to Recover from Other Modes
Carry flag (CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	The contents of the items before MCU reset are not retained. It is necessary to initialize tnem by software.
Accumulator (A)		
B register (B)		
W register (w)		
X/SPX registers (X/SPX)		
Y/SPY registers (Y/SPY)		
Serial data register (SR)		
RAM	The contents of RAM before MCU reset (just before STOP instruction) are retained.	Same as above for RAM.

Internal Oscillator Circuit

Figure 20 shows the block diagram of the internal oscillator circuit. A ceramic filter can be connected to OSC_1 and OSC_2. A 32.768-kHz crystal oscillator can be connected to X1 and X2. An external clock operation is available for the system oscillator.

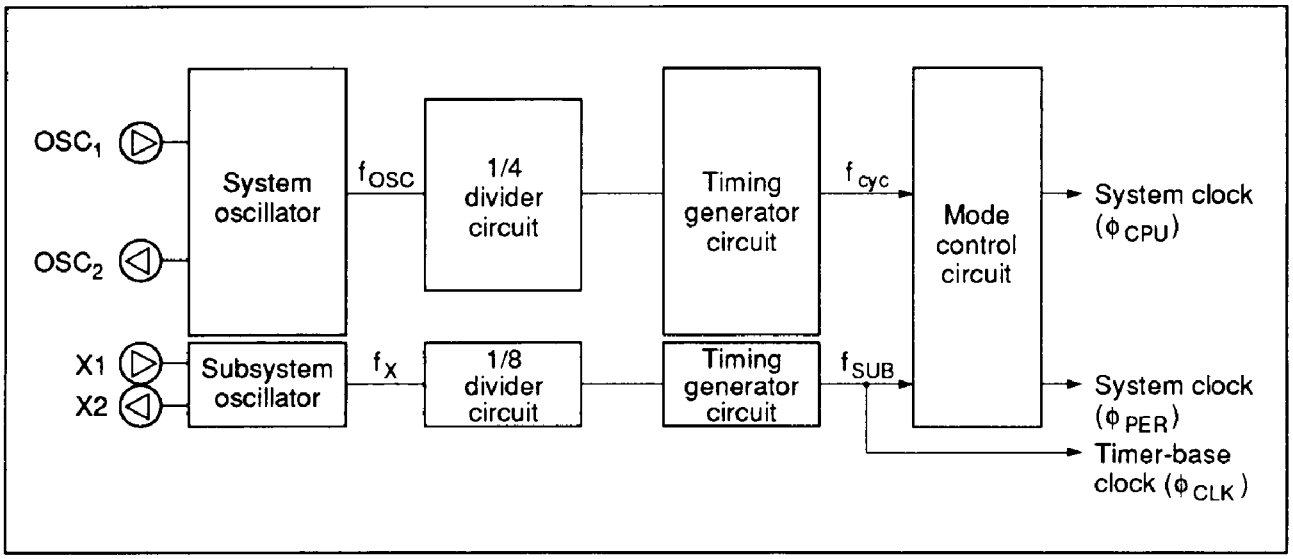


Figure 20 Internal Oscillator Circuit

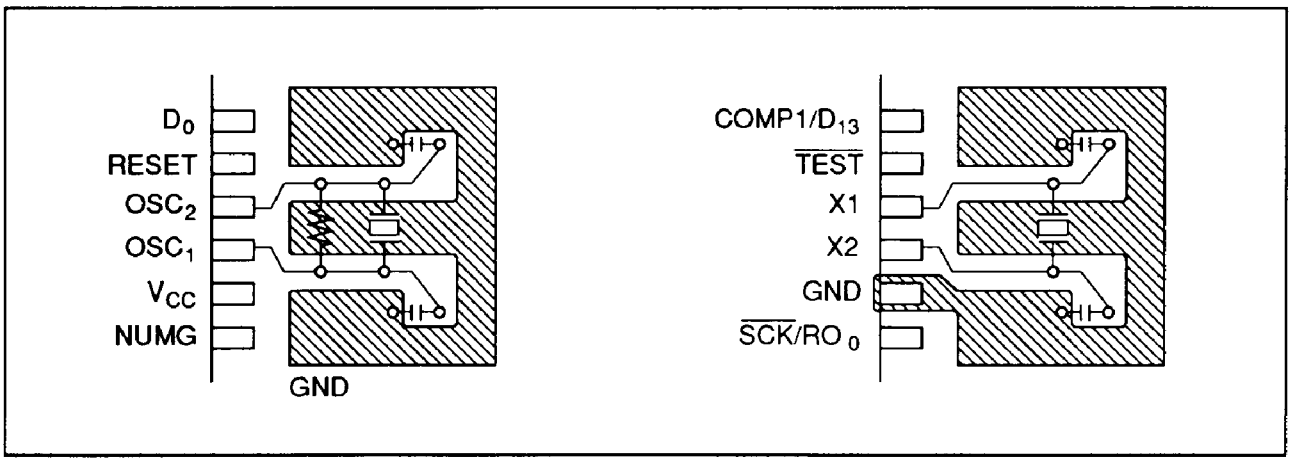


Figure 21 Layout of Crystal and Ceramic Filters

Table 22 Examples of Oscillator Circuits

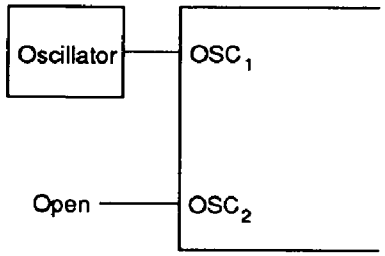
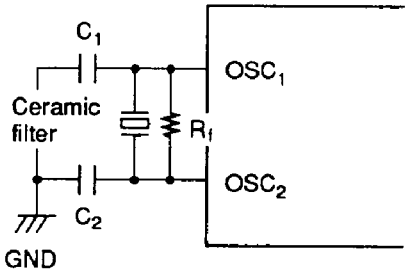
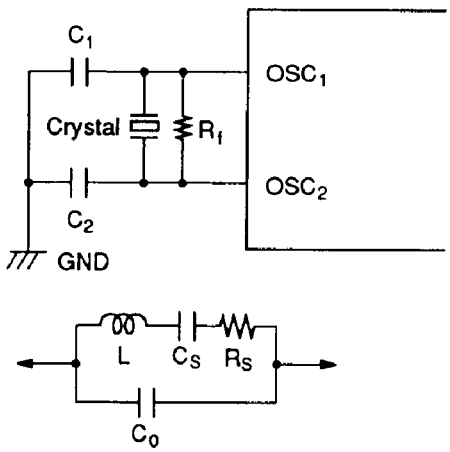
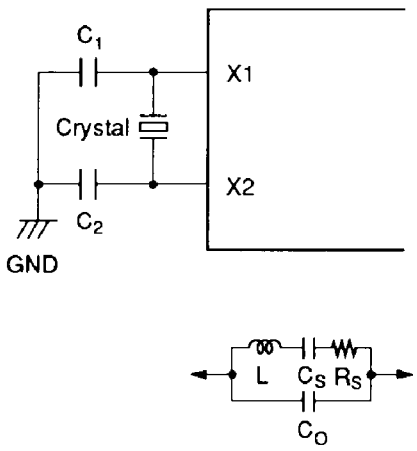
	Circuit Configuration	Circuit Constants
External clock operation		
Ceramic filter oscillator		HD404818, HD404814, HD4074818 Ceramic filter: CSA4.00MG (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 30 pF ± 20%
		HD40L4818, HD40L4814, HD407L4818 Ceramic filter: CSB400P (Murata) CSB400P22 (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 220 pF ± 5% Ceramic filter: CSB800J (Murata) CSB800J122 (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 220 pF ± 5%
Crystal oscillator	 	HD404818, HD404814, HD4074818 C_1: 10 to 22 pF ± 20% C_2: 10 to 22 pF ± 20% R_f = 1 MΩ ± 20% Crystal: Equivalent to circuit shown at bottom left C_0: 7 pF max. R_s: 100 Ω max.

Table 22 Examples of Oscillator Circuits (cont)

	Circuit Configuration	Circuit Constants
Crystal oscillator	 	Crystal: 32.768 kHz: MX38T (Nippon Denpa Kogyo) C_1 = 20 pF ± 20% C_2 = 20 pF ± 20% R_s = 14 kΩ C_0 = 1.5 pF

Notes: 1. The circuit parameters above are recommended by the crystal or ceramic filter maker. The circuit parameters are affected by the crystal, ceramic filter resonator, and the floating capacitance when designing the board. When using the resonator, consult with the crystal or ceramic filter maker to determine the circuit parameters.

2. Wiring among OSC_1 and OSC_2, or X1 and X2, and other elements should be as short as possible, and avoid crossing other wires. Refer to figure 21.
3. When the 32.768-kHz crystal oscillator is not used, pin X1 must be fixed to V_{CC} and pin X2 must be left open.

Liquid Crystal Display (LCD)

The MCU contains 4 common signal pins, the controller, and the driver. The controller and the driver drive 32 segment signal pins. The controller consists of display data RAM, the LCD control register (LCR), and the LCD duty-cycle/clock control register (LMR) (figure 22). Four duty cycles and LCD clocks are available by program control. Since the MCU contains a dual port RAM, display data can be transferred to segment signal pins automatically without program control. When selecting the 32-kHz oscillation clock as the LCD clock source, the system allows the LCD to display even in the watch mode, in which the system clock halts.

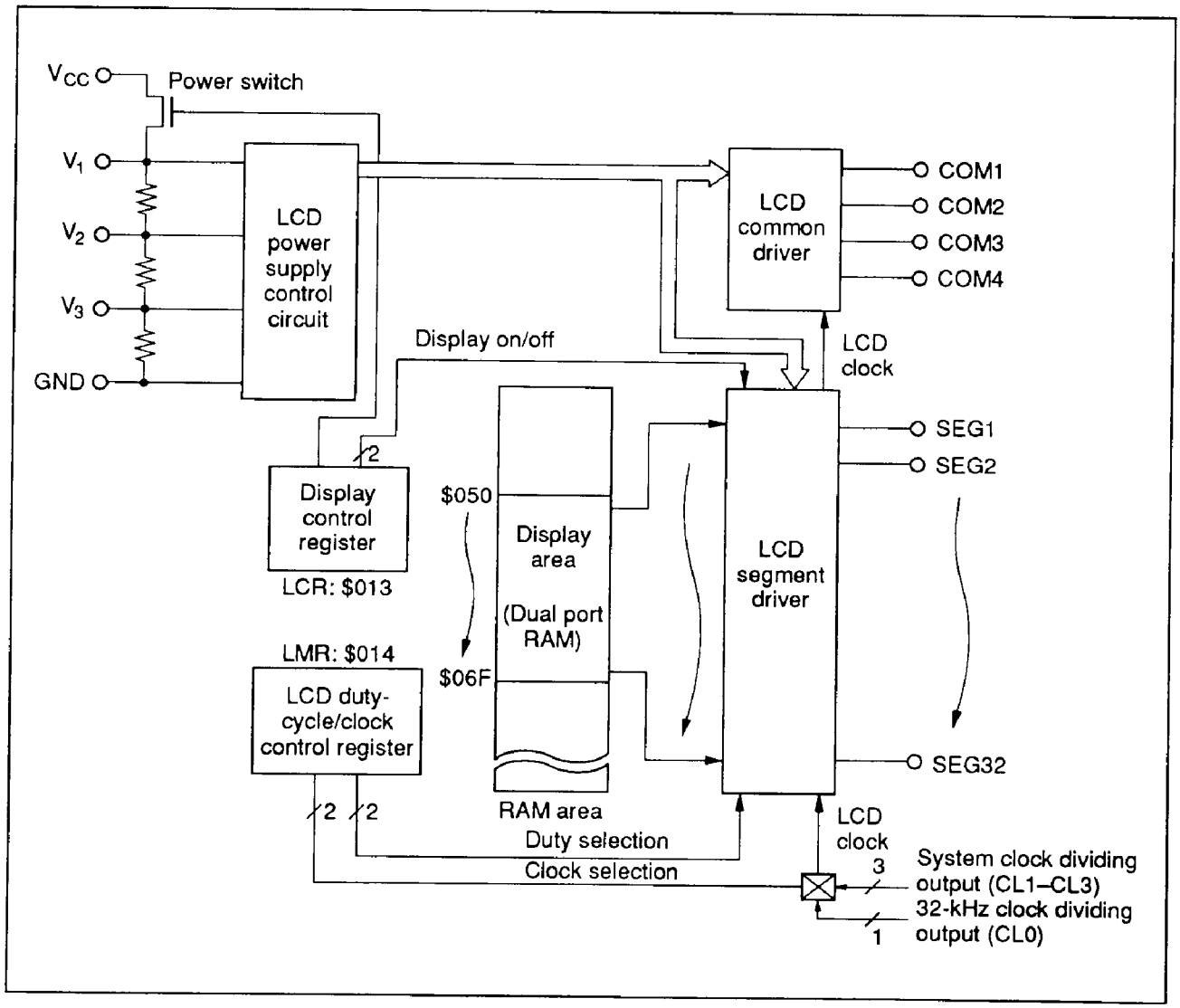


Figure 22 LCD Driver Configuration

LCD Data Area and Segment Data ($050 to $06F): Figure 23 shows the configuration of the LCD RAM area. Each bit of this area, corresponding to 4 types of duty cycles, can be transmitted to the segment driver as display data by programming the area corresponding to the duty cycle.

LCD Control Register (LCR: $013): The LCD control register is a 3-bit write-only register which controls the blanking of the LCD, activation of the power switch, and the display in the watch mode/subactive mode (table 23).

- Blank/display

  Blank: Segment signal is faded regardless of the LCD RAM data.

  Display: LCD RAM data is transmitted as a segment signal.

- Power switch on/off

  Off: Power switch is off.

  On: Power switch is on and V_1 is V_{CC}.

- Watch mode/subactive mode display

  Off: In the watch mode/subactive mode, all common/segment pins are fixed to GND, and the power switch is off.

  On: In the watch mode/subactive mode, LCD RAM data is transmitted as a segment signal.

LCD Duty-Cycle/Clock Control Register (LMR: $014): The LCD duty-cycle/clock control register is a write-only register which specifies 4 display duty cycles and the reference clock for the LCD (table 24).

	Bit 3	Bit 2	Bit 1	Bit 0	
80	SEG1	SEG1	SEG1	SEG1	$050
81	SEG2	SEG2	SEG2	SEG2	$051
82	SEG3	SEG3	SEG3	SEG3	$052
83	SEG4	SEG4	SEG4	SEG4	$053
84	SEG5	SEG5	SEG5	SEG5	$054
85	SEG6	SEG6	SEG6	SEG6	$055
86	SEG7	SEG7	SEG7	SEG7	$056
87	SEG8	SEG8	SEG8	SEG8	$057
88	SEG9	SEG9	SEG9	SEG9	$058
89	SEG10	SEG10	SEG10	SEG10	$059
90	SEG11	SEG11	SEG11	SEG11	$05A
91	SEG12	SEG12	SEG12	SEG12	$05B
92	SEG13	SEG13	SEG13	SEG13	$05C
93	SEG14	SEG14	SEG14	SEG14	$05D
94	SEG15	SEG15	SEG15	SEG15	$05E
95	SEG16	SEG16	SEG16	SEG16	$05F
	COM4	COM3	COM2	COM1	

	Bit 3	Bit 2	Bit 1	Bit 0	
96	SEG17	SEG17	SEG17	SEG17	$060
97	SEG18	SEG18	SEG18	SEG18	$061
98	SEG19	SEG19	SEG19	SEG19	$062
99	SEG20	SEG20	SEG20	SEG20	$063
100	SEG21	SEG21	SEG21	SEG21	$064
101	SEG22	SEG22	SEG22	SEG22	$065
102	SEG23	SEG23	SEG23	SEG23	$066
103	SEG24	SEG24	SEG24	SEG24	$067
104	SEG25	SEG25	SEG25	SEG25	$068
105	SEG26	SEG26	SEG26	SEG26	$069
106	SEG27	SEG27	SEG27	SEG27	$06A
107	SEG28	SEG28	SEG28	SEG28	$06B
108	SEG29	SEG29	SEG29	SEG29	$06C
109	SEG30	SEG30	SEG30	SEG30	$06D
110	SEG31	SEG31	SEG31	SEG31	$06E
111	SEG32	SEG32	SEG32	SEG32	$06F
	COM4	COM3	COM2	COM1	

Figure 23 Configuration of LCD RAM Area (Dual Port RAM)

Table 23 LCD Control Register

LCR Bit 2	Watch Mode/ Subactive Mode Display	LCR Bit 1	Power Switch On/Off	LCR Bit 0	Blank/ Display
0	Off	0	Off	0	Blank
1	On	1	On	1	Display

Note: With the LCD in the watch mode, use the divider output of the 32-kHz oscillator as an LCD clock and set LCR bit 2 to 1. When the system oscillator divider output is used as an LCD clock, set LCR bit 2 to 0.

Table 24 LCD Duty-Cycle/Clock Control Register

LMR Bit 3	LMR Bit 2	LMR Bit 1	LMR Bit 0	Duty Cycle Select/Input Clock Select
		0	0	1/4 duty cycle
		0	1	1/3 duty cycle
		1	0	1/2 duty cycle
		1	1	Static
0	0			CL0 (32.768 kHz/64; when 32.768-kHz oscillator is used)
0	1			CL1 (f_{cyc}/256)
1	0			CL2 (f_{cyc}/2048)
1	1			CL3 (Refer to table 25)

Note: f_{cyc} is the system oscillator divider output.

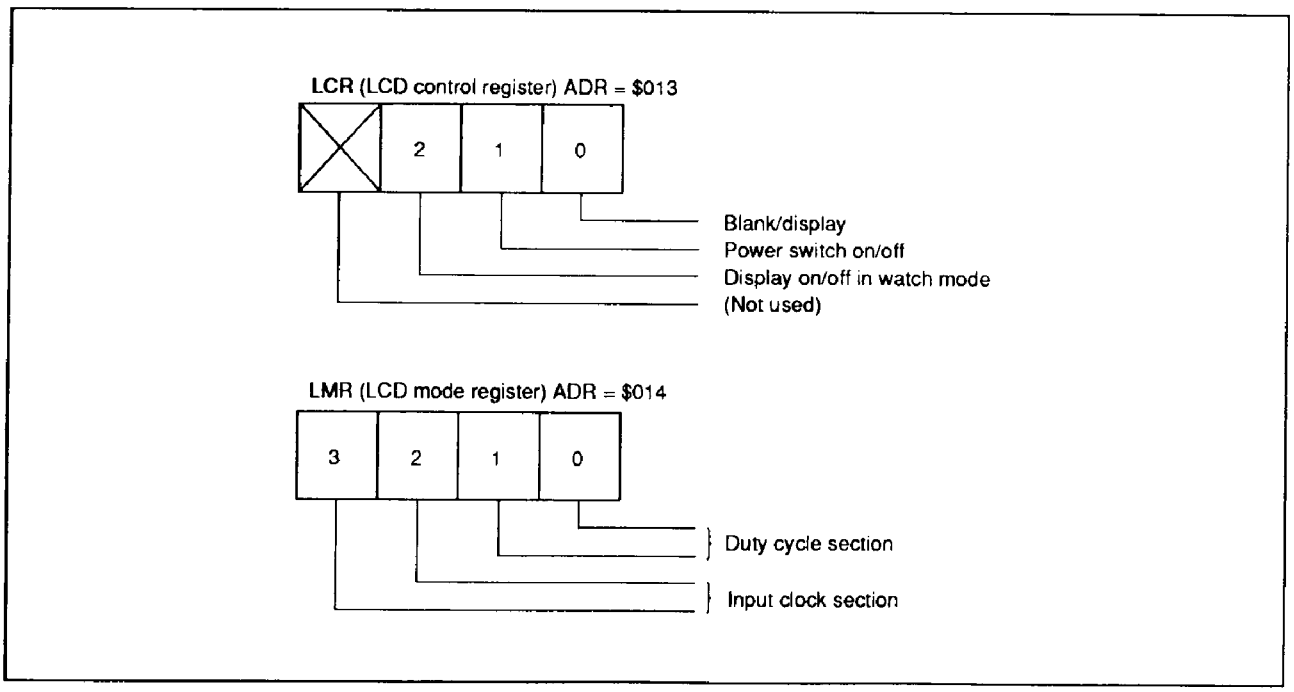


Figure 24 LCD Control Register

Table 25 LCD Frame Frequency

Static	LMR							
	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2
Instruction cycle time	0	0	0	1	1	0	1	1
	CL0		CL1		CL2		CL3	*
10 µs	512 Hz		390.6 Hz		48.8 Hz		24.4 Hz/64 Hz	
1 µs	512 Hz		3906 Hz		488Hz		244 Hz/64 Hz	

1/2 Duty Cycle	LMR							
	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2
Instruction cycle time	0	0	0	1	1	0	1	1
	CL0		CL1		CL2		CL3	*
10 µs	256 Hz		195.3 Hz		24.4 Hz		12.2 Hz/32 Hz	
1 µs	256 Hz		1953 Hz		244 Hz		122 Hz/32 Hz	

1/3 Duty Cycle	LMR							
	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2
Instruction cycle time	0	0	0	1	1	0	1	1
	CL0		CL1		CL2		CL3	*
10 µs	170.6 Hz		130.2 Hz		16.3 Hz		8.1 Hz/21.3 Hz	
1µs	170.6 Hz		1302 Hz		162.6 Hz		81.3 Hz/21.3 Hz	

1/4 Duty Cycle	LMR							
	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2
Instruction cycle time	0	0	0	1	1	0	1	1
	CL0		CL1		CL2		CL3	*
10 µs	128 Hz		97.7 Hz		12.2 Hz		6.1 Hz/16 Hz	
1 µs	128 Hz		977 Hz		122 Hz		61 Hz/16 Hz	

Note: * Division ratio differs depending on the value of bit 3 of timer mode register A (TMA3 = 0/TMA3 = 1). If TMA3 = 0, CL3 = f_{cyc}/4096; if TMA3 = 1, CL3 = 32.768 kHz/512.

Large LCD Panel Driving and Driving Voltage (V_{LCD}): When using a large LCD panel, lower the dividing resistance by attaching external resistors in parallel to the internal dividing resistors (see figure 25).

Since the liquid crystal display board is of a matrix configuration, the path of the charge/discharge current through the load capacitors is very complicated. Moreover, since it varies depending on display conditions, the value of resistance cannot be determined by simply referring to the load capacitance of the liquid crystal display. The value of resistance must be experimentally determined according to the demand for power consumption of the equipment in which the liquid crystal display is implemented. Capacitor C (0.1 to 0.3 µF) is recommended to be attached. In general, R is 1 kΩ to 10 kΩ.

Figure 25 shows a connection when changing the liquid crystal driving voltage (V_{LCD}). In this case, the power supply switch for the dividing resistors (power switch) must be turned off. (Bit 1 of the LCR register is 0.)

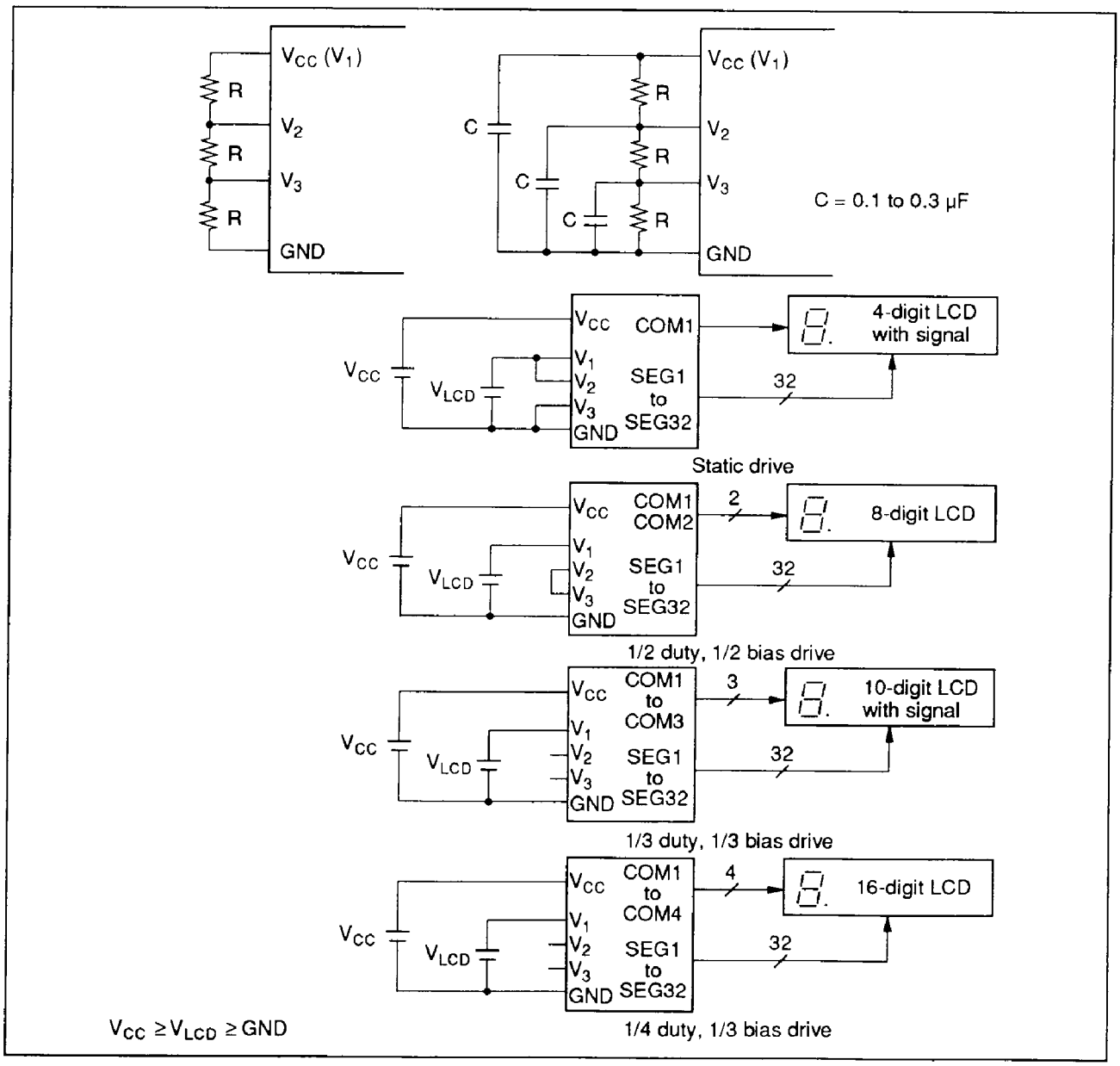


Figure 25 Examples of LCD Connections

Operating Modes

The MCU has five operating modes that are specified by how the clock is used. The functions available in each mode are listed in table 26, and operations are shown in table 28. Transitions between operating modes are shown in figure 26.

Table 27 provides additional information for table 26.

Active Mode: The MCU operates according to the clock generated by the system oscillators OSC_1 and OSC_2.

Table 26 Functions Available in Each Operating Mode

		Mode Name				
		Active	**Standby**	**Stop**	**Watch**	**Subactive*4**
Activation method		RESET cancellation, interrupt request	SBY instruction	TMA3 = 0, STOP instruction	TMA3 = 1, STOP instruction	$\overline{INT_0}$ or timer A interrupt request from watch mode
Status	System oscillator	Operating	Operating	Stopped	Stopped	Stopped
	Subsystem oscillator	Operating	Operating	Operating*1	Operating	Operating
	Instruction execution (ϕ_{CPU})	Operating	Stopped	Stopped	Stopped	Operating
	Peripheral function interrupt (ϕ_{PER})	Operating	Operating	Stopped	Stopped	Operating
	Clock function interrupt (ϕ_{CLK})	Operating	Operating	Stopped	Operating*2	Operating*2
	RAM	Operating	Retained	Retained	Retained	Operating
	Registers/flags	Operating	Retained	Reset	Retained	Operating
	I/O	Operating	Retained	High impedance*3	Retained*3	Operating*3
Cancellation method		RESET input, STOP/SBY instruction	RESET input, interrupt request	RESET input	RESET input, $\overline{INT_0}$ or timer A interrupt request	RESET input, STOP/SBY instruction

Notes: 1. To reduce current dissipation, stop all oscillation in external circuits.
2. Refer to the Interrupt Frame section for details.
3. Refer to table 30.
4. Subactive mode is an optional function to be specified on the function option list.
5. In the watch and subactive modes, the MCU requires a 32.768-kHz crystal oscillator.

		System Clock (ϕ_{CPU})	
		Operating	**Stopped**
Non-time-base peripheral function clock (ϕ_{PER})	Operating	Active mode	Standby mode
		Subactive mode	
	Stopped	—	Watch mode (TMA3 = 1)
			Stop mode (TMA3 = 0)

Standby Mode: The MCU enters standby mode when the SBY instruction is executed from active mode. In this mode, the oscillators, interrupts, timer/counters, and serial interface continue to operate, but all instruction execution-related clocks stop. The stopping of these clocks stops the CPU, retaining all RAM and register contents and maintaining the current I/O pin status.

Standby mode is terminated by a RESET input or an interrupt request. If it is terminated by a RESET input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and resumes, executing the next instruction after the SBY instruction. If the interrupt enable flag is 1, that interrupt is then processed; if it is 0, the interrupt request is left pending and normal instruction execution continues. A flowchart of operation in standby mode is shown in figure 27 .

Stop Mode: The MCU enters stop mode if the STOP instruction is executed in active mode when TMA3 = 0. In this mode, the system oscillator stops, which stops all MCU functions as well.

Stop mode is terminated by a RESET input as shown in figure 28. RESET must be high for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics section). When the MCU restarts after stop mode is cancelled, all RAM contents are retained, but the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

Watch Mode: The MCU enters watch mode if the STOP instruction is executed in active mode when TMA3 = 1, or if the STOP or SBY instruction is executed in subactive mode.

Watch mode is terminated by a RESET input or a timer-A/$\overline{INT_0}$ interrupt request. For details on RESET input, refer to the Stop Mode section. When terminated by a timer-A/$\overline{INT_0}$ interrupt request, the MCU enters active mode if LSON is 0, or subactive mode if LSON is 1. Any interrupt request generated during the transition to active mode is delayed for half the interrupt frame period (t_{RC}), to give the oscillation time to stabilize, as shown figure 29.

Table 27 I/O Status in Low-Power Dissipation Modes

	Output		Input
	Standby Mode, Watch Mode	Stop Mode	Active Mode, Subactive Mode
D_0–D_9	Retained	High impedance	Input enabled
D_{10}–D_{13}	—	—	Input enabled
R0–R3	Retained	High impedance	Input enabled

Table 28 Operations in Low-Power Dissipation Modes

Function	Stop Mode	Watch Mode	Standby Mode	Subactive Mode*2
CPU	Reset	Retained	Retained	
RAM	Retained	Retained	Retained	
Timer A	Reset			
Timer B	Reset	Stopped		
Timer C	Reset	Stopped		
Serial interface	Reset	Stopped*3		
LCD	Reset			
DTMF	Reset	Reset	Stopped	Reset
I/O	Reset*1	Retained	Retained	

Notes: Shaded region indicates operating.
1. Output pins are at high impedance.
2. Subactive mode is an optional function to be specified on the function option list.
3. Transmission/reception is activated if a clock is input in external clock mode. (However, interrupts are stopped.)

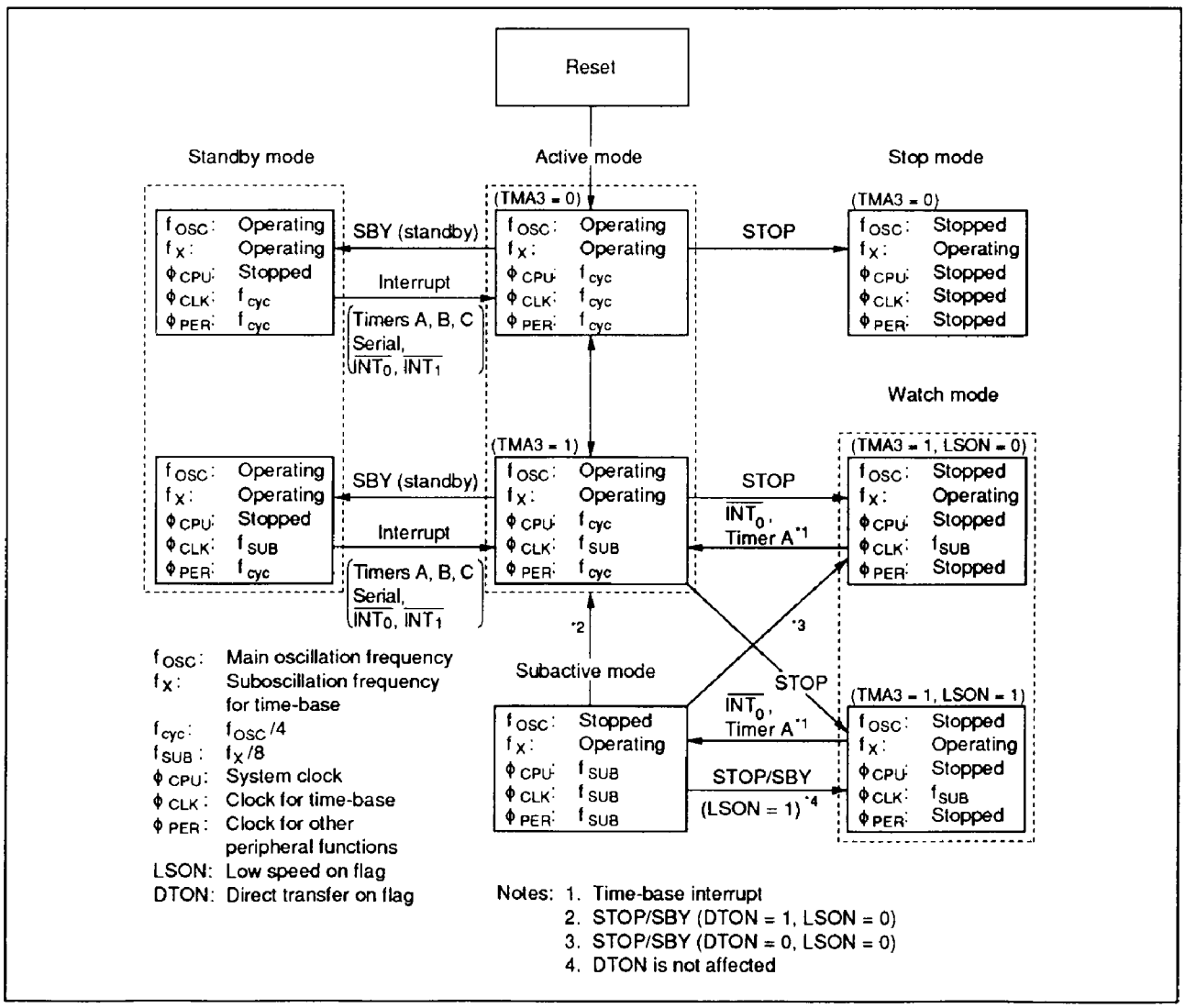


Figure 26 MCU Status Transitions

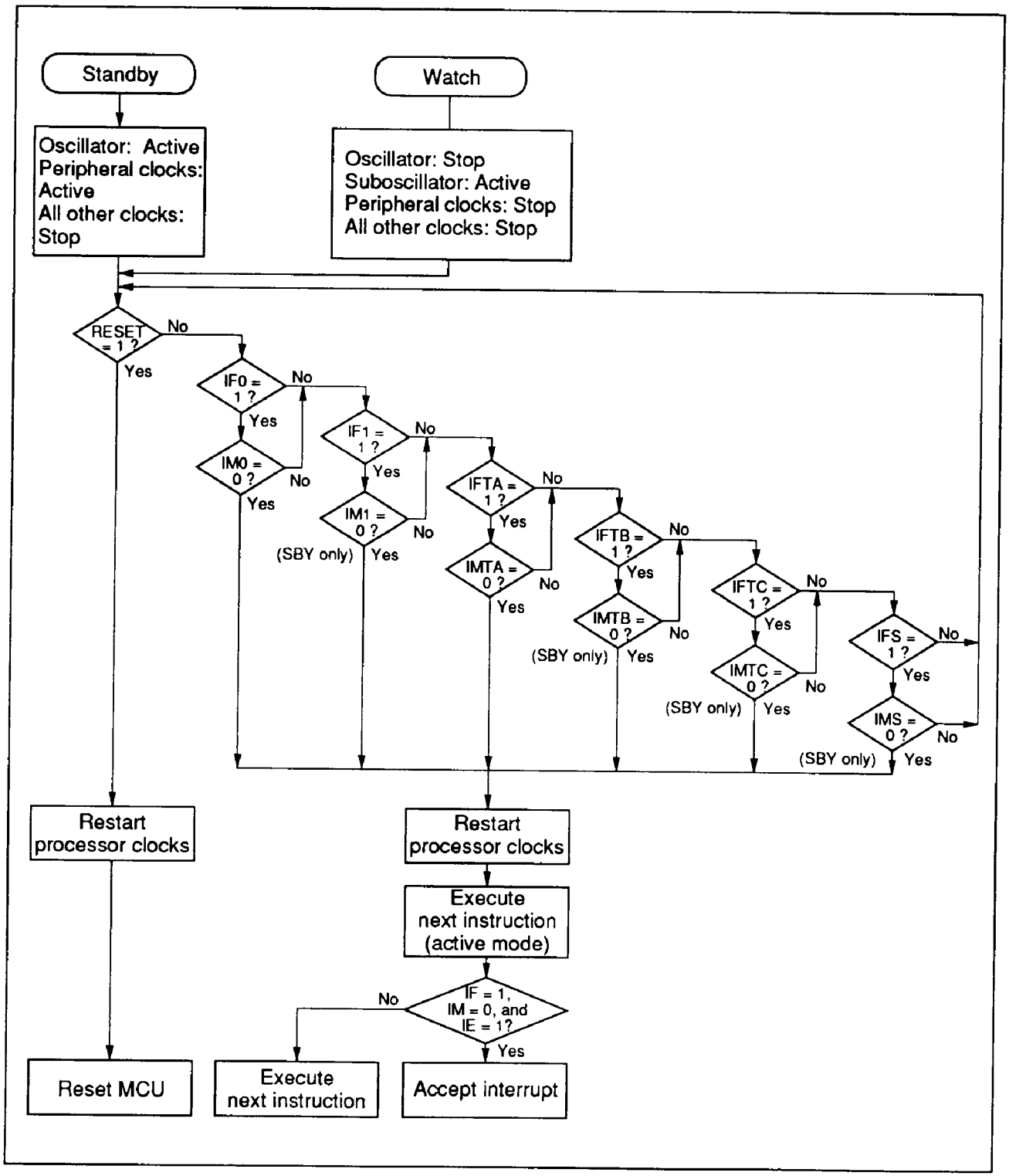


Figure 27 MCU Operating Flowchart of Watch and Standby Modes

Operation during mode transition is the same as that at standby mode cancellation (figure 27).

Subactive Mode: The CPU operates with a clock generated by the X1 and X2 oscillation circuits. Functions that can operate in subactive mode are listed in table 28. When the STOP or SBY instruction is executed in subactive mode, the MCU enters either watch or active mode, depending on the statuses of LSON and DTON. The DTON flag can only be set in subactive mode; it is automatically reset after a transition to active mode.

Subactive mode is an optional function that the user must specify on the function option list.

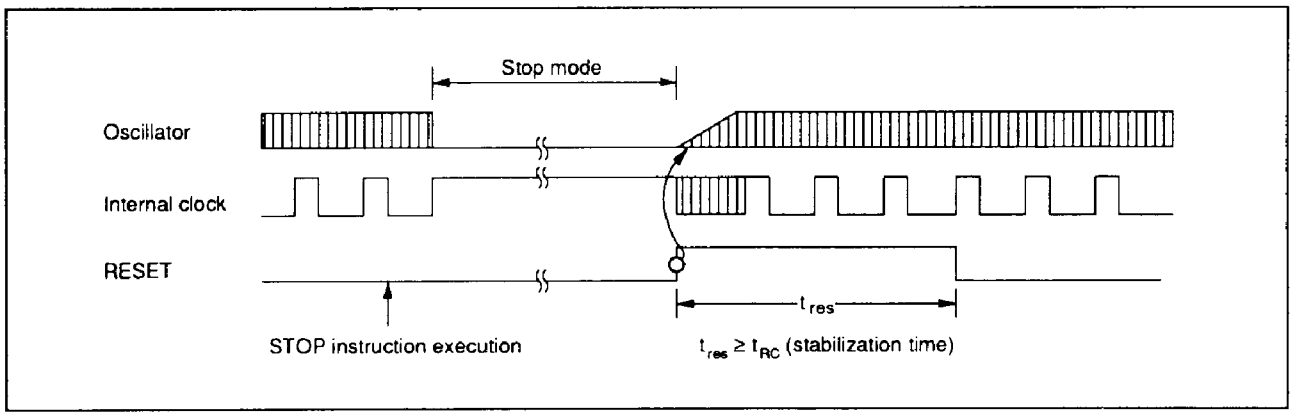


Figure 28 Timing of Stop Mode Cancellation

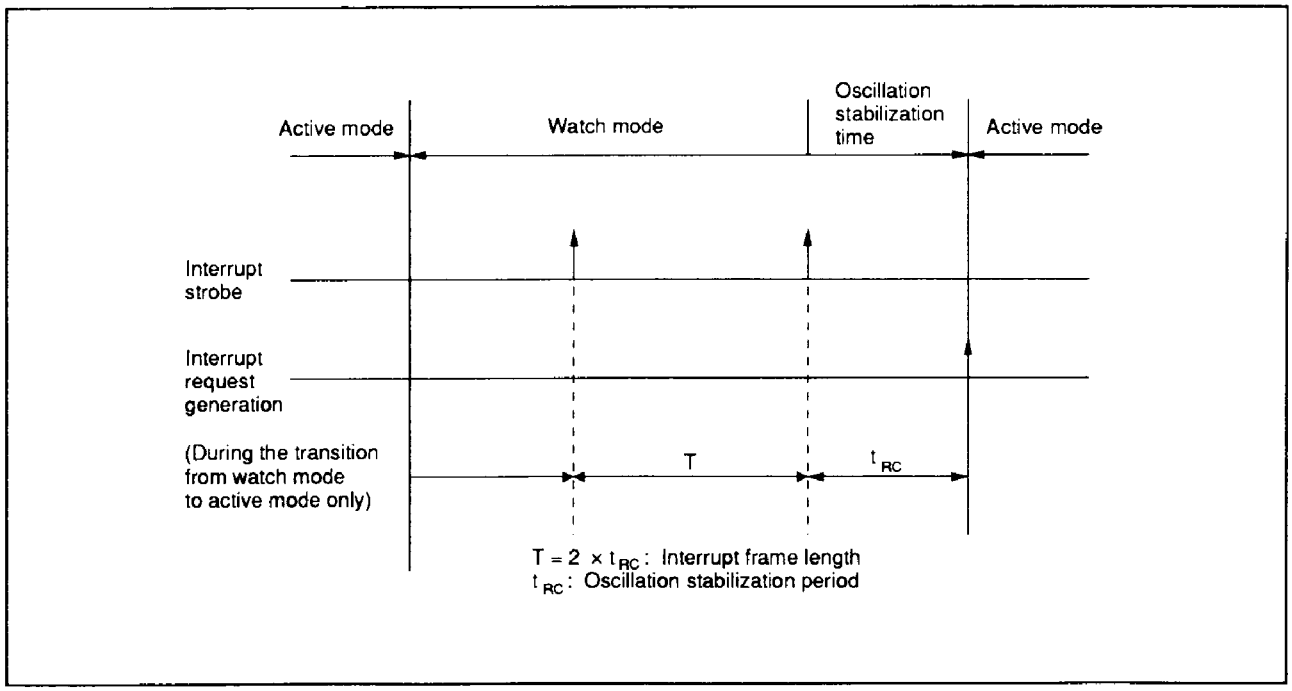
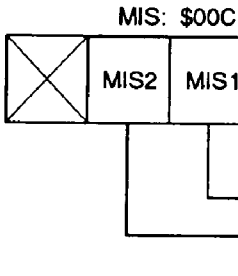


Figure 29 Interrupt Frame

Interrupt Frame: In watch and subactive modes, ϕ_{CLK} is supplied for timer A and the $\overline{INT_0}$ circuit. Prescaler W and timer A operate as time bases to generate interrupt frame timing. Three interrupt frame cycles (T) can be selected by the settings of the miscellaneous register, as shown in figure 30.

In watch and subactive modes, timer A and $\overline{INT_0}$ interrupts are generated in synchronism with the interrupt frame. An interrupt request is generated at the interrupt strobe timing, except when the MCU enters active mode from watch mode. The $\overline{INT_0}$ falling edge is acknowledged regardless of the interrupt frame, but the interrupt is executed simultaneously with the next interrupt strobe. Timer A generates an overflow and interrupt request at the timing of an interrupt strobe.



MIS		T^{*1}	t_{RC}^{*1}	Oscillation circuit condition
1 Bit	0 Bit			
0	0	0.24414 ms	0.12207 ms	External clock input
			0.24414 ms *2	
0	1	15.625 ms	7.8125 ms	Ceramic filter, crystal
1	0	62.5 ms	31.25 ms	
1	1	Not used		—

Notes: 1. The value of t_{RC} applies only when using a 32.768-kHz oscillator.
2. Only direct transfer.

Figure 30 Miscellaneous Register

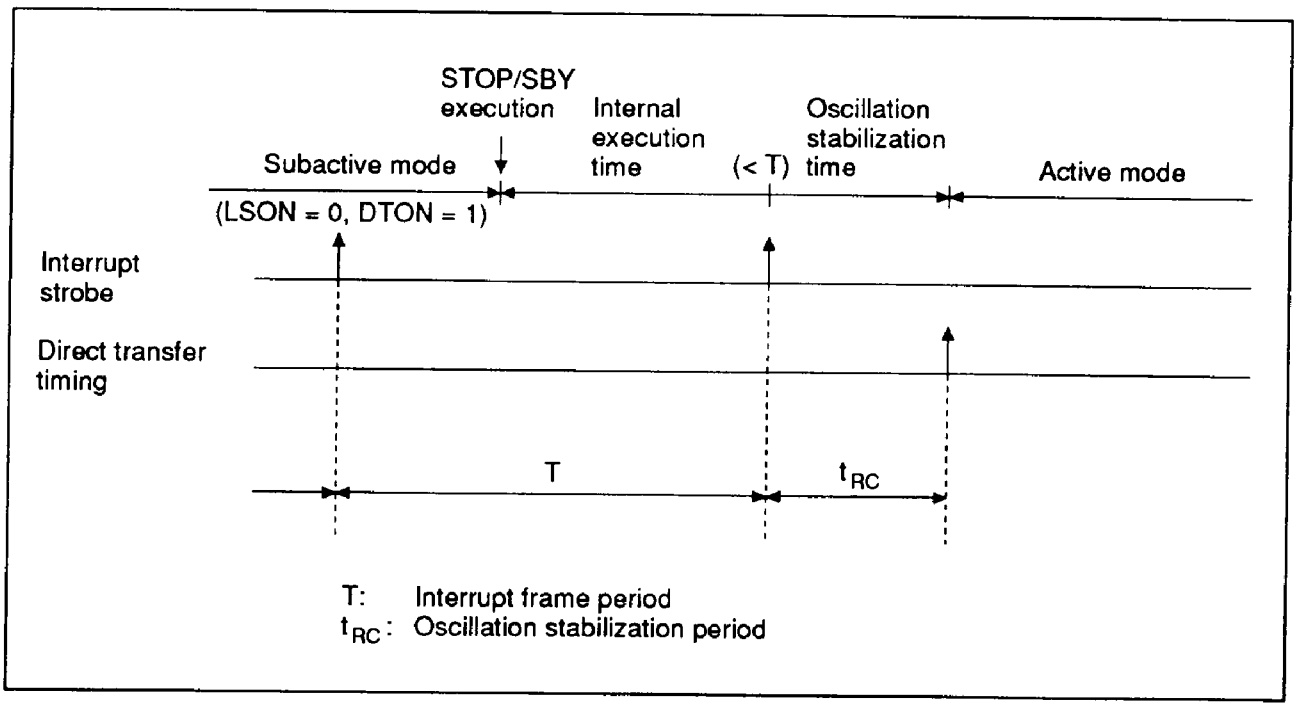


Figure 31 Direct Transfer Timing

Direct Transfer: By controlling the DTON, the MCU would be placed directly from the subactive to active mode. The detailed procedure is as follows:

- Set the DTON flag in subactive mode while LSON = 0.
- Execute the STOP or SBY instruction.
- After the oscillation stabilization time (a fixed value), the MCU will move automatically from subactive to active mode.

Note that DTON ($020, bit 3) is valid only in subactive mode. When the MCU is in active mode, this flag is always at reset.

The transition time (t_D) from subactive to active mode is $t_{RC} > t_D > T + t_{RC}$.

MCU Operating Sequence: The MCU operates in the sequence shown in figures 32 to 34. It is reset by an asynchronous RESET input, regardless of its state.

Limitation on Use: In subactive mode, the timer A interrupt request or the external interrupt request ($\overline{INT_0}$) occurs in synchronism with the interrupt strobe.

If the STOP or SBY instruction is executed at the same time with the interrupt strobe, these interrupt requests will be cancelled and its corresponding interrupt request flags (IFTA, IF0) will be not set.

In subactive mode, do not use the STOP or SBY instruction at the time of the interrupt strobe.

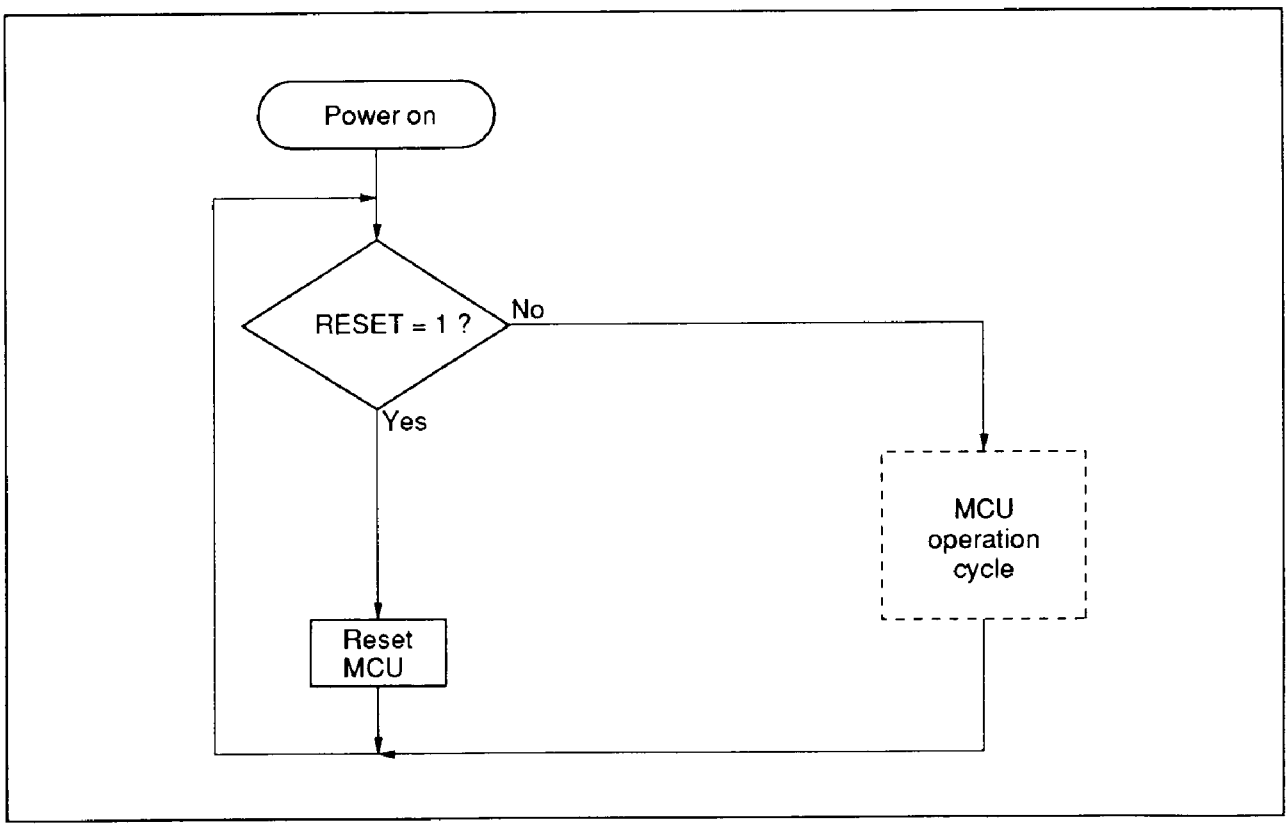


Figure 32 MCU Operating Sequence (Power On)

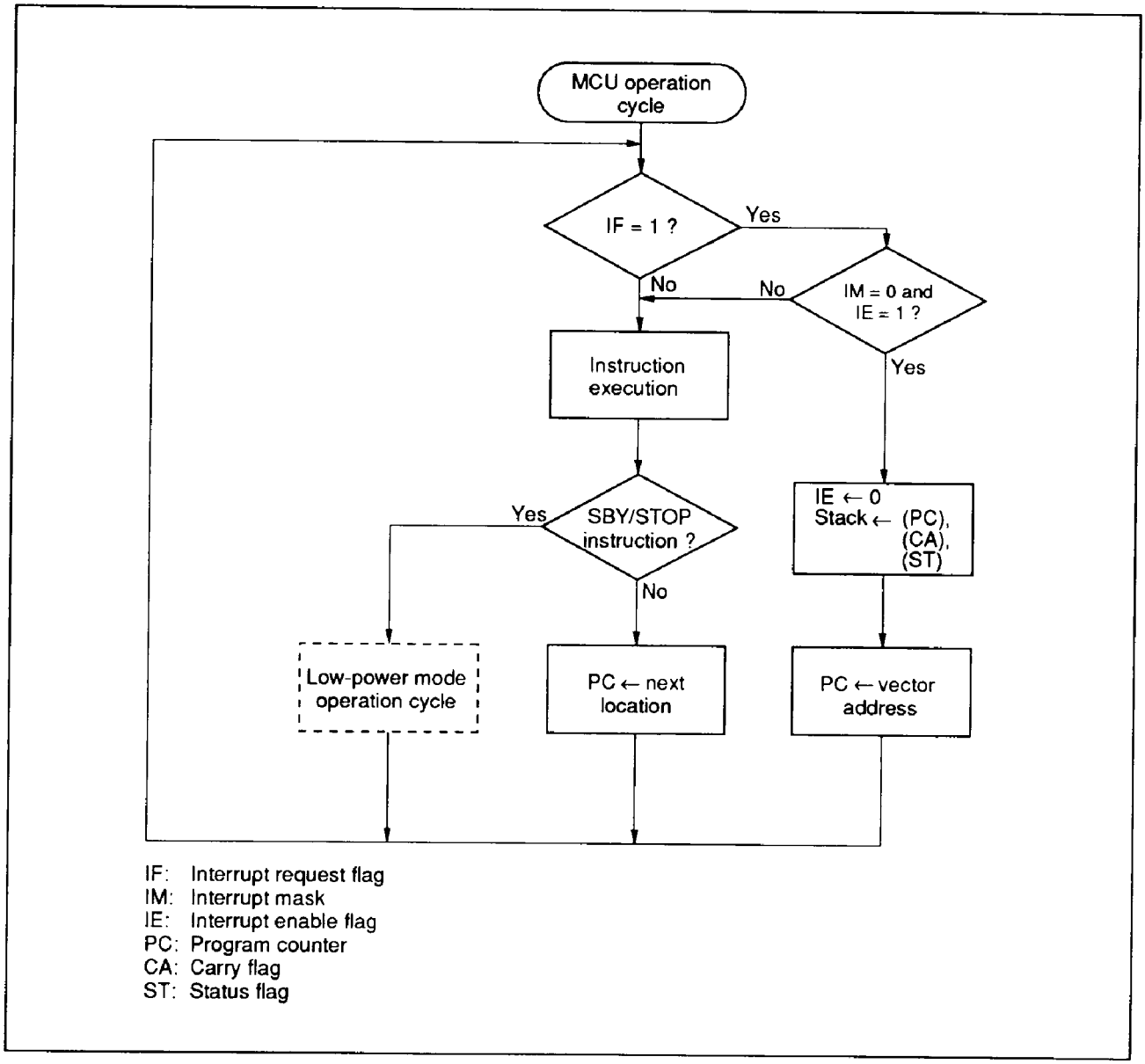
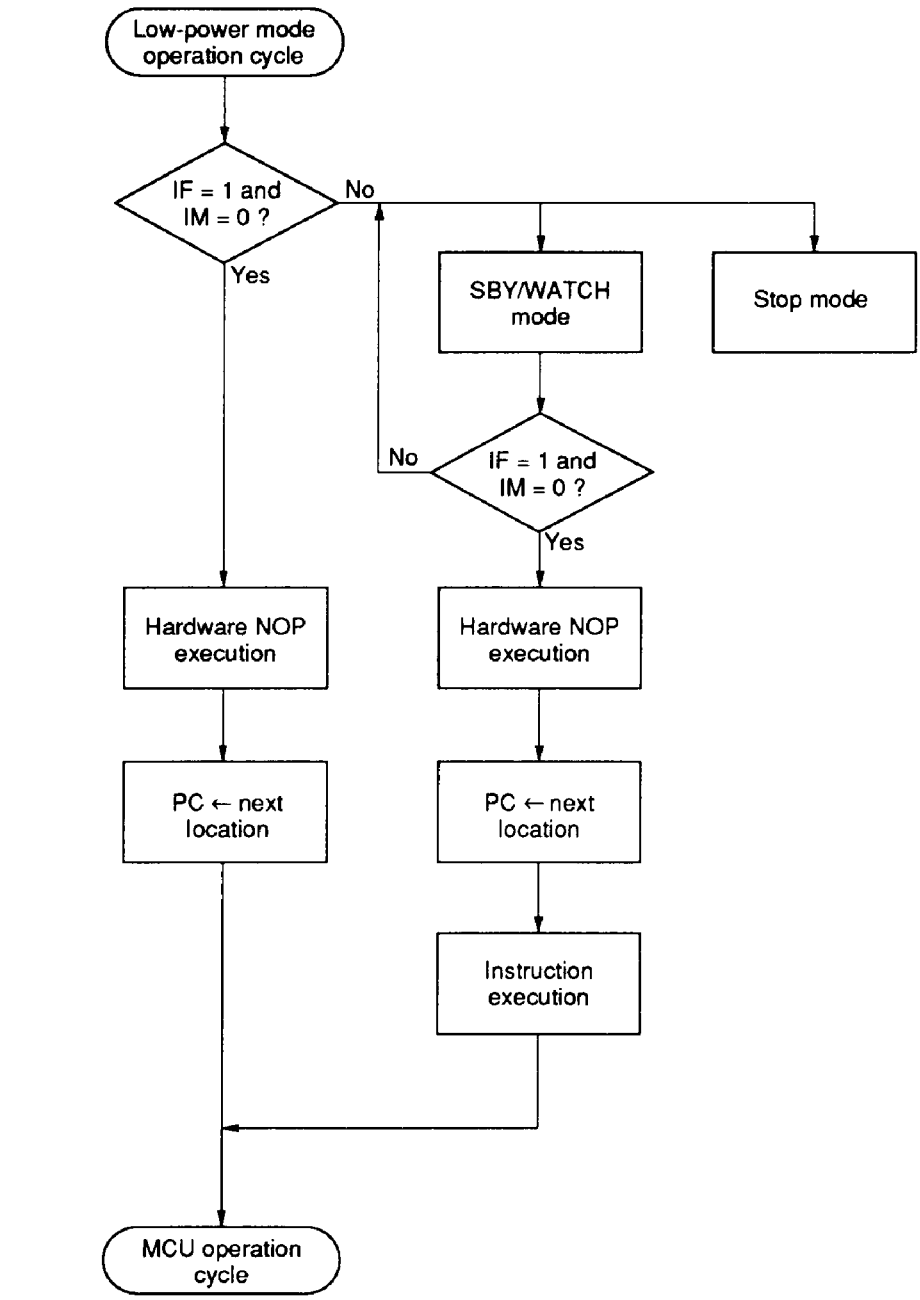


Figure 33 MCU Operating Sequence (MCU Operation Cycle)



For specific IF and IM, see figure 27, MCU Operating Flowchart

Figure 34 MCU Operating Sequence (Low-Power Mode Operation)

Pin Description in PROM Mode

The HD4074818/HD407L4818 is a ZTAT™ microcomputer incorporating a PROM. In the PROM mode, the MCU does not operate and the HD4074818/HD407L4818 can program the on-chip PROM.

Pin Number		MCU Mode		PROM Mode		Pin Number		MCU Mode		PROM Mode	
FP-80B	FP-80A TFP-80	Pin Name	I/O	Pin Name	I/O	FP-80B	FP-80A TFP-80	Pin Name	I/O	Pin Name	I/O
1	79	D_2	I/O	O_2	I/O	41	39	SEG9	O		
2	80	D_3	I/O	O_3	I/O	42	40	SEG10	O		
3	1	D_4	I/O	O_4	I/O	43	41	SEG11	O		
4	2	D_5	I/O	O_5	I/O	44	42	SEG12	O		
5	3	D_6	I/O	O_6	I/O	45	43	SEG13	O		
6	4	D_7	I/O	O_7	I/O	46	44	SEG14	O		
7	5	D_8	I/O			47	45	SEG15	O		
8	6	D_9	I/O			48	46	SEG16	O		
9	7	D_{10}	I	V_{PP}		49	47	SEG17	O		
10	8	D_{11}/VC_{ref}	I	A_9	I	50	48	SEG18	O		
11	9	D_{12}/COMP0	I	$\overline{M_0}$	I	51	49	SEG19	O		
12	10	D_{13}/COMP1	I	$\overline{M_1}$	I	52	50	SEG20	O		
13	11	$\overline{TEST}$	I	$\overline{TEST}$	I	53	51	SEG21	O		
14	12	X1	I	GND		54	52	SEG22	O		
15	13	X2	O			55	53	SEG23	O		
16	14	GND		GND		56	54	SEG24	O		
17	15	$R0_0/\overline{SCK}$	I/O	A_1	I	57	55	SEG25	O		
18	16	$R0_1$/SI	I/O	A_2	I	58	56	SEG26	O		
19	17	$R0_2$/SO	I/O	A_3	I	59	57	SEG27	O		
20	18	$R0_3$	I/O	A_4	I	60	58	SEG28	O		
21	19	$R1_0$	I/O	A_5	I	61	59	SEG29	O		
22	20	$R1_1$	I/O	A_6	I	62	60	SEG30	O		
23	21	$R1_2$	I/O	A_7	I	63	61	SEG31	O		
24	22	$R1_3$	I/O	A_8	I	64	62	SEG32	O		
25	23	$R2_0$	I/O	A_0	I	65	63	COM1	O		
26	24	$R2_1$	I/O	A_{10}	I	66	64	COM2	O		
27	25	$R2_2$	I/O	A_{11}	I	67	65	COM3	O		
28	26	$R2_3$	I/O	A_{12}	I	68	66	COM4	O		
29	27	$R3_0$	I/O	A_{13}	I	69	67	V_1			
30	28	$R3_1$/TIMO	I/O	A_{14}	I	71	69	V_2			
31	29	$R3_2/\overline{INT_0}$	I/O	$\overline{CE}$	I	71	69	V_3		V_{CC}	
32	30	$R3_3/\overline{INT_1}$	I/O	$\overline{OE}$	I	72	70	NUMO	O		
33	31	SEG1	O			73	71	NUMO	O		
34	32	SEG2	O			74	72	NUMG		V_{CC}	
35	33	SEG3	O			75	73	V_{CC}		V_{CC}	
36	34	SEG4	O			76	74	OSC_1	I	V_{CC}	
37	35	SEG5	O			77	75	OSC_2	O		
38	36	SEG6	O			78	76	RESET	I	RESET	I
39	37	SEG7	O			79	77	D_0	I/O	O_0	I/O
40	38	SEG8	O			80	78	D_1	I/O	O_1	I/O

Note: I/O: Input/output pin, I: Input pin, O: Output pin

Pins for PROM Mode (HD4074818)

V_{PP}: Apply the programming voltage (12.5 V ± 0.3 V) to this pin.

$\overline{CE}$: For programming the internal PROM and inputting the control signal to enable verification.

$\overline{OE}$: For inputting the data output control signal when verifying.

A_0–A_{14}: Address input pins of the internal PROM.

O_0–O_7: Data bus I/O pins of the internal PROM.

$\overline{M_0}$, $\overline{M_1}$: $\overline{M_0}$ and $\overline{M_1}$ are for PROM mode specification. To place the MCU into the PROM mode, pull $\overline{M_0}$, $\overline{M_1}$, and $\overline{TEST}$ low, and RESET high.

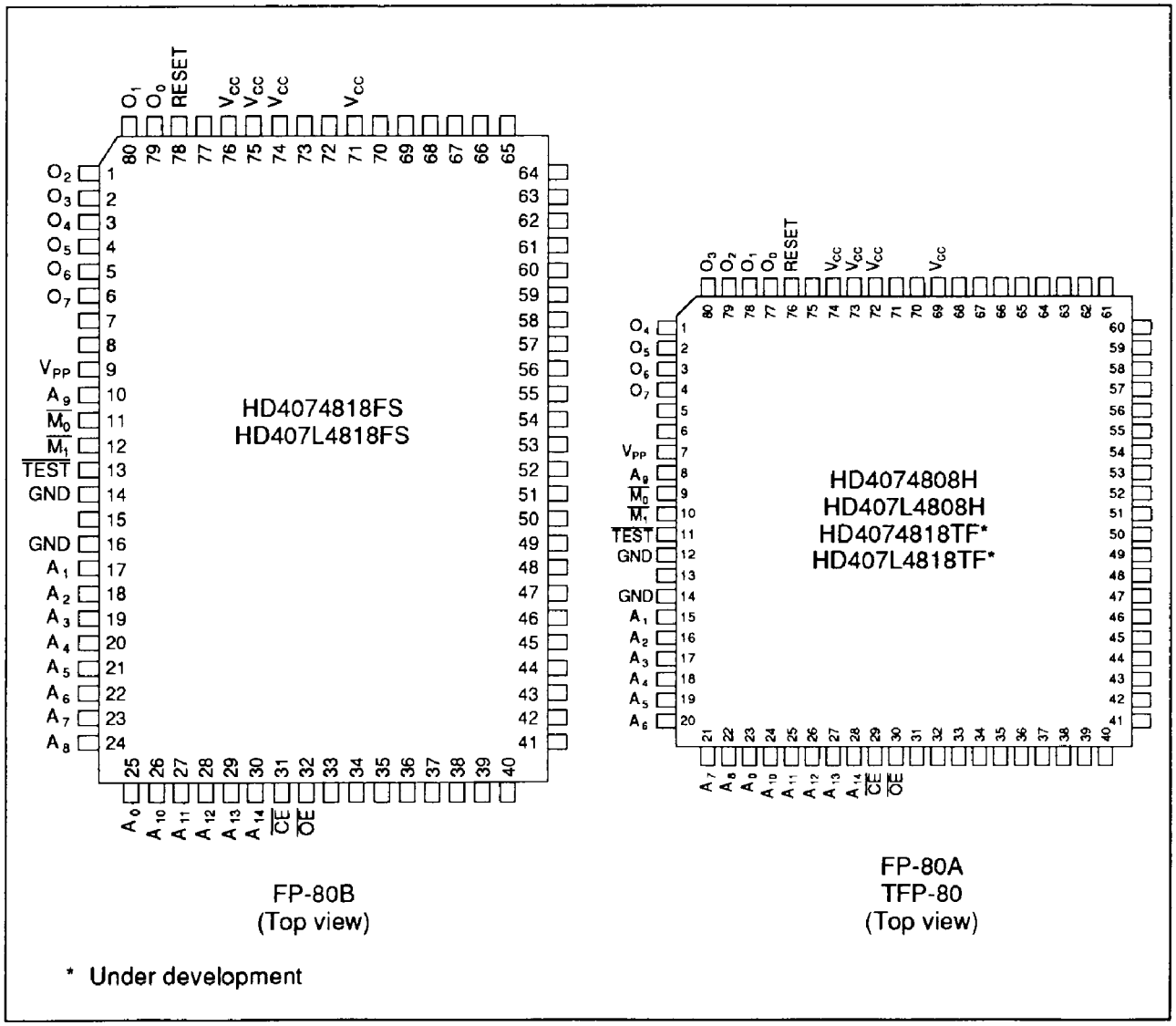


Figure 35 PROM Mode Pin Arrangement

Programmable ROM Operation

The MCU on-chip PROM is programmed in the PROM mode (figures 36 and 37). The PROM mode is set by pulling $\overline{TEST}$, $\overline{M_0}$, and $\overline{M_1}$ low, and RESET high, as shown in figure 36. In PROM mode, the MCU does not operate. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and an 80-to-28-pin socket adapter. Table 30 lists the recommended PROM programmers and socket adapters.

Since an instruction of the HMCS400 series consists of 10 bits, the HMCS400 series microcomputer incorporates a conversion circuit to enable the use of a general-purpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, the lower 5 bits and upper 5 bits, as shown in figure 37. For example, if 8 Kwords of on-chip PROM are programmed by a general-purpose PROM programmer, 16 Kbytes of addresses ($0000–$3FFF) should be specified.

Programming and Verification

The MCU can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 29 shows how programming and verification modes are selected.

Figure 38 is a programming flowchart, and figure 39 is a timing chart. For precautions on PROM programming, refer to the Precautions on PROM Programming section for applications.

Precautions

1. Addresses $0000 to $3FFF must be specified if the PROM is programmed by a PROM programmer. If addresses of $4000 or higher are accessed, the PROM may not be programmed or verified. Note that plastic package types cannot be erased and reprogrammed. Data in unused addresses must be set to $FF.

2. Ensure that the PROM programmer, socket adapter, and LSI match. Using the wrong programmer for the socket adapter may cause an overvoltage and damage the LSI. Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed onto the programmer.

3. The PROM should be programmed with V_{PP} = 12.5 V. Other PROMs use 21 V. If 21 V is applied to the MCU, the LSI may be permanently damaged. A voltage of 12.5 V is Intel's 27256 V_{PP}.

Table 29 PROM Mode Selection

	Pin			
Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	O_0–O_7
Programming	Low	High	V_{PP}	Data input
Verify	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Table 30 PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Maker	Type Name	Maker	Type Name	Package Type
DATA I/O	121B	Hitachi	HS460ESF01H	FP-80B
	29B		HS460ESH01H	FP-80A
			Under development	TFP-80
AVAL Corp.	PKW-1000	Hitachi	HS460ESF01H	FP-80B
			HS460ESH01H	FP-80A
			Under development	TFP-80

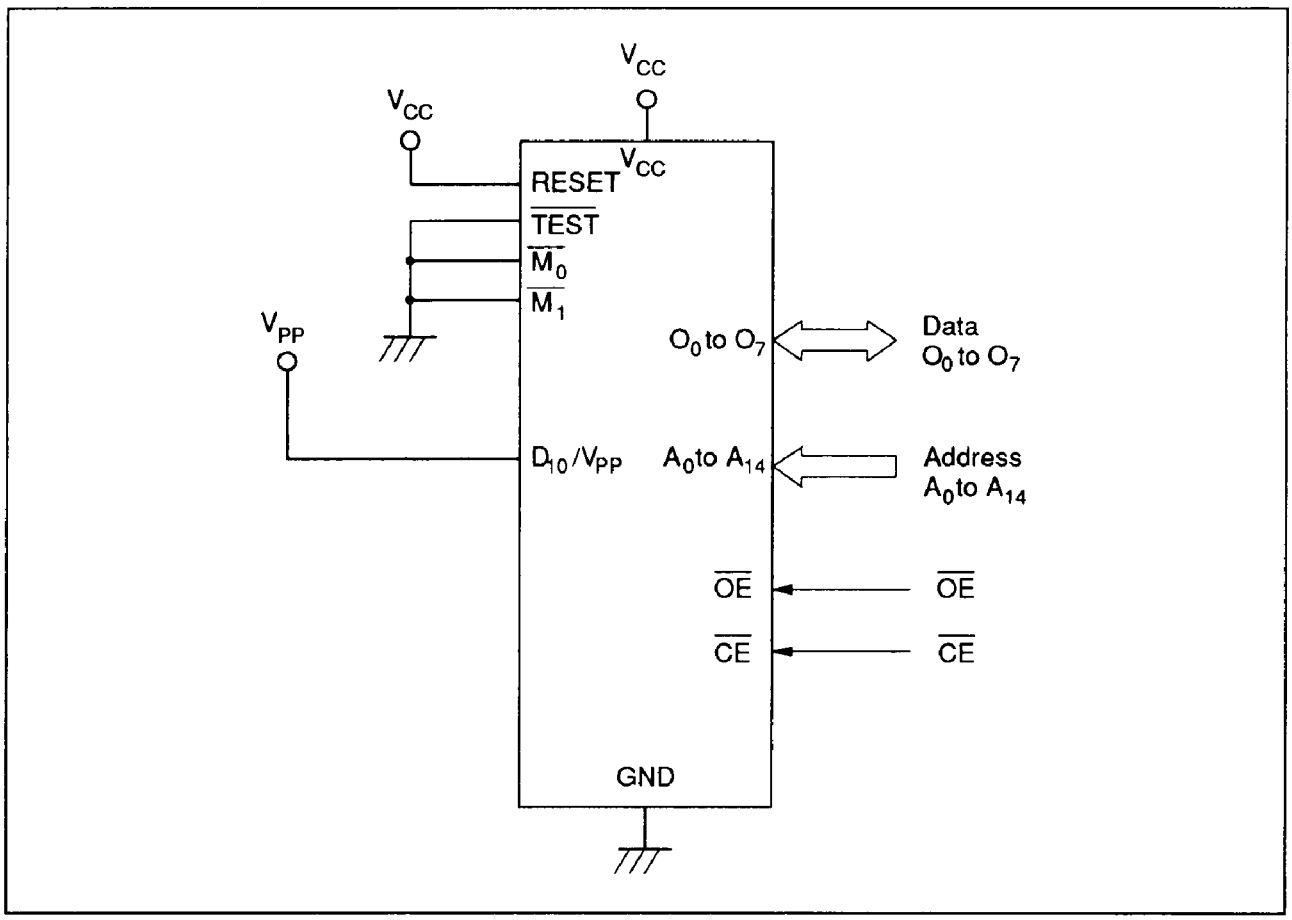


Figure 36 PROM Mode Function Diagram

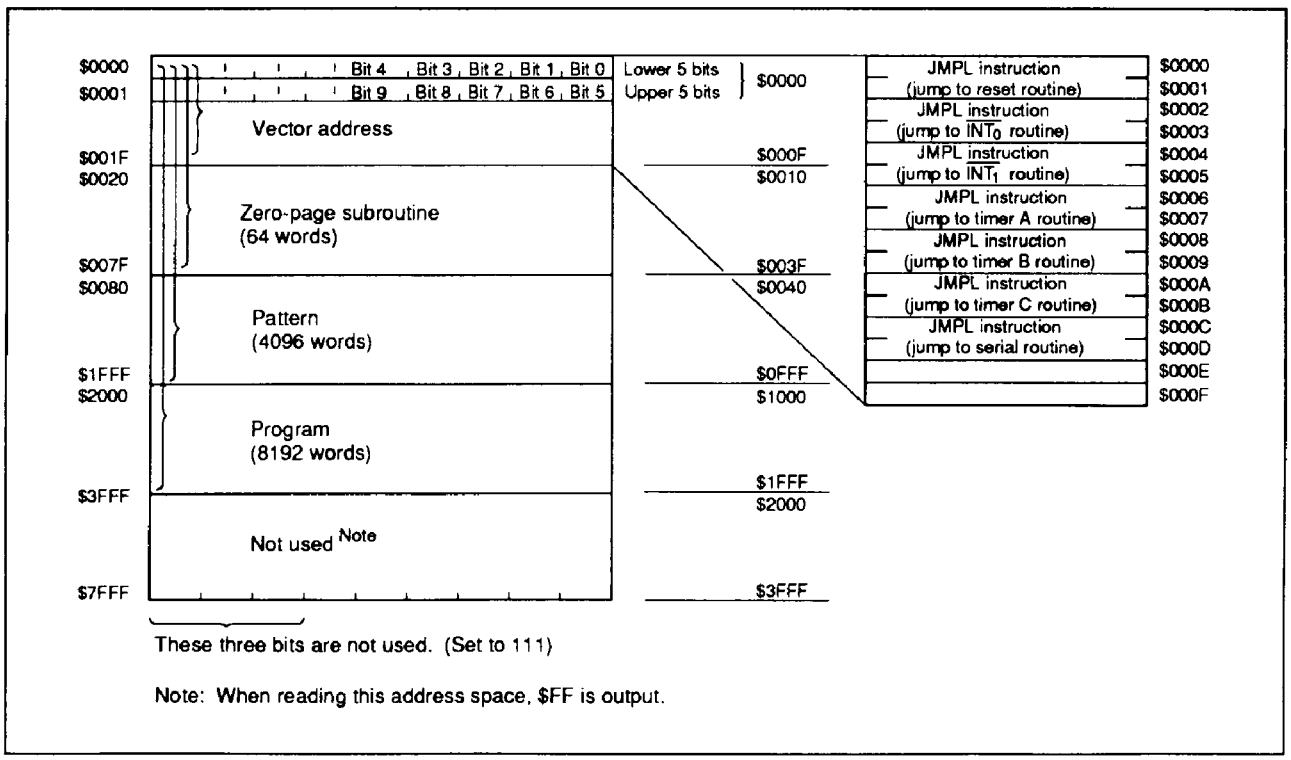


Figure 37 PROM Mode Memory Map

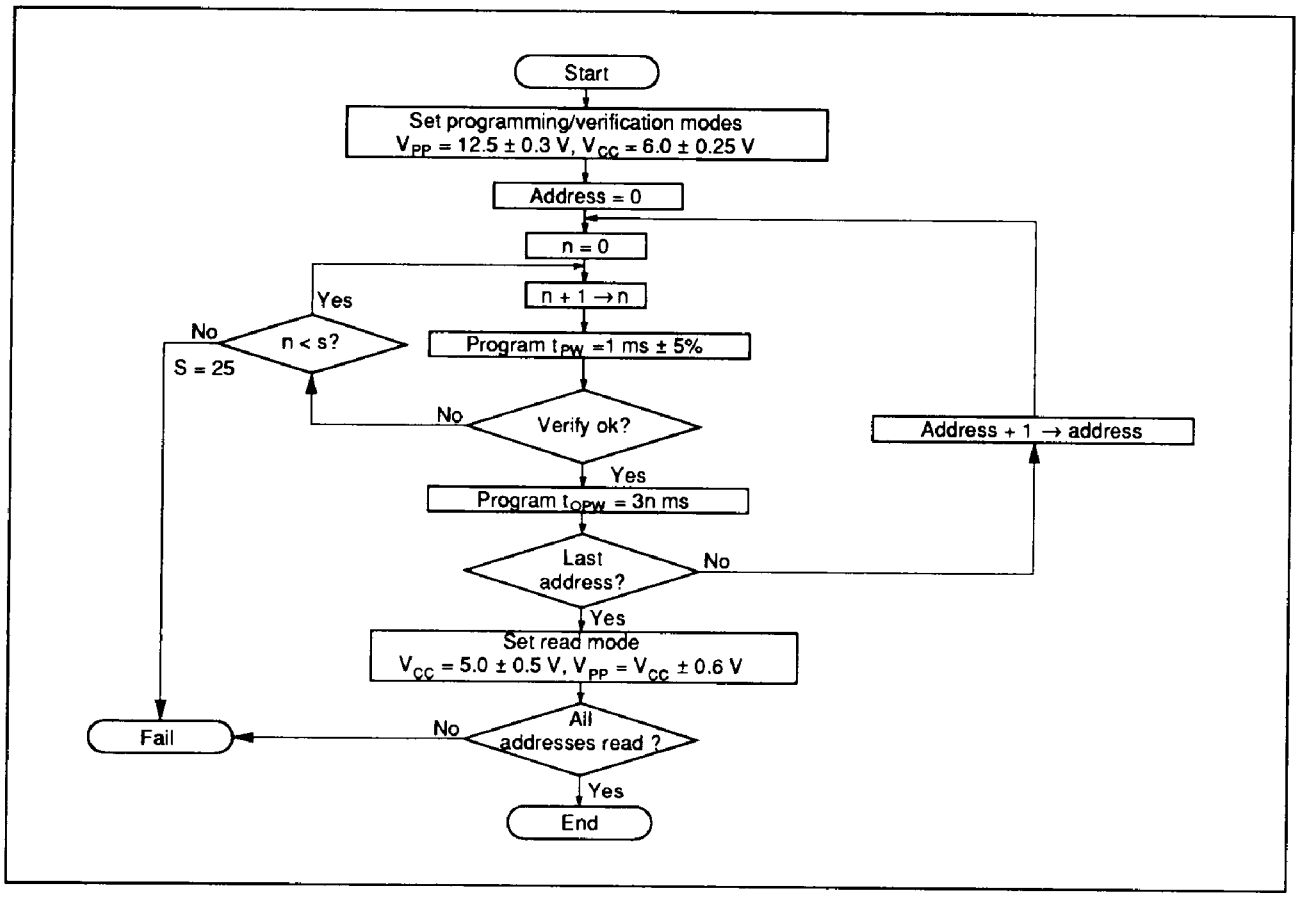


Figure 38 High-Speed Programming Flowchart

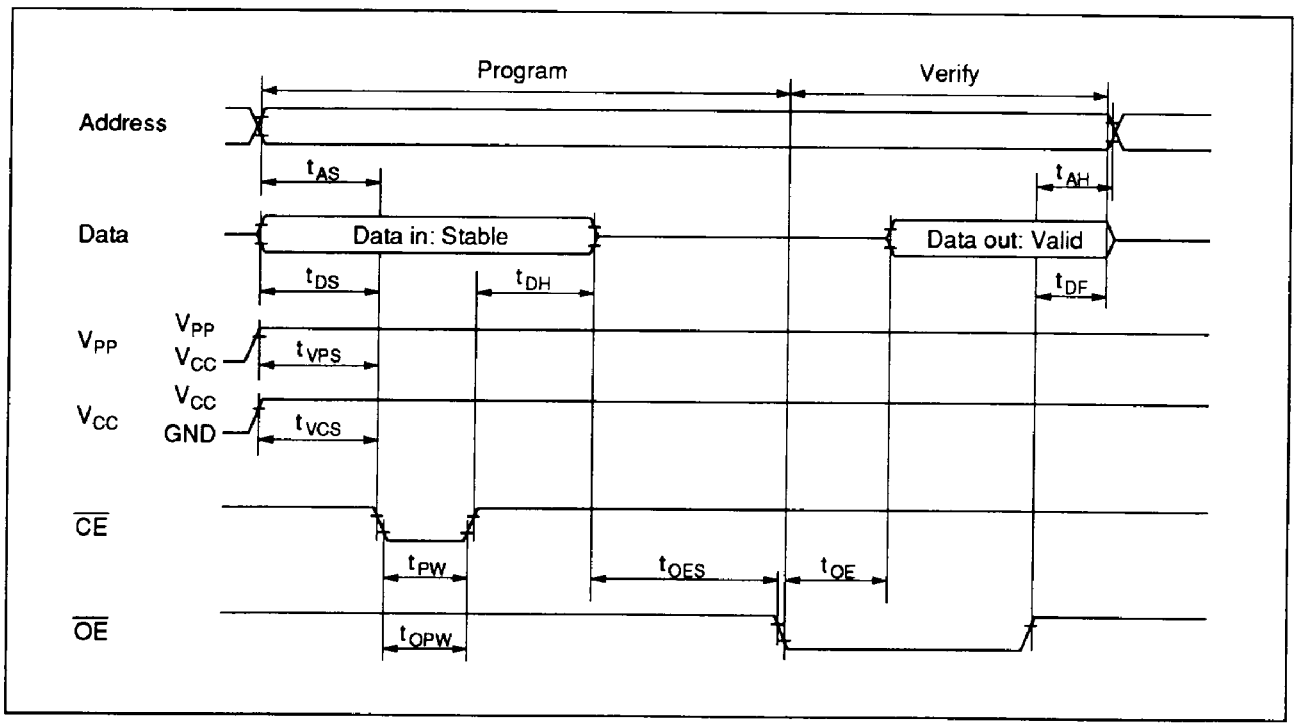


Figure 39 PROM Programming/Verification Timing

Programming and Verification Electrical Characteristics

DC Characteristics

(V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, V_{SS} = 0 V, T_a = 25°C ± 5°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition
Input high voltage	V_{IH}	O_0–O_7, A_0–A_{14}, $\overline{OE}$, $\overline{CE}$	2.2		V_{CC} + 0.3	V	
Input low voltage	V_{IL}	O_0–O_7, A_0–A_{14}, $\overline{OE}$, $\overline{CE}$	–0.3		0.8	V	
Output high voltage	V_{OH}	O_0–O_7	2.4			V	I_{OH} = –200 µA
Output low voltage	V_{OL}	O_0–O_7			0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\lvert I_{IL} \rvert$	O_0–O_7, A_0–A_{14}, $\overline{OE}$, $\overline{CE}$			2	µA	V_{IN} = 5.25 V/0.5 V
V_{CC} current	I_{CC}				30	mA	
V_{PP} current	I_{PP}				40	mA	

AC Characteristics

(V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25°C ± 5 °C, unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Address setup time	t_{AS}	2			µs	See figure 39; Input pulse level: 0.8 to 2.2 V; Input rising/falling time ≤ 20 ns; Input timing reference levels: 1.0 V, 2.0 V; Output timing reference levels: 0.8 V, 2.0 V
$\overline{OE}$ setup time	t_{OES}	2			µs	
Data setup time	t_{DS}	2			µs	
Address hold time	t_{AH}	0			µs	
Data hold time	t_{DH}	2			µs	
Output disable delay time	t_{DF}			130	ns	
V_{PP} setup time	t_{VPS}	2			µs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ pulse width when overprogramming	t_{OPW}	2.85		78.75	ms	
V_{CC} setup time	t_{VCS}	2			µs	
Data output delay time	t_{OE}	0		500	ns	

Precautions on PROM Programming

Principles of PROM Programming/Erasing

The ZTAT™ microcomputer has the same type of memory cell as an EPROM. The PROM is programmed by applying a high voltage to the control gate and drain, and injecting hot electrons into the floating gate, in the same way as EPROM programming. The electrons in the floating gate remain stabilized, surrounded by an energy barrier of SiO_2 film. By these electrons, the threshold voltage in the memory cell changes and the corresponding bit goes to 0.

The hot electrons are reduced over time. This reduction is caused by the following:

- Ultraviolet light: The electrons are discharged by ultraviolet light (according to the erasure principle).
- Heat: The electrons, which are excited by heat, are discharged.
- Application of high voltage: The number of electrons is reduced due to the high voltage which is applied to the control gate and drain.

If there is any failure in the oxide film, the charge is markedly reduced; however, in general such a reduction does not occur since devices which failed are usually excluded during screening tests.

When the memory cell does not have any hot electrons in the floating gate, the corresponding bit goes to 1.

PROM Programming

PROM programming should be performed under specified voltage and timing conditions. The higher the program voltage (V_{PP}) and the longer the program pulse width (t_{PW}), the more electrons will be injected into the memory cell. If an overvoltage is applied, a pn junction may be permanently damaged. It is especially important to note that an overshoot occurs in the PROM writer. Moreover, negative voltage noise causes a parasitic transistor effect, which can reduce the apparent breakdown voltage.

During PROM programming, the ZTAT™ microcomputer is electrically connected with the PROM writer via the socket adapter. The user should ensure the following:

- Check that the socket adapter is firmly connected to the PROM writer before beginning PROM programming.
- Do not touch the socket adapter and the LSI during programming; this can cause faulty contacts, resulting in programming errors.

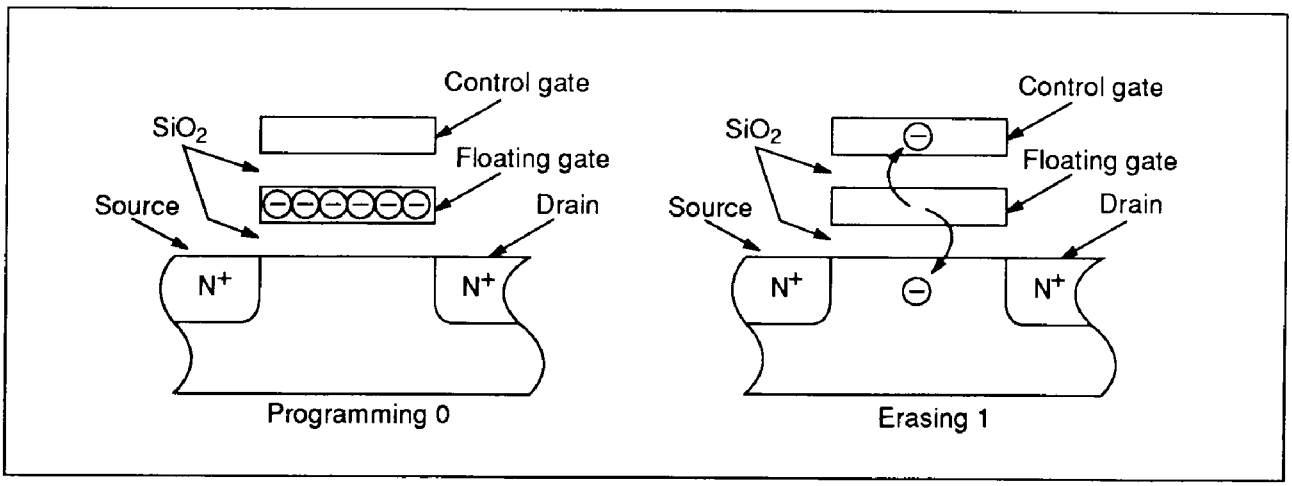


Figure 40 Cross-Sections of a EPROM Memory Cell

PROM Reliability after Programming: In general, semiconductor devices retain their reliability, if initial failures can be rejected. The initial failures can be rejected by adequate screening. Baking the device under high-temperature conditions is a screening method which eliminates initial short-time data hold failures in the memory cell. (See the previous Principles of PROM Programming/Erasing section). ZTAT™ microcomputer devices realize good reliability because they have been subjected to such screening during the wafer fabrication process. It is recommended that the user expose the device to 150°C at one atmosphere after programming in order to verify device performance.

Figure 41 shows the recommended screening procedure.

Note: If programming errors occur sequentially during PROM programming, the user should suspend programming and determine whether there is any trouble with the PROM writer or the socket adapter. If programming verification indicates errors in programming or after high-temperature exposure, please inform Hitachi of the trouble.

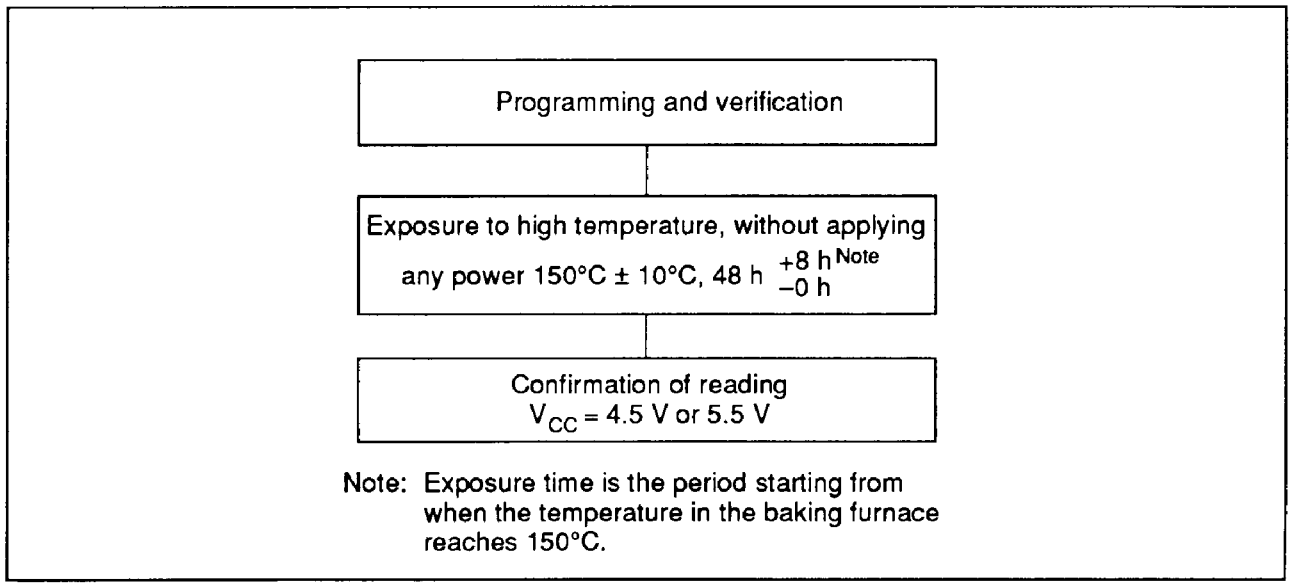


Figure 41 Recommended Screening Procedure

Addressing Modes

RAM Addressing Modes

As shown in figure 42, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing Mode: The W register, X register, and Y register contents (10 bits total) are used as the RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing Mode: The memory registers (16 digits from $040 to $04F) are accessed by executing the LAMR and XMRA instructions.

ROM Addressing Modes and the P Instruction

The MCU has four kinds of ROM addressing modes as shown in figure 43.

Direct Addressing Mode: The program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 32 pages of ROM with 256 words per page. By executing the BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with 8-bit immediate data.

When the BR instruction is on a page boundary (256n + 255) (figure 44), executing it transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR instruction is used on a page boundary. The HMCS400 series cross macroassembler has an automatic paging facility for ROM pages.

Zero-Page Addressing Mode: By executing the CAL instruction, the program can branch to the zero-page subroutine area, which is located at $0000–$003F. When the CAL instruction is executed, 6-bit immediate data is placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing Mode: By executing the TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referenced by the P instruction (figure 45). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output registers. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

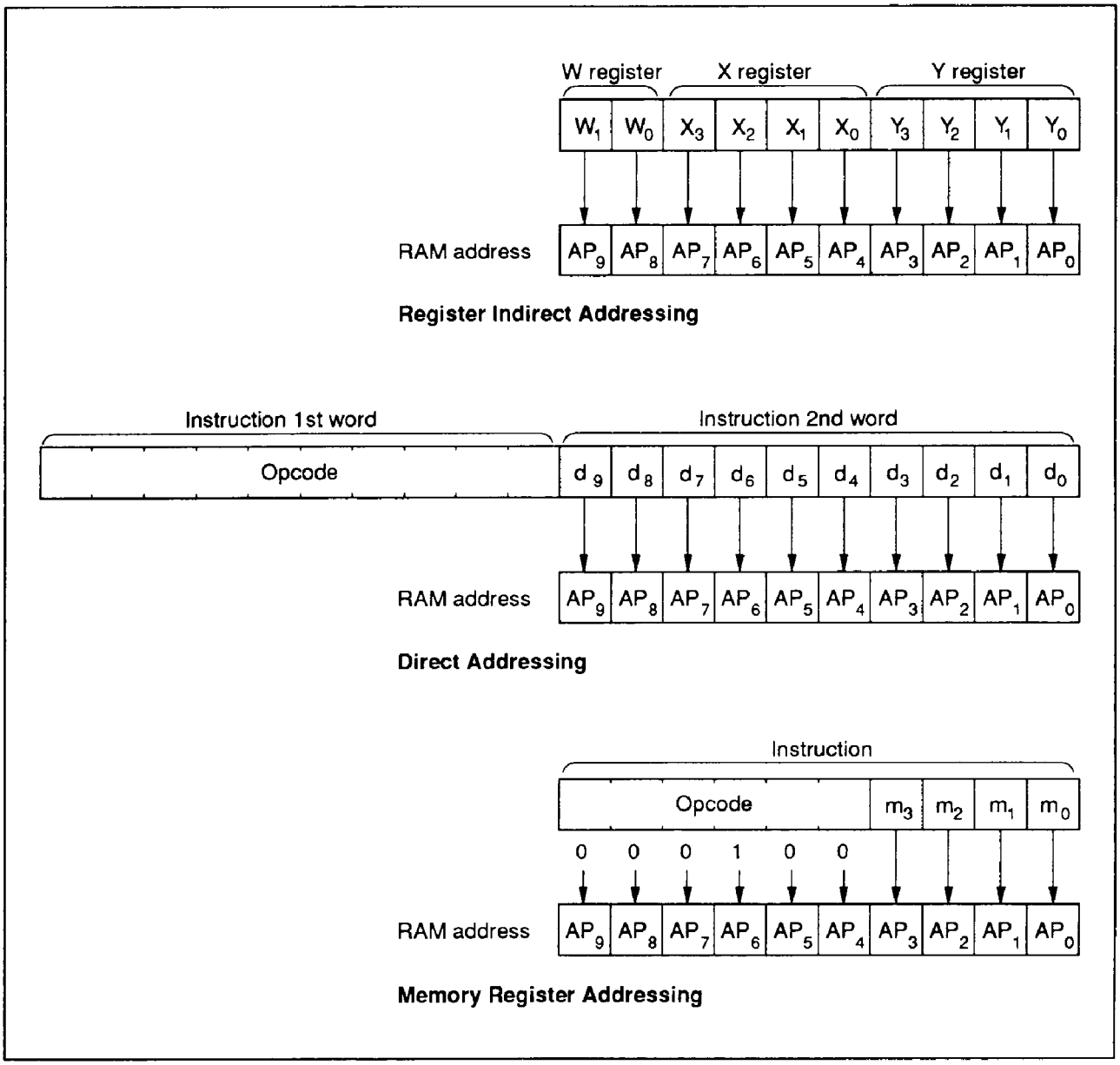


Figure 42 RAM Addressing Modes

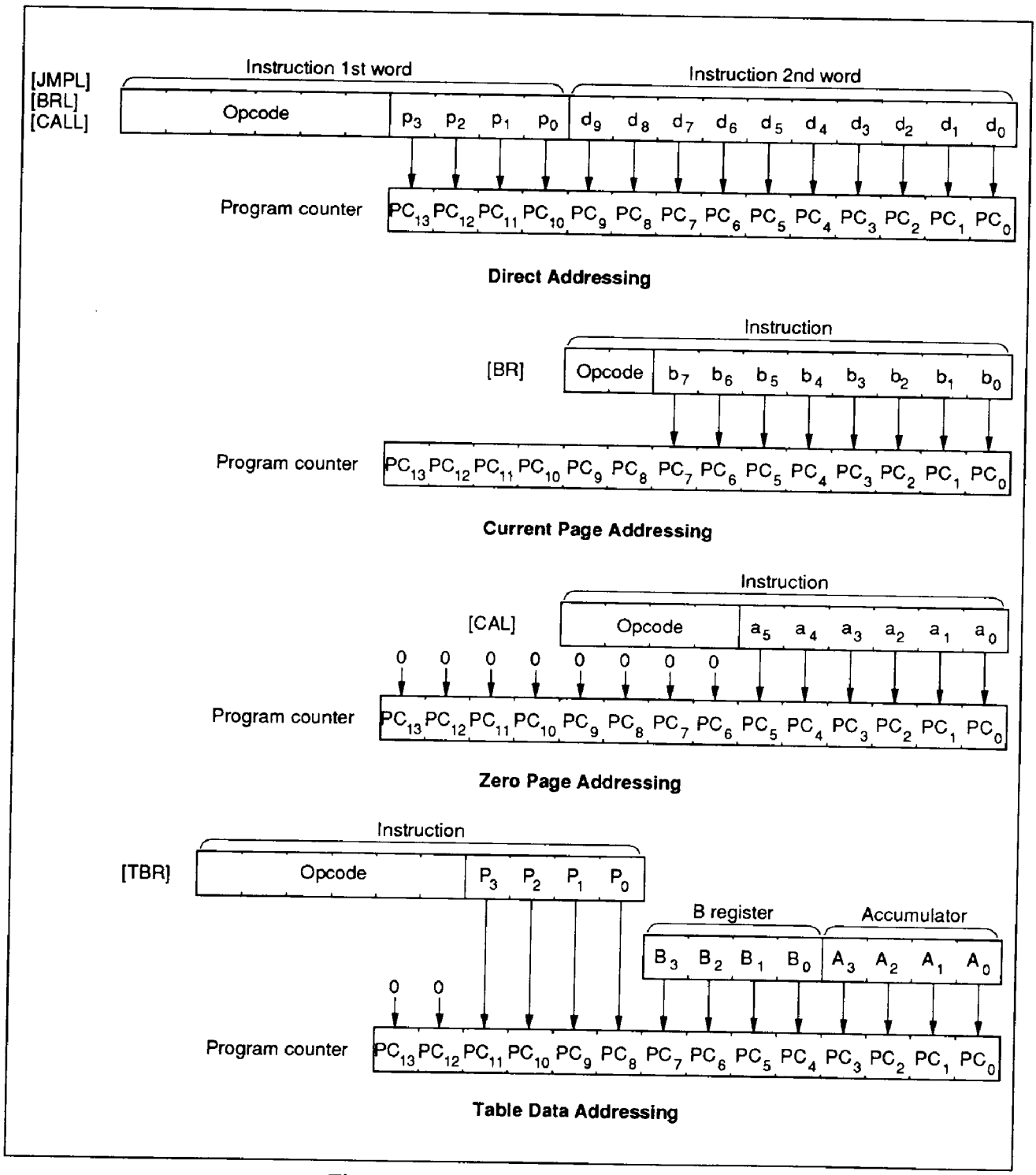


Figure 43 ROM Addressing Modes

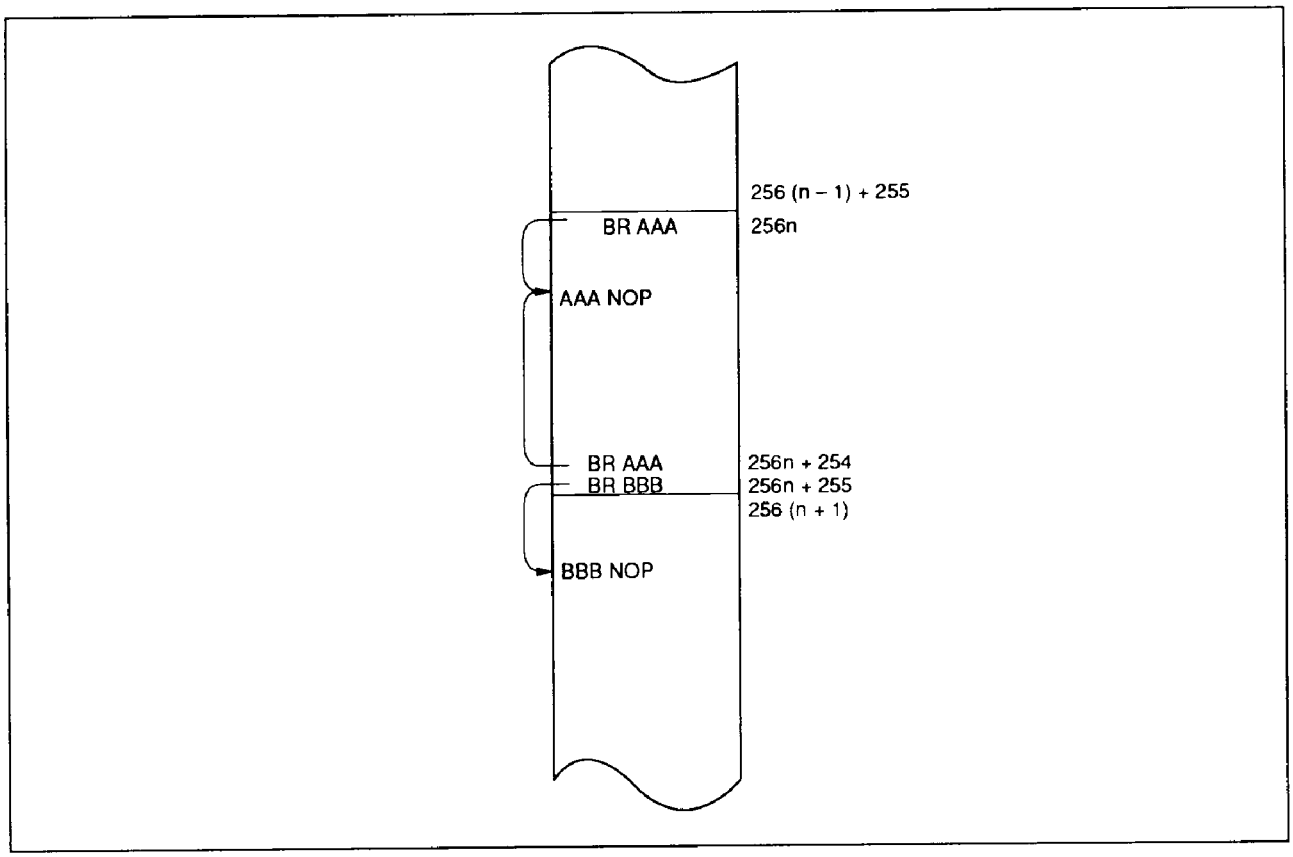


Figure 44 Page Boundary between BR Instruction and Branch Destination

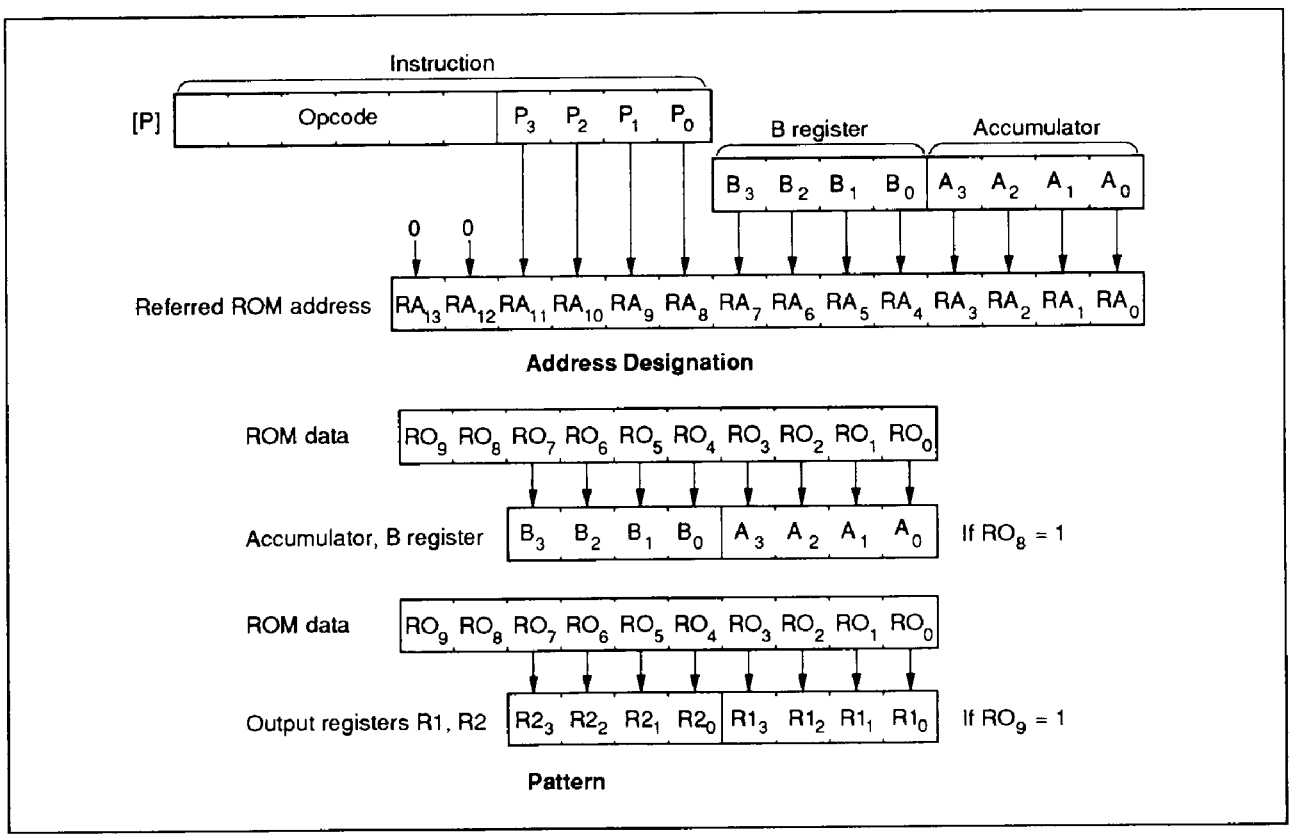


Figure 45 P Instruction

Absolute Maximum Ratings

HD404818, HD404814, and HD4074818 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	2
Pin voltage	V_T	–0.3 to V_{CC} +0.3	V	
Total permissible input current	ΣI_o	100	mA	3
Total permissible output current	$-\Sigma I_o$	50	mA	4
Maximum input current	I_o	4	mA	5, 6
		30	mA	5, 7
Maximum output current	$-I_o$	4	mA	8, 9
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation should be under the conditions of the electrical characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of the LSI.
2. D_{10} (V_{PP}) of the HD4074818.
3. Total permissible input current is the sum of the input currents which flow in from all I/O pins to GND simultaneously.
4. Total permissible output current is the sum of the output currents which flow out from V_{CC} to all I/O pins simultaneously.
5. Maximum input current is the maximum amount of input current from each I/O pin to GND.
6. R0–R3.
7. D_0–D_9.
8. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
9. D_0–D_9 and R0–R3.

HD40L4818, HD40L4814, and HD407L4818 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	2
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	
Total permissible input current	ΣI_o	100	mA	3
Total permissible output current	$-\Sigma I_o$	50	mA	4
Maximum input current	I_o	4	mA	5, 6
		30	mA	5, 7
Maximum output current	$-I_o$	4	mA	8, 9
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	
Storage temperature (bias)	T_{bias}	–25 to +80	°C	

Notes: 1. Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation should be under the conditions of the electrical characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of the LSI.
2. D_{10} (V_{PP}) of the HD407L4818.
3. Total permissible input current is the sum of the input currents which flow in from all I/O pins to GND simultaneously.
4. Total permissible output current is the sum of the output currents which flow out from V_{CC} to all I/O pins simultaneously.
5. Maximum input current is the maximum amount of input current from each I/O pin to GND.
6. R0–R3.
7. D_0–D_9.
8. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
9. D_0–D_9 and R0–R3.

Electrical Characteristics

HD404818, HD404814, and HD4074818 Electrical Characteristics

DC Characteristics

(HD404818, HD404814: V_{CC} = 4 to 6 V; HD4074818: V_{CC} = 4 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	RESET, $\overline{SCK}$, $\overline{INT_0}$, SI, $\overline{INT_1}$	0.8V_{CC}		V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5		V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{SCK}$, $\overline{INT_0}$, SI, $\overline{INT_1}$	–0.3		0.2V_{CC}	V		
		OSC_1	–0.3		0.5	V		
Output high voltage	V_{OH}	$\overline{SCK}$, TIMO, SO	V_{CC} – 1.0			V	$-I_{OH}$ = 1.0 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, TIMO, SO			0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\|I_{IL}\|$	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, TIMO, OSC_1			1	µA	V_{in} = 0 V to V_{CC}	1
Stop mode retaining voltage	V_{STOP}	V_{CC}	2			V	Without 32-kHz oscillator	5
Current dissipation in active mode	I_{CC1}	V_{CC}		3.5	7	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2, 4
	I_{CC2}	V_{CC}		6	12	mA	V_{CC} = 5 V, f_{OSC} = 4 MHZ, analog input mode (D_{12}/D_{13})	4, 6
Current dissipation in standby mode	I_{STBY}	V_{CC}		1	2	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3, 4
Current dissipation in subactive mode	I_{SUB}	V_{CC}		150	300	µA	V_{CC} = 5 V, LCD: On	7
				75	150			
Current dissipation in watch mode (1)	I_{WTC1}	V_{CC}		10	20	µA	V_{CC} = 5 V, LCD: Off	
Current dissipation in watch mode (2)	I_{WTC2}	V_{CC}		25	50	µA	V_{CC} = 5 V, LCD: On	
Current dissipation in stop mode	I_{STOP}	V_{CC}		1	10	µA	V_{CC} = 5 V, Without 32-kHz osc.	

Notes:
1. Excluding output buffer current.
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state
   - RESET, $\overline{TEST}$: V_{CC}
3. The timer operates and input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - Serial interface: Stop
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_{12}, D_{13}: Digital input mode
4. When f_{OSC} = x MHz, estimate the current dissipation as follows:
   Max. value f_{OSC} = x [MHz] = x/4 × max. value (f_{OSC} = 4 MHz)
5. RAM data retention.
6. D_{12}/D_{13} is in the analog input mode.
   Input/output current does not flow. VC_{ref}, D_{12}, D_{13}: GND
7. Applies to the HD404818 and HD404814.

Input/Output Characteristics for Standard Pins

(HD404818, HD404814: V_{CC} = 4 to 6 V; HD4074818: V_{CC} = 4 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Test Condition	Unit
Input high voltage	V_{IH}	D_0–D_{13}, R0– R3	0.7V_{CC}		V_{CC} + 0.3		V
Input low voltage	V_{IL}	D_0–D_{13}, R0–R3	–0.3		0.3V_{CC}		V
Output high voltage	V_{OH}	R0–R3	V_{CC} – 1.0			$-I_{OH}$ = 1.0 mA	V
Pull-up MOS current	$-I_p$	R0–R3	30	100	180	V_{CC} = 5 V, V_{in} = 0 V	µA
Output low voltage	V_{OL}	R0–R3			0.4	I_{OL} = 1.6 mA	V
Input/Output leakage current[Note]	$\|I_{IL}\|$	D_{11}–D_{13}, R0– R3			1	V_{in} = 0 V to V_{CC}	µA
		D_{10}			20		
Input high voltage	V_{IHA}	D_{12}, D_{13} (analog compare mode)	VC_{ref} + 0.1				V
Input low voltage	V_{ILA}	D_{12}, D_{13} (analog compare mode)			VC_{ref} – 0.1		V
Analog input reference voltage scope	VC_{ref}	VC_{ref}	0		V_{CC} – 1.2		V

Note: Output buffer current is excluded.

Input/Output Characteristics for High Voltage Pins

(HD404818, HD404814: V_{CC} = 4 to 6 V; HD4074818: V_{CC} = 4 to 5.5 V, GND = 0V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Test Condition	Unit
Input high voltage	V_{IH}	D_0–D_9	0.7V_{CC}		V_{CC} + 0.3		V
Input low voltage	V_{IL}	D_0–D_9	–0.3		0.3V_{CC}		V
Output high voltage	V_{OH}	D_0–D_9	V_{CC} – 1.0			$-I_{OH}$ = 1.0 mA	V
Pull-up MOS current	$-I_p$	D_0–D_9	30	100	180	V_{CC} = 5 V, V_{in} = 0 V	µA
Output low voltage	V_{OL}	D_0–D_9			2.0	I_{OL} = 15 mA, V_{CC} = 4.5 to 6 V	V
					0.4	I_{OL} = 1.6 mA	V
Input/output leakage current[Note]	$\|I_{IL}\|$	D_0–D_9			1	V_{in} = 0 V – V_{CC}	µA

Note: Output buffer current is excluded.

Liquid Crystal Circuit Characteristics

(HD404818, HD404814: V_{CC} = 4 to 6 V; HD4074818: V_{CC} = 4 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Segment driver voltage drop	V_{ds}	SEG1 to SEG32			0.6	V	I_d = 3 µA	1
Common driver voltage drop	V_{dc}	COM1 to COM4			0.3	V	I_d = 3 µA	1
LCD power supply dividing resistance	R_{well}		100	300	900	kΩ		
LCD voltage	V_{LCD}	V_1	4		V_{CC}	V		2

Notes: 1. Voltage drops from pins V_1, V_2, V_3, and GND to each segment and common pin.
2. Keep the relation $V_{CC} > V_1 > V_2 > V_3 > GND$ when V_{LCD} is supplied by an external power supply.

AC Characteristics

(HD404818, HD404814: V_{CC} = 4 to 6 V; HD4074818: V_{CC} = 4 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	1.6	4.0	4.2	MHz		
		X1, X2		32.768		kHz		
Oscillation frequency	f_{OSC}	OSC_1, OSC_2 (Without 32 kHz)	0.25	4.0	4.2	MHz		
Instruction cycle time	t_{cyc}		0.95	1	2.5	µs		
			0.95	1	16		Without 32 kHz	
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2			30	ms	Crystal	1
					7.5	ms	Ceramic filter f_{OSC} = 4 MHz	1
		X1, X2			3	s	T_a = –10° to 60°C	2
External clock frequency	t_{CP}	OSC_1	1.6		4.2	MHz		3
			0.25		4.2	MHz	Without 32 kHz	3
External clock high width	t_{CPH}	OSC_1	110			ns		3
External clock low width	t_{CPL}	OSC_1	110			ns		3
External clock rise time	t_{CPr}	OSC_1			20	ns		3
External clock fall time	t_{CPf}	OSC_1			20	ns		3
$\overline{INT_0}$ high width	t_{I0H}	$\overline{INT_0}$	2			t_{cyc}/ t_{SUBcyc}		4, 6
$\overline{INT_0}$ low width	t_{I0L}	$\overline{INT_0}$	2			t_{cyc}/ t_{SUBcyc}		4, 6
$\overline{INT_1}$ high width	t_{I1H}	$\overline{INT_1}$	2			t_{cyc}		4
$\overline{INT_1}$ low width	t_{I1L}	$\overline{INT_1}$	2			t_{cyc}		4
RESET high width	t_{RSTH}	RESET	2			t_{cyc}		5
Input capacitance	C_{in}	D_{10}			90	pF	f = 1 MHz, V_{in} = 0 V	8
		All pins except D_{10}			15	pF	f = 1 MHz, V_{in} = 0 V	
RESET fall time	t_{RSTf}				20	ms		5
Analog comparator stabilization time	t_{CSTB}	D_{12}, D_{13}			2	t_{cyc}		7

Notes: 1. The oscillator stabilization time is the period up until the time the oscillator (see figure 46) stabilizes after V_{CC} reaches 4.0 V at power-on, or after RESET goes high. At power-on or stop mode release, RESET must be kept high for at least t_{RC}. Since t_{RC} depends on the ceramic filter's circuit constant and stray capacitance, consult with the manufacturer when designing the reset circuit.

2. The oscillator stabilization time is the period up until the time the oscillator (see figure 47) stabilizes after V_{CC} reaches 4.0 V at power-on. The time required to stabilize the oscillator (t_{RC}) must be obtained. Since t_{RC} depends on the crystal circuit constant and stray capacitance, consult with the manufacturer.
3. See figure 48.
4. See figure 49. The unit t_{cyc} is applied when the MCU is in standby mode or active mode.
5. See figure 50.
6. See figure 49. The unit t_{SUBcyc} is applied when the MCU is in watch mode or subactive mode. t_{SUBcyc} = 244.14 µs (when a 32.768-kHz crystal oscillator is used.)
7. The analog comparator stabilization time is the period up until the analog comparator stabilizes and correct data can be read after entering D_{12}/D_{13} into the analog input mode.
8. The maximum value for the HD404818 and HD404814 is 15 pF.

Serial Interface Timing Characteristics

During Transmit Clock Output

(HD404818, HD404814: V_{CC} = 4 to 6 V; HD4074818: V_{CC} = 4 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1			t_{cyc}/ t_{SUBcyc}		1, 2, 4
Transmit clock high and low widths	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.5			t_{Scyc}		1, 2
Transmit clock rise and fall times	t_{SCKr}, t_{SCKf}	$\overline{SCK}$			100	ns		1, 2
Serial output data delay time	t_{DSO}	SO			300	ns		1, 2
Serial input data setup time	t_{SSI}	SI	200			ns		1
Serial input data hold time	t_{HSI}	SI	150			ns		1

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1			t_{cyc}/ t_{SUBcyc}		1, 4
Transmit clock high and low widths	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.5			t_{Scyc}		1
Transmit clock rise and fall times	t_{SCKr}, t_{SCKf}	$\overline{SCK}$			100	ns		1
Serial output data delay time	t_{DSO}	SO			300	ns		1, 2
Serial input data setup time	t_{SSI}	SI	200			ns		1
Serial input data hold time	t_{HSI}	SI	150			ns		1
Transmit clock completion detect time	t_{SCKHD}	$\overline{SCK}$	1			t_{cyc}/ t_{SUBcyc}		1,2, 3, 4

Notes: 1. See figure 51.
2. See figure 52.
3. The transmit clock completion detect time is the high level period after 8 pulses of transmit clocks are input. The SCI interrupt request flag is not set when the next transmit clock is input before the transmit clock completion detect time has passed.
4. The unit t_{SUBcyc} is applied when the MCU is in subactive mode. t_{SUBcyc} = 244.14 µs (for a 32.168-kHz crystal oscillator).

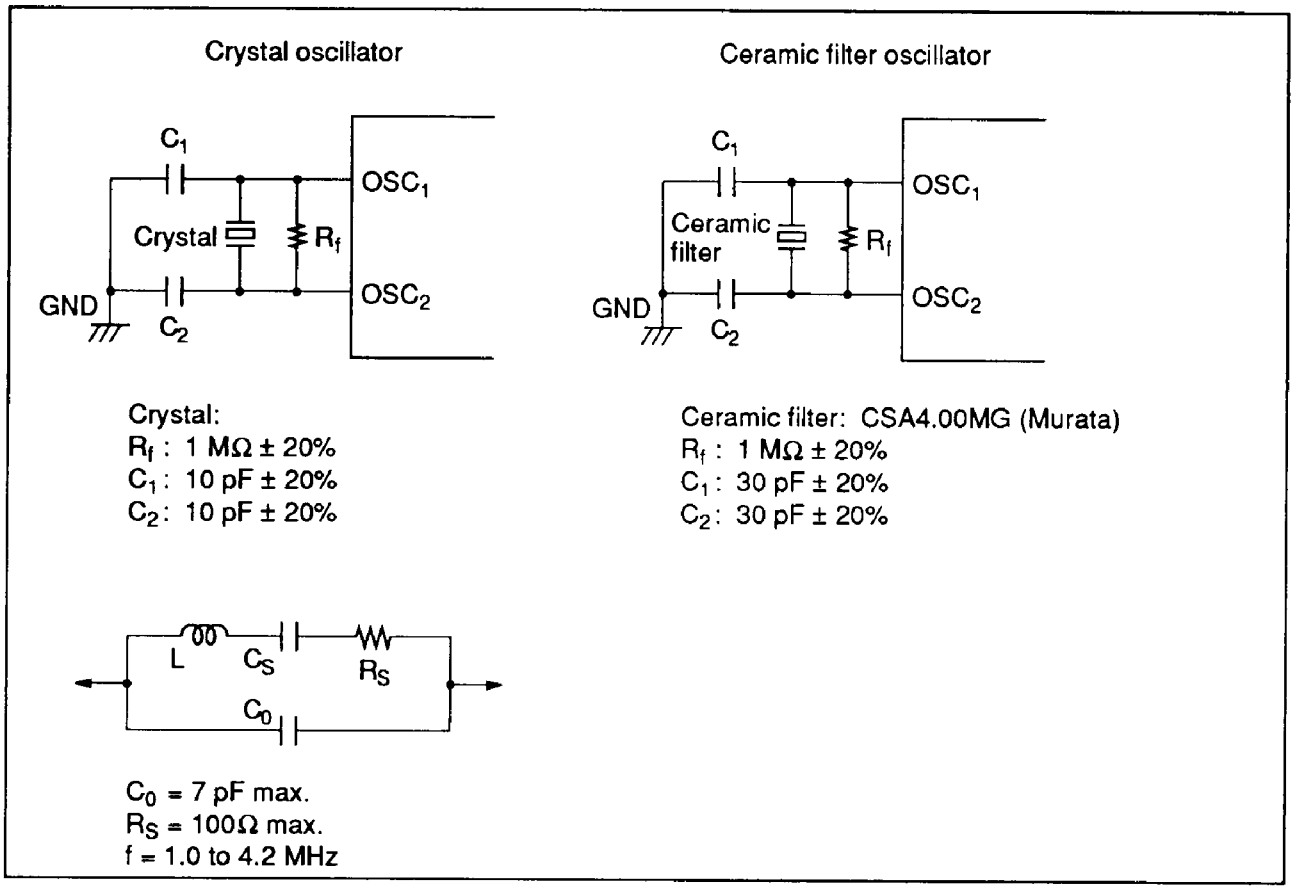


Figure 46 Oscillator Circuits (1)

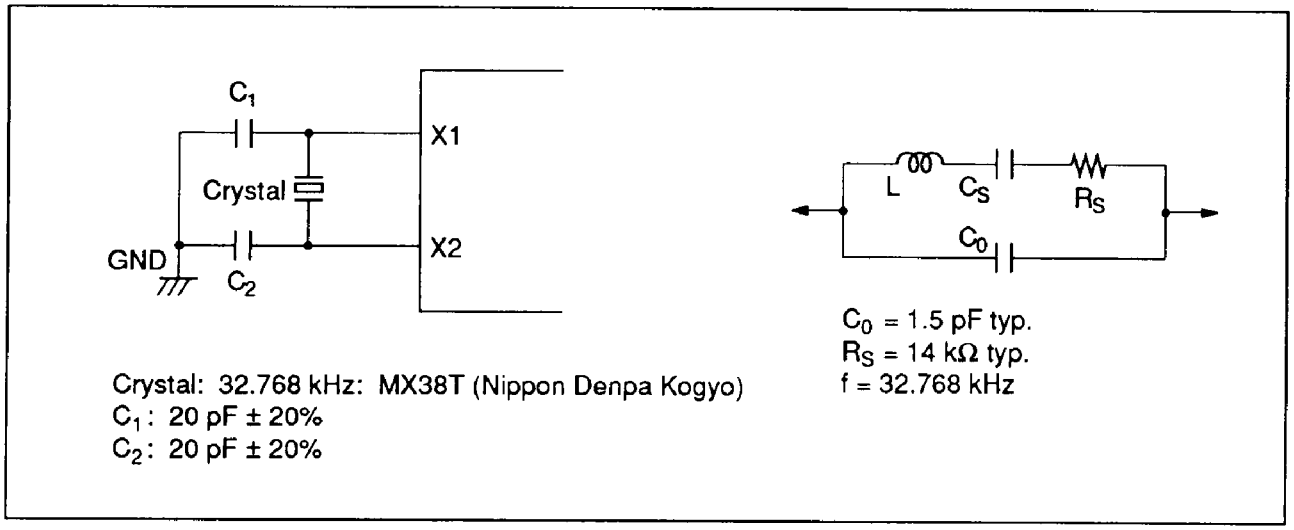


Figure 47 Oscillator Circuits (2)

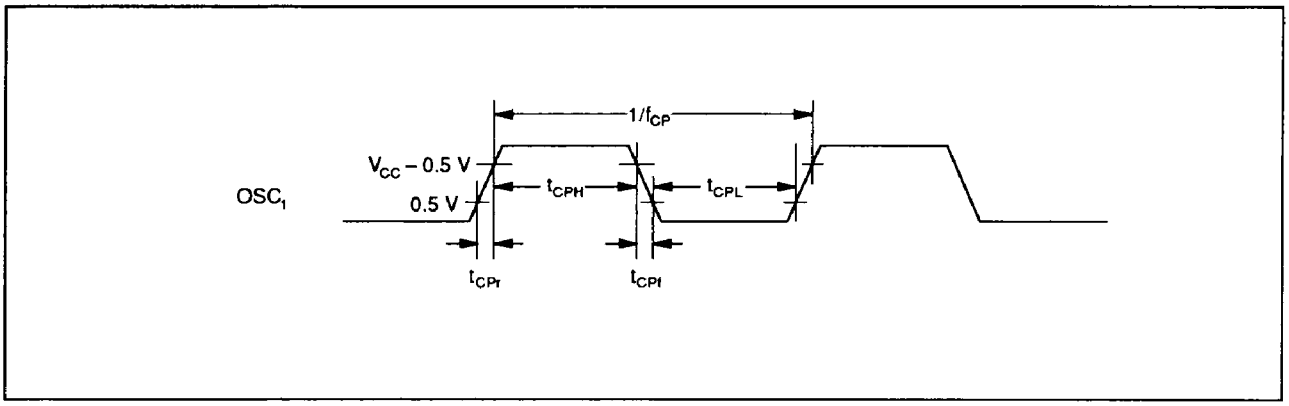


Figure 48 Oscillator Timing

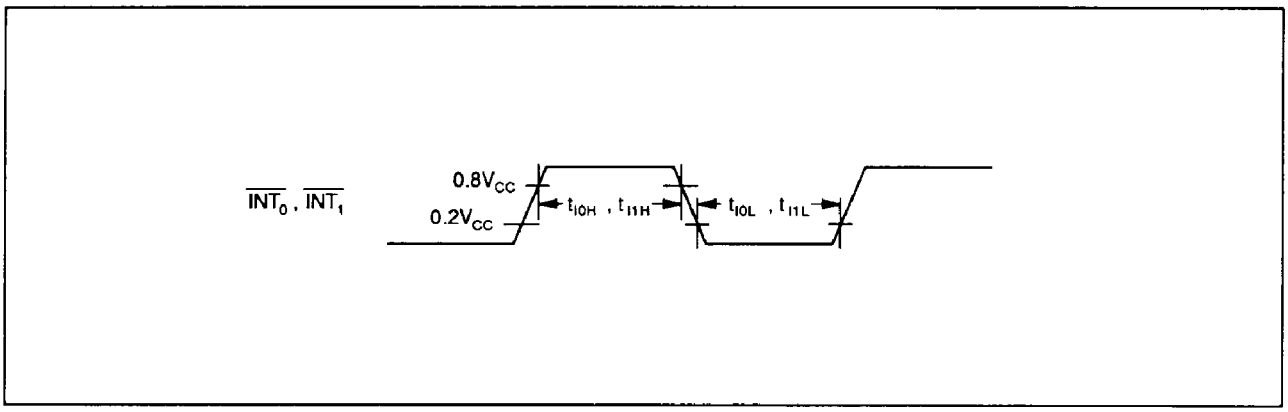


Figure 49 Interrupt Timing

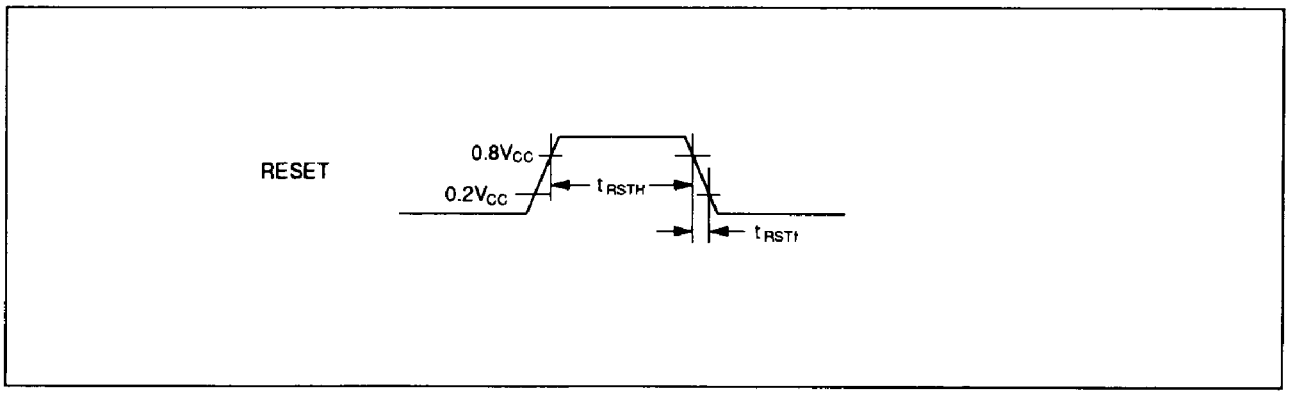


Figure 50 Reset Timing

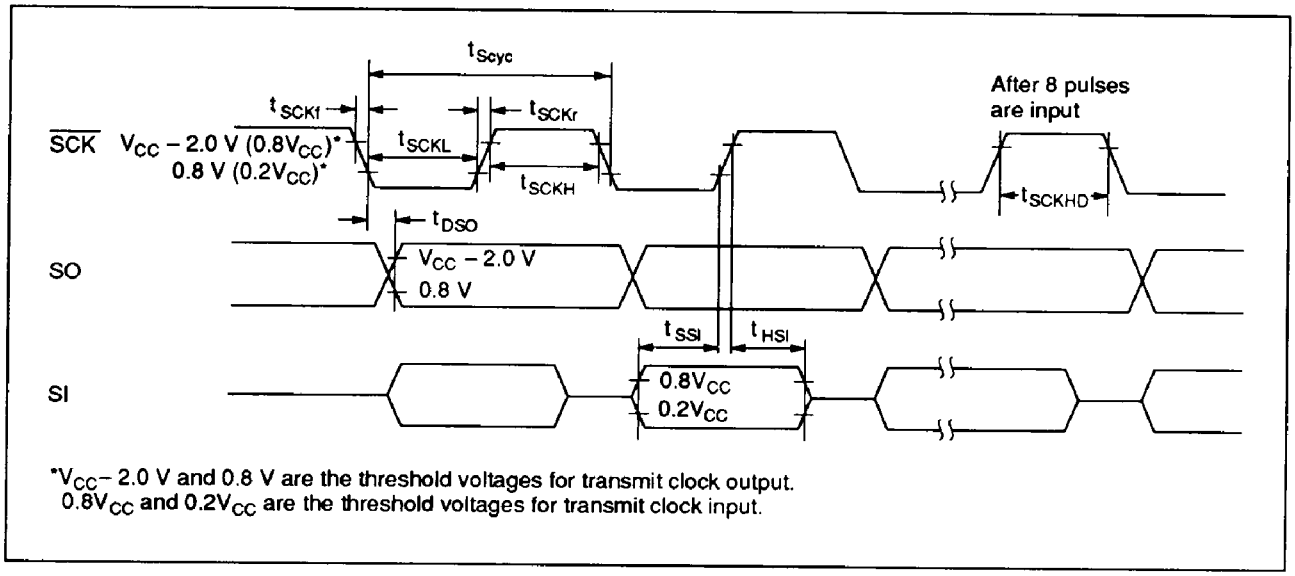


Figure 51 Timing of Serial Interface

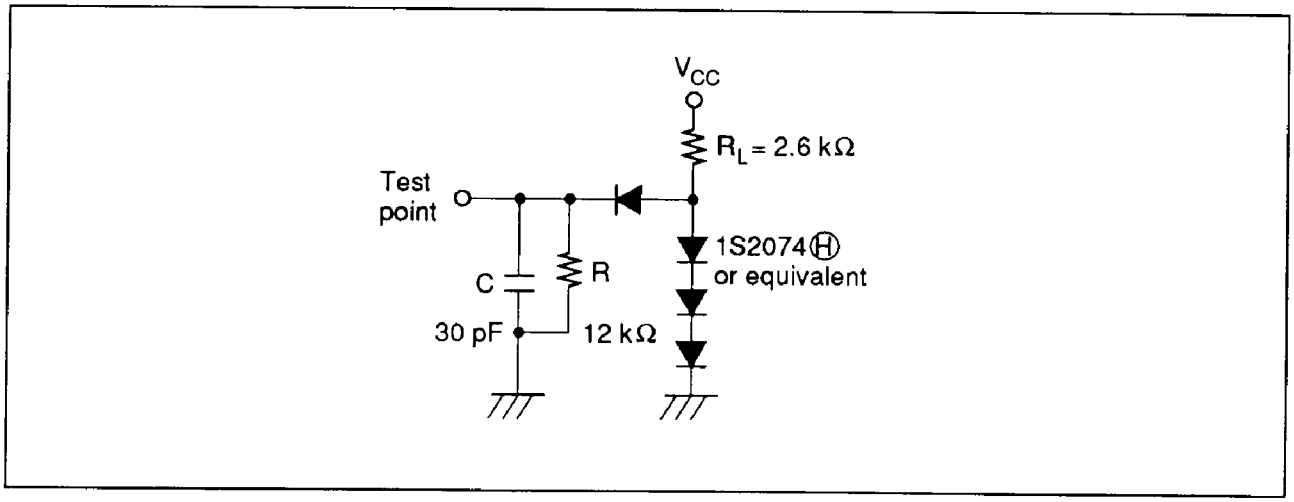


Figure 52 Timing Load Circuit

Electrical Characteristics

HD40L4818, HD40L4814, and HD407L4818 Electrical Characteristics

DC Characteristics

(HD40L4818, HD40L4814: V_{CC} = 2.7 to 6 V; HD407L4818: V_{CC} = 3 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	RESET, $\overline{SCK}$, $\overline{INT_0}$, SI, $\overline{INT_1}$	0.9V_{CC}		V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.3		V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{SCK}$, $\overline{INT_0}$, SI, $\overline{INT_1}$	–0.3		0.1V_{CC}	V		
		OSC_1	–0.3		0.3	V		
Output high voltage	V_{OH}	$\overline{SCK}$, TIMO, SO	V_{CC} – 1.0			V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, TIMO, SO			0.4	V	I_{OL} = 0.4 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, TIMO, OSC_1			1	µA	V_{in} = 0 V to V_{CC}	1
Stop mode retaining voltage	V_{STOP}	V_{CC}	2			V	Without 32-kHz oscillator	5
Current dissipation in active mode	I_{CC1}	V_{CC}		400	1000	µA	V_{CC} = 3V	2, 4
	I_{CC2}	V_{CC}		1	2	mA	V_{CC} = 3 V, analog input mode (D_{12}/D_{13})	4, 6
Current dissipation in standby mode	I_{STBY}	V_{CC}		200	500	µA	V_{CC} = 3 V	3, 4
Current dissipation in subactive mode	I_{SUB}	V_{CC}		50	100	µA	V_{CC} = 3 V,	
				35	70		LCD: On	7
Current dissipation in watch mode (1)	I_{WTC1}	V_{CC}		5	15	µA	V_{CC} = 3 V, LCD: Off	
Current dissipation in watch mode (2)	I_{WTC2}	V_{CC}		15	35	µA	V_{CC} = 3 V, LCD: On	
Current dissipation in stop mode	I_{STOP}	V_{CC}		1	10	µA	V_{CC} = 3 V, Without 32-kHz osc.	

Notes:
1. Excluding output buffer current.
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state
   - RESET, $\overline{TEST}$: V_{CC}
3. The timer operates and input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - Serial interface:Stop
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0–D_{13}, R0–R3: V_{CC}
   - D_{12}, D_{13}: Digital input mode
4. f_{osc} = 400 kHz
5. RAM data retention.
6. D_{12}/D_{13} is in the analog input mode.
   Input/output current does not flow. VC_{ref}, D_{12}, D_{13}: GND
7. Applies to the HD40L4818 and HD40L4814.

Input/Output Characteristics for Standard Pins

(HD40L4818, HD40L4814: V_{CC} = 2.7 to 6 V; HD407L4818: V_{CC} = 3 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Test Condition	Unit
Input high voltage	V_{IH}	D_0–D_{13}, R0–R3	$0.7V_{CC}$		V_{CC} + 0.3		V
Input low voltage	V_{IL}	D_0–D_{13}, R0–R3	–0.3		$0.3V_{CC}$		V
Output high voltage	V_{OH}	R0–R3	V_{CC} –1.0			$-I_{OH}$ = 0.5 mA	V
Pull-up MOS current	$-I_p$	R0–R3	5	40	90	V_{CC} = 3 V, V_{in} = 0 V	µA
Output low voltage	V_{OL}	R0–R3			0.4	I_{OL} = 0.4 mA	V
Input/output leakage current[Note]	$\|I_{IL}\|$	D_{11}–D_{13}, R0–R3			1	V_{in} = 0 V to V_{CC}	µA
		D_{10}			20		
Input high voltage	V_{IHA}	D_{12}, D_{13} (Analog compare mode)	VC_{ref} + 0.1				V
Input low voltage	V_{ILA}	D_{12}, D_{13} (Analog compare mode)			VC_{ref} – 0.1		V
Analog input reference voltage	VC_{ref}	VC_{ref}	0		V_{CC} – 1.2		V

Note: Output buffer current is excluded.

Input/Output Characteristics for High Voltage Pins

(HD40L4818, HD40L4814: V_{CC} = 2.7 to 6 V; HD407L4818: V_{CC} = 3 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Test Condition	Unit
Input high voltage	V_{IH}	D_0–D_9	$0.7V_{CC}$		V_{CC} + 0.3		V
Input low voltage	V_{IL}	D_0–D_9	–0.3		$0.3V_{CC}$		V
Output high voltage	V_{OH}	D_0–D_9	V_{CC} –1.0			$-I_{OH}$ = 0.5 mA	V
Pull-up MOS current	$-I_p$	D_0–D_9	5	40	90	V_{CC} = 3 V, V_{in} = 0 V	µA
Output low voltage	V_{OL}	D_0–D_9			2.0	I_{OL} = 15 mA V_{CC} = 4.5 to 6 V	V
					0.4	I_{OL} = 0.4 mA	V
Input/output leakage current[Note]	$\|I_{IL}\|$	D_0–D_9			1	V_{in} = 0 V – V_{CC}	µA

Note: Output buffer current is excluded.

Liquid Crystal Circuit Characteristics

(HD40L4818, HD40L4814: V_{CC} = 2.7 to 6 V; HD407L4818: V_{CC} = 3 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Segment driver voltage drop	V_{ds}	SEG1 to SEG32			0.6	V	I_d = 3 µA	1
Common driver voltage drop	V_{dc}	COM1 to COM4			0.3	V	I_d = 3 µA	1
LCD power supply dividing resistance	R_{well}		100	300	900	kΩ		
LCD voltage	V_{LCD}	V_1			V_{CC}	V		2, 3

Notes: 1. Voltage drops from pins V_1, V_2, V_3, and GND to each segment and common pin.
2. Keep the relation $V_{CC} > V_1 > V_2 > V_3 > GND$ when V_{LCD} is supplied by an external power supply.
3. V_{LCD} min. = 2.7 V (HD40L4818, HD40L4814)
V_{LCD} min. = 3 V (HD407L4818)

AC Characteristics

(HD40L4818, HD40L4814: V_{CC} = 2.7 to 6 V; HD407L4818: V_{CC} = 3 to 5.5 V, GND = 0 V, T_a = −20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.25	0.8	0.9	MHz		
		X1, X2		32.768		kHz		
Instruction cycle time	t_{cyc}		4.45	5	16	µs		
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2			7.5	ms	f_{OSC} = 400 kHz	1
					7.5	ms	f_{OSC} = 800 kHz	1
		X1, X2			3	s	T_a = −10° to 60°C	2
External clock frequency	f_{CP}	OSC_1	0.25		0.9	MHz		
External clock high width	t_{CPH}	OSC_1	525			ns		3
External clock low width	t_{CPL}	OSC_1	525			ns		3
External clock rise time	t_{CPr}	OSC_1			30	ns		3
External clock fall time	t_{CPf}	OSC_1			30	ns		3
$\overline{INT_0}$ high width	t_{I0H}	$\overline{INT_0}$	2			t_{cyc}/ t_{SUBcyc}		4, 6
$\overline{INT_0}$ low width	t_{I0L}	$\overline{INT_0}$	2			t_{cyc}/ t_{SUBcyc}		4, 6
$\overline{INT_1}$ high width	t_{I1H}	$\overline{INT_1}$	2			t_{cyc}		4
$\overline{INT_1}$ low width	t_{I1L}	$\overline{INT_1}$	2			t_{cyc}		4
RESET high width	t_{RSTH}	RESET	2			t_{cyc}		5
Input capacitance	C_{in}	D_{10}			90	pF	f = 1 MHz, V_{in} = 0 V	8
		All pins except D_{10}			15	pF	f = 1 MHz, V_{in} = 0 V	
Reset fall time	t_{RSTf}				20	ms		5
Analog comparator stabilization time	t_{CSTB}	D_{12}, D_{13}			2	t_{cyc}		7

Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches 2.7 V (HD407L4818: V_{CC} = 3.0 V) at power-on until when the oscillator stabilizes, or after RESET goes high. At power-on or recovering from stop mode, RESET must be kept high for more than t_{RC}. Since t_{RC} depends on the ceramic filter's circuit constant and stray capacitance, consult with the ceramic filter manufacturer when designing the reset circuit.

2. The oscillator stabilization time is the period from when V_{CC} reaches 2.7 V (HD407L4818: V_{CC} = 3.0 V) at power-on until when the oscillator stabilizes. The time required to stabilize the oscillator (t_{RC}) must be obtained. Since t_{RC} depends on the ceramic filter's circuit constant and stray capacitance, consult with the ceramic filter manufacturer.
3. See figure 53.
4. See figure 54. The unit t_{cyc} is applied when the MCU is in standby mode or active mode.
5. See figure 55.
6. See figure 54. The unit t_{SUBcyc} is applied when the MCU is in the watch mode or subactive mode. t_{SUBcyc} = 244.14 µs (when a 32.768-kHz crystal oscillator is used.)
7. The analog comparator stabilization time is the period from when D_{12}/D_{13} is input to enter the analog input mode until when the analog comparator stabilizes and correct data can be read.
8. The maximum value of the HD40L4818 and HD40L4814 is 15 pF.

Serial Interface Timing Characteristics

During Transmit Clock Output

(HD40L4818, HD40L4814: V_{CC} = 2.7 to 6 V; HD407L4818: V_{CC} = 3 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1			t_{cyc}/ t_{SUBcyc}		1, 2, 4
Transmit clock high and low widths	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.5			t_{Scyc}		1, 2
Transmit clock rise and fall times	t_{SCKr}, t_{SCKf}	$\overline{SCK}$			200	ns		1, 2
Serial output data delay time	t_{DSO}	SO			500	ns		1, 2
Serial input data setup time	t_{SSI}	SI	300			ns		1
Serial input data hold time	t_{HSI}	SI	300			ns		1

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1			t_{cyc}/ t_{SUBcyc}		1, 4
Transmit clock high and low widths	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.5			t_{Scyc}		1
Transmit clock rise and fall times	t_{SCKr}, t_{SCKf}	$\overline{SCK}$			200	ns		1
Serial output data delay time	t_{DSO}	SO			500	ns		1, 2
Serial input data setup time	t_{SSI}	SI	300			ns		1
Serial input data hold time	t_{HSI}	SI	300			ns		1
Transmit clock completion detect time	t_{SCKHD}	$\overline{SCK}$	1			t_{cyc}/ t_{SUBcyc}		1, 2, 3, 4

Notes: 1. See figure 56.
2 See figure 57.
3. The transmit clock completion detect time is the high level period after 8 pulses of transmit clocks are input. The SCI interrupt request flag is not set when the next transmit clock is input before the transmit clock completion detect time has passed.
4. The unit t_{SUBcyc} is applied when the MCU is in the subactive mode. t_{SUBcyc} = 244.14 µs (for a 32.168-kHz crystal oscillator).

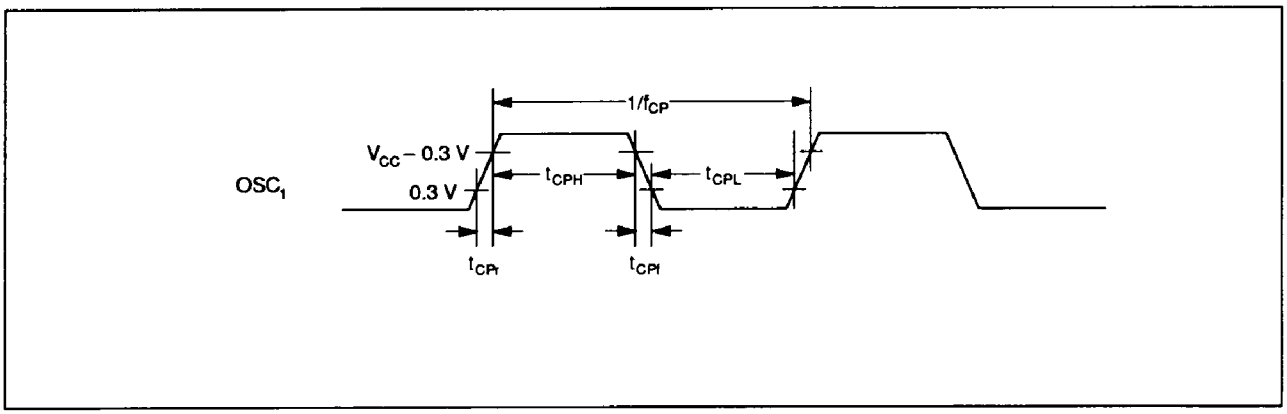


Figure 53 Oscillator Timing

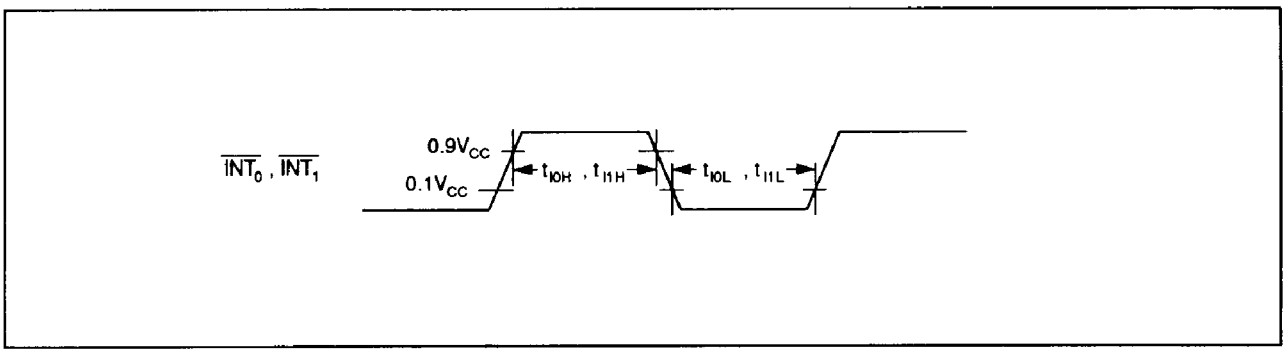


Figure 54 Interrupt Timing

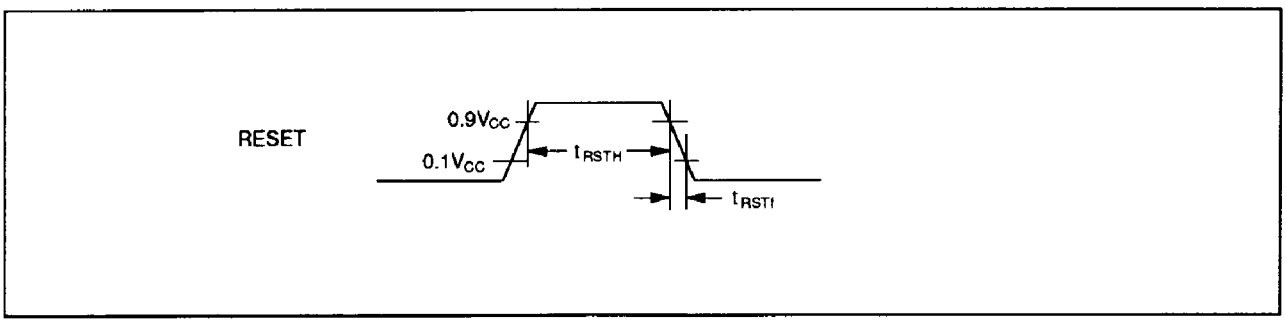


Figure 55 Reset Timing

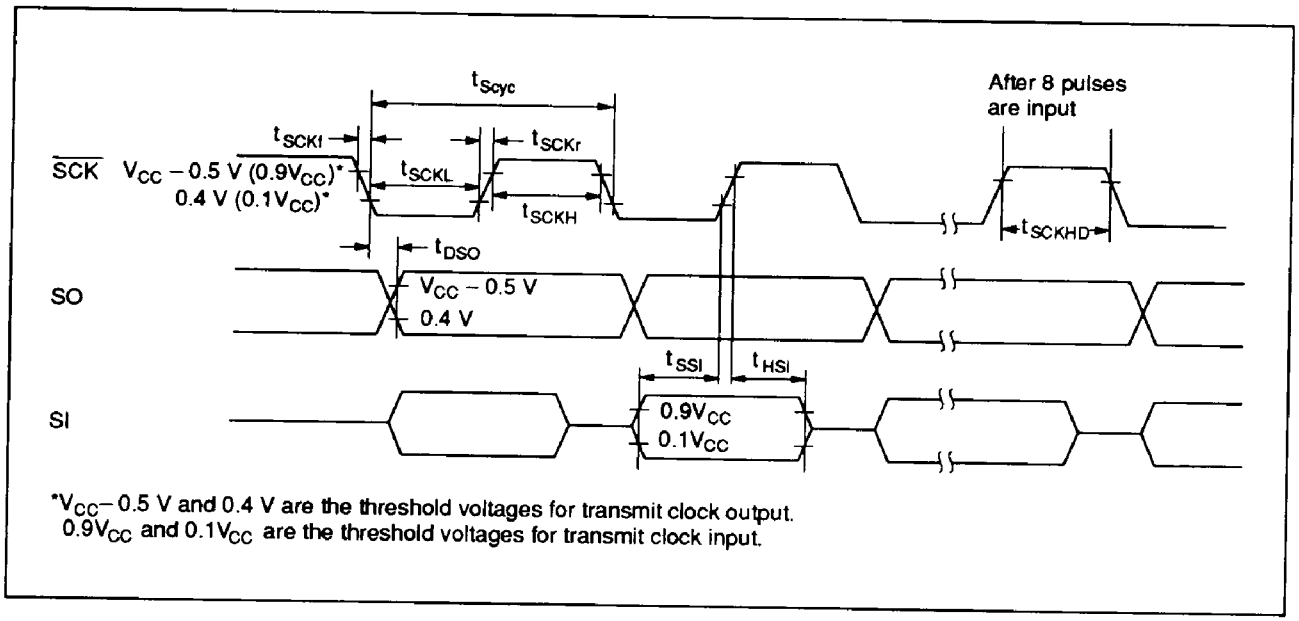


Figure 56 Timing of Serial Interface

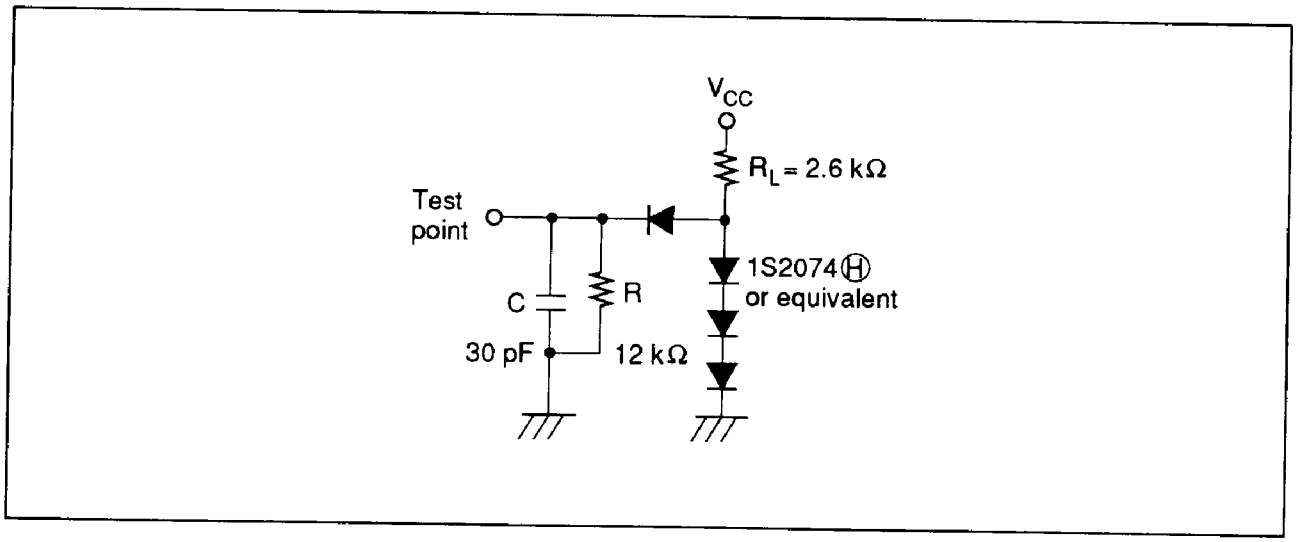


Figure 57 Timing Load Circuit

HD404818, HD404814 Option List

Please check by ■, ×, or ✓ within ❒.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI type number	
Hitachi's entry	

1. Functional option

❒	With 32-kHz CPU operation and with watch time base
❒	Without 32-kHz CPU operation and with watch time base
❒	Without 32-kHz CPU operation and without watch time base

2. Package

❒	FP-80A
❒	FP-80B
❒	TFP-80*

* Under development

3. ROM Code Media

ROM Code Media	
■	EPROM on-package microcomputer type

4. Oscillator

HD404818, HD404814				
Main	❒	Crystal oscillator	(f=	MHz)
	❒	Ceramic filter oscillator	(f=	MHz)
	❒	External clock	(f=	MHz)
Sub	❒	f = 32.768-kHz crystal oscillator		
	❒	Not used		

HD40L4818, HD40L4814 Option List

Please check by ■, ×, or ✓ within ❒.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI type number	
Hitachi's entry	

1. Functional option

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