PREPARED BY: DATE	SHARP	SPEC No. LC92X1OA
		FILE No.
APPROVED BY: DATE	LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION	ISSUE Ott.29,1992
		PAGE 19 Pages
		REPRESENTATIVE DIVISION
	SPECIFICATION	■ DUTY Panel Development center

DEVICE SPECIFICATION for
Passive Matrix LCD Unit
(320x240 dots)

Model No.
LM320081

❑ ICUSTOMER'S APPROVAL

BY _____

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SHARP

RECORDS OF REVISION

MODEL No.
LM320081

DOC. FIRST ISSUE
Oct. 29. 1992

IDENT. DATA No.
LC92X10A

DATE	REF. PAGE PARAGRAPH DRAWING No.	REVISED No.	SUMMARY	CHECK & APPROVAL
Jun. 12 1993	Page. 7 (Fig. 2)	1	Data input timing was revised	K. Shimizu

1. Application

This data sheet is to introduce the specification of LM320081, Passive Matrix type LCD Unit.
(320x240 dot, FSTN, Reflective, positive type)

2. Construction and Outline

Construction : 320x240 full dot graphic display unit
Outline : See Fig. 8 .
Connection : See Fig. 8 . and Table. 5 .

There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.
Rejection criteria shall be noted in Inspection Standard S-U-012-01.

3. Mechanical Specifications

Table 1

Parameter	Specification	Unit
Outline dimensions	134(W) x 96(H) x 6.5 MAX(D) Note 1	mm
Effective viewing area	100(W) x 76(H)	mm
Display format	320(W) x 240(H) full dot	—
Dot size	0.28(W) x 0.28(H)	mm
Dot spacing	0.02	mm
Character color	Black Note2	–
Background color	White Note2	–
Weight	Approx. 105	g

Note1 : Excluded the mounting tab. (See Fig.8)
Note2 : Due to the characteristics of the LC Material, the colors vary with environmental temperature.

4. Absolute Maximum Retings

4-1. Electrical Absolute Maximum Ratings

Table 2

Parameter	Symbo 1	Min	MAX	Unit	Remark
SupplY voltage (Logic)	$V_{DD}-V_{SS}$	0	6.0	V	Ta=25°C
Supply voltage (LCD Driver)	$V_{DD}-V_{EE}$	O	28.5	V	
Input voltage	V_{IN}	O	VDD	V	

4-2. Environmental Condition

Table 3

Item	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient. temperature	-25℃	+60℃	0℃	+45℃	
Humidity	Note 1		Note 1		No condensation
Vibration	Note 2		Note 2		3 directions (X/Y/Z)
Shock	Note 3		Note 3		6 directions (±X/± Y/±Z)

Note 1) Ta≦40℃……90% RH Max
Ta>40℃……Absolute humidity shall be less than Ta=40℃ /90% RH

Note 2) These test conditions are in accordance with "IEC 68-2-6"
Frequency : 10 ～ 55HZ
Viblation width : 1.5mm
Interval : 10HZ ～ 55HZ ～ 10HZ
(1 rein)
2 hours for each direct. on of X/Y/Z (6 hours as total)

Note 3) Accerelation : 490m/S² (50G)
Pulse width : 11ms
3 times for each direction of ±X/±Y/±Z.

5. Electrical Specifications

5.1 Electrical characteristics

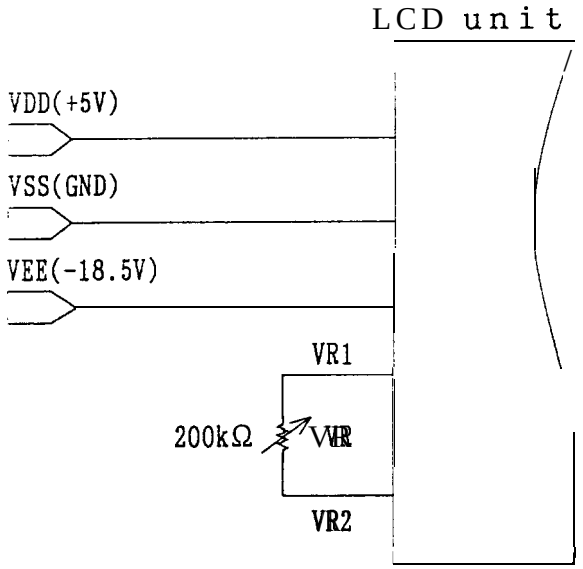
Table 4

Ta=25°C, VDD=5V±5%

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}		4.75	5.0	5.25	V
Supply voltage (LCD drive)	V_{EE}-V_{SS}	V_{DD}=5V (Note 1)	-19.5	-18.5	-17.5	V
Input signal voltage	V_{IN}	"H" level	0.8VDD	-	VDD	V
		"L" level	O	-	0.2VDD	V
Input leakage current	I_{IL}	"H" level	-	-	20	μA
		"L" level	-20.0	—	—	μA
Supply current (Logic)	I_{DD}	V_{DD}=5V, V_{EE}=-18.5V	—	9	13	mA
Supply current (LCD)	I_{EE}	VR=100kΩ	—	7	11	mA
Power consumption (LCD)	PdLCD	F=80HZ (Note 2)	-	185	270	mW

Note 1) The viewing angle(6) where obtains the maximum contrast can be set by adjusting variable resistor between VR1 and VR2.
Refer to Fig. 4 for the difinition of θ.

Note 2) Display high frequency pattern.

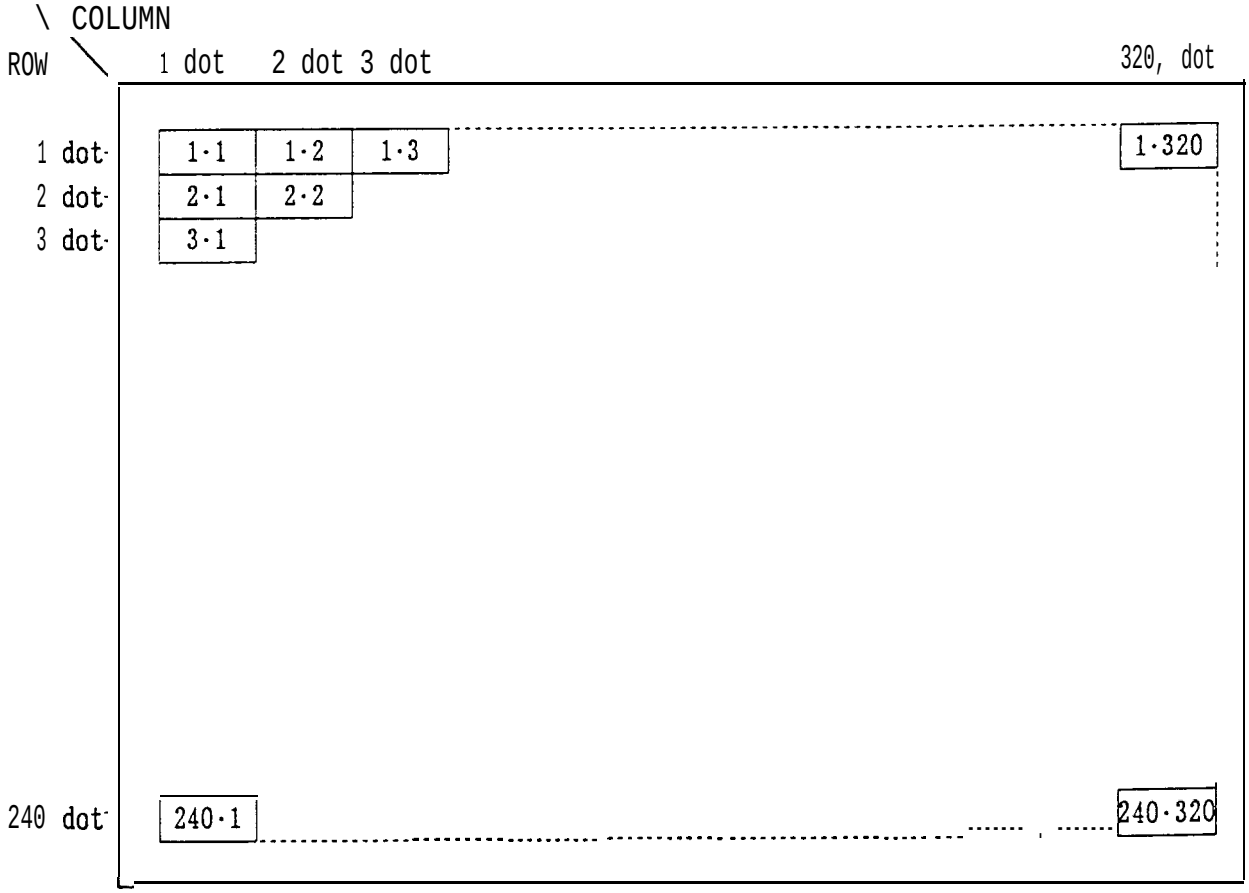


5-2. Interface signals

C N 1 Table 5

Pin No.	Symbols	Description	Level
1	s	Scan start-up signal	" H "
" 2	CP1	Input data latch signal	H→L
3	CP2	Data input clock signal	H→L
4	VDD	Power SUPPIY for logic and LCD (+5v)	–
5	VSS	Ground potential (0v)	
6	VEE	Power supply for LCD	–
7	DO	Display data signal	H(ON),L(OFF)
8	D1		
9	D2		
10	D3		
11	VR1	LCD Contrast Adjust (A)	–
12	VR2	LCD Contrast Adjust (B)	

Used Connector : 52103-1217 [Molex]
Mating Cable : 1.0mm pith , 12pins F.F.C.



Note) 1·2 means 1st row 2nd column dot.

Fig. 1 Dot Chart of Display Area

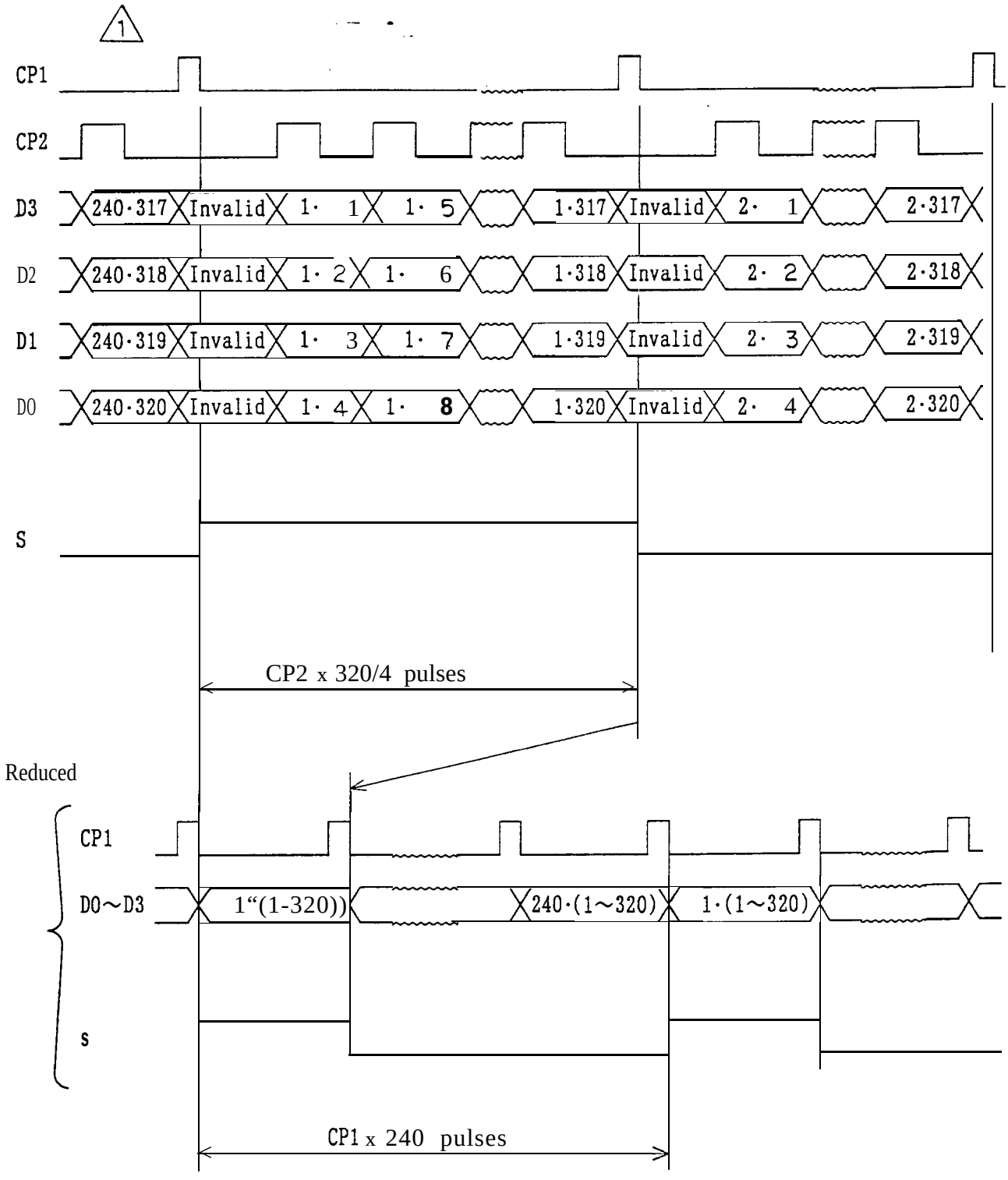


Fig. 2 Data Input Timing

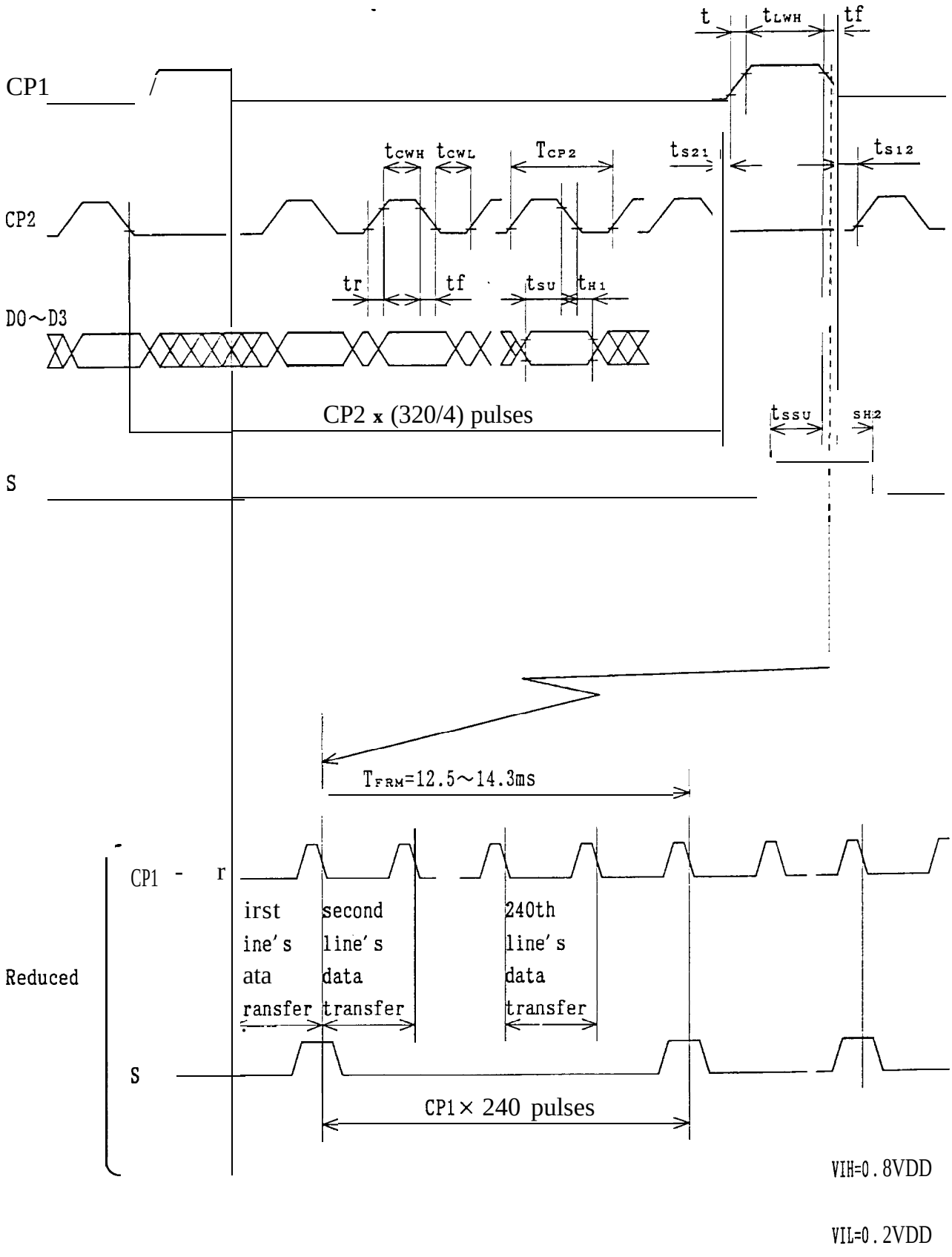


Fig. 3 Interface Timing Chart

Table. 6 Interface timing ratings

Item	Symbol	Rating			Unit
		MIN.	TYP.	MAX.	
Frame cycle	T_{FRM}	12.5		14.3	ms
CP2 clock cycle	T_{CP2}	170		—	ns
"H' level clock width	t_{CWH}	100		—	ns
"L" level clock width	t_{CWL}	100		—	ns
"H" level latch clock width	t_{LWH}	100		—	ns
Data set up time	t_{SU}	80		—	ns
Data hold time	t_{H1}	80		—	ns
CP2 ↑ clock allowance time from CP1↓	t_{s12}	0		—	ns
CP1 ↑ clock allowance time from CP2 ↓	t_{s21}	o		—	ns
Clock rise/fall time	tr, tf			50	ns
S Signal Data set up time	t_{SSU}	100			ns
S Signal Data hold time	t_{sH2}	100			ns

6.Unit Driving Method

6-1. Circuit Configuration

Fig.7 shows the block diagram of the Unit's circuitry.

6-2. Display ?ace Configuration

The display face electrically consists of signal display segment of 320 ×240 dots.

6-3. Input Data and Control Signal

The LCD driver is 80 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits.

Display data which are externally divided into data for each row (320 dots) will be sequentially transferred in the form of 4–bit parallel data through shift resisters by Clock Signal CP2 from the left top of the display face.

When data of one row (320 dots) have been inputted, then latched in the from of parallel data for 320 lines of signal electrodes by Latch Signal CP1. Then the corresponding drive signal will be transmitted to the 320 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal S has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st rows of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD.
While the 1st rows of data are being displayed, the 2nd rows of data are entered. When 320 dots of data have been transferred then latched on the falling edge of CP1 clock, the display face proceeds to the 2nd rows of display.

Such data input will be repeated uptothe 240th row of each display segment, from upper to lower rows, to complete one frame of display by time sharing ❑ ethod. Then data input proceeds to the next display face.

Scan start-up Signal S generates scan signal to drive horizontal electrodes.

The unit shall be driven at the speed of 70～80Hz/frame to avoid flickering.

Since DC voltage, if applied to LCD panel, causes chemical reaction which will deteriorate LCD panel, drive waveform shall be inverted to prevent the generation of such DC voltage. And to prevent such problem, AC waveform circuit generated by counting CP1 (M generator) is built in this circuit.

"Because of the characteristics of the CMOS driver LSI, the power consumption of the unit gose UP as the operating frequency CP2 increases. Thus the driver LSI applies the system of transferring 4-bit palallel data through the 4 lines of shift resistors to reduce the data transfer speed CP2. Thanks to the LSI, the power consumption of the unit will be minimized.

In this circuit configuration, 4-bit display data shall be therefore inputted to data input pins of D0~D3.

Furthermore the LCD unit adopts bus line system for data input to minimize the power consumption. In this system data input terminal of each driver LSI is activated only when relevant data input is fed.

Data input for colum electrodes of both the upper and the lower display segment and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 80 dots data (20 CP2) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face.

This process is simultaneously followed at the column driver LSI's of both the upper and the lower display segments. Thus data input through 4-bit bus line sequentially from the left end of the display face.

Since this graphic display unit contains no reflesh RAM, it requires data and timing pulse inputs even for static display.

The timing chart of input signals are shown in Fig.3.

7. Optical Characteristics

(Table 7 shows the optical characteristics when the viewing angle obtaining the maximum contrast (ϕ) is adjusted to O degrees.)

Table 7 VDD=5V, Ta=25°C

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Remark
Viewing angle range	$\theta_2-\theta_1$	ϕ=0°	Co≧4.0	60	–	–	dgr.	Note 1
	61	$\theta_1<\theta_2$	Co=4.0	–	–	-30	dgr.	Note 1
	θ_2			25	–	-	dgr.	Note 1
	$\theta_2-\theta_1$	ϕ=90°	Co≧4.0	65	-	-	dgr.	Note 1
	θ_1		Co=4.0	–	–	-35	dgr.	Note 1
	θ_2	$\theta_1<\theta_2$		25	–	-	dgr.	Note 1
Contrast ratio	Co	θ=0°、ϕ=0°		8.0	10.0	-		Note 2
Response speed	τr	e =0°、ϕ=0°		-	100	150	m s	Note 3
	τd	θ=()"\ # =0°		–	150	200	m s	Note 3

Note 1) The viewing angle range may bedefined as shown below.

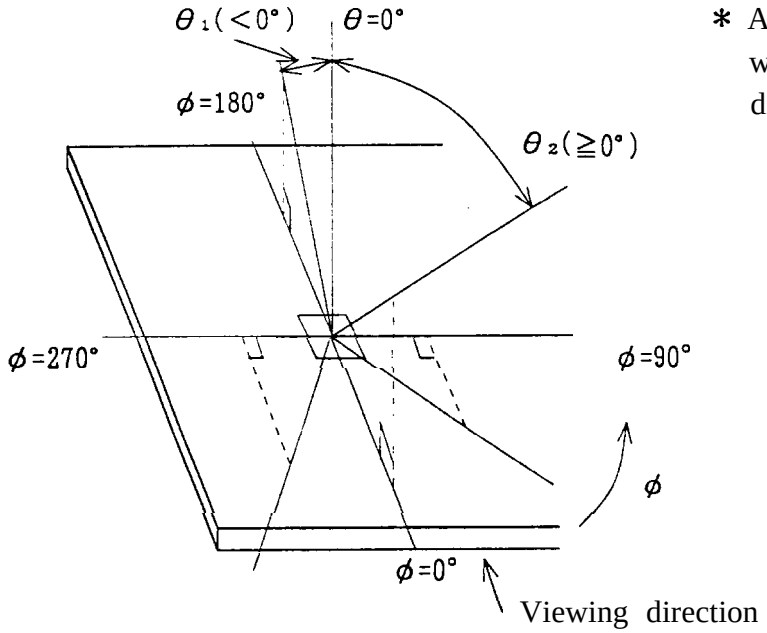


Fig. 4 Definition of Viewing Angle

* Angles θ_1, θ_2 and ϕ shall fall within the range overwhich the displayed character each be read.

Note 2) Contrast ratio may be defined as follows:

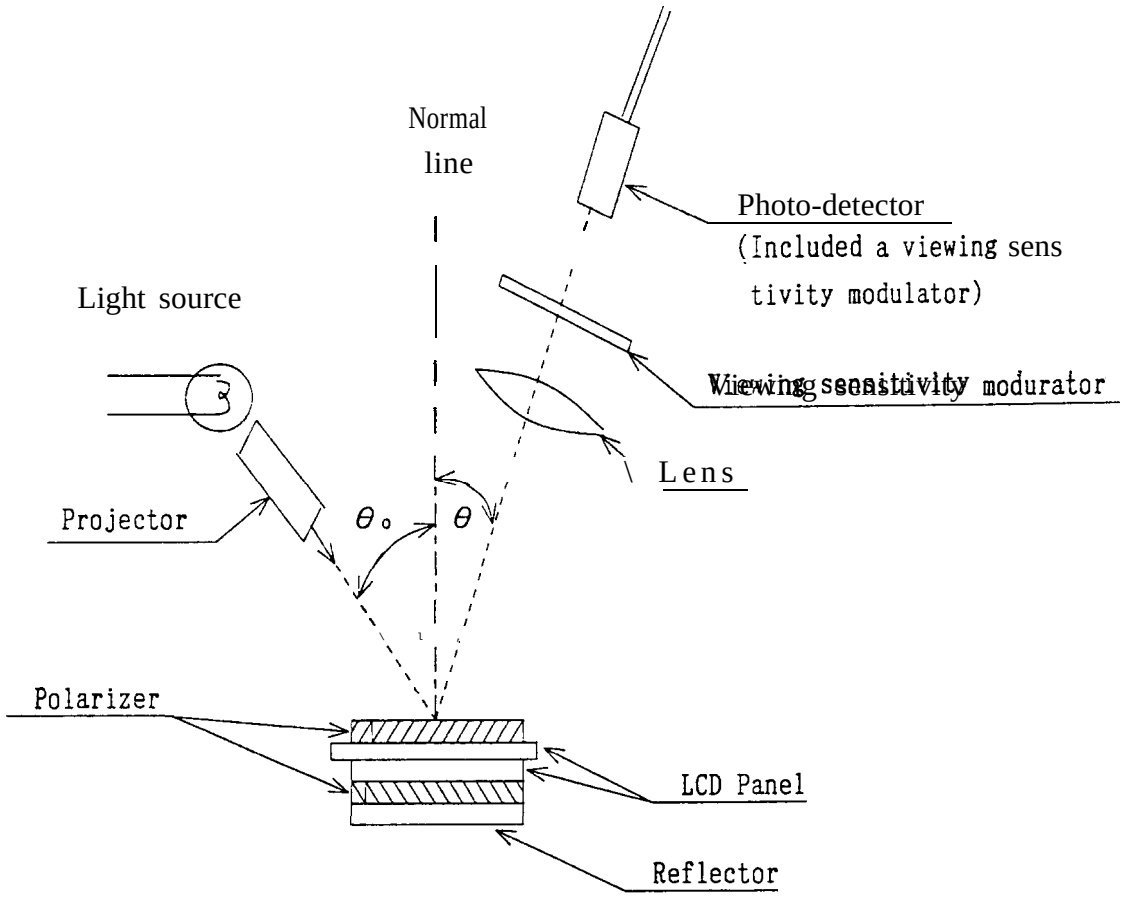
Contrast ratio is calculated by using the following formula when the waveform voltage (Fig.6) is applied in optical characteristics test method (Fig.5).

$$\text{Contrast ratio} = \frac{\text{Photo-detector output voltage with non-select waveform beig applied}}{\text{Photo-detector output vo ltage with select waveform being applied}}$$

Note 3) The response characteristics of photo-detector output are measured as shown in Fig.6, assuming that input signals are applide so as to select and deselect the dots to be measured, in the optical characteristics test method shown in Fig.5.

Note 4) Table 7 shown the optical characteristics detected when the LCD app. ied voltage waveforms are in the highest frequency *.

* The most critical cond. ion for the characteristics of LCD.



Light source

Fig. 5 Optics Characteristics Test Method

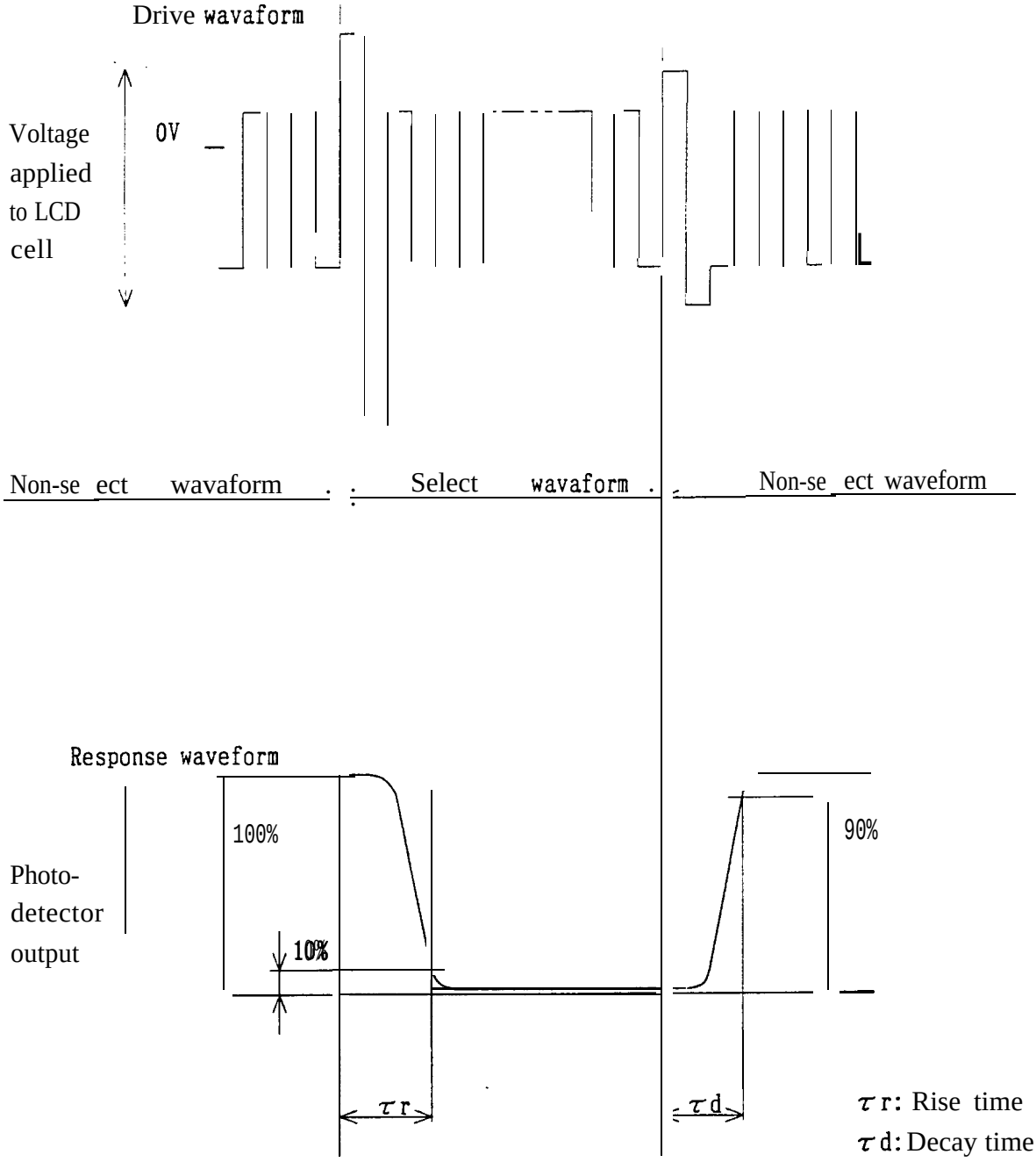


Fig. 4 Definition of Response Time

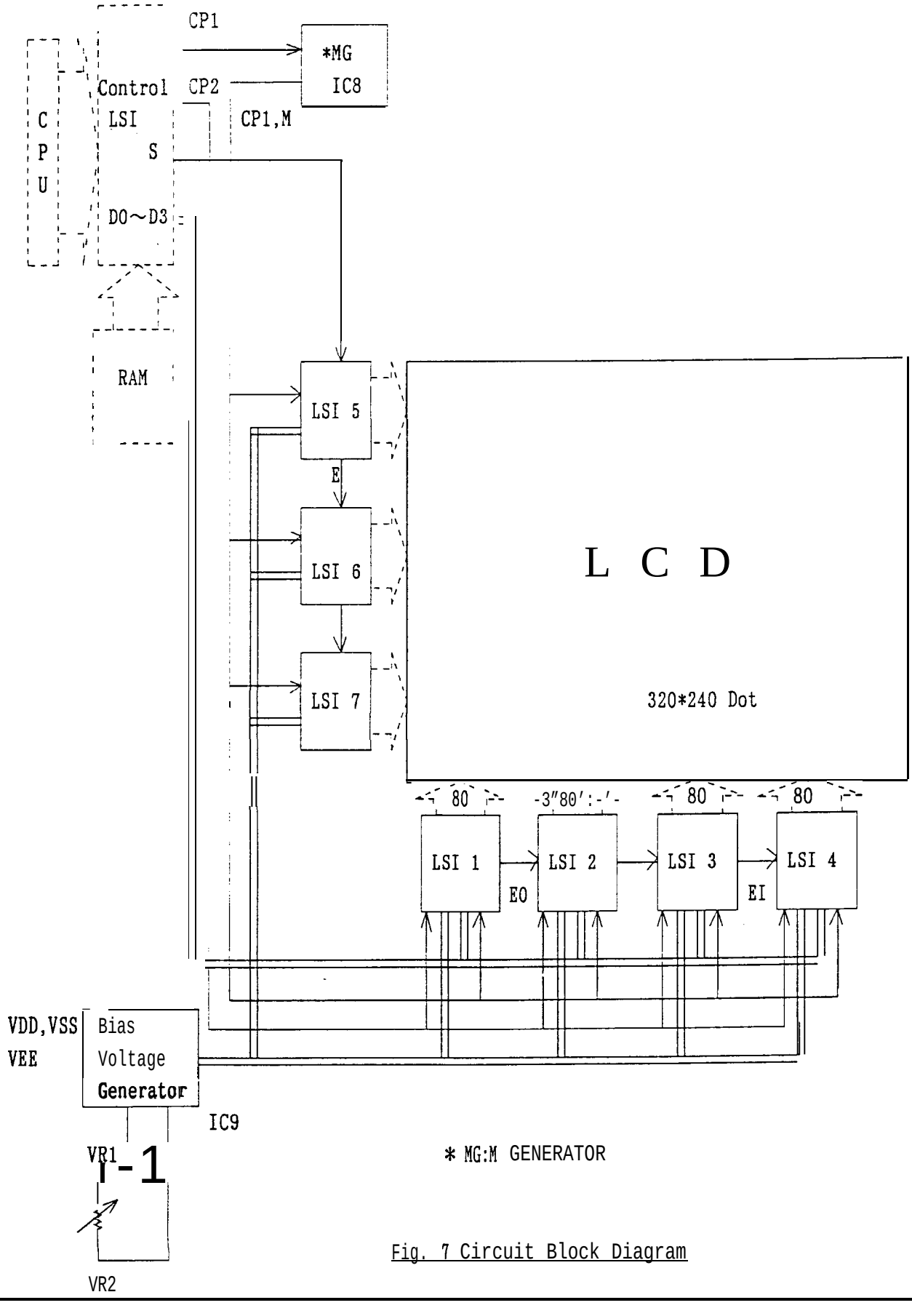
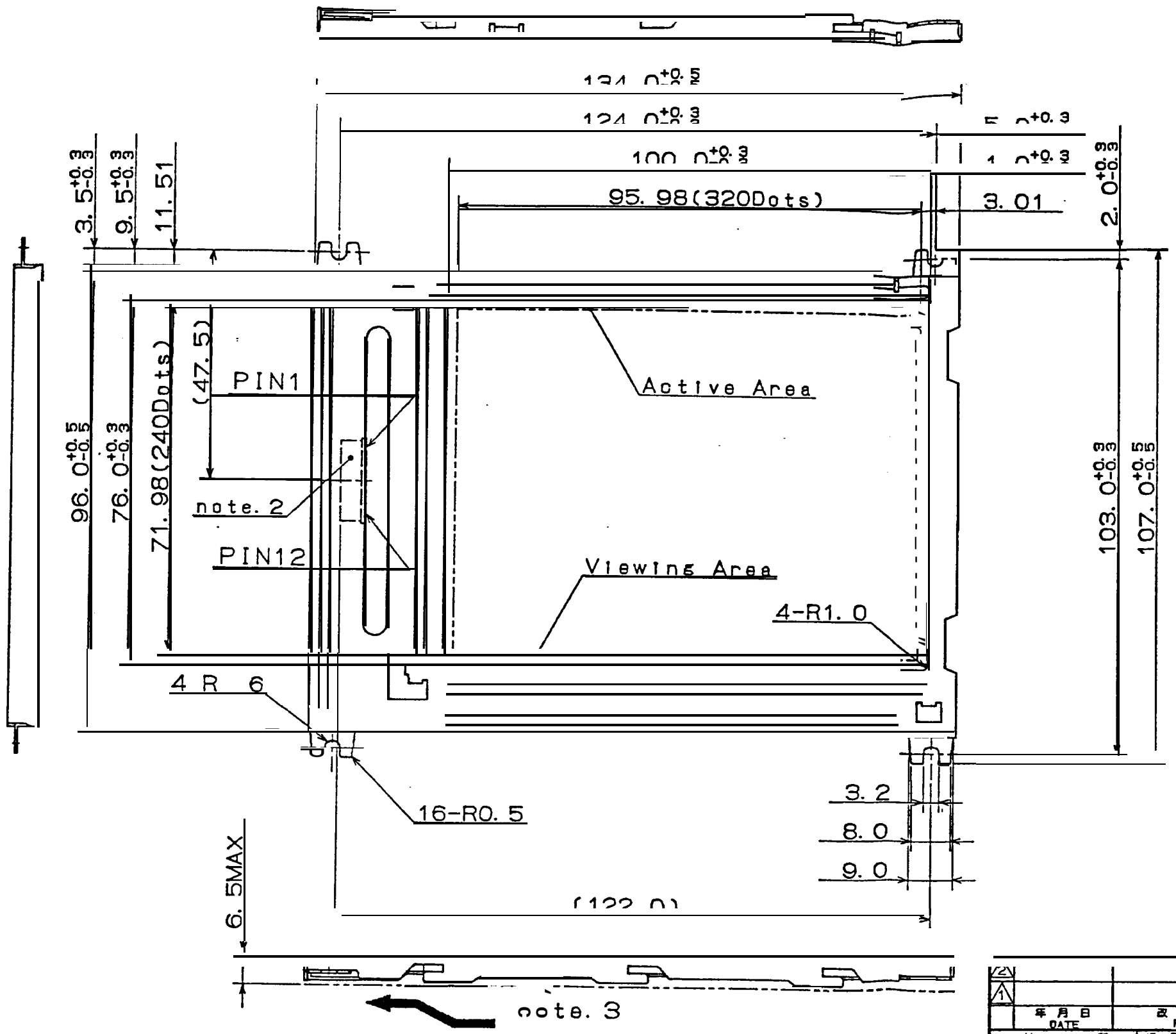
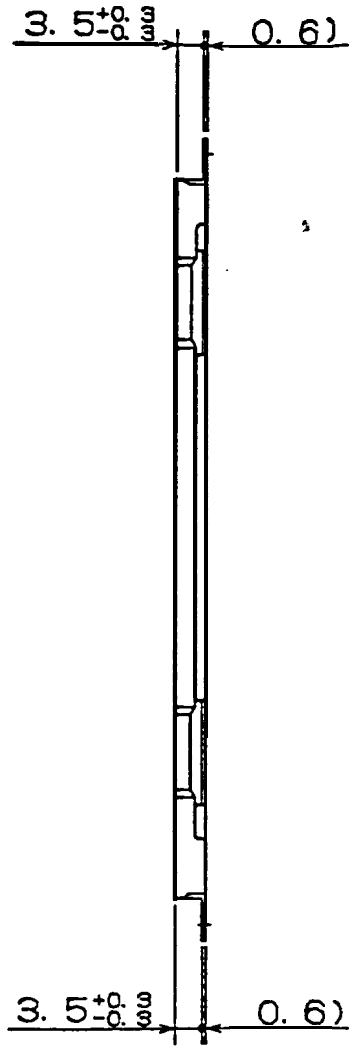
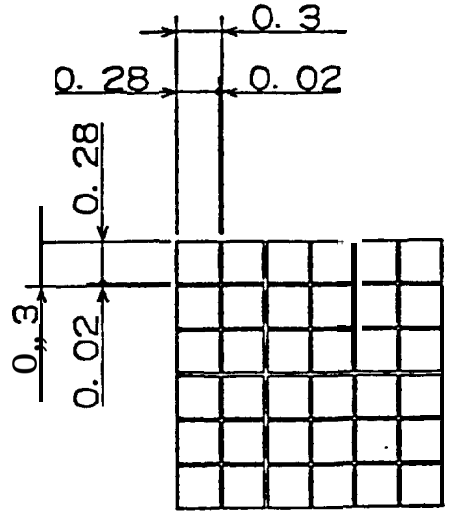


Fig. 7 Circuit Block Diagram





DOT SIZE 20/1□



PIN NO	SIMBOL
1	S
2	CP1
3	CP2
4	VDD
5	VSS
6	VEE
7	D0
8	D1
9	D2
10	D3
11	VR1
12	VR2

note
3.
2. C...52.03 .2...M...
B p Z

Fig. 8

指示なき寸法公差は ±0.7 とする
UNSPECIFIED TOL TO BE

					LM32008F	名称 NAME	LCD MODULE OUTLINE DIMENSIONS		
年月日 DATE	改定記事 RIVISE	配通 No	担当 PREPA	適用機種 MODEL					
材質 MATERIAL	板厚 THICKNESS	仕上 FINSH		尺度 SCALE	1/1	記号 SYMBOL			
						部品コード PARTS CODE			
設計 DESIGN	写図 TRACE	検図 CHECK	検図 CHECK	承認 APPROVE	SHARP CORPORATION	作成日付 DATE	1991・Oct・11・		
I		T.			シャープ株式会社 液晶(事本)	図番	LCS2X0A-F3020		

8. Precautions

8-1. Angle when installing the unit

This unit's viewing angle is illustrated in Fig.9.

$\theta_1 <$ viewing range $< e_2$ ($\theta_1 < 0°$, $\theta_2 \geqq 0°$)

Please consider the optimum viewing conditions according to the purpose when installing the unit.

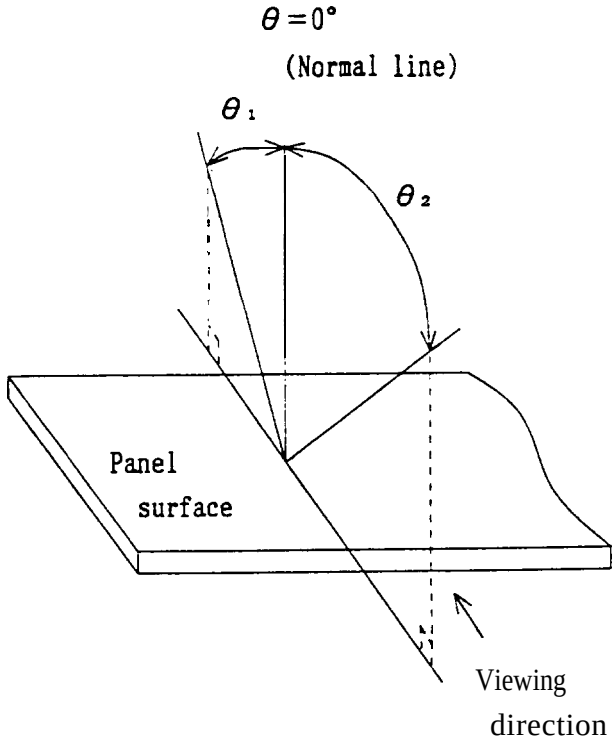


Fig. 9 Dot matrix LCD viewing angle

8-2. Handing cautions

This unit is installed using mounting tabs at the four corners of PCB or bezel.

When installing the unit, pay attention and handle carefully not to allow any undue stress such as twist or bend.

A transparent acrylic resin board or other type of protective panel should be attached to the front of the unit to protect the polarizer, LCD cells, etc.

8-3. Notes on attachment

(1) Since the front polarizer is easily dameged, please paY attention not to scratch on its face.
(2) If the surface of the LCD cells need to be cleaned, wipe it swiftly with cotton or other soft cloth. If still not completely clear, blow on it and wipe.
(3) Water droplets, etc. must be wiped off immediately since they may cause color changes, stain, etc. if remained for a long time.
(4) Since LCD is made of glass plates, dropping the unit or banging it against hard objects may cause cracking the or fragmentation.
(5) CMOS LSIS are equipped in this unit, so care must be taken to avoid the electro-static charge, by earthing human body, etc. Take the following measures, to protect the unit from the electric discharge via mounting tabs from the main system electrified with static electricity.
  (1) Earth the metallic case of the main system (contact of the unit and main system).
  (2) Insulate the unit and main system by attaching insulating washers made of backlite or nylon, etc.

8-4. Notes on operation

(1) The unit should be driven according to the specified ratings to avoid malfunction or parmanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continous application of the signal M. Especially the power ON/OFF sequence shown on next page shall be followed to avoid latch-up of driver LSIS and application of DC voltage to LCD panel.

8-5. Others

(1) Avoid to expose the unit to the direct sun-light, strong ultraviolet light, etc. for a long time.
(2) If stored at temperatures below specified storage temperature, the LC may fleeze and be deteriorated. If storage temperature exceed the specified rating, the molecular orientation of the LC may charge to that of a liquid, and they may not return to their original state.
(3) If the LCD panel is removed from the LCD unit, it may cause the poor contact. So please avoid to dismantle the unit.
(4) Do'nt use any materials which emit following gas from epoxy resin (amines hardener) and silicon adhesive agent (dealcohol or deoxym) to prevent change polarizer color owing to gas.

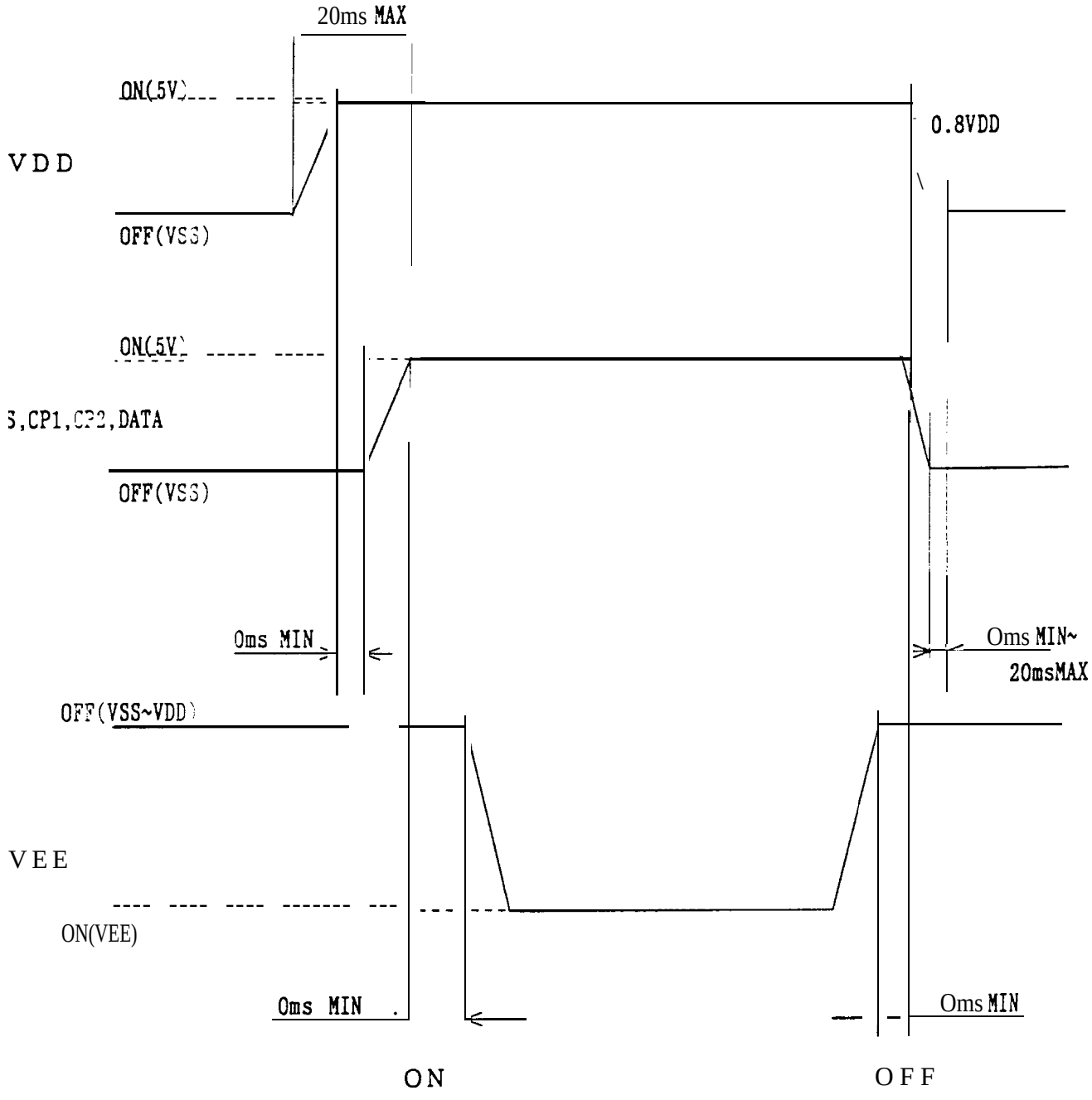


Fig. 10 Power ON/OFF sequence