GENERAL DESCRIPTION

Hua Ko has designed and manufactured a CMOS 8 bit microprocessor family with a total number of 18 microprocessors. The family consists of two series of devices: One series, designated HKE65SCXX is pin-to-pin compatible with the NMOS 6500 microprocessor series. The other series, designated HKE65SC1XX has several hardware enhancement not available in the NMOS 6500 series. Both series of the CMOS 8 bit microprocessors offered by Hua Ko are manufactured using the state-of-the-art silicon gate CMOS technology. Both series are TTL and CMOS compatible. All 18 microprocessors are software compatible within the family and all are bus compatible with MC6800 series. The family provides the designer with a wide selection range of addressable memory (4K or 64K), input interrupt options, and on-chip or external clock options.

The HKE65SCXX series consists of 10 microprocessors (i.e. HKE65SC02 – 07 and HKE65SC12 – 15). They can be used as drop-in replaceable of the NMOS 6500 microprocessors currently on the market. However, the CMOS family is specifically designed for use in the fully CMOS systems, such as industrial controllers, battery operated or portable computers, controllers and other instruments. The CMOS microprocessor is most valuable in industry because CMOS overcomes all the problems suffered by NMOS and TTL such as excessive power consumption, poor electrical noise immunity, and narrow operating-temperature range. Almost all industrial environments have problems with electrical noise and large temperature fluctuations. A CMOS system works best for all kinds of industrial applications because of its higher noise immunity and wider temperature range. The low-power consumption of a CMOS system is certainly essential to systems located remotely and powered by battery; it is also becoming an essential factor even for office equipment. For example, in an NMOS or TTL system, the regulated power supply easily occupies up to 50% of the total system volume and often requires a cooling fan. By using a CMOS system, the power supply can be reduced to less than 10% of the total system volume. In addition, the cooling fan can be eliminated. This would give a much smaller, lighter and more reliable system. Most importantly, the total system cost using all CMOS components is most likely to be below that of an NMOS or TTL system, due to the simplification of its power supply and other related components.

The ten microprocessors in the HKE65SCXX series offer designer more than just drop-in compatible with NMOS 6500 microprocessors and advantages of leading edge CMOS technology. Several hardware, software and operational enhancements are designed into the HKE65SCXX series that are not available to users of the NMOS 6500. The specifications and details of the improvement of CMOS 65SCXX over the NMOS 6500 are described in a later section.

The eight microprocessors in the HKE65SC1XX series offer designer an extra feature of an on-chip divide-by-four oscillator such that an economical television crystal (3.579545 MHz) can be used. The access time (t_{ACC}) is increased by approximately 25 percent due to this advantageous on-chip oscillator design.

All versions of the HKE65SCXX and HKE65SC1XX microprocessors are available in 1, 2, 3 and 4 MHz maximum operating frequencies. The standard package of the microprocessors is plastic. However, ceramic, cerdip or leadless chip carrier packaging are available as customer's options.

FEATURES

* Silicon-Gate COMS process
* Pin-to-pin compatible with NMOS 6500 series microprocessors
* TTL and CMOS I/O compatible
* Uses single +5 volt (±20%) power supply
* Low power consumption (4mA @ 1 MHz)
* 1, 2, 3 or 4 MHz versions
* Choice of 4K, 8K or 64K – byte addressable memory
* Enhanced instruction set:
  64 instructions
  178 operational codes
  15 addressing modes
* Choice of external or on-chip clock generator operation
* On-chip clock generator/oscillator can be driven by an external single-phase clock input, an RC network, or a crystal circuit
* Advanced memory access timing (ϕ4) on selected versions
* Early address valid allows use with any type of speed memory
* Early write data for dynamic memories
* 8-bit parallel processing
* Decimal and binary arithmetic
* Pipeline architecture
* Programmable stack pointer
* Variable length stack
* Interrupt capability
* Non-maskable interrupt
* 8-bit bidirectional data bus
* "Ready" input (for single cycle execution)
* Direct memory access capability
* Bus compatible with M6800
* Available on selected versions, a memory lock output and bus enable input signals simplify multiprocessor design
* Available in either 28 or 40 pin dual-in-line packaging
* Commercial and industrial temperature versions

IMPROVEMENT OF CMOS HKE65SCXX OVER NMOS 6500

The HKE65SCXX microprocessors are pin-to-pin compatible with the NMOS 6500 microprocessors currently offered by many other manufacturers. However, several hardware, software and operational enhancements have been designed and implemented to provide the designer with more options that are not available to users of the NMOS 6500. The enhancements include: Addressing modes, microprocessor instructions, and operational codes. The enhancements are discussed in details and compared with the NMOS 6500 series as follows:

Expanded Addressing Modes: NMOS 6500 has 13 addressing modes. The CMOS HKE65SCXX has 15 addressing modes, thus provide the designer with the highest degree of flexibility in addressing in all the 8-bit microprocessors (Intel 8080/8085 has 5 addressing modes; M6800 has 7 addressing modes; Z-80 has 10; and Texas 9900 has 8). The expanded addressing modes are very useful in reducing the memory space for storing a program and increasing the operational effeciency.

Exapnded Instruction Set: The microprocessor instructions of HKE65SCXX has been expanded from 56 to 64 instructions. The 8 expanded instructions have improved the performance of the microprocessor and made it more powerful in controlling system.

Expanded Operational Codes: The NMOS 6500 has 151 codes. The CMOS HKE65SCXX has expanded to 178 operational codes. This has substantially improved the effective use of the microprocessor instructions.

The hardware enhancements of the CMOS HKE65SCXX are summerized in Table I.
The operational enhancements of the CMOS HKE65SC1XX are summerized in Table II.

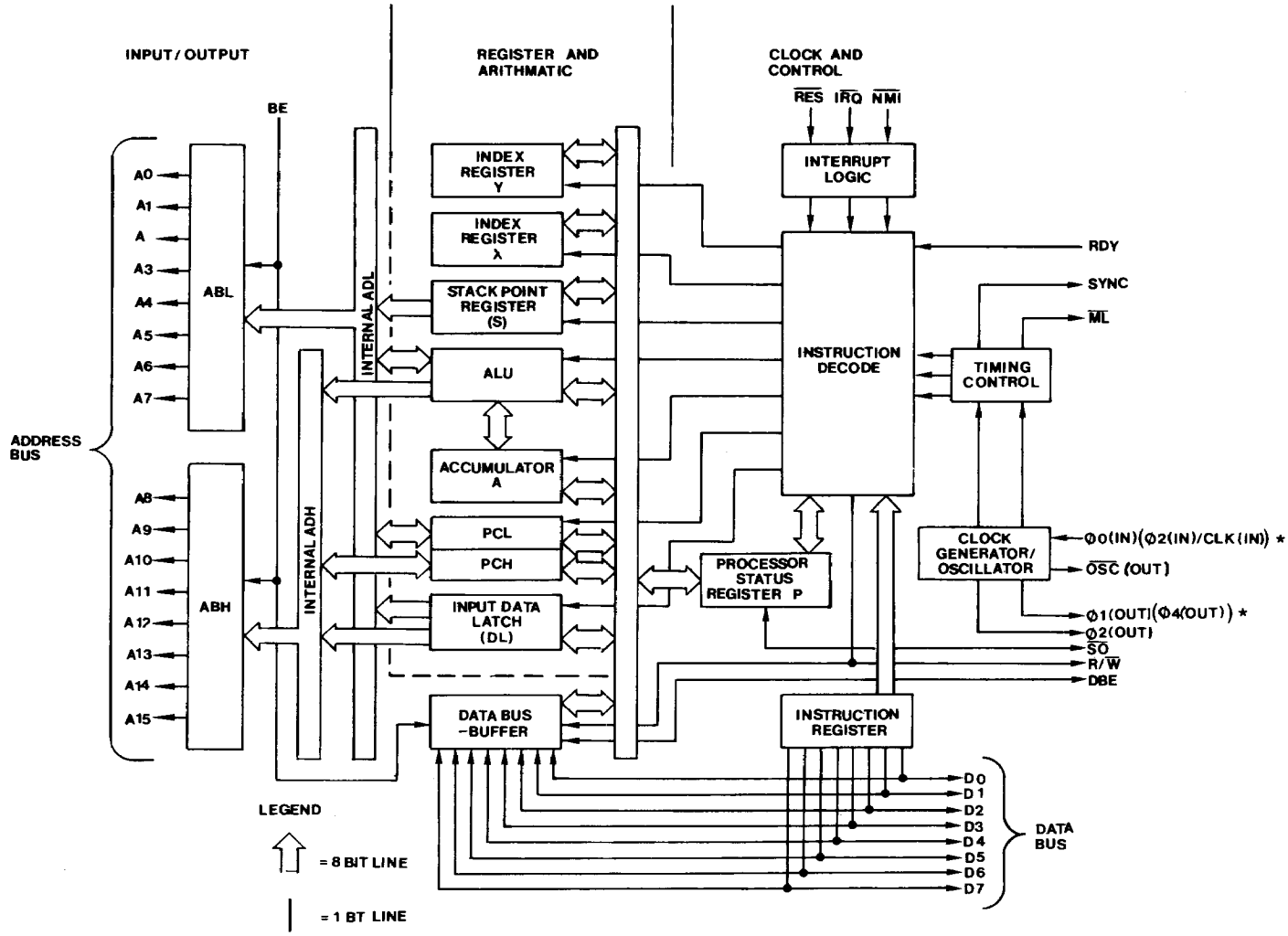
TABLE I MICROPROCESSOR HARDWARE ENHANCEMENTS

Function	NMOS 6500	HKE65SCXX Family
Oscillator	Requires external active components	Crystal or RC network will oscillate when connected as Figure 4(a) and 4(b).
Assertion of Ready (RDY) during write Operations.	Ignored	Stops processor during $\phi 2$.
1X series clock inputs	Two non-overlapping clock input ($\phi 1$ and $\phi 2$) are required.	$\phi 2$ (IN) is the only required clock input.
Unused input-only pins ($\overline{IRQ}$, $\overline{NMI}$, RDY, $\overline{RES}$, $\overline{SO}$, DBE*, BE**).	Must be connected to low impedance signal to avoid noise problems.	Connected internally by a high-resistance to V_{DD} (approximately 1 Megohm).

* DBE is used in the HKE65SC12 only.
**BE is used in the HKE65SC102 and 112.

TABLE II MICROPROCESSOR OPERATIONAL ENHANCEMENTS

Function	NMOS 6500 Microprocessor	HKE65SCXX Family Microprocessor
Indexed addressing across page boundary.	Extra read of invalid address.	Extra read of last instruction byte.
Execution of invalid op codes	Some terminate only by reset. Results are undefined.	All are NOPs (reserved for future use). Op Code — Bytes — Cycles X2 — 2 — 2 X3, X7, XB, XF — 1 — 1 44 — 2 — 3 54, D4, F4 — 2 — 4 5C — 3 — 8 DC, FC — 3 — 4
Jump indirect, operand =XXFF	Page address does not increment.	Page address increments. One additional cycle.
Read/modify/write instructions at effective address.	One read and two write cycles.	Two read and one write cycle.
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D=0) after reset and interrupts.
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flags. One additional cycle.
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded, BRK vector is ignored.	BRK is executed, then interrupt is executed.



* Refer to Signal Description

Figure 1. Internal Architecture Block Diagram

FUNCTIONAL DESCRIPTION

A block diagram of the internal architecture of HKE65SCXX and HKE65SC1XX are shown in Figure 1. The basic on-chip units implemented in the microprocessor include: Clock generator, timing control, logic control, arithmetic and logic unit, accumulator, program counter, registers, I/O, and data address bus drivers, etc. The functional description of each on-chip unit is given as follows:—

Clock Generator and Timing Control

The clock generator generates the clock signal for the timing control and provides other clock signals for external use. The timing control unit keeps track of the instruction cycle. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse ($\phi 1$) for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

Program Counter

The 16-bit program counter is divided into a program-counter lower-byte (PCL) and higher-byte (PCH), when a instruction or data is fetched, this unit always places an address of the instruction code or data to be fetched on the 16-bit address bus. When the BRK, Jump instruction or a special operation, for example: Reset, Interrupt request, or Nomaskable interrupts is executed, a 16-bit (in two 8-bits) now address ór a 16-bit (in two 8-bits) new vector address is entered into this Counter Via and 8-bit data Bus. This counter can be automatically incremented each time after an instruction or data is fetched.

Instruction Register and Decoder

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register then decoded, along with timing and interrupt signals, to generate control signals for the registers.

Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

Index Registers

Two 8-bit index registers, labelled as X and Y registers, are used to count program steps or to provide an index value for generating effective address.

In executing instructions with specific indexed addresses, the CPU fetches the op code and the base address from the memory, and modifies the address by adding the index register to the base address prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible.

Stack Pointer

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$ and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts.

Processor Status Register

The 8-bit processor status register contains seven status flags and one empty bit. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

A simplified architectural diagrams of the internal registers is given in Figure 2a and 2b.

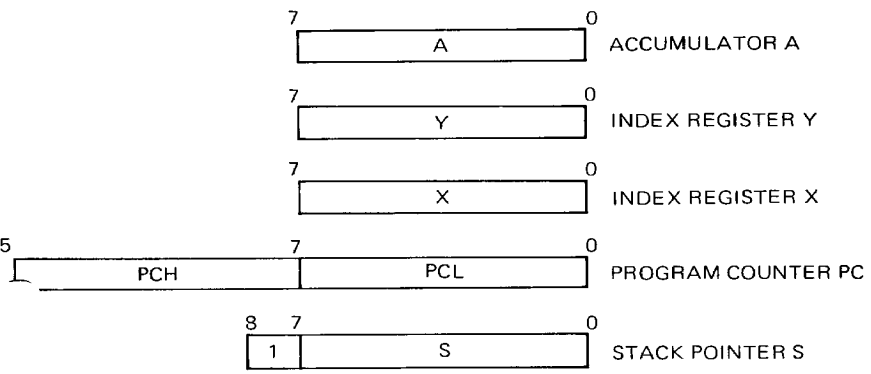


Fig. 2a Architecture of internal registers

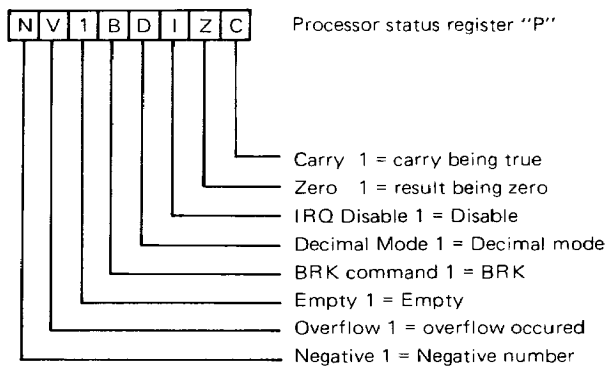


Fig 2b Architecture of internal register "P"

SIGNAL DESCRIPTION

The signals of the HKE65SCXX and HKE65SC1XX microprocessors can be divided into four basic groups:

(1) Address bus (A0 to A15),
(2) Data bus (D0 to D7),
(3) Clock and timing ($\phi 0$ to $\phi 4$), and
(4) Control signals (BE, DBE, $\overline{ML}$, $\overline{RES}$, RDY, R/$\overline{W}$, $\overline{SO}$, SYNC, $\overline{IRQ}$, $\overline{NMI}$).

Each microprocessor of the 18 members of the family consists a specific set of signals. Detail identification of each microprocessor is given in a later section under the title of FAMILY MEMBER DESCRIPTION. A brief description of all the signals is given as follows:

Address Bus (A0 to A11 for 4K, A0 to A12 for 8K and A0 to A15 for 64K addressable memory)

Packaging options of 28-pin and 40-pin are available. In the 40-pin package, A0 to A15 forms a 16-bit address bus and is capable of addressing 64K byte memories. In the 28-pin package, two versions of address bus are available. One (A0 to A11) is capable of addressing 4K byte and the other (A0 to A12) is capable of addressing 8K byte memories. The address lines are set (See BE below) to the high impedance state by the bus enable (BE) signal*. The output of each address line is TTL compatible, capable of driving one standard TTL load and 130pF.

Data Bus (D0 to D7)

The data lines (D0 – D7) consists of an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are three-state buffers capable of driving one TTL load and 130pF. The data lines are set to the high impedance state by BE or DBE.

Bus Enable (BE)

This signal allows external control of the data and the address output buffers and R/$\overline{W}$. For normal operation, BE is high causing the address buffers and R/$\overline{W}$ to be active and the data buffers to be active during a write cycle. For external control, BE is held low to disable the buffers. This signal is designed into HKE65C102 and 112 only (see Tabel III)

*BE is used in HKE65SC102 and 112 only.

Data Bus Enable (DBE)*

This TTL-compatible input allows external control of the three-state data output buffers. In normal operation, DBE would be driven by the phase two ($\phi 2$) clock, thus allowing data input from microprocessor only during $\phi 2$. During the read cycle, the data bus buffers are internally disabled, becoming essentially an open circuit. To disable the data bus externally, DBE should be held low. The signal is designed into HKE65SC112 only.

Memory Lock ($\overline{ML}$)**

In a multiprocessor system, $\overline{ML}$ indicates the need to defer the rearbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. $\overline{ML}$ goes low during ASL, DEC, INC, LSR, ROL, ROR, TRB, TSB memory referencing instructions. This signal is low for the modify and write cycles.

Reset ($\overline{RES}$)

The $\overline{RES}$ must be set high for normal operation. The microprocessor will not operate if $\overline{RES}$ is low. A positive transition on this line causes an initialization sequence to begin. Reset must be held low for at least two clock cycles after V_{DD} reaches operating voltage from a power down condition. After this time, R/$\overline{W}$ is high and SYNC is low.

When a positive edge is detected, there is an initialization sequence lasting six clock cycles. Then the interrupt mask flag is set, the decimal mode is cleared, and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFC (high byte). This is the start location for program control.

Ready (RDY)

This input signal allows the user to operate on the microprocessor by single-cycle on all cycles including write cycles. A negative transition to the low state during or coincident with phase one ($\phi 1$) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two ($\phi 2$) in which the ready signal is low. This feature allows microprocessor with low-speed memory as well as direct memory access (DMA).

Set Overflow ($\overline{SO}$)

A negative transition on this line sets the overflow flag-bit in the status code register. The signal is sampled on the trailing edge of $\phi 1$

Synchronize (SYNC)

This output line is provided to identify those cycles during which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $\phi 1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\phi 1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Read/Write (R/$\overline{W}$)

This signal is normally in the high state indicating that the microprocessor is reading data from memory or I/O bus. In the low state the data bus has valid data from the microprocessor to be stored at the addressed memory location. R/$\overline{W}$ is set to the high impedance state by BE. (HKE65SC102 and 112 only).

Interrupt Request ($\overline{IRQ}$)

This signal requests the microprocessor to execute an interrupt sequence. If $\overline{IRQ}$ is sampled during $\phi 2$ and the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during $\phi 1$ of next cycle. Then the program counter and processor status register are stored in the stack and the microprocessor will set the interrupt mask flag high so that no further interrupts may occur. At the end of this interrupt process, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, i.e. the starting address of the interrupt service-routine is transferred into the program counter. The RDY signal must be in the high state for any interrupt to be recognized. A 3K ohm external resistor should be used for proper wire-OR operation.

Non-maskable Interrupt ($\overline{NMI}$)

This signal causes the microprocessor to execute a non-maskable interrupt sequence, when it is at low state and sampled during $\phi 2$. After the current instruction is completed ,the interrupt sequence begins during $\phi 1$. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine. However, it should be noted this is an edge-sensitive input. As a result another interrupt will occur if there is another negative-going transition on this line and the program has not returned from a previous interrupt. Also, no new interrupt will occur if $\overline{NMI}$ is low and negative-going edge has not occurred since the last non-maskable interrupt.

The following descriptions of timing signals are refered to Figure 3a and Figure 3b.

Phase 0 IN ($\phi 0$ (IN))

This is the buffered clock input to the internal clock generator on the HKE65SCOX series. Clock output $\phi 1$(OUT) and $\phi 2$(OUT) are derived from this signal. All three signals are on-chip signals in HKE65SC02.

Phase 1 Out ($\phi 1$ (OUT))

This signal is derived from $\phi 0$ and is the inversion signal of $\phi 2$ (out). $\phi 1$ (out) provides timing for external R/$\overline{W}$ operations.

Phase 2 Out ($\phi 2$ (OUT))

This signal is derived from $\phi 0$ and provides timing for external bus R/$\overline{W}$ operation. Addresses are valid after the address setup time (tADS) from the falling edge of $\phi 2$ (OUT).

Clock In (CLK (IN))

The 65SC10X series is supplied with an internal clock generator operating at four times the $\phi 2$ frequency. The frequency of these clocks are externally controlled by the crystal or oscillator circuit shown in Figure 3b.

* DBE is used in the HKE65SC12 only.
** $\overline{ML}$ is designed into the HKE65SC102, 112 and 115 only.

Timing Diagram of

HKE65SC02 ~ 07
HKE65SC12 ~ 15
HKE65SC112 ~ 115

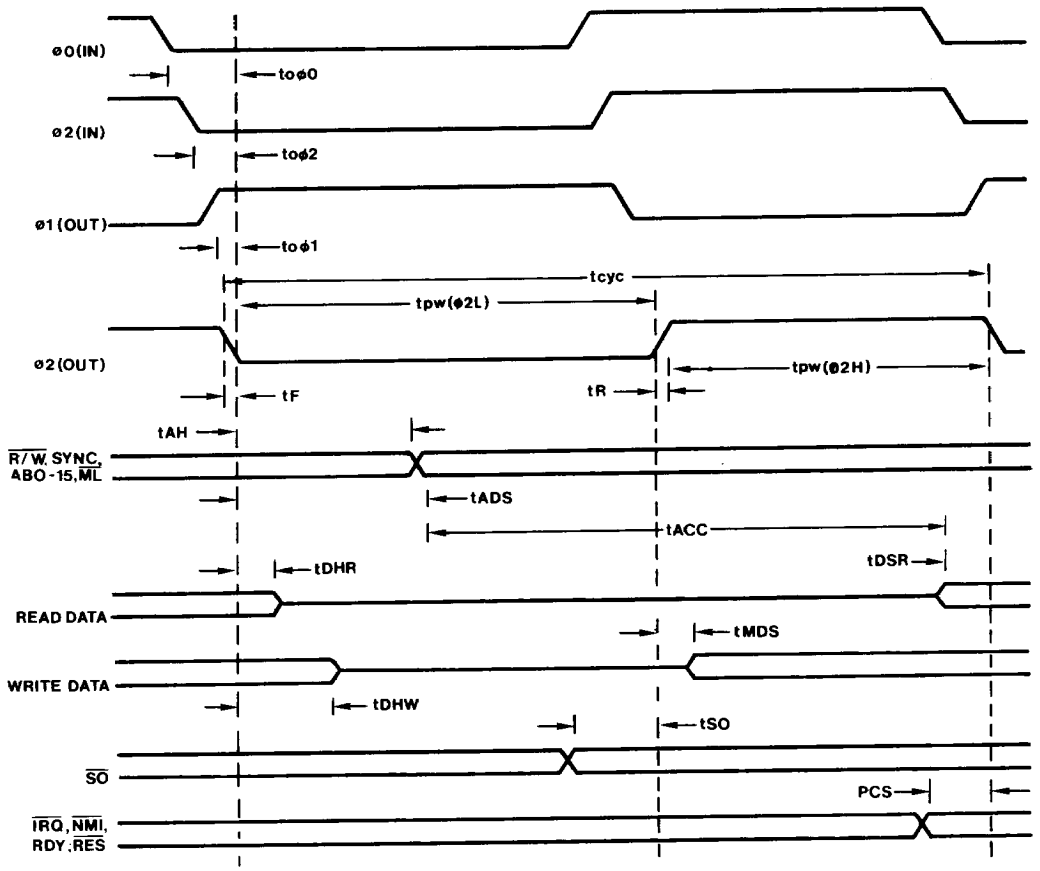


Fig. 3a

Timing Diagram of

HKE65SC102 ~ 107

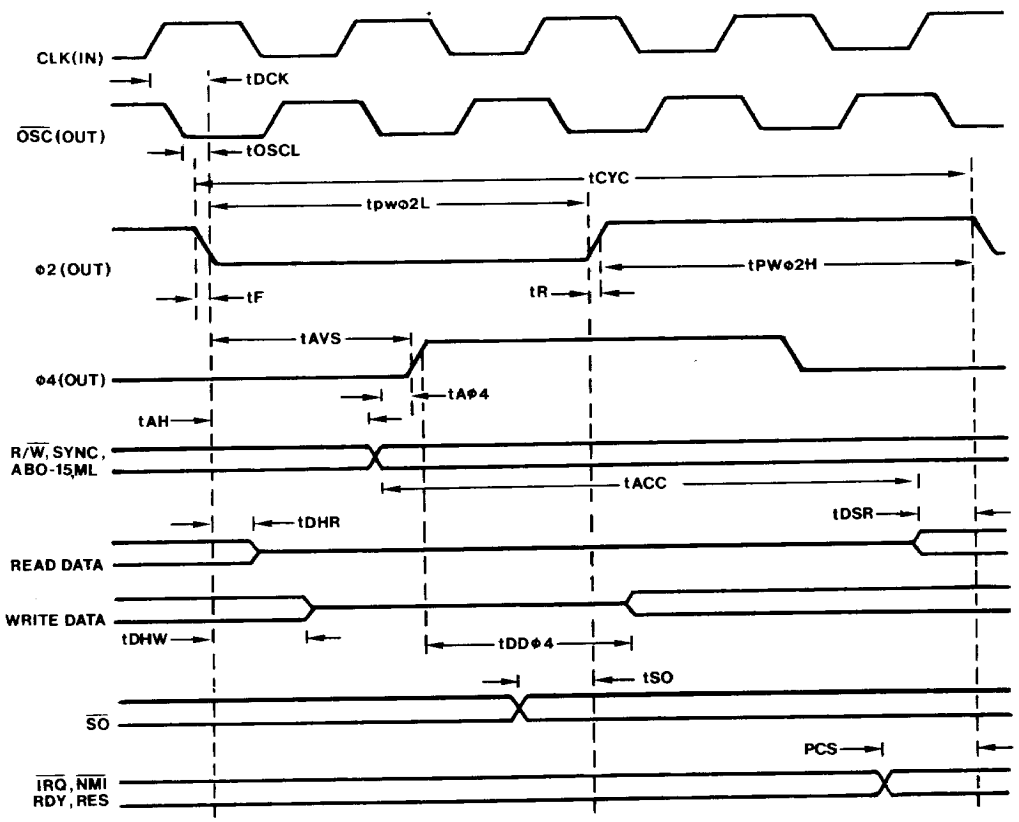


Fig. 3b

Notes : • Load = 100pf
• Voltage levels shown are $V_L < 0.4$ V, $V_H > 2.4$V unless otherwise specified.
• Measurement points shown are 0.8V & 2.0V unless otherwise specified.

Phase 2 In (ϕ2(IN))

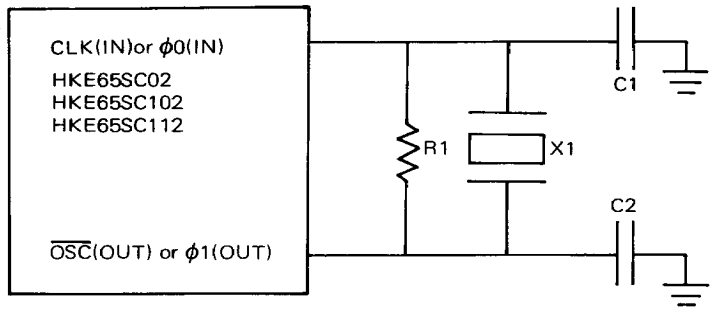
This is the unbuffered clock input to the internal clock generator on the HKE65SC1X and HKE65SC11X series. The clock output, ϕ2 (OUT) is derived from this signal.

Oscillator Out ($\overline{OSC}$(OUT))

On the HKE65SC102 microprocessor, an internal inverter is connected between pins 35 and 37. The inverter has sufficient loop gain to provide oscillation using an external crystal.

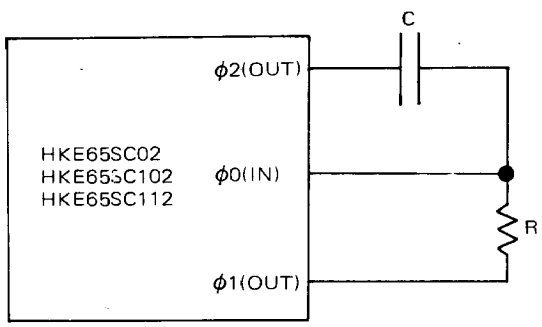
Phase 4 Out (ϕ4(OUT))

This signal is delayed by tAVS from ϕ2(OUT). The address output is valid prior to the rising edge of ϕ4(OUT), this signal is used in HKE65SC104 only. Examples of crystal and RC circuits for internal oscillation timing signals are given in Figure 4 (a) and (b), respectively. The crystal circuit for external oscillation timing signal is given in Figure 4 (c).



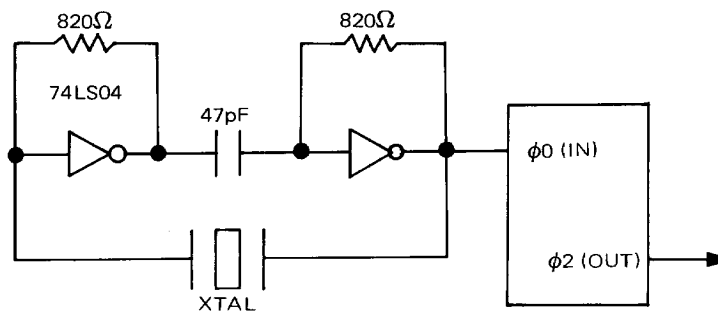
C1, C2 = 51pF
R1 = 200K
X1 = 1MHz

Fig. 4(a) Crystal Circuit for internal Oscillator



Suggested RC network configuration for internal oscillator.

Fig. 4(b) RC Circuit for Internal Oscillator



CRYSTAL: CTS KNIGHTS MP SERIES OR EQUIVALENT

Fig. 4(c) Crystal Circuit for External Oscillator

ADDRESSING MODES

Fifteen addressing modes are available to the user of the HKE65SCXX and HKE65SC1XX series of microprocessors. The addressing modes are described in the following paragraphs:

1. **Implied Addressing [implied] or [imp.]**

   In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction. Only one byte of memory is required for an instruction in this addressing mode.

2. **Accumulator Addressing [Accu.]**

   This addressing is similar to the implies addressing. It is represented with an one-byte instruction and implies that an operand is in the accumulator.

3. **Immediate Addressing [Imm.]**

   With immediate addressing, the operand is contained in the second byte of the instruction; no further memory addressing is required. Two bytes of memory space is required in this addressing mode.

4. **Absolute Addressing [Abs.]**

   For absolute addressing the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Therefore, this addressing mode allows access to the total 64K bytes of addressable memory. Three bytes of memory space is required.

5, 6. **Absoulte Indexed Addressing [Abs, X] or [Abs, Y]**

   Absolute indexed addressing is used in conjunction with X or Y index register and is referred to as "Absolute, X," and "Absolute, Y". Three bytes of memory space is required. The effective address is formed by adding the contents of X or Y to the address contained in the second byte of the instruction; the carry, if occured, is added to third byte of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

7. **Zero Page Addressing [Z. Page]**

   Zero page addressing allows shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. The careful use of zero page addressing can result in significant increase in code efficiency.

8, 9. **Zero Page Indexed Addressing [Z. Page, X] or [Z. Page, Y]**

   Zero page addressing mode is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page Zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page boundaries does not occur. Two bytes of the memory space are required for this instruction using this addressing mode.

10. **Relative Addressing [Rela.]**

    Relative addressing mode is used only with branch instruction; it establishes a distination for the conditional branch. Two bytes of memory space is required.

11. **+Zero Page Indirect Addressing [(Z. PG)]**

    In this form of addressing the second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits is always zero. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address. Two bytes of memory space is required.

12. **Absolute Indirect Addressing [(Abs.)]**

    The second byte of the instruction contains the low order eight bits of a memory location, which is referred to as the indirect address. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address, and the effective address composed of two bytes is loaded into the 16 bits of the program counter.

13. **Indirect Indexed Addressing [(Z. PG), Y]**

    This form of addressing is usually referred to as Indirect, Y. The second byte of the instruction points to a memory location in page Zero. The contents of this memory location is added to the contents of the Y index register, the result being order eight bits of the effective address. The carry from this addition is added to the contents of the next location in page zero, the result being the high order eight bits of the effective address. The indirect indexed addressing may contain various combinational addresses of which, however, only the zero-page-indirect combinating with Y-index is available to the HKE65SCXXX.

14. **Zero Page Indexed Indirect Addressing [(Z. PG, X)]**

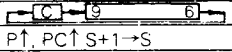
    With zero page indexed indirect addressing (usually referred to as indirect X) the second byte of the instruction is added to the contents of the X index register; the carry is discarded. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero. This addressing mode is not available to the index register X. Each instruction, using this mode occupies two bytes of memory space.

15. **+Absolute Index Indirect Addressing [(Abs, X)]**

    The second byte of the instruction is added to the contents of the X index register. The high order eight bits of that memory location is contained in the third byte of the instruction. The result of this addition points to a memory location whose contents is the low order eight bits of the effective address. The next memory location contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address, i.e. An absolute X-index addressing followed by an absolute indirect addressing mode.

+ New addressing mode available to the CMOS HKE65SCXXX microprocessors only. It is not designed in the NMOS6500.
* ( ) represents indirect addressing.

The 64 instructions and 178 machine Codes of HKE65SCXXX (Typical example: HKE65SC02) Microprocessors

No.	Mnemonic	OPERATION	imp.			accu.			imm.			Z.PG			Z.PG, X			PG, Y			
			op	#	n	op	#	n	op	#	n	op	#	n	op	#	n	op	#	n	op
1	ADC+	A+M+C→A 2							69	2	2	65	2	3	75	2	4				6D
2	AND+	A∧M→A							29	2	2	25	2	3	35	2	4				2D
3	ASL	C←76543210←0				0A	1				2	06	2	5	16	2	6				0E
4	BCC	Branch occurs, if C=0 1																			
5	BCS	Branch occurs, if C=1 1																			
6	BEQ	Branch occurs, if Z=1 1																			
7	BIT+	A∧M→Z, M7→N, M6→V							89+	2	2	24	2	3	34+	2	4				2C
8	BMI	Branch occurs, if N=1 1																			
9	BNE	Branch occurs, if Z=0 1																			
10	BPL	Branch occurs, if V=0 1																			
11	BRA++	Unconditional Branch																			
12	BRK	PC+2↓, P↓FFFE, FFFF→PCL, PCH	00	1	7																
13	BVC	Branch occurs V=0 1																			
14	BVS	Branch occurs V=1 1																			
15	CLC	0→C	18	1	2																
16	CLD	0→D	D8	1	2																
17	CLI	0→I	58	1	2																
18	CLV	0→V	B8	1	2																
19	CMP+	A−M→N.Z.C.							C9	2	2	C5	2	3	D5	2	4				CD
20	CPX	X−M→N.Z.C.							E0	2	2	E4	2	3							EC
21	CPY	Y−M→N.Z.C.							C0	2	2	C4	2	3							CC
22	DEC+	A−1→A or M−1→M				3A+	1	2				C6	2	5	D6	2	6				CE
23	DEX	X−1→X	CA	1	2																
24	DEY	Y−1→Y	88	1	2																
25	EOR+	A∇M→A							49	2	2	45	2	3	55	2	4				4D
26	INC+	A+1→A or M+1→M				1A+	1	2				E6	2	5	F6	2	6				EE
27	INX	X+1→X	E8	1	2																
28	INY	Y+1→Y	C8	1	2																
29	JMP+	(PC+1)→PCL, (PC+2)→PCH																			4C
30	JSR	(PC+2)↓, (PC+1)→PCL(PC+2)→PCH																			20
31	LDA+	M→A							A9	2	2	A5	2	3	B5	2	4				AD
32	LDX	M→X							A2	2	2	A6	2	3				B6	2	4	AE
33	LDY	M→Y							A0	2	2	A4	2	3	B4	2	4				AC
34	LSR	0→76543210→C				4A	1	2				46	2	5	56	2	6				4E
35	NOP	No operation	EA	1	2																
36	ORA+	A∨M→A							09	2	2	05	2	3	15	2	4				0D
37	PHA	A↓(A→Ms), S−1→S	48	1	3																
38	PHP	P↓(P→Ms), S−1→S	08	1	3																
39	PHX++	X↓(X→Ms), S−1→S	DA+	1	3																
40	PHY++	Y↓(Y→Ms), S−1→S	5A+	1	3																
41	PLA	A↑(Ms→A), S+1→S	68	1	4																
42	PLP	P↑(Ms→P), S+1→S	28	1	4																
43	PLX++	X↑(Ms→X), S+1→S	FA+	1	4																
44	PLY++	Y↑(Ms→Y), S+1→S	7A+	1	4																
45	ROL					2A	1	2				26	2	5	36	2	6				2E
46	ROR					6A	1	2				66	2	5	76	2	6				6E
47	RTI	P↑, PC↑ S+1→S	40	1	6																
48	RTS	PC↑, PC+1→PC S+1→S	60	1	6																
49	SBC+	A−M−C̄→A, C̄:Borrow 2							E9	2'	2	E5	3	4	F5	2	4				ED
50	SEC	1→C	38	1	2																
51	SED	1→D	F8	1	2																
52	SEI	1→I	78	1	2																
53	STA+	A→M										85	2	3	95	2	4				8D
54	STX	X→M										86	2	3				96	2	4	8E
55	STY	Y→M										84	2	3	94	2	4				8C
56	STZ++	00→M										64+	2	3	74+	2	4				9C+
57	TAX	A→M	AA	1	2																
58	TAY	A→Y	AB	1	2																
59	TRB++	Ā∧M→M										14+	2	5							1C+
60	TSB++	A∨M→M										04+	2	5							0C+
61	TSX	S→X	BA	1	2																
62	TXA	X→A	8A	1	2																
63	TXS	X→S	9A	1	2																
64	TYA	Y→A	98	1	2																
		Function	imp.			accu.			imm.			Z.PG			Z.PG.X			Z.PG,Y			

Notes:

* Add 1 to n if page boundary is crossed.
1. Add 1 to n if branch occurs to same pate. Add 2 to n if branch occurs to different page.
2. Add 1 to n if decimal mode.
++ New instruction
\+ (with) additional addressing mode(s)

A Accu
X index
Y index
M Mem

ressing Modes																						Stute flag								
abs. X			abs. Y			rela.			(abs.)			(Z. PG, X)			(Z. PG), Y			(Z.PG)+			(abs, X)			7	6	5	4	3	2	1	0	
o	#	n	op	#	n	op	#	n	op	#	n	op	#	n	op	#	n	op	#	n	op	#	n	N	V		B	D	I	Z	C	
D	3	4*	79	3	4*							61	2	6	71	2	5*	72+	2	5				N	V					Z	C	ADC+
	3	4*	39	3	4*							21	2	6	31	2	5*	32+	2	5				N						Z		AND+
E	3	7																						N						Z	C	ASL
						90	2	2																								BCC
						B0	2	2																								BCS
						F0	2	2																								BEQ
C+	3	4*																						M7	M6					Z		BIT+
						30	2	2																								BMI
						D0	2	2																								BNE
						10	2	2																								BPL
						80+	2	3																								BRA++
																											1	0	1			BRK
						50	2	2																								BVC
						70	2	2																								BYS
																														0		CLC
																												0				CLD
																													0			CLI
																									0							CLV
D	3	4*	D9	3	4*							C1	2	6	D1	2	5*	D2	2	5*				N						Z	C	CMP
																								N						Z	C	CPX
																								N						Z	C	CPY
E	3	7																						N						Z		DEC+
																								N						Z		DEX
																								N						Z		DEY
D	3	4*	59	3	4*							41	2	6	51	2	5*	52+	2	5				N						Z		EOR
E	3	7																						N						Z		INC+
																								N						Z		INX
																								N						Z		INY
									6C	3	5										7C+	3	6									JMP+
																																JSR
D	3	4*	B9	3	4*							A1	2	6	B1	2	5*	B2+	2	5				N						Z		LDA
			BE	3	4*																			N						Z		LDX
	3	4*																						N						Z		LDY
E	3	7																						0						Z	C	LSR
																																NOP
D	3	4*	19	3	4*							01	2	6	11	2	5*	12+	2	5				N						Z		ORA
																																PHA
																																PHP
																																PHX++
																																PHY++
																								N						Z		PLA
																								N	V		1	D	1	Z	C	PLP
																								N						Z		PLX++
																								N						Z		PLY++
E	3	6*																						N						Z	C	ROL
E	3	6*																						N						Z	C	ROR
																								N	V		1	D	1	Z	C	RTI
																	*															RTS
D	3	4*	F9	3	4*							E1	2	6	F1	2	5*	F2+	2	5				N	V					Z	C	SBC+
																															1	SEC
																												1				SED
																													1			SEI
D	3	5	99	3	5							81	2	6	91	2	6	92+	2	6												STA+
																																STX
																																STY
E+	3	5																														STZ++
																								N						Z		TAX
																								N						Z		TAY
																								M7	M6							TRB++
																								M7	M6					Z		TSB++
																								N						Z		TSX
																								N						Z		TXA
																								N						Z		TXS
																								N						Z		TYA
abs, X			abs,Y			rela.			(abs.)			(Z.PG,X)			(Z.PG), Y			(Z.PG)+			(abs, X)+			N	V		B	D	I	Z	C	

effective address

Ms Memory byte per stack pointer
Bytes per instruction
n Cycles per instruction
M6 bit 6 of memory byte
M7 bit 7 of memory byte
N~C Flag bit of state register
+/- ADD/Substrate
Λ/V AND/OR
∇ Exclusive OR
Trans. from . . . to . . .
Push . . . on stack
Pull . . . from stack

INSTRUCTION SET

INSTRUCTION SET ALPHABETIC SEQUENCE (Typical Version: HKE65SC02

Mnemonic	Function	Mnemonic	Function
(1) ADC+	Add Memory to Accumulator with Carry	(33) LDY	Load Index Y with Memory
(2) AND+	"AND" Memory with Accumulator	(34) LSR	Shift One Bit Right (Memory or Accumulator)
(3) ASL	Shift Left One Bit (Memory or Accumulator)	(35) NOP	No Operation
(4) BCC	Branch on Carry Clear	(36) ORA+	"OR" Memory with Accumulator
(5) BSC	Branch on Carry Set	(37) PHA	Push Accumulator on Stack
(6) BEQ	Branch on Result Zero	(38) PHP	Push Processor Status on Stack
(7) BIT+	Test Bits in Memory with Accumulator	(39) PHX++	Push X Register on Stack
(8) BMI	Branch on Result Minus	(40) PHY++	Push Y Register on Stack
(9) BNE	Branch on Result not Zero	(41) PLA	Pull Accumulator from Stack
(10) BPL	Branch on Result Plus	(42) PLP	Pull Processor Status from Stack
(11) BRA++	Branch Always	(43) PLX++	Pull X Register from Stack
(12) BRK	Force Break	(44) PLY++	Pull Y Register from Stack
(13) BVC	Branch on Overflow Clear	(45) ROL	Rotate One Bit Left (Memory or Accumulator)
(14) BVS	Branch on Overflow Set	(46) ROR	Rotate One Bit Right (Memory or Accumulator)
(15) CLC	Clear Carry Flag	(47) RTI	Return from Interrupt
(16) CLD	Clear Decimal Mode	(48) RTS	Return from Subroutine
(17) CLI	Clear Interrupt Disable Bit	(49) SBC	Subtract Memory from Accumulator with Borrow
(18) CLV	Clear Overflow Flag	(50) SEC	Set Carry Flag
(19) CMP+	Compare Memory and Accumulator	(51) SED	Set Deciami Mode
(20) CPX	Compare Memory and Index X	(52) SEI	Set Interrupt Disable Status
(21) CPY	Compare Memory and Index Y	(53) STA+	Store Accumulator in Memory
(22) DEC+	Decrement Memory by One	(54) STX	Store Index X in Memory
(23) DEX	Decrement Index X by One	(55) STY	Store Index Y in Memory
(24) DEY	Decrement Index Y by One	(56) STZ++	Store Zero
(25) EOR+	"Exclusive-OR" Memory with Accumulator	(57) TAX	Transfer Accumulator to Index X
(26) INC+	Increment Memory by One	(58) TAY	Transfer Accumulator to Index Y
(27) INX	Increment Index X by One	(59) TRB++	Test and Reset Bits
(28) INY	Increment Index Y by One	(60) TSB++	Test and Set Bits
(29) JMP+	Jump to New Location	(61) TSX	Transfer Stack Pointer to Index X
(30) JSR	Jump to New Location Saving Return Address	(62) TXA	Transfer Index X to Accumulator
(31) LDA+	Load Accumulator with Memory	(63) TXS	Transfer Index X to Stack Register
(32) LDX	Load Index X with Memory	(64) TYA	Transfer Index Y to Accumulator

Notes: ++ New Instruction, + Previous Instruction with additional addressing mode(s)

INSTRUCTION SET OP CODE MATRIX (TYPICAL VERSION: HKE65SC02)

LSB / MSB	0	1	2	3	4	5	6	8	9	A	B	C	D	E	F	
0	BRK Impl 17	ORA (ZP,X) 26			TSB ZP 25	ORA ZP 23	ASL ZP 25	PHP Impl 13	ORA IMM 22	ASL Accum 12		TSB ABS 36	ORA ABS 34	ASL ABS 36		0
1	BPL Rela 22**	ORA (ZP),Y 25*	ORA (ZP) 25		TRB ZP 25	ORA ZP, X 24	ASL ZP,X 26	CLC Impl 12	ORA ABS,Y 34*	INC Accum 12		TRB ABS 36	ORA ABS, X 34*	ASL ABS, X 37		1
2	JSR Abs 36	AND (ZP,X) 26			BIT ZP 23	AND ZP 23	ROL ZP 25	PLP Impl 14	AND IMM 22	ROL Accum 12		BIT ABS 34	AND ABS 34	ROL ABS 36		2
3	BMI Rela 22**	AND (ZP), Y 25*	AND (ZP) 25		BIT ZP, X 24	AND ZP, X 24	ROL ZP, X 26	SEC Impl 12	AND ABS,Y 34*	DEC Accum 12		BIT ABS, X 34*	AND ABS, X 34*	ROL ABS, X 37		3
4	RTI Impl 16	EOR (ZP,X) 26				EOR ZP 23	LSR ZP 25	RHA Impl 13	EOR IMM 22	LSR Accum 12		JMP ABS 33	EOR ABS 34	LSR ABS 36		4
5	BVC Rela 22**	EOR (ZP), Y 25*	EOR (ZP) 25			EOR ZP, X 24	LSR ZP, X 26	CLI Impl 12	EOR ABS,Y 34*	PHY Impl 13			EOR ABS, X 34*	LSR ABS, X 37		5
6	RTS Impl 16	ADC (ZP,X) 26+			STZ ZP 23	ADC ZP 23+	ROR ZP 25	PLA Impl 14	ADC IMM 22+	ROR Accum 12		JMP (ABS) 35	ADC ABS 34+	ROR ABS 36		6
7	BVS Rela 22**	ADC (ZP), Y 25*+	ADC ZP,X 25+		STZ ZP,X 24	ADC ZP, X 24+	ROR ZP, X 26	SEI Impl 12	ADC ABS,Y 34*+	PLY Impl 14		JMP (ABS,X) 36	ADC ABS, X 34*+	ROR ABS, X 37		7
8	BRA Rela 23	STA (ZP,X) 26			STY ZP 23	STA ZP 23	STX ZP 23	DEY Impl 12	BIT IMM 22	TXA Impl 12		STY ABS 34	STA ABS 34	STX ABS 34		8
9	BCC Rela 22**	STA (ZP), Y 26	STA (ZP) 26		STY ZP,X 24	STA ZP, X 24	STX ZP, Y 24	TYA Impl 12	STA ABS,Y 35	TXS Impl 12		STZ ABS 34	STA ABS,X 35	STZ ABS, X 35		9
A	LDY IMM 22	LDA (ZP,X) 26	LDX IMM 22		LDY ZP 23	LDA ZP 23	LDX ZP 23	TAY Impl 12	LDA IMM 22	TAX Impl 12		LDY ABS 34	LDA ABS 34	LDX ABS 34		A
B	BCS Rela 22**	LDA (ZP), Y 25*	LDA (ZP) 25		LDY ZP, X 24	LDA ZP,X 24	LDX ZP, Y 24	CLV Impl 12	LDA ABS,Y 34*	TSX Impl 12		LDY ABS, X 34*	LDA ABS, X 34*	LDX ABS, Y 34*		B
C	CPY IMM 22	CMP (ZP, X) 26			CPY ZP 23	CMP ZP 23	DEC ZP 25	INY Impl 12	CMP IMM 22	DEX Impl 12		CPY ABS 34	CMP ABS 34	DEC ABS 36		C
D	BNE Rela 22**	CMP (ZP), Y 25*	CMP (ZP) 25			CMP ZP, X 24	DEC ZP, X 26	CLD Impl 12	CMP ABS,Y 34*	PHX Impl 13			CMP ABS, X 34*	DEC ABS, X 37		D
E	CPX IMM 22	SBC (ZP, X) 26+			CPX ZP 23	SBC ZP 23+	INC ZP 25	INX Impl 12	SBC IMM 22+	NOP Impl 12		CPX ABS 34	SBC ABS 34+	INC ABS 36		E
F	BEQ Rela 22**	SBC (ZP), Y 25*+	SBC (ZP) 25			SBC ZP, X 24+	INC ZP, X 26	SED Impl 12	SBC ABS,Y 34*+	PLX Impl 14			SBC ABS,X 34*+	INC ABS, X 37		F
	0	1	2	3	4	5	6	8	9	A	B	C	D	E	F	

BRK / Impl / 17 — OP Code / Addressing Mode / Instruction Bytes, Machine Cycles

☐ — New Opcode

LSB — Least significant Byte

MSB — Most significant Byte

\+ Add 1 to N if in decimal mode.

* Add 1 to N if page boundary is crossed.

** Add 1 to N if branch occurs to same page;
Add 2 to N if branch occurs to different page.

DC CHARACTERISTICS

DC Characteristics: V_{DD}= 5.0V ±5%, V_{SS}= 0V, T_A= -40°C to +85°C

Parameter	Symbol	Min	Typ	Max	Unit
Input High Voltage					
ϕ0 (IN), CLK (IN)	V_{IH}	V_{SS}+ 2.4	–	V_{DD}+ 0.3	V
ϕ2 (IN)		V_{DD}- 0.2	–	V_{DD}+ 0.3	V
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, $\overline{SO}$, DBE, BE		V_{SS}+ 2.0	–	V_{DD}+ 0.3	V
Input Low Voltage					
ϕ0 (IN), CLK (IN)	V_{IL}	V_{SS}- 0.3	–	V_{SS}+ 0.4	V
ϕ2 (IN)		V_{SS}- 0.3	–	V_{SS}+ 0.2	V
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, $\overline{SO}$, DBE, BE		V_{SS}- 0.3	–	V_{SS}+ 0.8	V
Input Leakage Current (V_{IN} = 0 to 5.25V, V_{DD} = 5.25V)					
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, $\overline{SO}$, DBE, BE (internal Pull-up)	I_{IN}	-20	–	1.0	uA
ϕ2(IN), ϕ0(IN),CLK (IN)		-1	–	1.0	uA
Address, Data, R/$\overline{W}$ (Off State)		-10	–	10.0	uA
Output High Voltage (I_{OH} = -100μA, V_{DD}= 4.75V) SYNC, Data, A0-A15, R/$\overline{W}$	V_{OH}	V_{SS} + 2.4	–	–	V
Output Low Voltage (I_{OL} = 1.6mA, V_{DD}= 4.75V) SYNC, Data, A0-A15, R/$\overline{W}$	V_{OL}	–	–	V_{SS}+ 0.4	V
Supply Current f = 1 MHz	I_{CC}	–	–	4	mA
f = 2 MHz				8	
f = 3 MHz				12	
f = 4 MHz				16	
Capacitance (V_{IN}= 0, T_A = 25°C, f = 1 MHz					pF
Logic, ϕ0 (IN), CLK (IN)	Cin	–	–	10	
A0-A15, R/$\overline{W}$, Data (Off State)	C_{TS}	–	–	15	
ϕ2 (IN)	C2 (IN)	–	–	40	

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to + 7.0	V
Input Voltage	V_{IN}	-0.3 to + 7.0	V
Operating Temperature	T_A	-40 to + 85	^{O}C
Storage Temperature	T_S	-55 to + 150	^{O}C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.

AC CHARACTERISTICS

AC Characteristics
HKE65SC02 – 07
HKE65SC12 – 15
HKE65SC112 – 115
V_{DD} = 5.0V ±5%, T_A = –40°C to + 85°C

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		MIN	Max	Min	Max	Min	Max	Min	Max	
Delay Time, ϕ0(IN) to ϕ2 (OUT)	tDϕ0	–	100	–	100	–	100	–	100	nS
Delay Time, ϕ2(IN) to ϕ2 (OUT)	tDϕ2	–	75	–	75	–	75	–	75	nS
Delay Time, ϕ1(OUT) to ϕ2 (OUT)	tDϕ1	–	50	–	50	–	50	–	50	nS
Cycle Time	tCYC	1.0	DC	0.50	DC	0.33	DC	0.25	DC	nS
Clock Pulse Width Low	tPW(ϕ2L)	470	–	240	–	160	–	115	–	nS
Clock Pulse Width High	tPW(ϕ2H)	470	–	240	–	160	–	115	–	nS
Fall Time, Rise Time	tF, tR	–	25	–	25	–	15	–	15	nS
Address Hold Time	tAH	30	–	30	–	15	–	10	–	nS
Address Setup Time	tADS	225	–	140	–	110	–	90	–	nS
Access Time	tACC	650	–	310	–	170	–	110	–	nS
Read Data Hold Time	tDHR	10	–	10	–	10	–	10	–	nS
Read Data Setup Time	tDSR	100	–	50	–	50	–	50	–	nS
Write Data Delay Time	tMDS	–	175	–	100	–	75	–	70	nS
Write Data Hold Time	tDHW	30	–	30	–	30	–	30	–	nS
$\overline{SO}$ Setup Time	tSO	100	–	50	–	35	–	25	–	nS
Processor Control Setup Time	tPCS	200	–	200	–	150	–	120	–	nS

AC Characteristic
HKE65SC102 – 107
V_{DD} = 5.0V ±5%, T_A = –40°C to + 85°C.

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Delay Time, CLK (IN) to ϕ2 (OUT)	tDCLK	–	100	–	100	–	100	–	100	nS
Delay Time, $\overline{OSC}$(OUT) to ϕ2 (OUT)	tDOSC	–	75	–	75	–	75	–	75	nS
Cycle Time	tCYC	1.0	DC	0.50	DC	0.33	DC	0.25	DC	nS
Clock Pulse Width Low	tPW(ϕ2L)	470	–	240	–	160	–	115	–	nS
Clock Pulse Width High	tPW(ϕ2H)	470	–	240	–	160	–	115	–	nS
Fall Time, Rise Time	tF, tR	–	25	–	25	–	15	–	15	nS
Delay Time, ϕ2(OUT) to ϕ4(OUT)	tAVS	–	250	–	125	–	83	–	63	nS
Address Valid to ϕ4 (OUT)	tAϕ4	50	–	25	–	16	–	12	–	nS
Address Hold Time	tAH	30	–	20	–	20	–	20	–	nS
Access Time	tACC	695	–	340	–	220	–	170	–	nS
Read Data Hold Time	tDHR	10	–	10	–	10	–	10	–	nS
Read Data Setup Time	tDSR	80	–	40	–	30	–	20	–	nS
Write Data Hold Time	tDHW	30	200	30	–	30	–	30	–	nS
Write Data Delay Time	tDDϕ4	–	–	–	110	–	70	–	30	nS
$\overline{SO}$ Setup Time	tSO	100	–	50	–	35	–	25	–	nS
Processor Control Setup Time	tPCS	100	–	50	–	35	–	25	–	nS

FAMILY MEMBER DESCRIPTION

(A) Functional

The capabilities of each microprocessor in the HKE65SCXXX family is summarized in Table III.

Table III HKE65SCXXX FAMILY MICROPROCESSOR CAPABILITIES

ITEM NO.	HKE PART NUMBER	DIP PINS	ADDRESSABLE MEMORY (BYTES)	ON-CHIP CLOCK OSCILLATOR (SEE NOTE)	EXTERNAL CLOCK GENERATOR REQUIRED	ADVANCED MEMORY ACCESS (ϕ4)	$\overline{IRQ}$	$\overline{NMI}$	$\overline{SO}$	DBE	BE	SYNC	RDY	$\overline{ML}$	$\overline{RES}$
1	✓65SC02	40	04/0130 65K	•			•	•	•			•	•		•
2	✓65SC03	28	4K		•		•	•							•
3	✓65SC04	28	8K		•		•								•
4	✓65SC05	28	4K		•		•						•		•
5	✓65SC06	28	4K		•		•								•
6	✓65SC07	28	8K		•								•		•
7	✓65SC12	40	65K		•		•	•		•		•			•
8	✓65SC13	28	4K		•		•	•							•
9	✓65SC14	28	8K		•		•								•
10	✓65SC15	28	4K		•		•						•		•
11	✓65SC102	40	65K	•		•	•	•	•		•	•	•	•	•
12	✓65SC103	28	4K		•	•	•	•							•
13	✓65SC104	28	8K		•	•	•								•
14	✓65SC105	28	4K		•	•	•						•		•
15	✓65SC106	28	4K		•	•	•								•
16	✓65SC107	28	8K		•	•							•		•
17	✓65SC112	40	65K	•			•	•	•		•	•	•	•	•
18	✓65SC115	28	4K		•		•						•	•	•

NOTE: These devices can operate in any of the following clock generation modes: 1. External crystal 2. External RC network 3. ϕ0(IN) from external clock source

As shown in Table III, the family includes 18 microprocessors of which three have on-chip oscillators while the others require an external clock generator. The HKE65SC02, HKE65SC102 or HKE65SC112 on-chip oscillators may be driven by an external crystal (Figure 4(a)), an RC network (Figure 4(b)) or by an external clock source. The rest (15 microprocessors) of the microprocessors in the family require an external oscillator. An example of the crystal circuit of an external oscillator is given in Figure 4(c)

The versions of the microprocessor which require an external clock source are generally intended for multiprocessor applications where maximum timing control is necessary. The three family members with on-chip oscillators are intended for high performance, low cost operations where single phase inputs, crystals, or RC inpouts provide the time base.

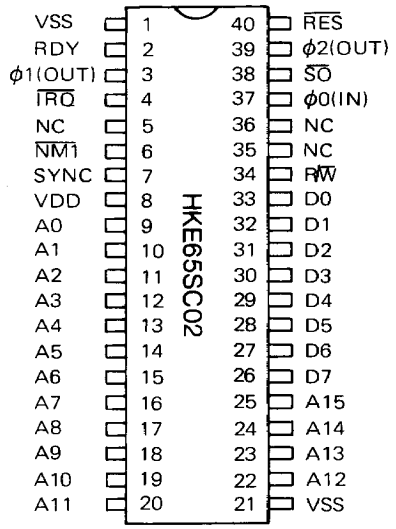
(B) Pin Configuration

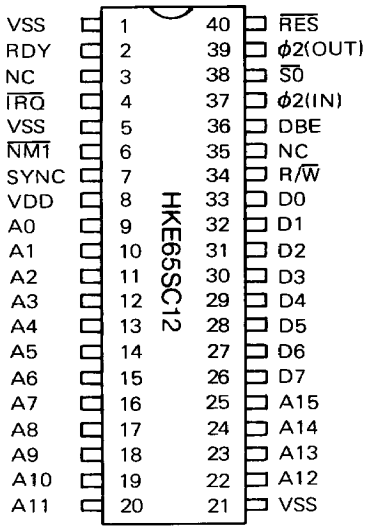
PIN FUNCTION TABLE

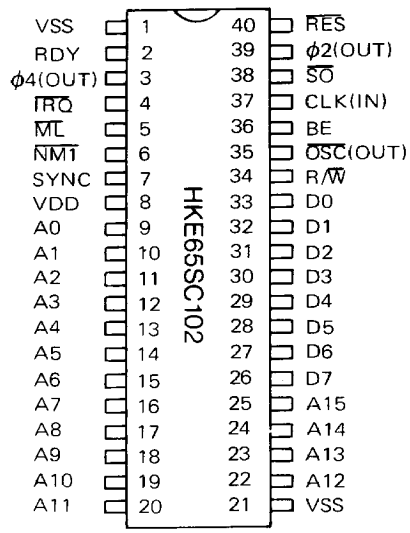
Pin	Description
A0-Axx	Address Bus
BE	Bus Enable
CLK(IN)	Clock Input
ϕ0 (IN)	Phase 0 In
ϕ2 (IN)	Phase 2 In
DBE	Data Bus Enable
D0-D7	Date Bus
$\overline{IRQ}$	Interrupt Request
ML	Memory Lock
NC	No Connection
$\overline{NMI}$	Non-Maskable Interrupt

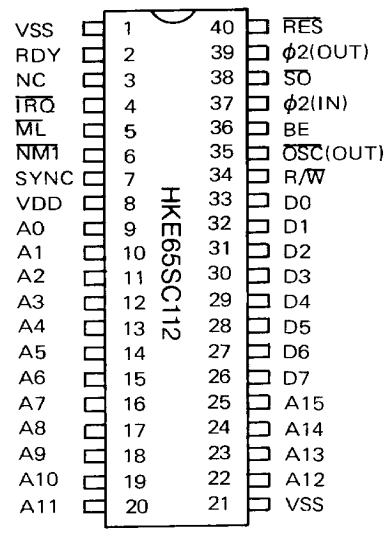
Pin	Description
$\overline{OSC}$ (OUT)	Oscillator Output
ϕ1(OUT)	Phase 1 Out
ϕ2(OUT)	Phase 2 Out
ϕ4(OUT)	Phase 4 Out
RDY	Ready
$\overline{RES}$	Reset
R/$\overline{W}$	Read/Write
$\overline{SO}$	Set Overflow
SYNC	Synchronize
V_{DD}	Positive Power Supply (+5.0 Volts)
Vss	Internal Logic Ground

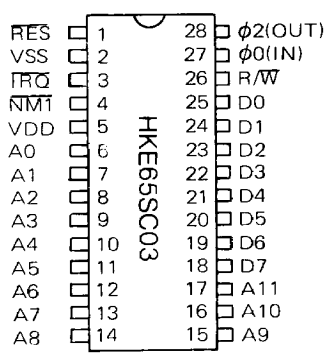
Pin Configuration

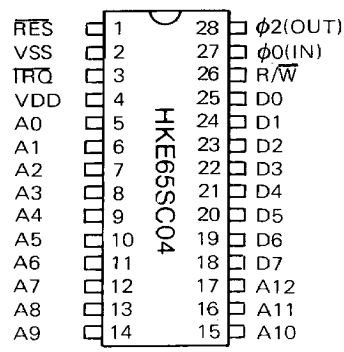




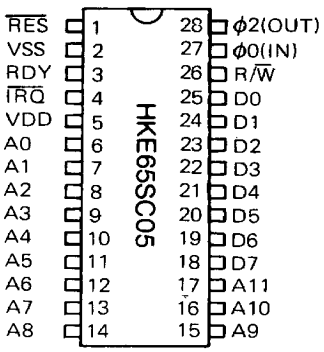


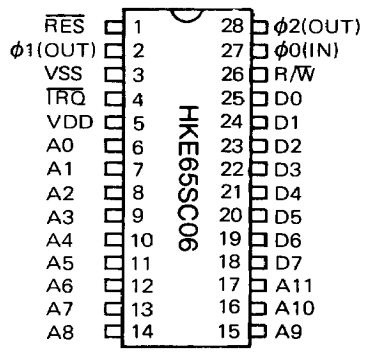


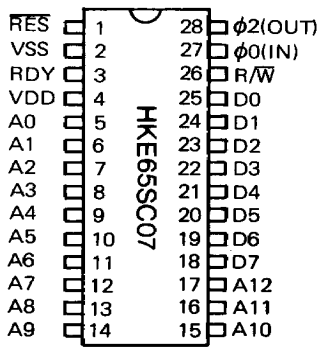


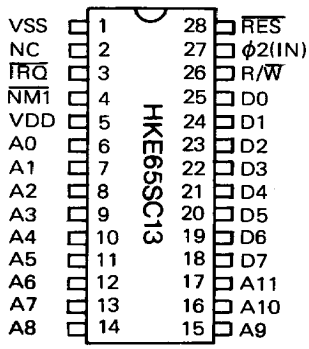


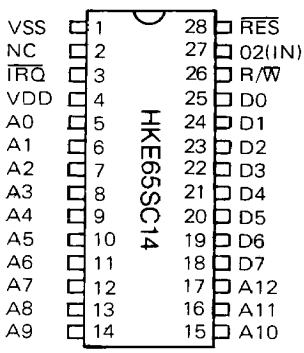
Pin Configuration

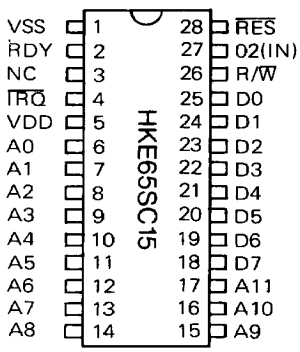


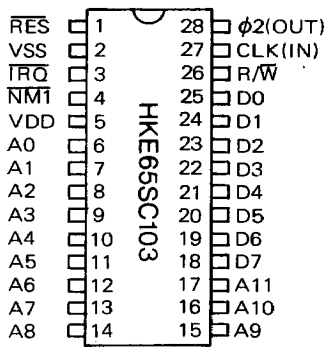


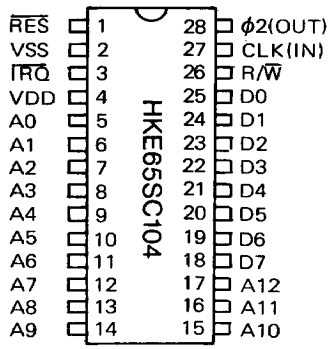


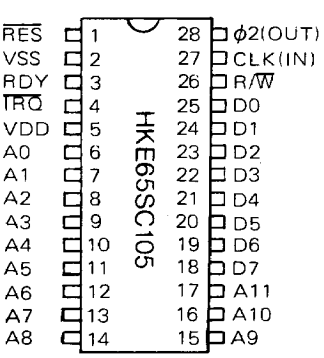


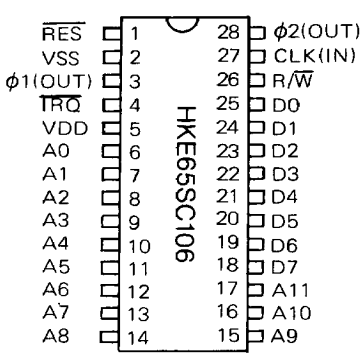


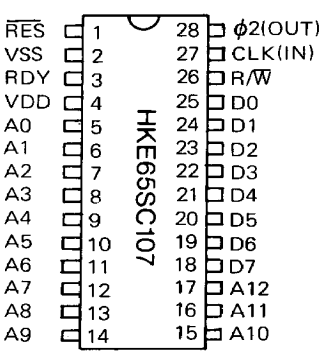


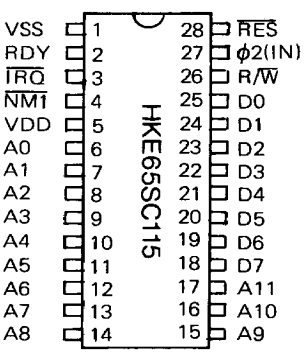






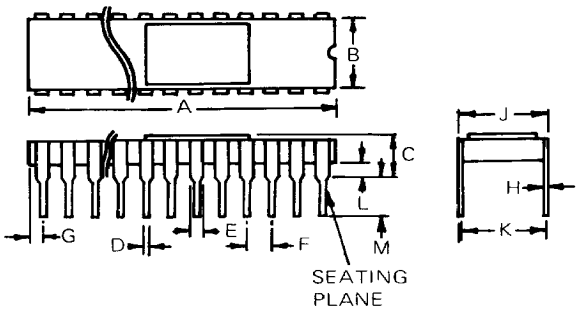




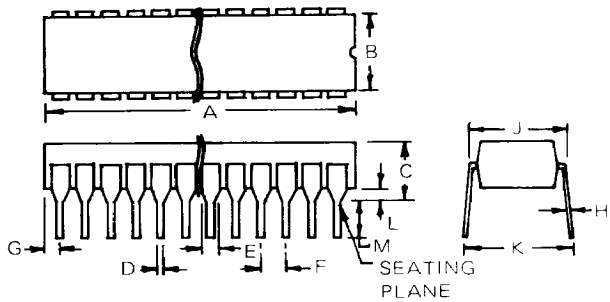


PACKAGING INFORMATION

Typical Outline Drawing (Ceramic)



Typical Outline Drawing (Plastic & Cerdip)



DIM	40 PIN CERAMIC PACKAGE			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.419	51.181	1.985	2.015
B	14.605	15.367	0.575	0.605
C		3.810		0.150
D	0.381	0.533	0.015	0.021
E	0.889	1.524	0.035	0.060
F	2.286	2.794	0.090	0.110
G	1.016	1.524	0.040	0.060
H	0.203	0.305	0.008	0.012
J	15.113	15.875	0.590	0.620
K	15.24	REF	0.600	REF
L	0.889	1.651	0.035	0.065
M	2.540	3.556	0.100	0.140

DIM	40 PIN PLASTIC PACKAGE			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
E	1.02	1.52	0.040	0.060
F	2.54	TYP	0.100	TYP
G	1.65	2.16	0.065	0.085
H	0.20	0.38	0.008	0.015
J	15.24	TYP	0.600	TYP
K				
L	0.51	1.02	0.020	0.040
M	2.92	3.43	0.115	0.135

DIM	40 PIN CERDIP PACKAGE			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		53.57		2.109
B	12.19	14.98	0.480	0.590
C				
D	0.381	0.508	0.015	0.020
E	1.016	1.651	0.040	0.065
F	2.540	TYP	0.100	TYP
G				
H	0.203	0.305	0.008	0.012
J	14.99	15.490	0.590	0.610
K				
L	0.381		0.015	
M	2.290		0.090	

DIM	28 PIN CERAMIC PACKAGE			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	35.20	35.92	1.386	1.414
B	14.43	14.94	0.568	0.588
C	3.05	4.19	0.120	0.165
D	0.41	0.51	0.016	0.020
E	1.12	1.42	0.044	0.056
F	2.54 BSC		0.100 BSC	
G	1.12	1.42	0.044	0.056
H	0.23	0.26	0.008	0.011
J	14.83	15.14	0.584	0.596
K				
L	0.51	0.52	0.020	0.060
M	2.54	4.19	0.100	0.165

DIM	28 PIN PLASTIC PACKAGE			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.32	37.34	1.430	1.470
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.38	0.51	0.015	0.020
E	1.02	1.52	0.040	0.060
F	2.41	2.67	0.095	0.105
G	1.65	2.16	0.065	0.085
H	0.20	0.30	0.008	0.012
J	14.99	15.49	0.590	0.610
K				
L	0.51	1.02	0.020	0.040
M	3.05	3.56	0.120	0.140

DIM	28 PIN CERDIP PACKAGE			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
E	1.02	1.52	0.040	0.060
F	2.54	TYP	0.100	TYP
G	1.65	2.16	0.065	0.085
H	0.20	0.38	0.008	0.015
J	15.24	TYP	0.600	TYP
K				
L	0.51	1.02	0.020	0.040
M	2.92	3.43	0.115	0.135

ORDERING INFORMATION

HKE — 65SCXXX — P — L — -2

Hua Ko Electronics

Product Identification Number

Version

Package

P – Plastic
C – Ceramic
D – Cerdip
E – Leadless Chip Carrier
X – Dice

Temperature/Processing

Non – 0° to +70°C
C – -40°C to + 80°C (Commercial)
L – -55°C to + 125°C (Industrial)

Performance Designator

Designators selected for speed and power specifications
–1 1MHz
–2 2MHz
–3 3MHz