Features

- **Fast Interleave Cycle Time - 35 ns**
- **Continuous Memory Interleaving**
  - **Unlimited Linear Access Data Output**
- **Dual Voltage Range Operation**
  - **Low-Voltage Power Supply Range, 3.0V to 3.6V or Standard 5V ± 10% Supply Range**
- **Low-power CMOS Operation**
  - **108 mW max. Active at 25 MHz for V_{CC} = 3.6V**
  - **14.4 mW max. Standby for V_{CC} = 3.6V**
- **JEDEC Standard Surface Mount Packages**
  - **44-lead PLCC**
  - **40-lead VSOP (10 x 14mm)**
- **High-reliability CMOS Technology**
  - **2,000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid™ Programming Algorithm - 50 µs/word (typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
  - **JEDEC Standard for LVTTL**
- **Integrated Product Identification Code**
- **Commercial and Indvtustrial Temperature Ranges**

Description

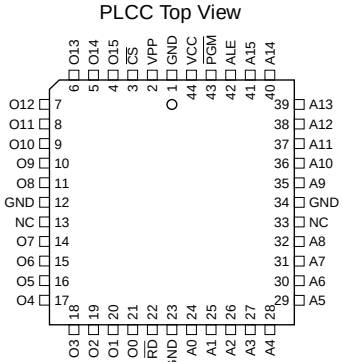
The AT27LV1026 is a high performance 16-bit interleaved low-voltage 1,048,576-bit one-time programmable read only memory (OTP EPROM) organized as 2 x 32K x 16 bits. It requires only one supply in the range of 3.0V to 3.6V in normal read mode operation.

Pin Configurations

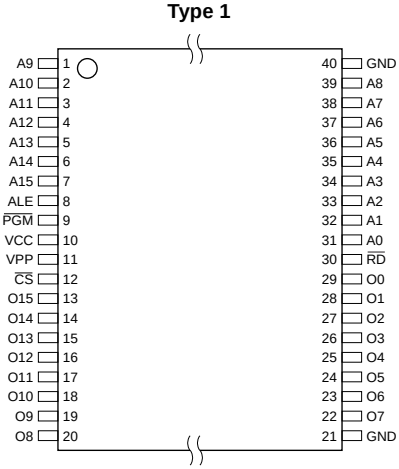
Pin Name	Function
A0 - A15	Addresses
O0 - O15	Outputs
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Strobe
ALE	Address Latch Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

Note: Both GND pins must be connected.

PLCC Top View



VSOP Top View
Type 1



1-Megabit (2 x 32K x 16) 16-bit Interleaved Low-Voltage OTP EPROM

AT27LV1026

Rev. 0956F–01/99

This device is internally architected as two 32K x 16 memory banks, odd and even. To begin a non-linear access NLA cycle, (which typically equals a minimum of two linear access LA cycles), ALE is asserted high and $\overline{CS}$ is asserted low. The two internal 15-bit counters store the address for the odd and even banks and increment alternately during each subsequent linear access LA cycle. The LA cycle will be terminated when $\overline{CS}$ is asserted high putting the device in standby mode, or another NLA cycle starts. The LA cycle can be resumed when $\overline{CS}$ is asserted low and ALE stays low. The AT27LV1026 will continuously output data within each LA cycle which is determined by the read $\overline{RD}$ signal. Continuous interleave read operation is possible as there is no physical limit to the linear access LA output. When the last address in the array is reached the counters will wrap around to the first address location and continue.

For a NLA cycle where A0 = 0 (ALE asserted high, $\overline{CS}$ asserted low), both even and odd counters will be loaded with new address (A1 - A15). Outputs (O0 - O15) from the even bank will be valid in t_{ACCNLA} within the NLA cycle, the outputs from the odd bank will become valid in t_{ACCLA} within the following LA cycle while the even counter increments by one to ready the data out for the next LA cycle. The outputs will have even or odd data alternating and the counters increment for the consecutive LA cycles until $\overline{CS}$ is asserted high putting the device in standby mode, or a new NLA cycle begins.

For a NLA cycle where A0 = 1 (ALE asserted high, $\overline{CS}$ asserted low), the odd counter will be loaded with the new address (A1 - A15) while the even counter gets loaded with the new address+1. Outputs (O0 - O15) from odd bank of memory will be valid in t_{ACCNLA} within the NLA cycle, the data output from the even bank of memory will become valid in t_{ACCLA} within the following LA cycle while the odd counter increments by one to ready the data out for the next LA cycle. The outputs will have data from the odd or even memory bank alternately and the counters increment for the following consecutive LA cycles until $\overline{CS}$ is asserted high putting the device in standby mode, or a new NLA cycle begins. When coming out of standby mode, the device can either enter into a new NLA cycle or resume where the previous LA operation left off and was terminated by standby mode.

System Considerations

Switching under active conditions may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Operating Table

If A0 = 0 at beginning of NLA cycle:

Consecutive Cycle	Counter		Outputs
	Even	Odd	
NLA	Address	Address	from Even Bank
LA	+1	-	from Odd Bank
LA	-	+1	from Even Bank
LA	+1	-	from Odd Bank
LA	-	+1	from Even Bank
Standby			Hi-Z
LA	+1	-	from Odd Band
LA	-	+1	from Even Bank

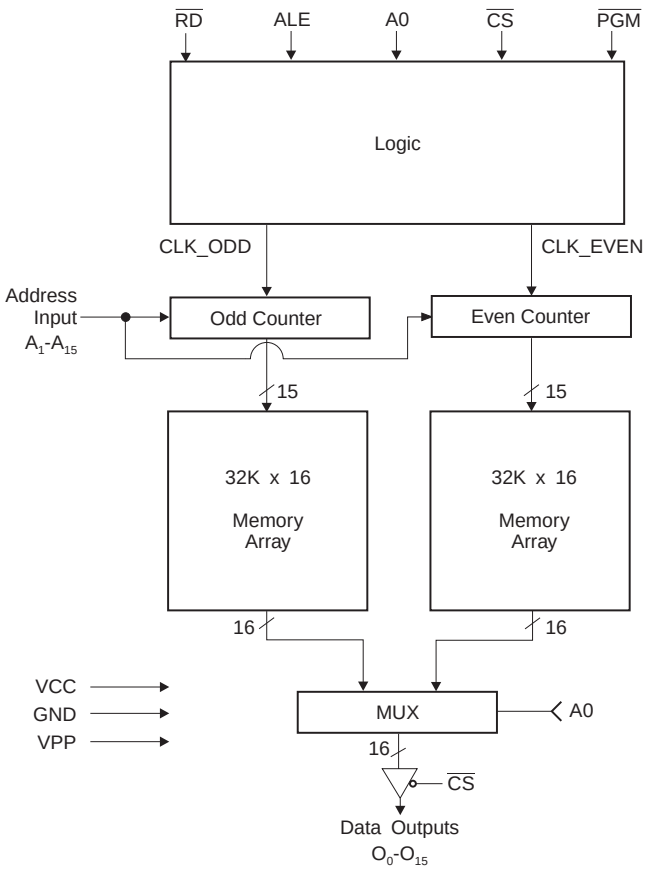
and so on.

If A0 = 1 at beginning of NLA cycle:

Consecutive Cycle	Counter		Outputs
	Even	Odd	
NLA	Address+1	Address	from Odd Bank
LA	-	+1	from Even Bank
LA	+1	-	from Odd Bank
LA	-	+1	from Even Bank
LA	+1	-	from Odd Bank
Standby			Hi-Z
LA	-	+1	from Even Bank
LA	+1	-	from Odd Band

and so on.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

Mode/Pin	ALE	$\overline{CS}$	$\overline{RD}$	$\overline{PGM}$	A_0	A_1 - A_{15}	V_{PP}	V_{CC}	Outputs
Non-Linear Access Cycle[2]	⎍	V_{IL}	V_{IL}	V_{IH}	V_{IL}/V_{IH}	Ai	X	V_{CC}[2]	D_{OUT}
Linear Access Cycle[2]	V_{IL}	V_{IL}	⎍	V_{IH}	X[1]	X	X	V_{CC}[2]	D_{OUT}
Standby[2]	X	V_{IH}	X	V_{IH}	X	X	X	V_{CC}[2]	High Z
Rapid Program[3]	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}/V_{IH}	Ai	V_{PP}	V_{CC}[3]	D_{IN}
PGM Verify[3]	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}/V_{IH}	Ai	V_{PP}	V_{CC}[3]	D_{OUT}
PGM Inhibit[3]	X	V_{IH}	X	V_{IH}	X	X	V_{PP}	V_{CC}[3]	High Z
Product Identification[3][5]	X	V_{IL}	X	V_{IH}	V_{IL}/V_{IH}	$A_9 = V_H$ [4] A_1 - $A_{15} = V_{IL}$	V_{CC}	V_{CC}[3]	Identification Code

Notes:
1. X can be V_{IL} or V_{IH}.
2. Non-Linear and Linear Access Cycles, and standby modes require, $3.0V \le V_{CC} \le 3.6V$, or $4.5V \le V_{CC} \le 5.5V$.
3. Refer to Programming Characteristics. Programming modes require $V_{CC} = 6.5V$.
4. $V_H = 12.0 \pm 0.5V$.
5. Two identifier words may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification word and high (V_{IH}) to select the Device Code word.

DC and AC Operating Conditions for Read Operation

		AT27LV1026-35	AT27LV1026-45	AT27LV1026-55
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0V to 3.6V	3.0V to 3.6V	3.0V to 3.6V
		5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 3.0V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1}[2]	V_{PP}[1] Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC}[1] Standby Current	$\overline{CS}$ = V_{IH}		5	mA
I_{CC}	V_{CC} Active Current	f = 25 MHz, I_{OUT} = 0 mA, $\overline{CS}$ = V_{IL}		30	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1}[2]	V_{PP}[1] Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC}[1] Standby Current	$\overline{CS}$ = V_{IH}		8	mA
I_{CC}	V_{CC} Active Current	f = 25 MHz, I_{OUT} = 0 mA, $\overline{CS}$ = V_{IL}		50	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}

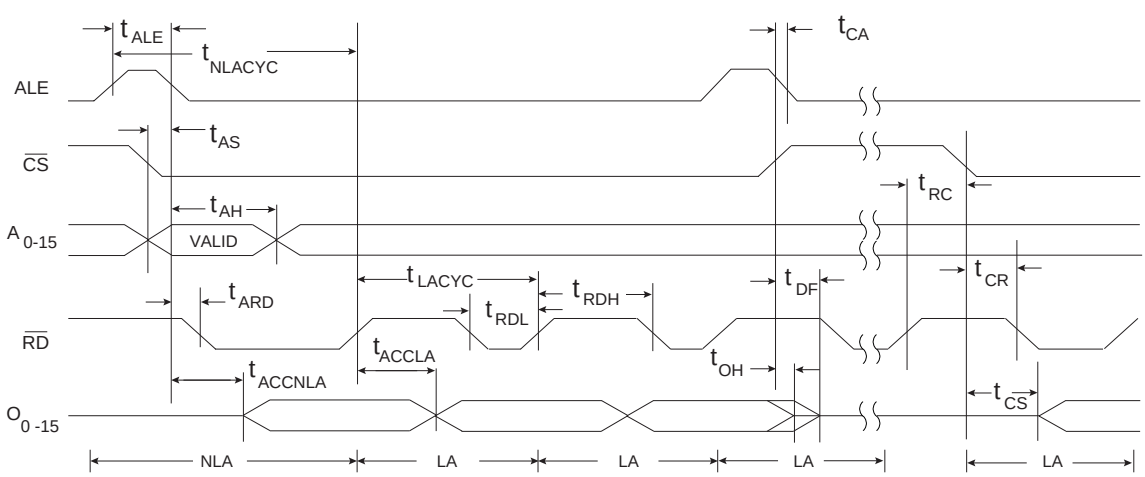
AC Characteristics for Read Operation

V_{CC} = 3.0V to 3.6V and 4.5V to 5.5V

Symbol	Parameter	Condition	AT27LV1026			Units
			Min	Typ	Max	
t_{NLACYC}	Non-Linear Access Cycle		70	80		ns
t_{LACYC}	Linear Access Cycle	ALE = $\overline{CS}$ = V_{IL}	35	40		ns
t_{ALE}	ALE High Width		7.5			ns
t_{AS}	Address/$\overline{CS}$ Setup Time		2.5			ns
t_{AH}	Address Hold Time		20			ns
t_{ARD}	ALE Low to $\overline{RD}$ Low		4.5			ns
t_{RDL}	$\overline{RD}$ Low Width	ALE = $\overline{CS}$ = V_{IL}	12			ns
t_{RDH}	$\overline{RD}$ High Width	ALE = $\overline{CS}$ = V_{IL}	12			ns
t_{ACCNLA}	Address to Output Delay in Non-Linear Address Cycle from ALE Low				52	ns
t_{ACCLA}	Output Valid Delay in Linear Address Cycle from $\overline{RD}$ High	ALE = $\overline{CS}$ = V_{IL}			20	ns
t_{DF} (2)(3)	$\overline{CS}$ High to Output Float				14	ns
t_{OH}	Output Hold from $\overline{CS}$ High		0			ns
t_{CS}	Output Valid Delay from $\overline{CS}$ Low in Linear Address Cycle				17	ns
t_{RC}	$\overline{RD}$ High to $\overline{CS}$ Falling Edge Delay		2			ns
t_{CR}	$\overline{CS}$ Falling Edge to $\overline{RD}$ Low Delay		12			ns
t_{CA}	$\overline{CS}$ Rising Edge to ALE Low Delay		2.5			ns

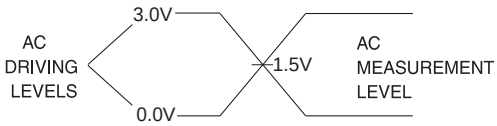
Notes: 1. 2, 3. - See AC Waveforms for Read Operation.

AC Waveforms for Read Operation(1)



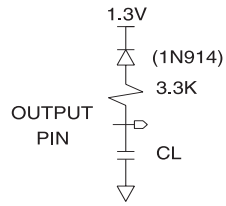
Notes: 1. Refer to Test Waveforms and Measurement Levels diagram on next page.
2. This parameter is only sampled and is not 100% tested.
3. Output float is defined as the point when data is no longer driven.
4. When reading a 27LV1026, a 0.1 µF capacitor is required across V_{CC} and ground to suppress spurious voltage transients.

Input Test Waveforms and Measurement Levels



t_R, t_F < 2.5 ns (10% to 90%)

Output Test Load



Note: C_L = 100 pF including jig capacitance.

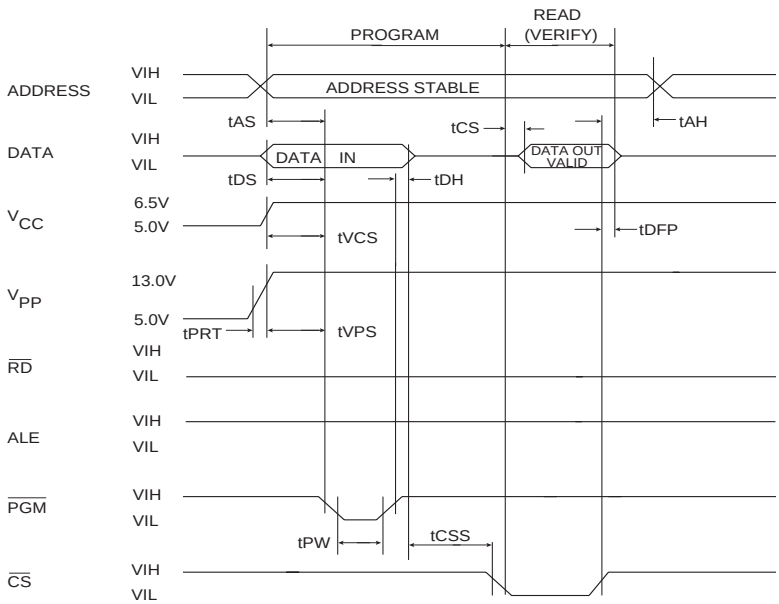
Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms (1)



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.

2. t_{CS} and t_{DFP} are characteristics of the device but must accompanied by the programmer.

3. When programming the AT27LV1026 a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

TA = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{PGM} = V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

TA = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions [1]	Limits		Units
			Min	Max	
t_{AS}	Address Setup Time	Input Rise and Fall Times (10% to 90%) 20 ns Input Pulse Levels 0.45V to 2.4V Input Timing Reference Level 0.8V to 2.0V Output Timing Reference Level 0.8V to 2.0V	2		µs
t_{CSS}	$\overline{CS}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CS}$ High to Output Float Delay [2]		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width [3]		45	55	µs
t_{CS}	Data Valid from $\overline{CS}$			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.

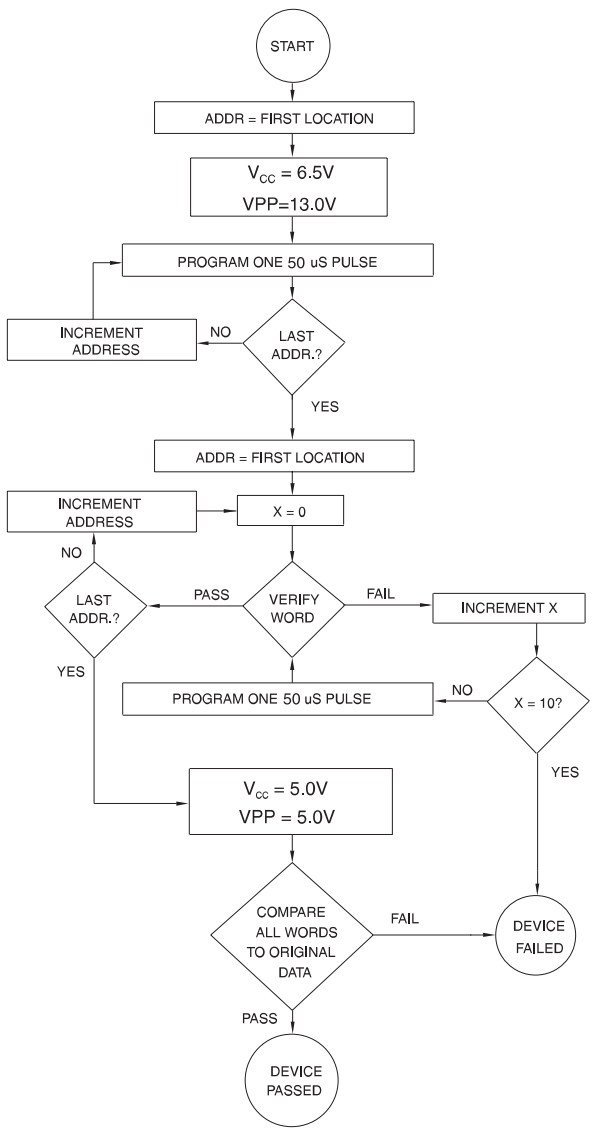
3. Program Pulse width tolerance is 50 µsec ± 5%.

Atmel's 27LV1026 Integrated Product Identification Code

Codes	Pins										Hex Data
	A0	O15-O8	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	0	1	1	0	0	0	0	1	0061

Rapid Programming Algorithm

A 50 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 50 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



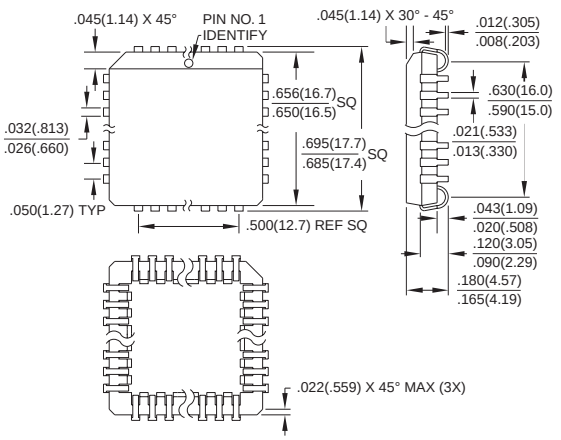
Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
35	30	0.1	AT27LV1026-35JC AT27LV1026-35VC	44J 40V	Commercial (0°C to 70°C)
	30	0.1	AT27LV1026-35JI AT27LV1026-35VI	44J 40V	Industrial (-40°C to 85°C)
45	30	0.1	AT27LV1026-45JC AT27LV1026-45VC	44J 40V	Commercial (0°C to 70°C)
	30	0.1	AT27LV1026-45JI AT27LV1026-45VI	44J 40V	Industrial (-40°C to 85°C)
55	30	0.1	AT27LV1026-55JC AT27LV1026-55VC	44J 40V	Commercial (0°C to 70°C)
	30	0.1	AT27LV1026-55JI AT27LV1026-55VI	44J 40V	Industrial (-40°C to 85°C)

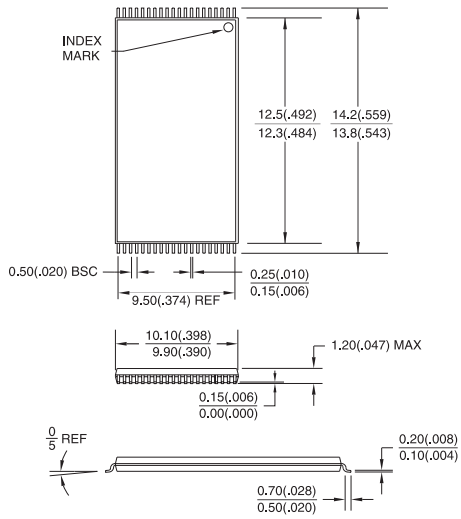
Package Type	
44J	44-Lead, Plastic J-Leaded Chip Carrier (PLCC)
40V	40-Lead, Plastic Thin Small Outline Package (VSOP) 10 x 14 mm

Packaging Information

44J, 44-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



40V, 40-Lead, Plastic Thin Small Outline Package (VSOP)
Dimension in Millimeters and (Inches)
JEDEC OUTLINE MO-142 CA



*Controlling dimension: millimeters

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686677
FAX (44) 1276-686697

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road
Tsimshatsui East
Kowloon, Hong Kong
TEL (852) 27219778
FAX (852) 27221369

Japan
Atmel Japan K.K.
Tonetsu Shinkawa Bldg., 9F
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4 42 53 60 00
FAX (33) 4 42 53 60 01

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

0956F–01/99/xM