ST-NXP Wireless

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- **Web site** - http://www.nxp.com is replaced with http://www.stnwireless.com

- **Contact information** - the list of sales offices previously obtained by sending an email to salesaddresses@nxp.com , is now found at http://www.stnwireless.com under Contacts.

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ST-NXP Wireless

TEA5760UK

Single chip FM stereo radio

Rev. 01 — 14 December 2006 Product data sheet

1. General description

The TEA5760UK is a single chip electronically tuned FM stereo radio for low voltage applications with fully integrated Intermediate Frequency (IF) selectivity and demodulation.

The radio is completely adjustment free and only requires a minimum of small and low cost external components.

The TEA5760UK does not meet all of the requirements from EN55020, a trade off was done to make possible the previously stated features.

The TEA5760UK application software is compatible to the TEA5761UK software to enable easy design in for customers.

2. Features

- High sensitivity due to integrated low noise Radio Frequency (RF) input amplifier
- FM mixer for conversion of the US/Europe (87.5 MHz to 108 MHz) and Japanese FM band (76 MHz to 90 MHz) to IF
- Preset tuning to receive Japanese TV audio up to 108 MHz and raster 100 kHz
- Autonomous search tuning, 100 kHz grid
- RF Automatic Gain Control (AGC) circuit
- LC tuner oscillator operating with one low cost chip inductor (external varicap not required)
- Fully integrated FM IF selectivity
- Fully integrated FM demodulator
- 32.768 kHz external reference frequency
- Phase-Locked Loop (PLL) synthesizer tuning system
- IF counter; 7-bit output via control interface
- Level detector, 4-bit level information output via the control interface
- Soft mute, signal level dependent mute function
- Signal level dependent mono/stereo blend, Stereo Noise Cancelling (SNC)
- Soft mute and SNC can be switched off via control interface
- Adjustment free stereo decoder
- I^2C-bus interface
- Standby mode
- One software programmable port
- Interrupt flag

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA5760UK	WLCSP25	wafer level chip-size package; 25 bumps; die 3 × 2.8 × 0.6 mm	TEA5760UK

4. Block diagram

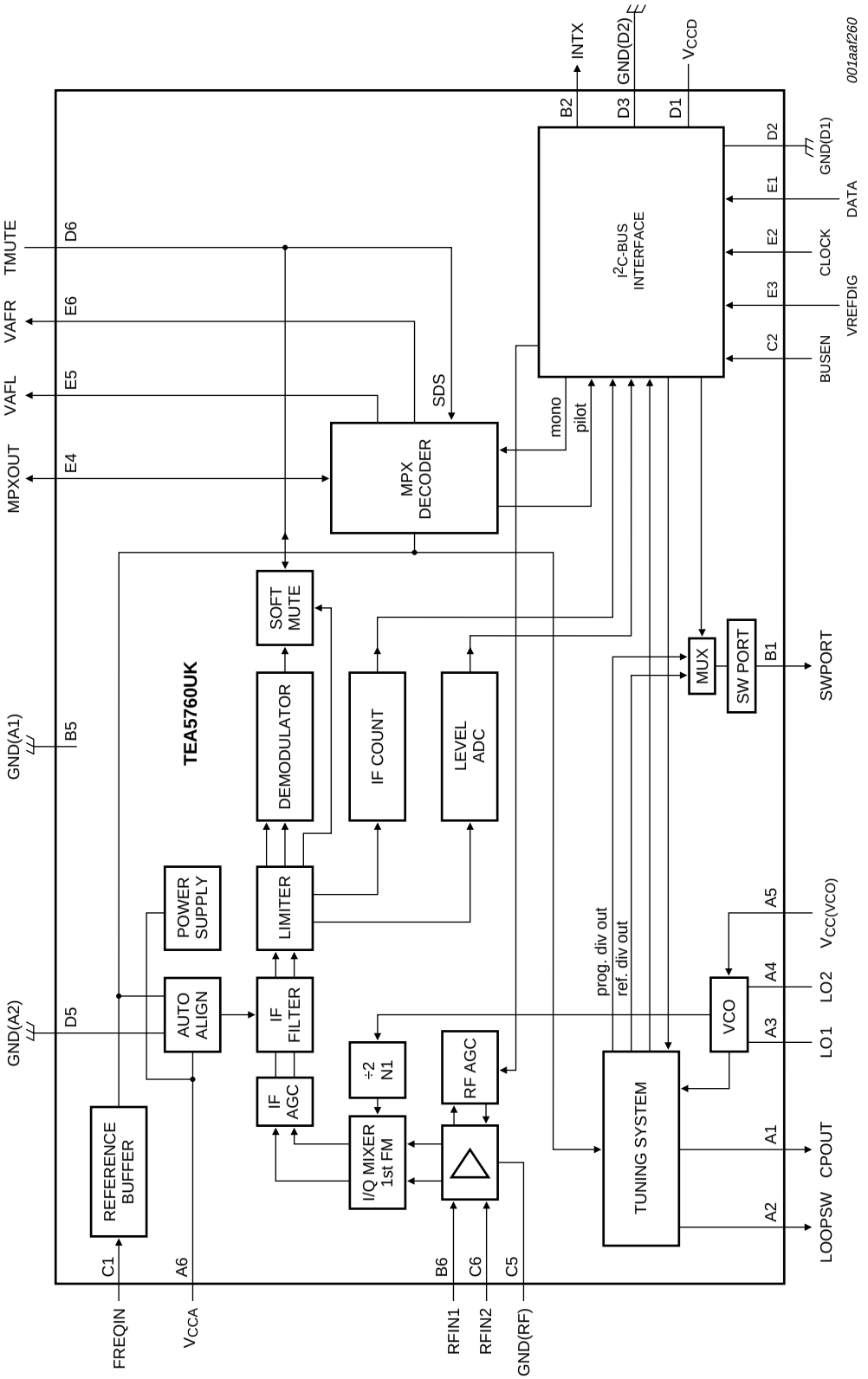


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

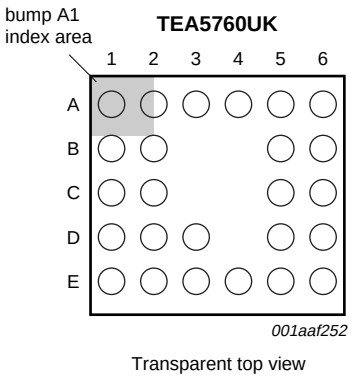


Fig 2. Ball configuration TEA5760UK

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
CPOUT	A1	charge pump output of synthesizer PLL
LOOPSW	A2	switch output of synthesizer PLL loop filter
LO1	A3	local oscillator coil connection
LO2	A4	local oscillator coil connection
$V_{CC(VCO)}$	A5	Voltage Controlled Oscillator (VCO) supply voltage
V_{CCA}	A6	analog supply voltage
SWPORT	B1	software programmable port
INTX	B2	interrupt
GND(A1)	B5	analog ground 1
RFIN1	B6	RF input 1
FREQIN	C1	input for 32.768 kHz reference frequency
BUSEN	C2	bus enable input for control interface
GND(RF)	C5	RF ground
RFIN2	C6	RF input 2
V_{CCD}	D1	digital supply voltage
GND(D1)	D2	digital ground 1
GND(D2)	D3	digital ground 2
GND(A2)	D5	analog ground 2
TMUTE	D6	time constant for soft mute
DATA	E1	control interface data line input/output
CLOCK	E2	control interface clock line input
VREFDIG	E3	digital reference voltage for control interface

Table 2. Pin description *...continued*

Symbol	Pin	Description
MPXOUT	E4	multiplex signal (MPX) output pin
VAFL	E5	left audio output
VAFR	E6	right audio output

6. Functional description

6.1 Low noise RF amplifier

The Low Noise Amplifier (LNA) input impedance together with the LC RF input circuit defines an FM band filter. The gain of the LNA is controlled by the RF AGC circuit to prevent overdrive of the subsequent circuits.

6.2 FM mixer

The FM quadrature mixer converts the received RF (76 MHz to 108 MHz) to an IF of 225 kHz. Downconversion is achieved by multiplying the RF with the Local Oscillator (LO) frequency. Image frequency suppression is achieved by using quadrature signal processing.

6.3 VCO

The LC tuned VCO provides the LO signal for the FM quadrature mixer. The VCO frequency range is 150 MHz to 217 MHz. No external varactor is required.

6.4 Reference frequency

An external 32.768 kHz reference frequency is used as the system clock. The reference frequency specifications are given in Section 10.

The reference frequency is used for:

- Synthesizer PLL reference frequency
- Timing for the IF counter
- Adjustment of the frequency of the stereo decoder VCO
- Auto alignment of the selectivity as well as the demodulator filters

6.5 PLL tuning system

The PLL synthesizer tuning system is designed to operate with a 32.768 kHz reference frequency. A 14-bit word is used to tune the radio (see Table 11 and Table 12). Calculation of this 14-bit word is as follows.

Formula for high-side injection: $N_{DEC} = \frac{[4 \times (f_{RF} + f_{IF})]}{f_{ref}}$

Formula for low-side injection: $N_{DEC} = \frac{[4 \times (f_{RF} - f_{IF})]}{f_{ref}}$

where:

N_{DEC} = decimal value of PLL word

f_{RF} = wanted tuning frequency (Hz)

f_{IF} = intermediate frequency (Hz): 225 kHz

f_{ref} = reference frequency (Hz): 32.768 kHz

Example for receiving a channel at 100.1 MHz:

$$N_{DEC} = \frac{[4 \times (100.e6 + 225e3)]}{32768} = 12246.704$$

The result must always be rounded to the lowest integer value. If rounded down to the lowest integer value of N_{DEC} = 12246, the PLL word becomes 2FD6h.

Via the control interface this value can be written to register FRQSET and the TEA5760UK will then start an autonomous search beginning at this frequency or go to a preset channel at this frequency. When the application is built according the application diagram (see Figure 11) and with the preferred components, the tuning system will settle to the new frequency within 40 ms.

The PLL is triggered by writing one of the following bytes: FRQSETMSB, FRQSETLSB, TNCTRL1, TNCTRL2, TESTBITS and TESTMODE.

Accurate validation of the PLL locking onto the new frequency can take 40 ms. Bit LD in register TUNCHK (see Table 18) is set when a lock is detected.

6.6 Band limits

The TEA5760UK can be switched to the Japanese FM band or the US/Europe FM band. With bit BLIM in register TNCTRL (see Table 13) set to logic 0 it enables the US/European FM band (87.5 MHz to 108 MHz), while setting bit BLIM to logic 1 enables the Japanese FM band (76 MHz to 90 MHz).

6.7 RF AGC

The RF AGC prevents overloading and limits the amount of intermodulation products created by strong adjacent channels. The default setting for the RF AGC is on and it can be turned off via the control interface. The TEA5760UK also has an inband AGC to prevent overloading by the wanted channel itself. The inband AGC is always on.

6.8 IF filter

Fully integrated IF filter with a center frequency of 225 kHz.

6.9 FM demodulator

Fully integrated FM quadrature demodulator.

6.10 IF counter

The received RF signal is converted down to a 225 kHz IF. The IF is measured by means of a frequency counter. A correct IF frequency measurement result indicates that the radio is tuned to a valid channel and not to an image or a channel with high interference. The 7-bit IF counter output can be read via the control interface. The IF counter is active when the tuning algorithm is active (see Figure 3) and the outcome can be read via the control interface. It activates a flag if the IF count result lies outside a predefined window. The IF count period can be set to 1.953 ms or 15.625 ms with bit IFCTC in register TNCTRL (see Table 13).

6.11 Level voltage generator and analog-to-digital converter

The level voltage reflects the received field strength at the antenna. The analog level voltage is digitized to 4 bits by the level Analog-to-Digital Converter (ADC). During a search or preset tuning cycle the level ADC is activated and the recorded level ADC information is stored in the registers. The level ADC information is used during search as well as preset tuning to compare the received signal strength with a search stop level (see Section 7.1.4.3). A flag will be set to indicate that the level voltage is below the predefined search stop level (see Figure 3). When the tuning algorithm is finished the level ADC is deactivated.

6.12 Mute

6.12.1 Soft mute

The low-pass filtered level voltage drives the soft mute attenuator. At low RF input levels, the audio output is faded and hence also the noise. The soft mute function can be disabled with bit SMUTE in register TNCTRL (see Table 13).

6.12.2 Hard mute

With bit MU in register TNCTRL (see Table 14) the audio outputs VAFL and VAFR can be hard muted, this means they are put in high ohmic mode. The same can be done by setting bits LHM (Left Hard Mute) or RHM (Right Hard Mute) in register TESTREG (see Table 19), which mutes only one output at a time (or both when both set). When one output is muted, the stereo decoder switches to mono. If the TEA5760UK is in Standby mode the audio outputs are in high impedance mode, see Table 3.

Table 3. Specification of mute modes

Type	Description	Left		Right	
		Impedance	Mode	Impedance	Mode
AFM	Audio Frequency Mute	350 Ω	muted	350 Ω	muted
MU	Hard Mute	500 kΩ	muted	500 kΩ	muted
LHM	Left Hard Mute	500 kΩ	muted	350 Ω	mono audio
RHM	Right Hard Mute	350 Ω	mono audio	500 kΩ	muted
Standby	Standby	1 MΩ	muted	1 MΩ	muted
SMUTE	Soft Mute	RF level sensitive audio level. Has no influence on mute or pin impedance.			

6.12.3 Audio Frequency Mute (AFM)

With bit AFM in register TNCTRL (see Table 13), the audio signal can be muted. The audio pins maintain their functional impedance and DC-biasing level while the audio signal is muted. The audio frequency mute is automatically activated during preset as well as search tuning modes as shown in the flowchart of Figure 3.

6.13 MPX decoder

The PLL stereo decoder is adjustment free. The stereo decoder can be switched to mono via the control interface.

6.14 Signal depending mono/stereo blend (stereo noise cancellation)

With decreasing RF input level the MPX decoder blends from stereo to mono to limit the output noise. The continuous mono-to-stereo blend can also be programmed via the control interface to an RF level depending on the switched mono-to stereo transition. Stereo Noise Cancellation (SNC) can be switched on/off via the control interface using bit SNC in register TNCTRL (see Table 13). The RF input voltage where blending starts can be switched with bit SNCLEV in register TESTREG (see Table 20).

6.15 Software programmable port

One software programmable port (CMOS output) is available and can be controlled via the control interface.

- Bit SWPM = 1; the software port (SWPORT) functions as the output for bit FRRFLAG
- Bit SWPM = 0; the software port outputs bit SWP of the registers

In software test mode the software port outputs signals according to Table 21. Software test mode is selected setting bit TM of register TESTREG. The software port is not disabled by bit PUPD (see Section 6.16).

6.16 Standby

With the Power-Up/Power-Down (PUPD) bit the radio can be put in Standby mode. Standby mode is defined as where the TEA5760UK has all supply voltages available but the circuits are powered down via software or after power-on reset. The TEA5760UK is still accessible via the control interface, but takes only a very limited amount of power from the supply. The software programmable port remains active to allow peripheral devices to be controlled. The audio outputs are hard muted.

When pin BUSEN is HIGH and the circuits are powered down via software (PUPD) the TEA5760UK is in Sleep mode. In Sleep mode the TEA5760UK is accessible via the I^2C-bus, but the radio part is not active. The digital supply current (I_{CCD}) is higher than in Standby mode.

When the supply voltage V_{CCA} and V_{CCD} are at 0 V and pin VREFDIG is HIGH, all I/Os, the audio outputs and the reference clock input are high-ohmic.

The power supplies can be switched on in any order.

6.17 Power-on reset

After start-up of V_{CCA} and V_{CCD}, a power-on-reset circuit will generate a reset pulse and the registers will be set to their default values as shown in Table 8. The power-on reset is effectively generated by V_{CCD}. To prevent any uncontrolled control interface response, before power is switched on, pin BUSEN must be LOW. The audio output pins are high-ohmic (hard mute), all other bits are set default according to Table 8.

6.18 Control interface

The I^2C-bus operates with a maximum clock frequency of 400 kHz.

6.19 Auto search and preset mode

6.19.1 Search mode

In Search mode the TEA5760UK can search channels automatically.

When the INTX signal is used as an interrupt to the host processor to indicate a search stop, the INTMSK register must be reset and only the FRRMSK must be set. In this way the host processor will only be interrupted when the search/preset algorithm is ready.

Search mode is initiated by setting the SM bit to logic 1 in the FRQSET register. When bit SUD = 0 then it searches down, when SUD = 1 it searches up. The tuner starts searching at the frequency where it is or at a new start frequency programmed to the tuner. In the case the programmed frequency is a valid channel and auto search is initiated, the radio will stay tuned to programmed frequency. To continue the auto search tune algorithm under such conditions, an offset frequency relative to the tuned frequency has to be programmed (for example 100 kHz) to search for subsequent channels. With the Search Stop Level (SSL) bits the minimum field strength of channels to be found can be set. The tuner will stop on a channel with a field strength equal to or higher than this reference level and then will check the IF frequency. When both are valid the Search mode terminates. If the level check or the IF count fails, it keeps on searching. When no channels are found the TEA5760UK stops searching when it has reached the band limit and the BLFLAG goes HIGH. A search always stops with the FRRFLAG being set and a hardware interrupt. Figure 3 describes this procedure.

After this interrupt the TEA5760UK will keep its status and will not update the INTREG, FRQCHK and TUNCHK tuner registers for a period of 15.625 ms. The state of the TEA5760UK can be checked by reading tuning registers INTREG, FRQCHK and TUNCHK. Table 4 shows the possible states after an auto search or a preset.

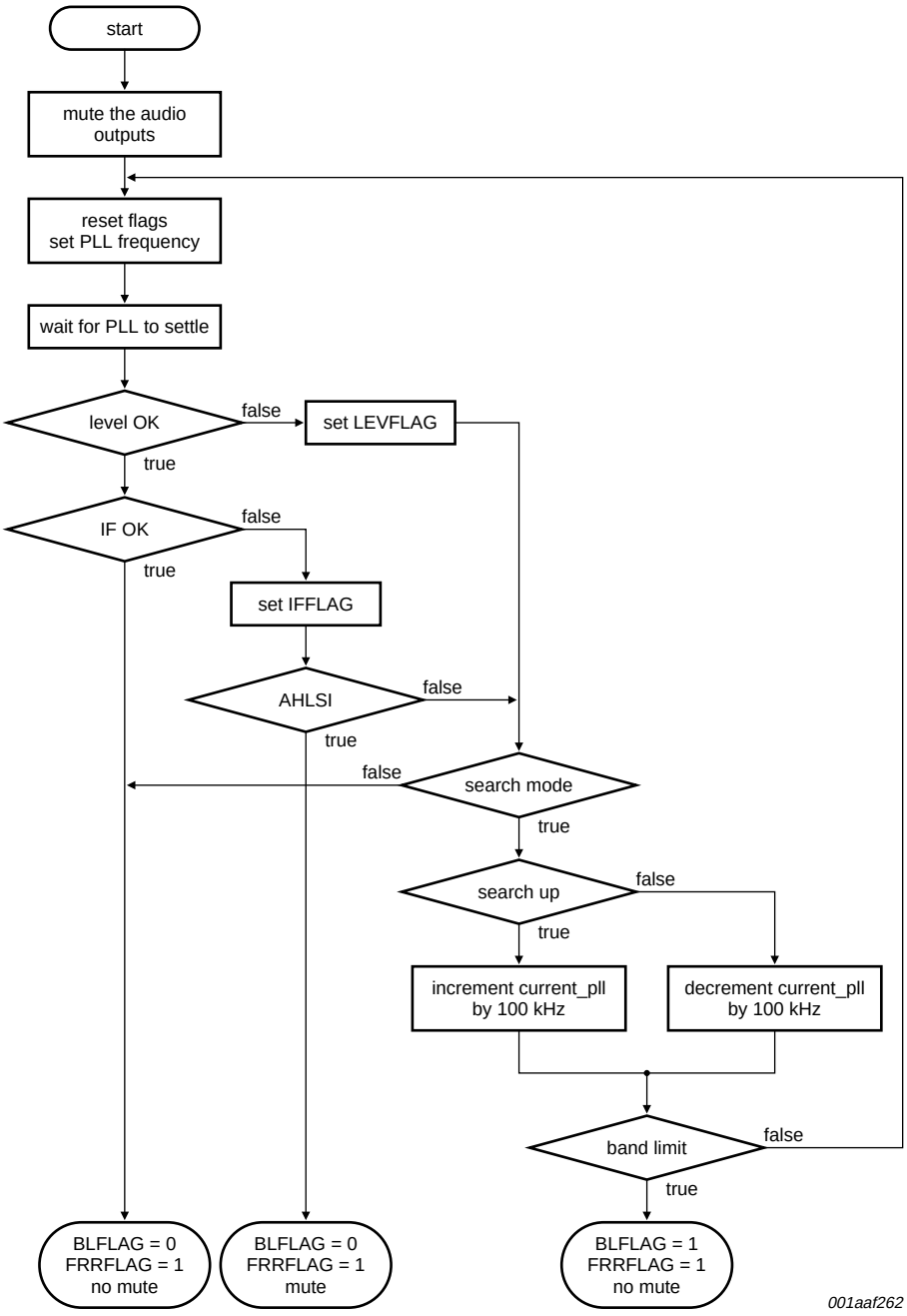


Fig 3. Flowchart auto search or preset (IF statement down = true)

6.19.2 Preset mode

A preset is done by setting bit SM to logic 0 and writing a frequency to register FRQSET. The tuner jumps to the selected frequency and sets the FRRFLAG when it is ready. After this interrupt the TEA5760UK will not update the tuner registers for a period of 15.625 ms. The state of the TEA5760UK can be checked by reading registers INTREG, FRQCHK and TUNCHK. Table 4 shows the possible states after an auto search or preset.

Table 4. Tuner truth table

Bit			Comment
IFFLAG	BLFLAG	FRRFLAG	
0	0	0	if INTX has gone low and IFMSK, LEVMSK, FRRMSK and BLMSK were set then this cannot occur
0	0	1	channel found during search, BLMSK and FRRMSK set
0	1	0	not a valid combination
0	1	1	no channel found and the band limit has been reached during a search, BLMSK and FRRMSK set
1	0	0	not possible during a preset or a search
1	0	1	A preset or search has been done, but the wanted channel has a valid RSSI level but fails the IF count. When AHLSI was set HLSI must be toggled and a new PLL value must be programmed.
1	1	0	not a valid combination
1	1	1	band limit is reached during search, no valid channel found

6.19.3 Auto high-side and low-side injection stop switch

The channel quality can sometimes be improved in case of image frequency interference. This can be achieved if the LO injection is positioned at the opposite side of the wanted channel (see Figure 4). Indication for image frequency interference can be derived from the IF frequency counter. To enable this feature bit AHLSI has to be set to logic 1.

The search/preset algorithm will stop and generate an interrupt event after detection of a valid RSSI level in combination with a frequency outside the IF frequency window. The host processor can detect this state by reading the interrupt register. Swap of the LO injection is achieved by inversion of bit HLSI in combination with a new tuning word for the changed oscillator frequency (see Section 6.5).

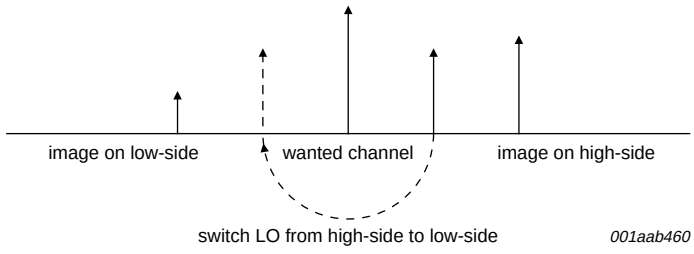


Fig 4. Switch from high-side injection of LO to low-side injection using the HLSI bit

6.19.4 Muting during search or preset

During a preset and search tuning the tuner is always muted, this is done by the algorithm itself. When bit AHLSI is set and the tuner stopped during a preset or a search because of a wrong IF count, the tuner stays muted and generates an interrupt event. In this way the host processor can switch the Hi-Lo setting quietly and wait for the new result.

All these mute actions are done by blocking the audio signal inside the soft mute attenuator, so the audio output will keep its DC level and stay low-ohmic i.e. 350 Ω (a hard mute with bit MU will cause a plop) (see Table 3).

7. Interrupt handling

7.1 Interrupt register

The first two bytes of the I²C-bus register contain the interrupt masks and the interrupt flags. A flag is set when it is 1.

Table 5. INTREG byte0R

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	IFFLAG	LEVFLAG	-	FRRFLAG	BLFLAG

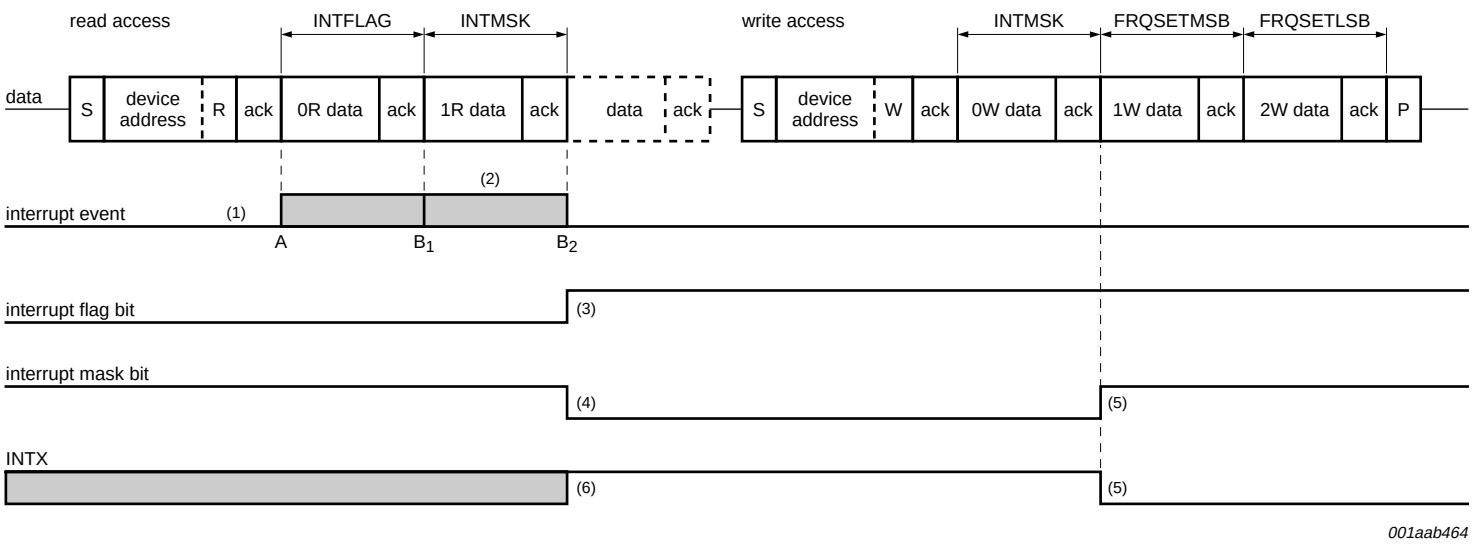
Table 6. INTREG byte0W

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	IFMSK	LEVMSK	-	FRRMSK	BLMSK

The interrupt flag register contains the flags set according to the behavior outlined in Section 7.1.4. When these are set they can also cause the INTX to go active [HardWare (HW) interrupt line] depending on the status of the corresponding mask bit in Table 6. A logic 1 in the mask register enables the HW interrupt for that flag.

Hence it is conceivable that, with all the mask bits cleared, the SoftWare (SW) could operate in a polling mode by continuous read operation of the interrupt flag register to look for bits being set.

Interrupt mask bits are always cleared after reading the interrupt register of the first two I²C-bus bytes. This is to control multiple HW interrupts (see Figure 5).



(1) Interrupt events that occur outside of the region A-B set their respective flag bits in the normal way immediately and can thus trigger a hardware interrupt if the mask bits are set.

(2) The blocking of interrupts is marked by the region A-B_1 / B_2 depending on the actual read cycle.

B_1 is when only the INTFLAG is read and a stop condition is received (only INTFLAG is read so only this will be cleared).

B_2 is when both registers are read and hence cleared and this is terminated by either an acknowledge or stop bit.

(3) Interrupt events that occur between A and B set their respective flags after the mask bits are cleared. Which means that in this diagram an interrupt event occurred in period A-B, so after A-B the flag goes to logic 1.

(4) All interrupt mask bits are cleared after the interrupt flag and mask bytes are read.

(5) Software writes to the mask byte and enables the required mask bits. Any flags currently set will then trigger a hardware interrupt.

(6) INTX is set HIGH (inactive) after the interrupt mask bytes are read.

Fig 5. I^2C-bus interrupt sequence, read and write operation

7.1.1 Interrupt clearing

The interrupt flag and mask bits are always cleared after:

- They have been read via the control interface
- A power-on reset

7.1.2 Timing

The timing sequence for the general operation interrupts is shown in Figure 5 shows a read access of the interrupt register INTREG and a subsequent (though not necessarily immediate) write to the mask register. It also indicates two key timing points A and B.

If an interrupt event occurs while the register is being read (after point A) it must be held until after the mask register is cleared at the end of the read operation (point B).

Point A is defined as: the R/W bit has been decoded. Point B is where the acknowledge has been received from the master after the first two bytes have been sent.

The low time for the INTX line (t_p) has a maximum value specified in Section 11. It can be shorter when a read action of the INTREG registers occurs within t_p.

7.1.3 Reset

A reset can be performed (at any time) by a simple read of the interrupt register (byte0R and byte1R), which automatically clears the interrupt flags and masks.

7.1.4 Interrupt flags and behavior

7.1.4.1 Multiple interrupt events

If the interrupt mask register bit is set then the setting of an interrupt flag for that bit causes a HW interrupt (INTX goes LOW). If the event occurs again, before the flag is cleared, then this does not trigger any further HW interrupts until that specific flag is cleared. However two different events can occur in sequence and generate a sequence of HW interrupts.

Only when read, followed by a write of the INTMSK byte has been done, can a second interrupt can be generated, as the first interrupt blocks the input of the INTX oneshot generator.

If subsequent interrupts occur within the INTX LOW period then these do not cause the INTX period to extend beyond its specified maximum period (see Section 7.2).

7.1.4.2 IF frequency: IFFLAG

During automatic frequency search or preset, the FM part of the TEA5760UK performs a check on the received IF frequency. If an incorrect IF frequency is received then this indicates the presence of strong interference or tuning to the image frequency. In case of preset tuning or search tuning with the AHLSI bit set the IFFLAG will be set and the algorithm will stop. When a search or preset is finished the FRRFLAG will be set and an interrupt is generated if the corresponding mask bit is set. The host processor can now read the outcome of the registers which will contain the IF count value and the IFFLAG status of the channel it is tuned to.

7.1.4.3 RSSI threshold: LEVFLAG

The level voltage reflects the field strength received by the antenna. The level voltage is analog-to-digital converted with 4 bits and output via the control interface. This 4-bit level value can be compared to a threshold level set by the SSL bits (see Table 14). The level ADC (which converts the analog value to digital) is triggered by a search or preset cycle.

During a tuning step, which can be a search or a preset it is triggered by these algorithms and compares the level with the threshold set by the SSL bits. The LEVFLAG bit is set if the RSSI level drops below the threshold level set by the SSL bits (see Table 14), the HW interrupt is only generated if the corresponding mask bit is set.

7.1.4.4 Frequency ready flag: FRRFLAG

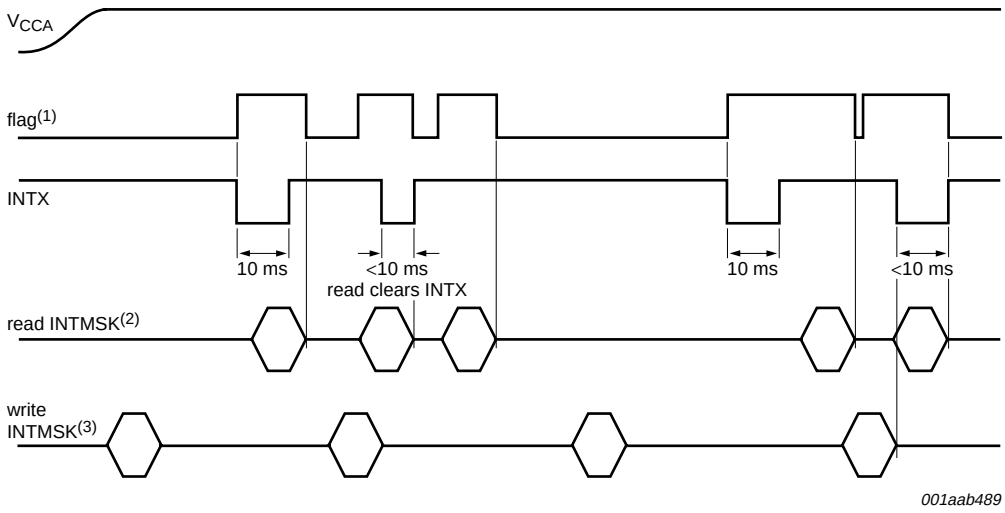
The frequency ready flag bit FRRFLAG is set to logic 1 when the automatic tuning has finished a search or preset. The description of this bit is given in Table 9. This bit is cleared by a read of the flag register.

7.1.4.5 Band limit: BLFLAG

The band limit bit BLFLAG is set to logic 1 when the automatic tuning has detected the end of the tuning band. This bit is described in Table 9. This bit is cleared by a read of the flag register.

7.2 Interrupt line

The interrupt line driver is a MOS transistor with a nominal sink current of 900 μA. It is pulled HIGH by an 18 kΩ resistor connected to pin VREFDIG. The interrupt line can be connected to one other similar device with an interrupt output and an 18 kΩ pull-up resistor, providing a wired-OR function. This allows any of the drivers to pull the interrupt line LOW by sinking the current (see Section 11). When a flag is set and not masked it generates an interrupt.



(1) When Flag is set next interrupts are blocked until Read/Write INTMSK.

(2) Read INTMSK clears Flag, INTMSK and INTX.

(3) Write INTMSK enables INTX.

Fig 6. Interrupt line behavior

8. I²C-bus interface

The I²C-bus interface is based on *The I²C-bus specification*, version 2.1 January 2000, expanded by the following definitions.

8.1 Write and read mode

S	BYTE 1		A	BYTE 2	A	BYTE n	A	BYTE 8	NAK	P
	chip address	R/$\overline{W}$		byte0W		.....		byte6W		
	0010 0000	0		xxxx xxxx		xxxx xxxx		xxxx xxxx		

001aac341

Fig 7. Write mode

S	BYTE 1		A	BYTE 2	A	BYTE n	A	BYTE 17	A	P
	chip address	R/W		byte0R		.....		byte15R		
	0010 0000	1		xxxx xxxx		xxxx xxxx		xxxx xxxx		

001aac342

Fig 8. Read mode

Table 7. I²C-bus transfer description

Code	Description
S	START condition
Byte 1	I²C-bus chip address (7 bits)
	R/$\overline{W}$ = 0 for write action and R/$\overline{W}$ = 1 for read action
A	acknowledge (SDA = LOW)
Byte 2, etc.	data byte (8 bits)
NAK	non acknowledge (SDA = HIGH)
P	STOP condition

8.2 Data transfer

Structure of the I²C-bus:

- Slave transceiver
- Subaddresses not used

Remark: The I²C-bus operates at a maximum clock rate of 400 kHz. It is not allowed to connect the TEA5760UK to an I²C-bus operating at a higher clock rate.

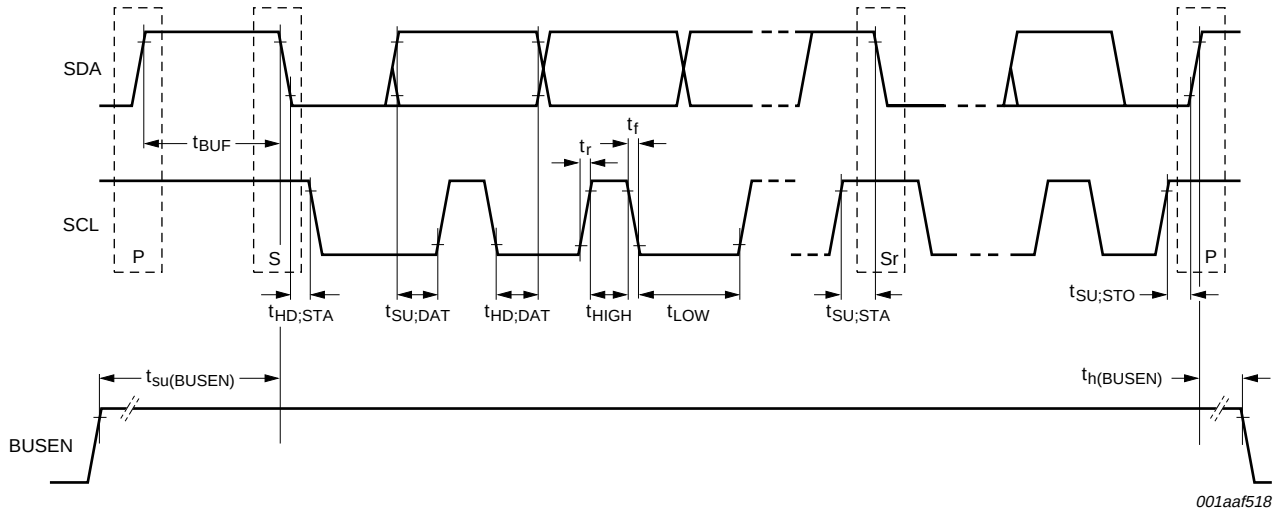
Data transfer to the TEA5760UK:

- Bit 7 of each byte is considered the MSB and has to be transferred as the first bit of the byte.
- The LSB indicates the write or read action.

- The data becomes valid byte-wise at the appropriate falling edge of the SCL clock.
- A STOP condition after any byte can shorten transmission times. When writing to the receiver by using the STOP condition before completion of the whole transfer:
  - The remaining bytes will contain the old information.
  - If the transfer of a byte is not completed the new bits will be used, but a new tuning cycle will not be started.

I²C-bus activity:

- With bit PUPD the TEA5760UK can be switched in a low current Standby mode. The I²C-bus is then still active.
- When the I²C-bus interface is de activated, by making pin BUSENABLE LOW and without programmed Standby mode, the TEA5760UK keeps its normal operation, but is isolated from the I²C-bus lines.
- Bus traffic can be started 10 µs after activating the bus again by making pin BUSENABLE HIGH.



t_f = fall time of both SDA and SCL signals: $20 + 0.1\ C_b < t_f < 300$ ns, where C_b = total capacitance on bus line in pF.

t_r = rise time of both SDA and SCL signals: $20 + 0.1\ C_b < t_r < 300$ ns, where C_b = total capacitance on bus line in pF.

$t_{HD;STA}$ = hold time (repeated) START condition. After this period, the first clock pulse is generated: > 600 ns.

t_{HIGH} = HIGH period of the SCL clock: > 600 ns.

$t_{SU;STA}$ = set-up time for a repeated START condition: > 600 ns.

$t_{HD;DAT}$ = data hold time: $300 < t_{HD;DAT} < 900$ ns.

Remark: 300 ns lower limit is added because the ASIC has no internal hold time for the SDA signal.

$t_{SU;DAT}$ = data set-up time: $t_{SU;DAT} > 100$ ns. If ASIC is used in a standard mode I²C-bus system, $t_{SU;DAT} > 250$ ns.

$t_{SU;STO}$ = set-up time for STOP condition: > 600 ns.

t_{BUF} = bus free time between a STOP and a START condition: > 600 ns.

C_b = capacitive load of one bus line: < 400 pF.

$t_{su(BUSEN)}$ = set-up time on pin BUSEN: $t_{su(BUSEN)} > 10$ µs.

$t_{h(BUSEN)}$ = hold time on pin BUSEN: $t_{h(BUSEN)} > 10$ µs.

Fig 9. Bus timing diagram

8.3 Register map

Table 8. Register overview

Register name	I²C-bus byte number		Access	Reset value	Reference
	Read	Write			
INTREG	0R		R	00h	Table 9
	1R	0W	R/W	00h	Table 10
FRQSET	2R	1W	R/W	80h	Table 11
	3R	2W	R/W	00h	Table 12
TNCTRL	4R	3W	R/W	08h	Table 13
	5R	4W	R/W	D2h	Table 14
FRQCHK	6R		R	-	Table 15
	7R		R	-	Table 16
TUNCHK	8R		R	-	Table 17
	9R		R	-	Table 18
TESTREG	10R	5W	R/W	00h	Table 19
	11R	6W	R/W	00h	Table 20
MANID	12R		R	20h	Table 22
	13R		R	2Bh	Table 23
CHIPID	14R		R	57h	Table 24
	15R		R	60h	Table 25

8.4 Register description

8.4.1 Register INTREG

Table 9. Register INTREG - byte0R

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 5	-	-	-	not used
4	IFFLAG	R	0*	IF count is correct
			1	IF count is not correct
3	LEVFLAG	R	0*	RSSI level is above VSSL[1:0]
			1	RSSI level has dropped below VSSL[1:0]
2	-	-	-	not used
1	FRRFLAG	R	0*	tuner state machine is not ready
			1	tuner state machine is ready
0	BLFLAG	R	0*	during a search the band limit has not been reached or no time-out
			1	during a search the band limit has been reached or time-out

Table 10. Register INTREG - byte1R/byte0W description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 5	-	-	-	not used
4	IFMSK	R/W	0*	does not mask bit IFFLAG
			1	masks bit IFFLAG
3	LEVMSK	R/W	0*	does not mask bit LEVFLAG
			1	masks bit LEVFLAG
2	-	-	-	restricted for RDS usage
1	FRRMSK	R/W	0*	does not mask bit FRRFLAG
			1	masks bit FRRFLAG
0	BLMSK	R/W	0*	does not mask bit BLFLAG
			1	masks bit BLFLAG

8.4.2 Register FRQSET

Table 11. Register FRQSET - byte2R/byte1W description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7	SUD	R/W	0	search down
			1*	search up
6	SM	R/W	0*	Preset mode
			1	Search mode
5 to 0	FR_[13:08]	R/W	00 0000*	frequency set; FR_13 is MSB

Table 12. Register FRQSET - byte3R/byte2W description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	FR_[07:00]	R/W	00*h	frequency set; FR_00 is LSB

8.4.3 Register TNCTRL

Table 13. Register TNCTRL - byte4R/byte3W

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7	-	R/W	-	not used
6	PUPD	R/W		power-up power-down MSB
			0*	FM off
			1	FM on
5	BLIM	R/W	0*	US/Europe FM band 87.5 MHz to 108 MHz
			1	Japan FM band 76 MHz to 90 MHz
4	SWPM	R/W	0*	software port is output of bit SWP
			1	software port is output of bit FRRFLAG
3	IFCTC	R/W	0	IF count time = 1.953 ms
			1*	IF count time = 15.625 ms

Table 13. Register TNCTRL - byte4R/byte3W *…continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
2	AFM	R/W	0*	audio not muted
			1	left and right audio muted
1	SMUTE	R/W	0*	soft mute off
			1	soft mute on
0	SNC	R/W	0*	stereo noise cancellation off
			1	stereo noise cancellation on

Table 14. Register TNCTRL - byte5R/byte4W description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7	MU	R/W	1	1 = L- and R- audio hard muted; 0 = no hard mute
6 and 5	SSL_[1:0]	R/W		search stop level
			00	ADC3
			01	ADC5
			10*	ADC7
			11	ADC10
4	HLSI	R/W	0	low-side injection
			1*	high-side injection
3	MST	R/W	0*	stereo on
			1	forced mono
2	SWP	R/W	0*	SWPORT = LOW
			1	SWPORT = HIGH
1	DTC	R/W	0	de-emphasis time constant = 75 µs
			1*	de-emphasis time constant = 50 µs
0	AHLSI	R/W	0*	tuner will search continuously
			1	tuner will stop during search on failed IF count and correct level

8.4.4 Register FRQCHK

Table 15. Register FRQCHK - byte6R description

Bit	Symbol	Access	Value	Description
7 and 6	-	-	-	not used
5 to 0	PLL_[13:08]	R	-	frequency found; PLL_13 is MSB

Table 16. Register FRQCHK - byte7R description

Bit	Symbol	Access	Value	Description
7 to 0	PLL_[07:00]	R	-	frequency found; PLL_00 is LSB

8.4.5 Register TUNCHK

Table 17. Register TUNCHK - byte8R description

Bit	Symbol	Access	Value	Description
7 to 1	IF_[6:0]	R	-	IF count; IF_6 is MSB, IF_0 is LSB
0	TUNTO	R	0	PLL has settled
			1	PLL tuning time-out

Table 18. Register TUNCHK - byte9R description

Bit	Symbol	Access	Value	Description
7 to 4	LEV_[3:0]	R	-	level count; LEV_3 is MSB, LEV_0 is LSB
3	LD	R	0	PLL is not locked
			1	PLL is locked
2	STEREO	R	0	mono
			1	stereo
1 and 0	-	-	-	not used

8.4.6 Register TESTREG

Table 19. Register TESTREG - byte10R/byte5W description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7	LHM	R/W	0*	left audio output is not muted
			1	left audio output is hard muted
6	RHM	R/W	0*	right audio output is not muted
			1	right audio output is hard muted
5 to 3	-	R/W	-	not used
2	TUN	R/W	0	no tuning programming error
			1	tuning programming error
1	RFAGC	R/W	0*	RFAGC on
			1	RFAGC off
0	INTCTRL	R/W	0*	no interrupt generated on INTX
			1	when INTCTRL is set to 1 and TM = 1; generates an interrupt on INTX

Table 20. Register TESTREG - byte11R/byte6W description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 and 6	-	R/W	-	not used
5	SNCLEV	R/W	1*	starting point mono/stereo blending, this is a write only bit
			0	30 µV (EMF value)
			1*	15 µV (EMF value)

Table 20. Register TESTREG - byte11R/byte6W description *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
4	TM	R/W	0*	normal operation
			1	TEA5760UK in Test mode and software port outputs according to Table 21
3 to 0	TB_[3:0]	R/W	0*h	test bits, Table 21 describes selection of output signals available at the SWPORT

Table 21. SWPORT

Bit					Output signal	Output pin
TM	TB_3	TB_2	TB_1	TB_0		
0/1	0	0	0	0	bit SWP of byte4W (SWPM = 0) or FRRFLAG (SWPM = 1)	SWPORT
1	0	0	0	1	oscillator output 32.768 kHz	SWPORT
1	0	0	1	0	lock detect bit LD	SWPORT
1	0	0	1	1	stereo bit STEREO	SWPORT
1	0	1	0	0	programmable divider	SWPORT
1	0	1	0	1	programmable divider	INTX

8.4.7 Register MANID

Table 22. Register MANID - byte12R description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 4	VERSION[3:0]	R	0010*	version code
3 to 0	MAN_ID[10:07}	R	0000*	manufacturer ID code

Table 23. Register MANID - byte13R description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 1	MAN_ID[06:00]	R	000 0101*	manufacturer ID code
0	IDAV	R	0	chip has no manufacturer ID
			1*	chip has manufacturer ID (available in IIC mode)

8.4.8 Register CHIPID

Table 24. Register CHIPID - byte14R description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	CHIP_ID[15:08]	R	57*h	TEA5760UK chip identification code

Table 25. Register CHIPID - byte15R description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	CHIP ID[07:00]	R	60*h	TEA5760UK chip identification code

9. Limiting values

Table 26. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
The quality requirements are derived from the GQS - General Quality Specification.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{LO1}	voltage on pin LO1			–0.6	+3.6	V
V_{LO2}	voltage on pin LO2			–0.6	+3.6	V
V_{CCD}	digital supply voltage			–0.6	+3.6	V
V_{CCA}	analog supply voltage			–0.6	+3.6	V
V_I	input voltage	with respect to ground		–0.6	+3.6	V
V_O	output voltage	with respect to ground		–0.6	+3.6	V
T_{stg}	storage temperature			–40	+125	°C
T_{amb}	ambient temperature	TEA5760UK functional, specification not guaranteed		–35	+85	°C
V_{esd}	electrostatic discharge voltage	MM	[1]	–200	+200	V
		HBM	[2]			
		all pins, except pin FREQIN		–2000	+2000	V
		pin FREQIN		–1750	+1750	V
		CDM	[3]	–500	+500	V

[1] MM: Machine Model; R = 0 Ω and C = 200 pF.

[2] HBM: Human Body Model; R = 1.5 kΩ and C = 100 pF.

[3] CDM: Charged Device Model; JEDEC Standard JESD22-C101.

10. Recommended operating conditions

Table 27. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reference clock 32.768 kHz						
f	frequency	T_{amb} = 25 °C	-	32.768	-	kHz
Δf/f	relative frequency difference	T_{amb} = 25 °C	-20×10^{-6}	-	$+20 \times 10^{-6}$	
		T_{amb} = –20 °C to +85 °C	-150×10^{-6}	-	$+150 \times 10^{-6}$	
δ	duty cycle	square wave	30	-	70	%
t_r	rise time		-	-	50	ns
t_f	fall time		-	-	50	ns
V_{IH}	HIGH-level input voltage	square wave	1.0	-	V_{CCD}	V
V_{IL}	LOW-level input voltage	square wave	0	-	0.7	V

11. Characteristics

The IEC filter as mentioned in the characteristics is defined in IEC60315-4. The audio bandwidth of this filter is between 200 Hz and 15 kHz.

The characteristics are valid under restriction of the reference clock as specified in Section 10.

Table 28. General characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	analog supply voltage		2.6	2.7	3.6	V
$V_{CC(VCO)}$	VCO supply voltage		2.6	2.7	3.6	V
V_{CCD}	digital supply voltage		2.6	2.7	3.6	V
I_{CCA}	analog supply current	operational	-	8.7	10	mA
		Standby mode	-	1	3	µA
$I_{CC(VCO)}$	VCO supply current	operational	-	5	7	mA
		Standby mode	-	0.8	2	µA
I_{CCD}	digital supply current	operational	-	350	450	µA
		Standby mode	-	5	10	µA
		Sleep mode; BUSEN = HIGH	-	16	25	µA
$V_{VREFDIG}$	voltage on pin VREFDIG	$V_{VREFDIG} \leq V_{CCD}$	1.65	1.8	3.6	V
$I_{VREFDIG}$	current on pin VREFDIG	operational	-	1	10	µA
		Standby mode	-	1	1	µA
$f_{i(FM)}$	FM input frequency		76	-	108	MHz
T_{amb}	ambient temperature	[1]	–20	-	+85	°C
		[2]				

[1] Fulfill specifications.

[2] Functional, indication required for reduced performance.

Table 29. Characteristics

All AC values are given in RMS unless otherwise specified. The minimum and maximum values include spread due to: voltage between 2.6 V and 3.6 V; T_{amb} = –20 °C to +85 °C; reference frequency offset plus deviation and process spread. $V_{VREFDIG}$ = 1.65 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Antenna input including matching circuit						
Z_i	input impedance	f_{RF} = 76 MHz to 108 MHz	-	50	-	Ω
$\|s_{11}\|^2$	input return loss	f_{RF} = 76 MHz to 108 MHz	–5	-	-	dB
Voltage controlled oscillator						
f_{VCO}	VCO frequency		150	-	217	MHz
Reference frequency input: pin FREQIN						
V_{FREQIN}	voltage on pin FREQIN	switching level	0.7	0.925	1.0	V
R_i	input resistance		500	-	-	kΩ
C_i	input capacitance		-	-	7	pF

Table 29. Characteristics *...continued*

All AC values are given in RMS unless otherwise specified. The minimum and maximum values include spread due to: voltage between 2.6 V and 3.6 V; T_{amb} = −20 °C to +85 °C; reference frequency offset plus deviation and process spread. $V_{VREFDIG}$ = 1.65 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Synthesizer						
Programmable divider						
t_s	settling time	single frequency jump in any direction to a frequency within the frequency band (87.5 MHz to 108 MHz or 76 MHz to 90 MHz); settling limit is ±5 kHz of target frequency	-	-	40	ms
D_{prog}	programmable divider	maximum; FRQSET[15:8] = XX01 1111; FRQSET[7:0] = 1111 1111	-	-	8191	
		minimum; FRQSET[15:8] = XX00 1000; FRQSET[7:0] = 0000 0000	2048	-	-	
$D_{prog(step)}$	programmable divider step		-	1	-	
f_{step}	step frequency	synthesizer auto search frequency	-	100	-	kHz
IF counter						
N_{IFc}	IF counter length		-	7	-	bit
V_{sens}	sensitivity voltage		-	-	3[1]	µV
$N_{IFc(result)}$	IF counter result	for search stop; stop level 3 V < V_{RF}[1] < 2 V	31	-	3C	hex
			49	-	60	dec
T	period	IFCTC = 1	-	15625	-	µs
		IFCTC = 0	-	1953	-	µs
$N_{IFc(res)}$	IF counter resolution		-	4096	-	Hz
Logic pins: pins BUSEN, CLOCK and DATA						
R_I	input resistance		10	-	-	MΩ
V_{IH}	HIGH-level input voltage		0.7 × $V_{VREFDIG}$	-	$V_{VREFDIG}$ + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	0.3 × $V_{VREFDIG}$	V
Software multi functional port pin: SWPORT						
$V_{O(max)}$	maximum output voltage	I_{load} = 150 µA	$V_{VREFDIG}$ − 0.25		$V_{VREFDIG}$	V
$V_{O(min)}$	minimum output voltage	I_{load} = 150 µA	0	0.2	0.45	V
I_{sink}	sink current	V_{SWPORT} = 1.8 V	500	-	-	µA
I_{source}	source current	V_{SWPORT} = 0 V	500	-	-	µA
Pin INTX						
$V_{O(max)}$	maximum output voltage		$V_{VREFDIG}$ − 0.2	-	$V_{VREFDIG}$ + 0.2	V
$V_{O(min)}$	minimum output voltage	1.65 V ≤ $V_{VREFDIG}$; pull-up resistor of second device connected to INTX 18 kΩ ± 20 %	0	-	0.22 × $V_{VREFDIG}$	V

Table 29. Characteristics *...continued*

All AC values are given in RMS unless otherwise specified. The minimum and maximum values include spread due to: voltage between 2.6 V and 3.6 V; T_{amb} = −20 °C to +85 °C; reference frequency offset plus deviation and process spread. $V_{VREFDIG}$ = 1.65 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{sink}	sink current	including internal $R_{pu(int)}$	600	900	1100	µA
$R_{pu(int)}$	internal pull-up resistance		14.4	18	24	kΩ
t_p	pulse duration		9	-	10	ms
FM signal channel						
FM RF input						
V_{sens}	sensitivity voltage	f_{RF} = 76 MHz to 108 MHz; Δf = 22.5 kHz; f_{mod} = 1 kHz; S+N/N = 26 dB; τ_{deemp} = 50 µs; L = R; IEC filter + A-weighting filter	-	2[1]	3.0[1]	µV
S/N	signal-to-noise ratio	f_{RF} = 76 MHz to 108 MHz; Δf = 22.5 kHz; f_{mod} = 1 kHz; L = R; τ_{deemp} = 50 µs; V_{RF} = 10 µV (EMF value); IEC filter + A-weighting filter	45		-	dBa
$IP3_{ib}$	in-band third-order intercept point	Δf1 = 200 kHz; Δf2 = 400 kHz; f_{RF} = 76 MHz to 108 MHz; RF AGC is off	82[1]	95[1]	-	dBµV
$IP3_{ob}$	out-band third-order intercept point	Δf1 = 4 MHz; Δf2 = 8 MHz; f_{RF} = 76 MHz to 108 MHz; RF AGC is off	88[1]	100[1]	-	dBµV
IF filter						
f_c	center frequency		220	225	230	kHz
S_{200}	200 kHz selectivity	Δf = ±200 kHz; f_{RF} = 76 MHz to 108 MHz;measured according to EN55020; τ_{deemp} = 50 µs	16	-	-	dB
S_{FM}	FM selectivity	Δf_{min} = 300 kHz; f_{RF} = 76 MHz to 108 MHz; except image frequency band measured according to EN55020; τ_{deemp} = 50 µs	35	-	-	dB
$\alpha_{f(image)}$	image frequency rejection	Δf = 450 kHz; measured according to EN55020; image rejection defined as difference between image and co-channel response; τ_{deemp} = 50 µs	25	-	-	dB
FM IF level detector and mute voltage; see Figure 10						
ΔG	gain deviation	deviation from average curve	−2		+2	dB
$V_{ADC(start)}$	start ADC voltage	extrapolated	0.75[1]	1.6[1]	2.5[1]	µV
$G_{ADC(step)}$	step of ADC gain	average	2.5	2.8	3	dB
Soft mute						
$V_{mute(start)}$	start mute voltage	SMUTE = 1	3[1]	3.8[1]	5[1]	µV
α_{mute}	mute attenuation	V_{RF} = 1.26 µV[1], L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; τ_{deemp} = 75 µs; IEC filter; SMUTE = 1	5	5.8	8	dB

Table 29. Characteristics *...continued*

All AC values are given in RMS unless otherwise specified. The minimum and maximum values include spread due to: voltage between 2.6 V and 3.6 V; T_{amb} = −20 °C to +85 °C; reference frequency offset plus deviation and process spread. $V_{VREFDIG}$ = 1.65 V to 3.6 V.

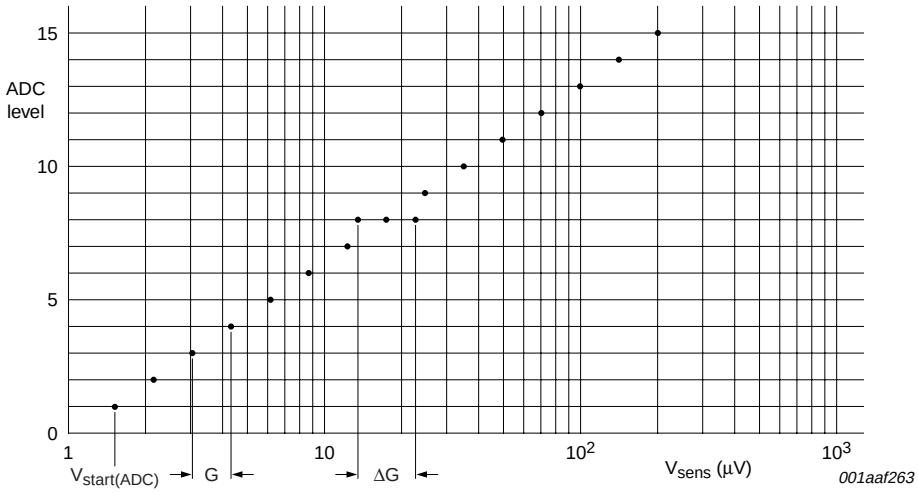
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Stereo decoder; pins VAFL and VAFR						
V_O	output voltage	V_{RF} = 2 mV[1]; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; τ_{deemp} = 75 µs	60	75	90	mV
R_O	output resistance	MU = LHM = RHM = 0; AFM = 0 or AFM = 1	250	350	400	Ω
		hard mute; MU = LHM = RHM = 1; AFM = 0 or AFM = 1	500	-	-	kΩ
		Standby mode; PUPD = 0	1	-	-	MΩ
I_O	output current	minimum load resistance = 10 kΩ	80	100	120	µA
$\lvert\Delta G_V\rvert$	voltage gain difference	V_{RF} = 2 mV[1]; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; IEC filter; τ_{deemp} = 75 µs	−0.5	-	+0.5	dB
$\alpha_{cs(stereo)}$	stereo channel separation	V_{RF} = 2 mV[1]; Δf = 75 kHz including 9 % pilot; R = 0 and L = 1 or R = 1 and L = 0; f_{mod} = 1 kHz; IEC filter; MST = 0; SNC = 1				
		SNCLEV = 1 or SNC = 0	30	40	-	dB
		SNCLEV = 0	27	36	-	dB
$f_{-3dB(l)}$	low frequency −3 dB point	audio band; V_{RF} = 2 mV[1]; Δf = 22.5 kHz, L = R, pre-emphasis = 75 µs; τ_{deemp} = 75 µs	-	-	20	Hz
$f_{-3dB(h)}$	high frequency −3 dB point	audio band; V_{RF} = 2 mV[1]; Δf = 22.5 kHz, L = R, pre-emphasis = 75 µs; τ_{deemp} = 75 µs	15	-	-	kHz
(S+N)/N	signal plus noise-to-noise ratio	V_{RF} = 2 mV[1]; Δf = 22.5 kHz; L = R; f_{mod} = 1 kHz; τ_{deemp} = 50 µs; IEC filter + A-weighting filter				
		mono	53	57	-	dBA
		stereo; Δf_{pilot} = 6.75 kHz	49	53	-	dBA
$\alpha_{resp(sp)}$	spurious response	relative to Δf = 22.5 kHz; fm = 1 kHz (mono); V_{RF} = 2 mV[1]; τ_{deemp} = 50 µs; IEC filter + A-weighting filter	-	-	−60	dBA
THD	total harmonic distortion	mono; V_{RF} = 2 mV[1]; L = R; τ_{deemp} = 75 µs				
		Δf = 75 kHz; f_{mod} = 400 Hz	-	0.4	0.8	%
		Δf = 75 kHz; f_{mod} = 1 kHz	-	0.4	0.8	%
		Δf = 75 kHz; f_{mod} = 3 kHz	-	0.4	0.8	%
		Δf = 100 kHz; f_{mod} = 1 kHz	-	0.5	1	%
		stereo; V_{RF} = 2 mV[1]; Δf = 75 kHz; L = R including 9 % pilot; τ_{deemp} = 75 µs				
		f_{mod} = 1 kHz	-	0.5	1.5	%
		f_{mod} = 3 kHz	-	0.5	1.5	%

Table 29. Characteristics *...continued*

All AC values are given in RMS unless otherwise specified. The minimum and maximum values include spread due to: voltage between 2.6 V and 3.6 V; T_{amb} = −20 °C to +85 °C; reference frequency offset plus deviation and process spread. $V_{VREFDIG}$ = 1.65 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
α_{AM}	AM suppression	L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; m = 0.3; τ_{deemp} = 75 µs, IEC filter					
		V_{RF} = 20 µV	[1]	40	-	-	dB
		V_{RF} = 200 µV to 20 mV	[1]	45	-	-	dB
α_{pilot}	pilot suppression	related to Δf = 75 kHz; including 9 % pilot; L = 0 and R = 1 or L = 1 and R = 0; f_{mod} = 1 kHz; τ_{deemp} = 75 µs		40	50	-	dB
Δf_{pilot}	pilot frequency deviation	stereo; required for pilot detection; V_{RF} = 2 mV	[1]	1.8	3.6	5.8	kHz
$\alpha_{hys(pilot)}$	pilot hysteresis	switch of pilot; V_{RF} = 2 mV	[1]	2	2.5	5	dB
τ_{deemp}	de-emphasis time constant	DTC = 1		40	50	60	µs
		DTC = 0		60	75	90	µs
Mono/stereo blend							
$V_{start(blend)}$	blend start voltage	stereo channel separation = 1 dB; SNC = 1					
		SNCLEV = 0		20[1]	30[1]	40[1]	µV
		SNCLEV = 1		10[1]	15[1]	20[1]	µV
$\alpha_{cs(stereo)}$	stereo channel separation	V_{RF} = 80 µV (EMF value); Δf = 75 kHz; R = 0 + L = 1 or R = 1 + L = 0; including 9 % pilot; f_{mod} = 1 kHz; MST = 0; SNC = 1 + SNCLEV = 1 or SNC = 0		4	10	16	dB
Mono/stereo switching							
V_{sw}	switch voltage	Δf = 75 kHz, including 9 % pilot; f_{mod} = 1 kHz; SNC = 0		60[1]	80[1]	110[1]	µV
$\lvert\Delta V_{sw}/V_{sw}\rvert$	switch voltage deviation over switch voltage ratio	Δf = 75 kHz, including 9 % pilot; f_{mod} = 1 kHz; SNC = 0		2	3	4	dB
Bus driven mute functions							
Tuning mute							
α_{mute}	mute attenuation	Δf = 75 kHz; mono, IEC filter					
		AFM = 1 or RHM = 1		-	-	−60	dB
		AFM = 1 or LHM = 1		-	-	−60	dB
		MU = 1		-	-	−80	dB

[1] EMF value.



$V_{ADC(start)}$ is the starting point of the curve. Taking the starting point the curve shows a monotone increase, increasing with the average step size $G_{ADC(step)}$. The maximum deviation from the average curve is ΔG

Fig 10. FM IF level detector and mute voltage

12. Application information

Table 30. List of components

Symbol	Value	Type
L1	120 nH	Murata LQW15ANR12J00 or equivalent, minimum Q = 20 (f = 100 MHz), tolerance = ±5 %
L2	47 nH	Murata LQW15AN47NJ00 or equivalent, minimum Q = 25 (f = 250 MHz), tolerance = ±5 %
R	10 kΩ, 100 kΩ	tolerance = ±10 % (max).
C	27 pF, 47 pF, 100 pF, 10 nF, 100 nF (2 ×)	tolerance = ±10 % (max).

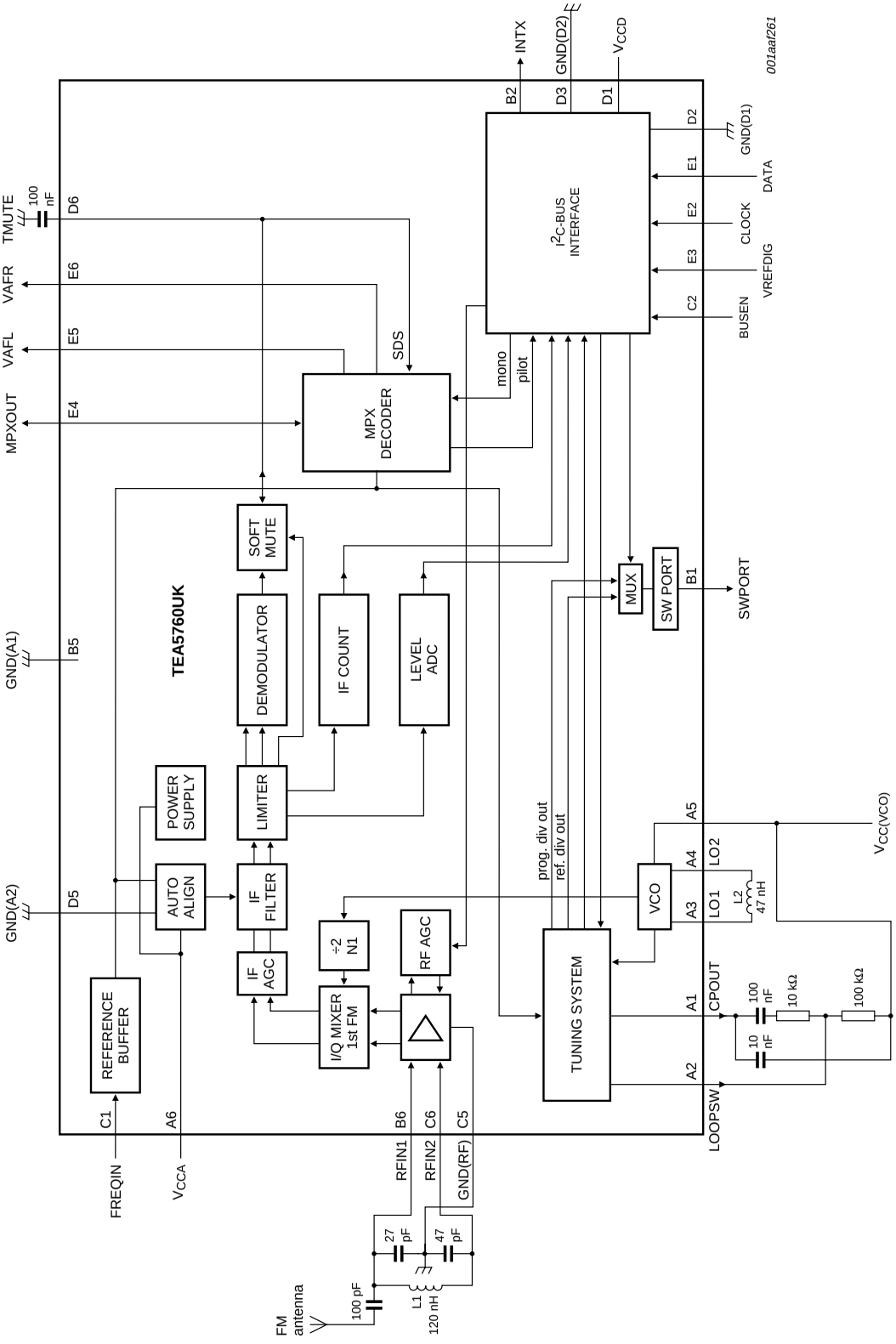
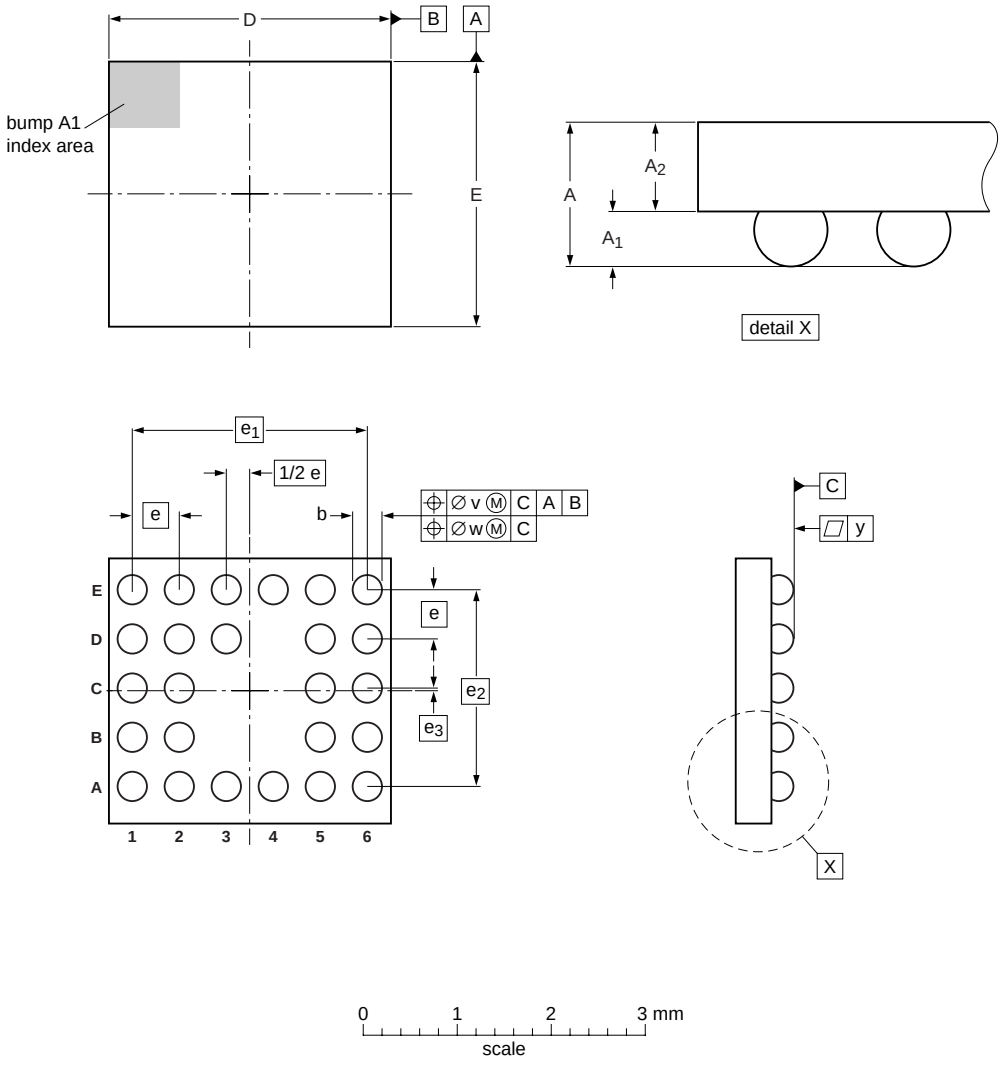


Fig 11. Application diagram

13. Package outline

WLCSP25: wafer level chip-size package; 25 bumps; 3 x 2.8 x 0.6 mm **TEA5760UK**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	e_3	v	w	y
mm	0.64	0.26 0.22	0.38 0.34	0.34 0.30	3.1 3.0	2.9 2.8	0.5	2.5	2	0.028	0.01	0.04	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
TEA5760UK						~~05-12-09~~ 06-07-06

Fig 12. Package outline TEA5760UK (WLCSP25)

14. Soldering

14.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in Application Note *AN10439 "Wafer Level Chip Scale Package"* and in *Application Note AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

14.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

14.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 31 and 32

Table 31. SnPb eutectic process (from J-STD-020C)

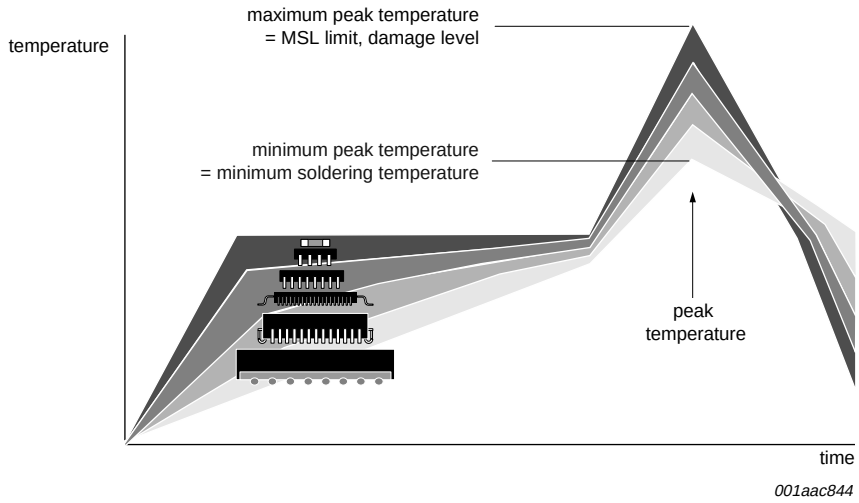
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 32. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.



MSL: Moisture Sensitivity Level

Fig 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

14.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

14.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in *Application Note AN10365 "Surface mount reflow soldering description"*.

14.3.4 Cleaning

Cleaning can be done after reflow soldering.

15. Revision history

Table 33. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA5760UK_1	20061214	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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