

# TOSHIBA CMOS GATE ARRAY

## FEATURES

The Toshiba CMOS Gate Array families are developed by the master slice method on the foundation of Toshiba's famous and proprietary HC<sup>2</sup>MOS and VLSI technologies.

The product lines are impressive. There are 6 types of base array, with gate complexity of 880 to 6K, in the TC15G series. The TC17G series comprises 9 types of base array, with gate complexity between 540 and 10K. The TC19G series, 5 base arrays of 3200 to 10K.

The great variety of I/O pads provided assures an extensive range of possible applications. For instance, for the smallest base array (540 gates), there are 52; and

for the largest base array (10K gates), there are 232.

These internal gates and I/O pads are wired in accordance with the logic design decided by the individual. These are what give these gate arrays their power and performance.

The LSI design is fully supported by famous LDS-II™, LDS-III™ and Toshiba CAD system. It is capable of executing design verification, logic simulation and auto place and route, having sub-systems for generating mask tapes and test tapes and for performing path analysis. Thus, a customer can develop an ASIC in a short time at a relatively low cost.

LDS-II, LDS-III are trademarks of LSI Logic Corp.

### Basic Characteristics

Product line-up	*TC15G series	*TC17G series	TC19G series
Process-technology	3μm	2μm	1.5μm
	HC <sup>2</sup> MOS Si-gate double layer metal		
Maximum toggle frequency	50MHz	100MHz	120MHz
Gate speed (inner gate, typ.)	2.5ns	1.5ns	1.0ns
Supply voltage	5V		
Application	LSTTL/ALSTTL	STTL	ASTTL

\* : TC15G/17G series are alternately-sourced by LSI Logic Corp.

### Product Lines

	Part Number	Gate Complexity	Maximum Pads <sup>1)</sup>		Maximum I/O Pads <sup>1)</sup>	
			Standard pitch	Fine pitch	Standard pitch	Fine pitch
TC15G series <sup>2)</sup>	TC15G008	880	74	/	70	/
	TC15G014	1,400	92		88	
	TC15G022	2,200	114		110	
	TC15G032	3,200	138		134	
	TC15G042	4,200	156		152	
	TC15G060	6,000	180		176	
TC17G series <sup>2)</sup>	TC17G005	540	47 <sup>3)</sup>	55 <sup>3)</sup>	44	52
	TC17G008	880	52	71 <sup>3)</sup>	46	68
	TC17G014	1,400	68	89 <sup>3)</sup>	62	86
	TC17G022	2,200	82	109 <sup>3)</sup>	76	106
	TC17G032	3,200	98	128	92	122
	TC17G042	4,200	118	150	112	144
	TC17G060	6,000	146	186	140	180
	TC17G080	8,000	174	222	168	216
TC19G series	TC19G100	10,000	180	232	174	226
	TC19G032	3,200	98	128	92	122
	TC19G042	4,200	118	150	112	144
	TC19G060	6,000	146	186	140	180
	TC19G080	8,000	174	222	168	216
TC19G100	10,000	180	232	174	226	

Notes: 1. Additional I/O pads may be configured as V<sub>DD</sub>/V<sub>SS</sub>, subject to number and drive of output buffers.

2. Alternately-sourced by LSI Logic Corp.

3. Includes 3 evaluation pads which cannot be configured as power pads.

### CAD System Features

Integrated Design System using Macrocell library for: ●Functional design ●Logic design  
●Auto place & route ●Test pattern generation

Hierarchical design using: ●Macrofunctions (which consist of Macrocells)

Maximum circuit size: ●10K gates

Timing verification of critical paths and safe margin check by Toshiba Delay Path analysis System (TDPS)

Automatic test pattern generation

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## DESIGN & DEVELOPMENT

### Development Flow & Customer Interface

		Functional & logic design	Network entry	Verify design	Functional & timing simulation	Verify node coverage	Auto place & route	Re-simulation	PG & MASK tooling
<b>Interface level</b>	Level 1	→							
	Level 2	→							
	Level 3	→							
	Level 4	→							

Notes: (1) At level-2, design procedure takes place by customer at Toshiba LSI Design Center and at customer site for level-3.  
 (2) The EWS interface such as LOGICIAN<sup>TM3)</sup>, IDEA Series<sup>TM4)</sup>, SCALDsystem<sup>TM5)</sup>, HP EDS<sup>8)</sup>, DASH<sup>TM6)</sup> and Workview<sup>TM7)</sup> is available.

In the note (2)  
 3) to 7) are Trademarks of.  
 3) Daisy Systems Corporation.  
 4) Mentor Graphics Corporation  
 8) is the system of HewlettPackard Corporation.

5) Valid Logic Systems Incorporated  
 6) FutureNet Corporation.  
 7) Viewlogic Systems Incorporated

### Electrical Specifications

#### Recommended Operating Conditions ( $V_{SS} = 0V$ )

Parameter	Symbol	Rating	Unit
DC supply voltage	$V_{DD}$	-0.3 to +7.0	V
DC input voltage	$V_{IN}$	-0.3 to $V_{DD} + 0.3$	V
Input current	$I_{IN}$	$\pm 20$	mA
Storage temperature	Tstg	-40 to +125	°C

Parameter	Symbol	Rating	Unit
DC supply voltage	$V_{DD}$	4.75 to 5.25	V
Ambient temperature	Ta	0 to +70	°C

### DC Electrical Specifications Under Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Max.	Unit				
$V_{IH}$	High Level Input Voltage				V				
	TTL Level		2.2						
	CMOS Level		3.5						
	SCHMITT Trigger		4.0						
$V_{IL}$	Low Level Input Voltage			0.8	V				
	TTL Level			1.5					
	CMOS Level			1.0					
	SCHMITT Trigger								
$I_{IH}$	High Level Input Current	$V_{IN} = V_{DD}$	-10	10	$\mu A$				
	Input Buffer with Pull-down		15G	1.0		30			
			17G	10		200			
			19G	10		200			
$I_{IL}$	Low Level Input Current	$V_{IN} = V_{SS}$	-10	10	$\mu A$				
	Input Buffer with Pull-up		15G	-30		-1.0			
			17G	-200		-10			
			19G	-200		-10			
$V_{OH}$	High Level Output Voltage		2.4		V				
	Buffer Type					15G	17G	19G	$I_{OH} = -2mA$
						B18	B18	B14	$I_{OH} = -4mA$
						B1	B1	B18	$I_{OH} = -8mA$
						B2 <sup>1)</sup>	B2 <sup>1)</sup>	B1	$I_{OH} = -16mA$
$V_{OL}$	Low Level Output Voltage		0.4		V				
	Buffer Type					15G	17G	19G	$I_{OL} = 2mA$
						B18	B18	B14	$I_{OL} = 4mA$
						B1	B1	B18	$I_{OL} = 8mA$
						B2 <sup>1)</sup>	B2 <sup>1)</sup>	B1	$I_{OL} = 16mA$
$I_{OZ}$	High Impedance Leakage Current	$V_{OUT} = V_{DD}$ or $V_{SS}$	-10	10	$\mu A$				
	Output Buffer with Pull-up		Same as $I_{IL}$ with Pull-up						
	Output Buffer with Pull-down		Same as $I_{IL}$ with Pull-down						
$I_{DD}$	Quiescent Supply Current	$V_{IN} = V_{DD}$ or $V_{SS}$		100 <sup>2)</sup>	$\mu A$				

Note: 1) Requires two I/O pads, others unspecified require one.  
 2) Customer-Design dependent

# TOSHIBA CMOS GATE ARRAY

## DESIGN DATA (As of Mar., 1988)

### Macrocell List (TC15G/17G/19G Series)

Function	Types		
	TC15G	TC17G	TC19G
LOGIC GATE	21	26	26
INVERTER/INTERNAL BUFFER	9	9	9
TRI-STATE INTERNAL BUFFER	5	5	5
LATCH	4	11	11
FLIP-FLOP	7	13	13
DECODER	2	4	4
MULTIPLEXER	3	5	5
INPUT BUFFER	5	17	17
OUTPUT BUFFER	9	14	14
BIDIRECTIONAL INPUT BUFFER	5	6	6
BIDIRECTIONAL OUTPUT BUFFER	7	28	28
OTHERS	0	3	3
<b>Total</b>	<b>77</b>	<b>141</b>	<b>141</b>

### Macrofunction List (TC17G/19G Series)

Function	Types	
	LSI Compatible	74HC Series Compatible
ADDERS	6	1
COMPARATORS	6	2
COUNTERS	19	11
DECODERS	10	4
FLIP-FLOPS	—	6
GATES	—	16
MULTIPLEXERS	11	10
REGISTERS	19	16
OTHERS	8	8
<b>Total</b>	<b>79</b>	<b>74</b>

## PACKAGE ADAPTABILITY LIST

Package	Part No.	TC15G						TC17G						TC19G								
		008	014	022	032	042	060	005	008	014	022	032	042	060	080	100	032	042	060	080	100	
DIP	16							A														
	18							A														
	24	A	A					A	A	A	A											
	28	A	A					A	A	A	A	A					A					
	40	A	A	A				A	A	A	A	A	A			A	A					
	42	A	A	A				A	A	A	A	A	A			A	A					
	48	A	A	A				A	A	A	A	A	A			A	A					
	42	A	A	A				A	A	A	A	A	A			A	A					
PGA	64	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	68	A	A	A	A	A	A		A	A	A	A	A	A	A	A	A	A	A	A	A	A
	84		A	A	A	A	A			A	A	A	A	A	A	A	A	A	A	A	A	A
	100			A	A	A	A				A	A	A	A	A	A	A	A	A	A	A	A
	120				A	A	A				A	A	A	A	A	A	A	A	A	A	A	A
	135				A	A	A					A	A	A	A	A	A	A	A	A	A	A
	144					A	A					A	A	A	A	A	A	A	A	A	A	A
	180						A	A						A	A	A	A	A	A	A	A	A
PPGA <sup>2)</sup>	120																A	A	A			
	144																	A				
MPGA <sup>2)</sup>	120									P	P	P	P				P	P	P			
	144										D	D	D	D	D		D	D	D	D	D	
CD <sup>2)</sup> PGA	95														P	P				P	P	
	155														P	P				P	P	
	223														D	D				D	D	
	299																					
PLCC	44							D	D	D	D	D	D				D	D				
	68	A	A	A	A			A	A	A	A	A	A	P	P		A	A	A	P	P	
	84		A	A	A				A	A	A	A	A	P	P		A	A	A	P	P	
PFP	SQUARE	44	A	A	A			A	A	A	A	A	A				A	A				
		60						A	A	A	A	A	A				A	A				
		100A <sup>1)</sup>	A	A						A												
		100 <sup>1)</sup>		A	A	A					A	A	A	A	D	D		A	A	A	D	D
	144												A	A	D	D		A	A	D	D	
	184														P	P				P	P	
	REC-TANGULAR	64	A	A	A					A	A	A	A	A				A	A			
		80	A	A	A					A	A	A	A	A				A	A			
100			A	A							A	A	A				A	A				
CFP	100 <sup>1)</sup>			A	A	A	A										A	A	A	A	A	
	144					A	A										A	A	A	A	A	
	184																P	P		P	P	

A: Adaptable  
D: Check with Toshiba for availability (Under development)  
P: Check with Toshiba for availability (Under planning)

Notes: 1) Flat Package 100 pin is classified into 2 types determined by number of inner leads available: 100A—84 inner leads, 100—100 inner leads.  
2) PPGA—Plastic PGA, MPGA—Metal PGA, CD PGA—Cavity Down PGA.  
3) Please refer to "Package Selector Guide" (Document I.D. SEMI-E-S1001) for further information in detail.

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