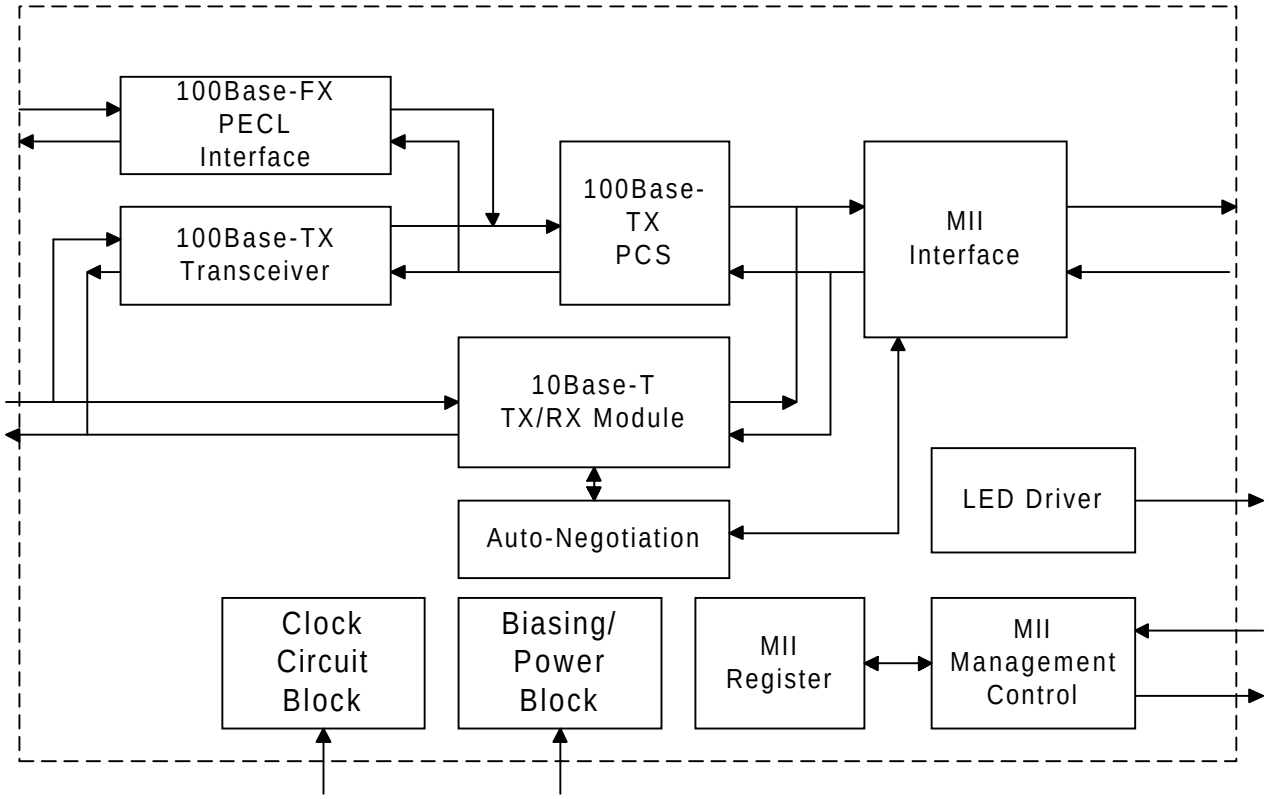
General Description

The DM9131 is a physical-layer, single-chip, low-power transceiver for 100BASE-TX and 10BASE-T operations. On the media side, it provides a direct interface either to Unshielded Twisted Pair Cable 5 (UTP5) for 100BASE-TX Fast Ethernet, or UTP5/UTP3 Cable for 10BASE-T Ethernet, and it also provides PECL interface to connect the external fiber optical transceiver. Through the Media Independent Interface (MII), the DM9131 connects to the Medium Access Control (MAC) layer, ensuring a high inter-operability among products from different vendors.

The DM9131 uses a low-power and high-performance CMOS process. It contains the entire physical layer functions of 100BASE-TX as defined by IEEE802.3u, including the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Twisted Pair Physical Medium Dependent Sublayer (TP-PMD), 10BASE-TX Encoder/Decoder (ENC/DEC), and Twisted Pair Media Access Unit (TPMAU). The DM9131 provides a strong support for the auto-negotiation function utilizing automatic media speed and protocol selection. Furthermore, due to the built-in wave-shaping filter, the DM9131 needs no external filter to transport signals to the media in 100M or 10M Ethernet operation.

Block Diagram



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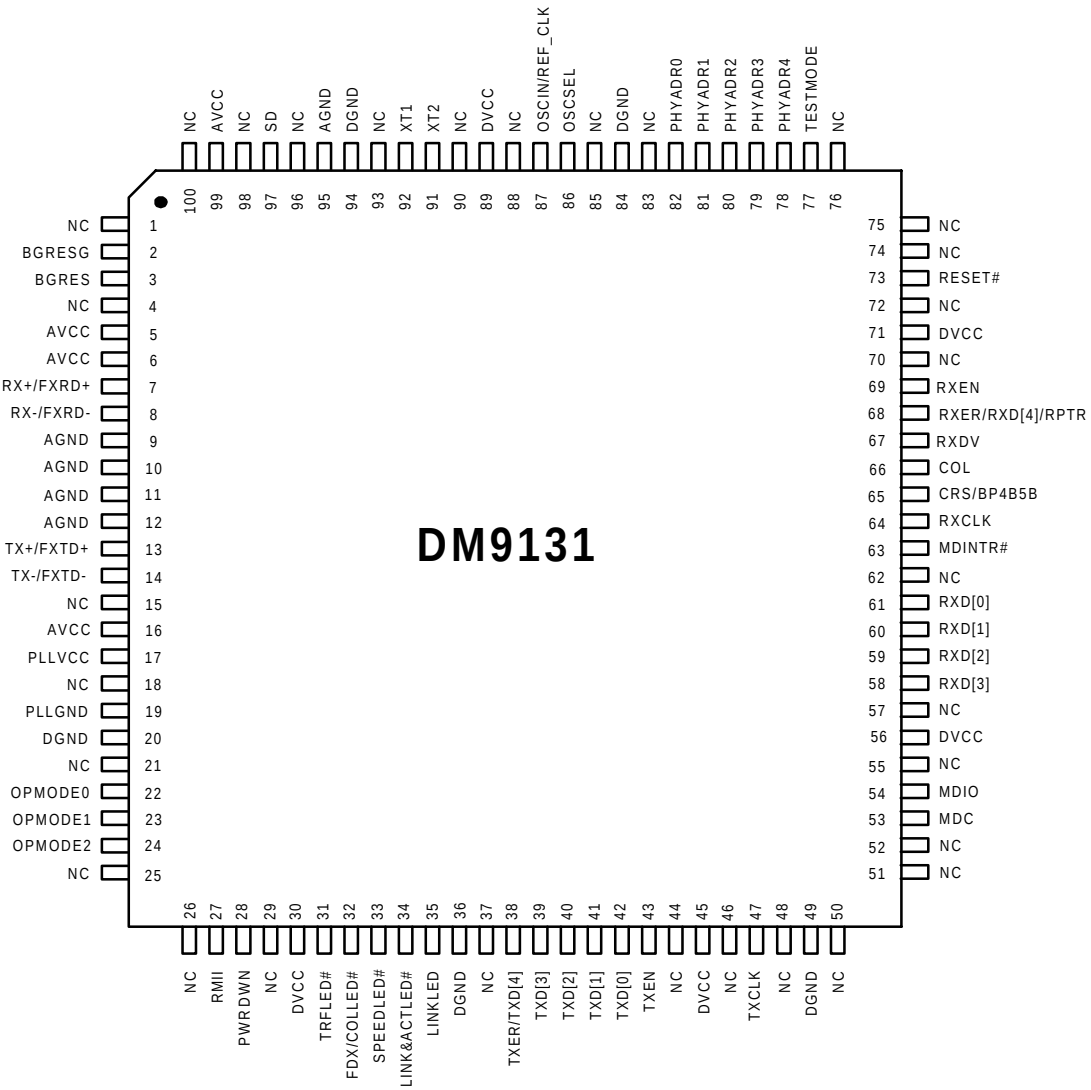
Features

- Fully compliant with IEEE 802.3u 10Base-T/100Base-TX
- Compliant with ANSI X3T12 TP-PMD 1995 standard
- Support Auto-Negotiation function, compliant to IEEE 802.3u
- Single-chip fully integrated Physical layer interface - directly to magnetic
- Integrated 10Base-T and 100Base-TX transceiver
- On-chip filtering, no need for external filters
- Selectable repeater or node mode
- Far end fault signaling option in FX mode
- Selectable twisted-pair or fiber mode output
- Selectable full-duplex or half-duplex operation
- MII management interface with maskable interrupts output capability
- Provides Loopback mode for easy system diagnostics
- Status LED output provides Link & Activity, Speed10/100 and Full-duplex/Collision LED
- Low-Power, Single-Supply 3.3V CMOS technology
- Compatible with 3.3V and 5.0V tolerant I/O
- 100-pin LQFP

Pin Configuration



Pin Description

I : Input, O : Output, LI : Latch input when power-up/reset, Z : Tri-State output

Normal MII interface, 21 pins

Pin No.	Pin Name	I/O	Description
38	TXER/TXD[4]	I	Transmit Error/The fifth TXD data bit In 100Mbps mode, when the signal actives high and TXEN actives, the HALT symbol is substituted for the actual data nibble. In 10Mbps, the input is ignored. In bypass mode (bypass BP4B5B), TXER becomes the TXD[4] pin, the fifth TXD data bit of the 5B symbol.
42,41,40,39	TXD[0:3]	I	Transmit Data 4 bits nibble data input (synchronous to the TXCLK) when in 10/100Mbps nibble mode. In 10Mbps serial mode, the TXD[0] pin is used as the serial data input pin, and TXD[1:3] are ignored.
43	TXEN	I	Transmit Enable Active high to indicate the presence of valid nibble data on the TXD[0:3] for both 100Mbps and 10Mbps nibble mode. In 10Mbps serial mode, active high indicates the presence of valid 10Mbps data on TXD[0].
47	TXCLK	O,Z	Transmit Clock The transmitting clock provides the timing reference for the transfer of the TXEN, TXD, and TXER. TXCLK is provided by the PHY. 25MHz in 100Mbps nibble mode, 2.5MHz in 10Mbps nibble mode, 10MHz in 10Mbps serial mode.
53	MDC	I	Management Data Clock Synchronous clock for the MDIO management data. This clock is provided by management entity, and it is up to 2.5MHZ
54	MDIO	I/O	Management Data I/O Bi-directional management data that may be provided by the station management entity or the PHY.
61,60,59,58	RXD[0:3]	O,Z	Receive Data Output 4 bits nibble data output (synchronous to RXCLK) when in 10/100Mbps nibble mode. In 10Mbps serial mode, the RXD[0] pin is used as the serial data output pin, and the RXD[1:3] are ignored.
63	MDINTR#	O	Status Interrupt Output: Asserted low whenever there is status change.(link, speed, duplex)
64	RXCLK	O,Z	Receive Clock, The received clock provides the timing reference for the transfer of the RXDV, RXD, and RXER. RXCLK is provided by PHY. The PHY may recover the RXCLK reference from the received data or it may derive the RXCLK reference from a nominal clock. 25MHz in 100Mbps nibble mode, 2.5MHz in 10Mbps nibble mode, 10MHz in 10Mbps serial mode.
65	CRS/(BP4B5B)	O,Z /LI	Carrier Sense Detect/Bypass 4B/5B encoder/decoder Asserted high to indicate the presence of carrier dues to receive or

			transmit activities in 10BASE-T or 100BASE-TX half-duplex mode. In repeater mode or full-duplex mode, this signal is asserted high to indicate the presence of carrier due only to the receive activity. This pin is also used as bypass 4B/5B encoder/decoder.(power up reset latch input) 0 = normal operation 1 = bypass 4B5B
66	COL	O,Z	Collision Detection Asserted high to indicate that detection of the collision conditions in 10Mbps and 100Mbps half-duplex mode. In full-duplex mode, this signal is always logical 0.
67	RXDV	O,Z	Receive Data Valid Asserted high to indicate that the valid data is present on the RXD[0:3].
68	RXER/RXD[4] /(RPTR/NODE)	O,Z /LI	Receive Data Error/The fifth RXD data bit of the 5B symbol Asserted high to indicate that an invalid symbol has been detected. In decoder bypass mode (bypass BP4B5B), RXER becomes RXD[4], the fifth RXD data bit of the 5B symbol. These pins are also used to select Repeater or Node mode. (power up reset latch input). 0 = node mode (default) 1 = repeater mode
69	RXEN	I	Receive Enable : Active high enable for receive signals RXD[0:3], RXCLK, RXDV and RXCLK. A low on this input tri-states these output pins. For normal operation in a node application, this pin should be pulled high. In repeater application, this pin may be connected to a repeater controller.
73	RESET#	I	Reset Active low input that initializes the DM9131.

Media interface, 5 pins

Pin No.	Pin Name	I/O	Description
7,8	RX+/FXRD+ RX-/FXRD-	I	Differential receive pair/PECL receive pair Differential data is received from the media. Differential Pseudo ECL signal is received from the media in fiber mode.
13,14	TX+/FXTD+ TX-/FXTD-	O	Differential transmit pair/PECL transmit pair Differential data is transmitted to the media in TP mode. Differential Pseudo ECL signal transmits to the media in fiber mode.
97	SD	I	Fiber-optic signal detect PECL signal which indicates whether or not the fiber-optic receive pair is receiving valid signal levels.

LED interface, 5 pins

Pin No.	Pin Name	I/O	Description
31	TRFLED#	O	Traffic LED Active low. It flashes when the DM9131 is transmitting or receiving data.
32	FDXLED /COLLED#	O	Full-Duplex LED/Collision LED : Active low. Indicates full-duplex mode for 100Mbps and 10Mbps operation. It is changed to collision LED function when bit 4 of register 16 is set to 1.

33	SPEEDLED#	O	Speed LED: Driven low when operating in 100Mbps and high when operating in 10Mbps. When bit 6 of Register 16 is set, it controls the SPEEDLED as 100Base-TX SD signal output. For debug only.
34	LINK&ACT LED#	O	Link LED & Activity LED : Active low to indicate good link for 10Mbps and 100Mbps operation. It is also a activity LED function when transmit or receive data.
35	LINKLED	O	Link LED Active high to indicate good link for 10Mbps and 100Mbps operation

Mode, 11 pins

Pin No.	Pin Name	I/O	Description
22,23,24	OPMODE0~2	LI	OPMODE0~OPMODE2 : These pins are used to control the forced or advertised operating mode of the DM9131 according to the following table. The value is latched into the DM9131 registers at power-up/reset. OP2 OP1 OP0 Function 0 0 0 auto negotiation enable with all capabilities 0 0 1 manual select 100TX FDX 0 1 0 manual select 100TX HDX 0 1 1 manual select 10TX FDX 1 0 0 manual select 10TX HDX 1 0 1 manual select 100FX FDX 1 1 0 manual select 100FX HDX 1 1 1 dual speed 100/10 HDX
27	RMII	I	Reduced MII enable: This pin is used to select Normal MII or Reduced MII. “0”= Normal MII, (default) “1”= Reduced MII. This pin always pull-low except that DM9131 is used as reduced MII.
28	PWRDWN	I	Power down control Assert high to force DM9131 into power down mode. When in power down mode, most of the DM9131 circuit block’s power is truned off, only the MII management interface (MDC, MDIO) logic is available (the PHY should respond to management transactions and should not generate spurious signals on the MII)). To leave power down mode, DM9131 need the hardware or software reset with the PWRDWN pin to low.
77	TESTMODE	I	Test mode control pin. 0 = normal operation 1 = enable test mode
82~78	PHYADR[0:4]	I	PHY address PHY address sensing input pins.

Bias and clock, 6 pins

Pin No.	Pin Name	I/O	Description
2	BGRESG	P	Bandgap Ground
3	BGRES	P	Bandgap Voltage Reference Resistor 6.2K ohm
86	OSCSEL	I	Oscillator or Crystal selection. “0” = Crystal, “1” = Oscillator
87	OSCIN / REF_CLK	I	Oscillator input (25MHz) or Reduced MII Reference Clock Input (50MHz for Reduced MII only).
91	XT2	O	Crystal Output
92	XT1	I	Crystal Input

Power and others, 52 pins

Pin No.	Pin Name	I/O	Description
5,6,16,99	AVCC	P	Analog Power
9,10,11,12,95	AGND	P	Analog Ground
30,45,56,71, 89	DVCC	P	Digital Power
20,36,49,84 ,94	DGND	P	Digital Ground
17	PLLVCC	P	Analog Power
19	PLLGND	P	Analog Ground
1,4,15,18,21, 25,26,29,37, 44,46,48,50, 51,52,55,57, 62,70,72,74, 75,76,83,85, 88,90,93,96, 98,100	NC		Not connected.

Functional Description

The DM9131 Fast Ethernet single-chip PHY transceiver, provides the functionality as specified in IEEE802.3, integrates the complete 100BASE-TX module and the complete 10BASE-T module. The DM9131 also provides a standard Media Independent Interface (MII) to connect a media access controller and a network media. The DM9131 performs all PCS, PMA, and TP-PMD sub-layer as defined by specification.

Transmit Section

The transmit section consists of the following blocks:
- PCS Transmit
- Clock Generator
- NRZ to NRZI. MLT3 encoder and driver
- MANCHESTER encoder
- 10BASET-TX filter and driver

100BASE-TX Operation

The 100BASE-TX transmitter receives 4-bit nibble-data clocked in at 25MHz at the MII and outputs scrambled 5-bit encoded MLT-3 signal to the media at 100Mbps. The on-chip clock circuit converts 25MHz clock into a 125MHz clock for internal use.

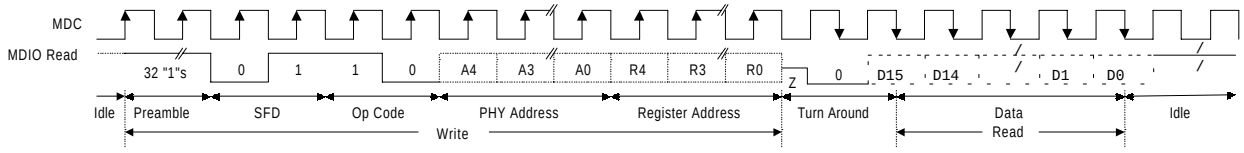
MII Serial Management Interface

The serial management interface uses a simple, two-wired serial interface to obtain and control the status of the physical layer through an MII interface (MDC and MDIO pins). The Management Data Clock (MDC) is equipped with a maximum clock rate of 2.5MHz, while Management Data Input /Output (MDIO) works as a bi-directional, open-drain pin shared by up to 32 devices.

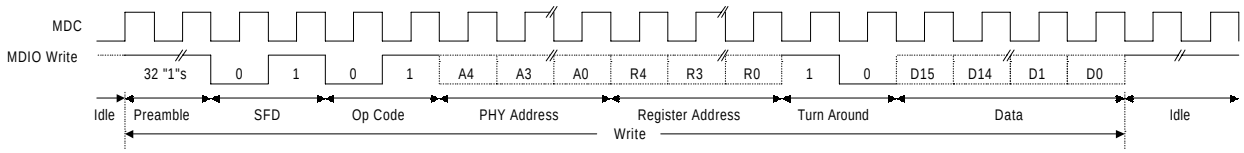
DM9131's management functions correspond to MII specification for IEEE 802.3u-1995 (Clause 22) and the registers 0 through 6 with vendor-specific registers 11,15,16,17,18.

In read/write operation, the management data frame is 64-bit long start with 32 contiguous logic one bits (preamble) synchronization clock cycles on MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by the operation code (OP):<10> indicates Read operation and <01> indicates Write operation. For read operation, a 2-bit turnaround (TA) filing between Resistor Address field and Data field is provided for MDIO to avoid contention. "Z" stands for high impedance state. Following turnaround time, a 16-bit data is read from or written onto management registers.

Management Interface - Read Frame Structure



Management Interface - Write Frame Structure



MII Register Description

ADD	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	CONTROL	Reset	Loop back	Speed select	Auto-N Enable	Power Down	Isolate	Restart Auto-N	Full Duplex	Coll. Test	Reserved						
01	STATUS	T4 Cap.	TX FDX Cap.	TX HDX Cap.	10 FDX Cap.	10 HDX Cap.	Reserved				Pream. Supr.	Auto-N Compl.	Remote Fault	Auto-N Cap.	Link Status	Jabber Detect	Extd Cap.
02	PHYID1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
03	PHYID2	1	0	1	1	1	0	Model No.					Version No.				
04	Auto-Neg. Advertise	Next Page	FLP Rcv Ack	Remote Fault	Reserved		FC Adv	T4 Adv	TX FDX Adv	TX HDX Adv	10 FDX Adv	10 HDX Adv	Advertised Protocol Selector Field				
05	Link Part. Ability	LP Next Page	LP Ack	LP RF	Reserved		LP FC	LP T4	LP TX FDX	LP TX HDX	LP 10 FDX	LP 10 HDX	Link Partner Protocol Selector Field				
06	Auto-Neg. Expansion	Reserved											Pardet Fault	LP Next Pg Able	Next Pg Able	New Pg Rcv	LP AutoN Cap.
16	Aux. Config.	BP 4B5B	BP SCR	BP ALIGN	BP_ADPOK	Repeat mode	TX/FX Select	FEF Enable	RMII Enable	Force 100LNK	SPDLED_CTL	Rsvd	FDXLED_CTL	Reset St. Mch	Pream. Supr.	Sleep mode	Remote LoopOut
17	Aux. Conf/Stat	100 FDX	100 HDX	10 FDX	10 HDX	Reserved			PHY ADDR [4:0]				Auto-N. Monitor Bit [3:0]				
18	10T Conf/Stat	Rsvd	LP Enable	HBE Enable	SQUE Enable	JAB Enable	10T Serial	Reserved									Polarity Reverse
21	MDINTR	INTR PEND	Rsvd	Rsvd	Rsvd	FDX Mask	SPD Mask	Link Mask	INTR Mask	Rsvd	Rsvd	Rsvd	FDX Change	SPD Change	Link Change	INT Enable	INTR Status
22	Rcv Error Counter	Receive Error Counter															
23	Disconnect Counter	Reserved									Disconnect Counter						

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type> / <Attribute(s)>

Where：

<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
X	No default value
(PIN#)	Value latched in from pin # at reset

<Access Type>:

RO = Read only
RW = Read/Write

<Attribute (s)>:

SC = Self clearing
P = Value permanently set
LL = Latching low
LH = Latching high

Basic Mode Control Register (BMCR) - 00

Bit	Bit Name	Default	Description
0.15	Reset	0, RW/SC	**Reset:** 1=Software reset 0=Normal operation This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed
0.14	Loopback	0, RW	**Loopback:** Loop-back control register 1 = Loop-back enabled 0 = Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appear at the MII receive outputs
0.13	Speed selection	1, RW	**Speed select:** 1 = 100Mbps 0 = 10Mbps Link speed may be selected either by this bit or by auto-negotiation. When auto-negotiation is enabled and bit 12 is set, this bit will return auto-negotiation selected media type.
0.12	Auto-negotiation enable	1, RW	**Auto-negotiation enable:** 1 = Auto-negotiation is enabled, bit 8 and 13 will be in auto-negotiation status
0.11	Power down	0, RW	**Power Down:** While in the power-down state, the PHY should respond to management transactions. During the transition to power-down state and while in the power-down state, the PHY should not generate spurious signals on the MII. 1=Power down 0=Normal operation
0.10	Isolate	0,RW	**Isolate:** 1 = Isolates the DM9131 from the MII with the exception of the serial management. (When this bit is asserted, the DM9131 does not respond to the TXD[0:3], TX_EN, and TX_ER inputs, and it shall present a high impedance on its TX_CLK, RX_CLK, RX_DV, RX_ER, RX[0:3], COL and CRS outputs. When PHY is isolated from the MII it shall respond to the management transactions) 0 = Normal operation
0.9	Restart auto-negotiation	0,RW/SC	**Restart auto-negotiation:** 1 = Restart auto-negotiation. Re-initiates the auto-negotiation process. When auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning a value of 1 until auto-negotiation is initiated by the DM9131. The operation of the auto-negotiation process will not be affected by the management entity that clears this bit 0 = Normal operation

0.8	Duplex mode	1,RW	**Duplex mode:** 1 = Full duplex operation. Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With auto-negotiation enabled, this bit reflects the duplex capability selected by auto-negotiation 0 = Normal operation
0.7	Collision test	0,RW	**Collision test:** 1 = Collision test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN 0 = Normal operation
0.6-0.0	Reserved	0,RO	**Reserved:** Write as 0, ignore on read

Basic Mode Status Register (BMSR) - 01

Bit	Bit Name	Default	Description
1.15	100BASE-T4	0,RO/P	**100BASE-T4 capable:** 1 = DM9131 is able to perform in 100BASE-T4 mode 0 = DM9131 is not able to perform in 100BASE-T4 mode
1.14	100BASE-TX full duplex	1,RO/P	**100BASE-TX full duplex capable:** 1 = DM9131 is able to perform 100BASE-TX in full duplex mode 0 = DM9131 is not able to perform 100BASE-TX in full duplex mode
1.13	100BASE-TX half duplex	1,RO/P	**100BASE-TX half duplex capable:** 1 = DM9131 is able to perform 100BASE-TX in half duplex mode 0 = DM9131 is not able to perform 100BASE-TX in half duplex mode
1.12	10BASE-T full duplex	1,RO/P	**10BASE-T full duplex capable:** 1 = DM9131 is able to perform 10BASE-T in full duplex mode 0 = DM9131 is not able to perform 10BASE-TX in full duplex mode
1.11	10BASE-T half duplex	1,RO/P	**10BASE-T half duplex capable:** 1 = DM9131 is able to perform 10BASE-T in half duplex mode 0 = DM9131 is not able to perform 10BASE-T in half duplex mode
1.10-1.7	Reserved	0,RO	**Reserved:** Write as 0, ignore on read
1.6	MF preamble suppression	0,RO	**MII frame preamble suppression:** 1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed
1.5	Auto-negotiation Complete	0,RO	**Auto-negotiation complete:** 1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed
1.4	Remote fault	0, RO/LH	**Remote fault:** 1 = Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM9131 implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0 = No remote fault condition detected
1.3	Auto-negotiation ability	1,RO/P	**Auto configuration ability:** 1 = DM9131 is able to perform auto-negotiation 0 = DM9131 is not able to perform auto-negotiation
1.2	Link status	0,RO/LL	**Link status:**

			1 = Valid link is established (for either 10Mbps or 100Mbps operation) 0 = Link is not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface
1.1	Jabber detect	0, RO/LH	**Jabber detect:** 1 = Jabber condition detected 0 = No jabber This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a DM9131 reset. This bit works only in 10Mbps mode
1.0	Extended capability	1,RO/P	**Extended capability:** 1 = Extended register capable 0 = Basic register capable only

PHY ID Identifier Register #1 (PHYID1) - 02

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM9131. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Bit Name	Default	Description
2.15-2.0	OUI_MSB	<0181h>	**OUI most significant bits:** This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

PHY Identifier Register #2 (PHYID2) - 03

Bit	Bit Name	Default	Description
3.15-3.10	OUI_LSB	<101110>, RO/P	**OUI least significant bits:** Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
3.9-3.4	VNDR_MDL	<000010>, RO/P	**Vendor model number:** Six bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3.3-3.0	MDL_REV	<0000>, RO/P	**Model revision number:** Four bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 3)

Auto-negotiation Advertisement Register(ANAR) - 04
This register contains the advertised abilities of this DM9131 device as they will be transmitted to its link partner during Auto-negotiation.

Bit	Bit Name	Default	Description
4.15	NP	0,RO/P	**Next page indication:** 0 = No next page available 1 = Next page available The DM9131 has no next page, so this bit is permanently set to 0
4.14	ACK	0,RO	**Acknowledge:** 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The DM9131's auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the auto-negotiation process. Software should not attempt to write to this bit.
4.13	RF	0, RW	**Remote fault:** 1 = Local device senses a fault condition 0 = No fault detected
4.12-4.11	Reserved	X, RW	**Reserved:** Write as 0, ignore on read
4.10	FCS	0, RW	**Flow control support:** 1 = Controller chip supports flow control ability 0 = Controller chip doesn't support flow control ability
4.9	T4	0, RO/P	**100BASE-T4 support:** 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 is not supported The DM9131 does not support 100BASE-T4 so this bit is permanently set to 0
4.8	TX_FDX	1, RW	**100BASE-TX full duplex support:** 1 = 100BASE-TX full duplex is supported by the local device 0 = 100BASE-TX full duplex is not supported
4.7	TX_HDX	1, RW	**100BASE-TX support:** 1 = 100BASE-TX is supported by the local device 0 = 100BASE-TX is not supported
4.6	10_FDX	1, RW	**10BASE-T full duplex support:** 1 = 10BASE-T full duplex is supported by the local device 0 = 10BASE-T full duplex is not supported
4.5	10_HDX	1, RW	**10BASE-T support:** 1 = 10BASE-T is supported by the local device 0 = 10BASE-T is not supported
4.4-4.0	Selector	<00001>, RW	**Protocol selection bits:** These bits contain the binary encoded protocol selector supported by this node. <00001> indicates that this device supports IEEE 802.3 CSMA/CD.

Auto-negotiation Link Partner Ability Register (ANLPAR) – 05

This register contains the advertised abilities of the link partner When received during Auto-negotiation.

Bit	Bit Name	Default	Description
5.15	NP	0, RO	**Next page indication:** 0 = Link partner, no next page available 1 = Link partner, next page available
5.14	ACK	0, RO	**Acknowledge:** 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The DM9131's auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit.
5.13	RF	0, RO	**Remote Fault:** 1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner
5.12-5.11	Reserved	X, RO	**Reserved:** Write as 0, ignore on read
5.10	FCS	0, RW	**Flow control support:** 1 = Controller chip supports flow control ability by link partner 0 = Controller chip doesn't support flow control ability by link partner
5.9	T4	0, RO	**100BASE-T4 support:** 1 = 100BASE-T4 is supported by the link partner 0 = 100BASE-T4 is not supported by the link partner
5.8	TX_FDX	0, RO	**100BASE-TX full duplex support:** 1 = 100BASE-TX full duplex is supported by the link partner 0 = 100BASE-TX full duplex is not supported by the link partner
5.7	TX_HDX	0, RO	**100BASE-TX support:** 1 = 100BASE-TX half duplex is supported by the link partner 0 = 100BASE-TX half duplex is not supported by the link partner
5.6	10_FDX	0, RO	**10BASE-T full duplex support:** 1 = 10BASE-T full duplex is supported by the link partner 0 = 10BASE-T full duplex is not supported by the link partner
5.5	10_HDX	0, RO	**10BASE-T support:** 1 = 10BASE-T half duplex is supported by the link partner 0 = 10BASE-T half duplex is not supported by the link partner
5.4-5.0	Selector	<00000>, RO	**Protocol selection bits:** Link partner's binary encoded protocol selector

Auto-negotiation Expansion Register (ANER)- 06

6.15-6.5	Reserved	X, RO	**Reserved:** Write as 0, ignore on read
6.4	PDF	0, RO/LH	**Local device parallel detection fault:** PDF = 1 : A fault detected via parallel detection function. PDF = 0 : No fault detected via parallel detection function
6.3	LP_NP_ABLE	0, RO	**Link partner next page able:** LP_NP_ABLE = 1 : Link partner, next page available LP_NP_ABLE = 0 : Link partner, no next page
6.2	NP_ABLE	0,RO/P	**Local device next page able:** NP_ABLE = 1 : DM9131, next page available NP_ABLE = 0 : DM9131, no next page DM9131 does not support this function, so this bit is always 0.
6.1	PAGE_RX	0, RO/LH	**New page received:** A new link code word page received. This bit will be automatically cleared when the register (register 6) is read by management.
6.0	LP_AN_ABLE	0, RO	**Link partner auto-negotiation able:** A "1" in this bit indicates that the link partner supports Auto-negotiation.

DAVICOM Specified Configuration Register (DSCR) - 16

Bit	Bit Name	Default	Description
16.15	BP_4B5B	(Pin#xx), RW	**Bypass 4B5B encoding and 5B4B decoding :** The value of the BP4B5B pin(xx) is latched into this bit at power-up/reset. 1 = 4B5B encoder and 5B4B decoder function bypassed 0 = Normal 4B5B and 5B4B operation
16.14	BP_SCR	0, RW	**Bypass scrambler/descrambler function :** 1 = Scrambler and descrambler function bypassed 0 = Normal scrambler and descrambler operation
16.13	BP_ALIGN	0, RW	**Bypass symbol alignment function:** 1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed 0 = Normal operation
16.12	BP_ADPOK	0, RW	**BYPASS ADPOK :** Force signal detector (SD) active. This register is for debug only, not release to customer. 1=Force SD is OK, 0=Normal operation
16.11	REPEATER	(Pin#xx),RW	**Repeater/Node mode :** The value of the Repeater/Node pin(xx) is latched into this bit at power-up/reset. 1 = Repeater mode 0 = Node mode
16.10	TX	1, RW	**100BASE-TX or FX mode control:** 1 = 100BASE-TX operation 0 = 100BASE-FX operation

16.9	FEF	0, RW	**Far End Fault enable :** Control the Far End Fault mechanism associated with 100Base-FX operation. 1 = Enable 0 = Disable
16.8	RMII_Enable	(Pin#xx), RW	**Reduced MII enable :** Select normal MII or reduced MII. The value of the RMII pin(xx) is latched into this bit at power-up/reset. 0 = Normal MII 1 = Enable Reduced MII
16.7	F_LINK_100	0, RW	**Force good link in 100Mbps:** 0 = Normal 100Mbps operation 1 = Force 100Mbps good link status This bit is useful for diagnostic purposes.
16.6	SPLED_CTL	0, RW	**Speed LED Disable :** 0 : Normal SPEEDLED output to indicate speed status 1 : Disable SPEEDLED output and enable SD signal monitor (for internal debug). When this bit is set, it control the SPEEDLED as 100BASE-X SD (not fiber mode) signal output .For debug only.
16.5	Reserved	0, RO	**Reserved**
16.4	FDXLED_CTL	0,RW	**Full-duplex LED mode select :** 0 = FDXLED output is configured to indicate full-duplex status 1 = COLLED output is configured to indicate the presence of collision activity operation.
16.3	SMRST	0, RW	**Reset state machine:** When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed.
16.2	MFPSC	0, RW	**MF preamble suppression control:** MII frame preamble suppression control bit 1 = MF preamble suppression bit on 0 = MF preamble suppression bit off
16.1	SLEEP	0, RW	**Sleep mode:** Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset
16.0	RLOUT	0, RW	**Remote loopout control:** When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for bit error rate testing

DAVICOM Specified Configuration and Status Register (DSCSR) - 17

Bit	Bit Name	Default	Description
17.15	100FDX	1, RO	**100M full duplex operation mode:** After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M full duplex mode. The software can read bit[15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode.
17.14	100HDX	1, RO	**100M half duplex operation mode:** After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M half duplex mode. The software can read bit[15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode.
17.13	10FDX	1, RO	**10M full duplex operation mode:** After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Full Duplex mode. The software can read bit[15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode.
17.12	10HDX	1, RO	**10M half duplex operation mode:** After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M half duplex mode. The software can read bit[15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode.
17.11-17.9	Reserved	0, RO	**Reserved:** Write as 0, ignore on read
17.8-17.4	PHYADR[4:0]	(PHYADR), RW	**PHY address Bit 4:0:** The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY.
17.3-17.0	ANMB[3:0]	0, RO	**Auto-negotiation monitor bits:** These bits are for debug only. The auto-negotiation status will be written to these bits.

b3	b2	b1	b0	
0	0	0	0	In IDLE state
0	0	0	1	Ability match
0	0	1	0	Acknowledge match
0	0	1	1	Acknowledge match fail
0	1	0	0	Consistency match
0	1	0	1	Consistency match fail
0	1	1	0	Parallel detects signal_link_ready
0	1	1	1	Parallel detects signal_link_ready fail
1	0	0	0	Auto-negotiation completed successfully

10BASE-T Configuration/Status (10BTCSR) - 18

Bit	Bit Name	Default	Description
18.15	Reserved	0, RO	**Reserved:** Write as 0, ignore on read
18.14	LP_EN	1, RW	**Link pulse enable:** 1 = Transmission of link pulses enabled 0 = Link pulses disabled, good link condition forced This bit is valid only in 10Mbps operation.
18.13	HBE	1,RW	**Heartbeat enable:** 1 = Heartbeat function enabled 0 = Heartbeat function disabled When the DM9131 is configured for full duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in full duplex mode).
18.12	SQUELCH	1, RW	**Squelch enable :** 1 = normal squelch 0 = low squelch
18.11	JABEN	1, RW	**Jabber Enable:** Enables or disables the Jabber function when the DM9131 is in 10BASE-T full duplex or 10BASE-T transceiver loopback mode 1 = Jabber function enabled 0 = Jabber function disabled
18.10	10BT_SER	0,RW	**10BASE-T serial mode:** 1 = 10BASE-T serial mode selected 0 = 10BASE-T nibble mode selected Serial mode is not supported for 100Mbps operation.
18.9-18.1	Reserved	0, RO	**Reserved:** Write as 0, ignore on read
18.0	POLR	0, RO	**Polarity reversed:** When this bit is set to 1, it indicates that the 10Mbps cable polarity is reversed. This bit is set and cleared by 10BASE-T module automatically.

DAVICOM Specified Interrupt Register – 21

Bit	Bit Name	Default	Description
21.15	INTR PEND	0, RO	**Interrupt pending :** Indicates that the interrupt is pending and is cleared by the current read. This bit shows the same result as bit 0. (INTR Status)
21.14-21.12	Reserved	0, RO	**Reserved**
21.11	FDX mask	1, RW	**Full-duplex interrupt mask :** When this bit is set, the Duplex status change will not generate the interrupt
21.10	SPD mask	1, RW	**Speed interrupt mask :** When this bit is set, the Speed status change will not generate the interrupt
21.9	LINK mask	1, RW	**Link interrupt mask :** When this bit is set, the link status change will not generate the interrupt
21.8	INTR mask	1, RW	**Master interrupt mask :** When this bit is set, no interrupts will be generated under any condition.
21.7-21.5	Reserved	0, RO	**Reserved**
21.4	FDX change	0,RO/LH	**Duplex status change interrupt :** “1” indicates a change of duplex since last register read. A read of this register will clear this bit.
21.3	SPD change	0, RO/LH	**Speed status change interrupt :** “1” indicates a change of speed since last register read. A read of this register will clear this bit.
21.2	LINK change	0, RO/LH	**Link status change interrupt :** “1” indicates a change of link since last register read. A read of this register will clear this bit.
21.1	INTR enable	0, RW	**Interrupt enable :** “1” = enable the interrupt mode, “0” = disable
21.0	INTR status	0, RO/LH	**Interrupt status :** The status of MDINTR# . “1” indicates that the interrupt mask is off that one or more of the change bits are set. A read of this register will clear this bit.

DAVICOM Specified Receive Error Counter Register (RECR) – 22

Bit	Bit Name	Default	Description
22.15-0	Rcv_Err_Cnt	0, RO	**Receive error counter :** Receive error counter that increments upon detection of REER

DAVICOM Specified Disconnect Counter Register (DISCR) – 23

Bit	Bit Name	Default	Description
23.15-23.8	Reserved	0, RO	**Reserved**
23.7-23.0	Disconnect Counter	0, RO	Disconnect Counter that increments upon detection of disconnection.

Absolute Maximum Ratings

Absolute Maximum Ratings (25°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVCC, AVCC	Supply Voltage	-0.3	3.6	V	
VIN	DC Input Voltage (VIN)	-0.5	5.5	V	
VOUT	DC Output Voltage(VOUT)	-0.3	3.6	V	
Tstg	Storage Temperature Rang (Tstg)	-40	+125	°C	
PD	Power Dissipation (PD)	---	0.43	W	
LT	Lead Temp. (TL, Soldering, 10 sec.)	---	240	°C	

Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVCC,AVCC	Supply Voltage	3.135	3.465	V	
Tc	Case Temperature	---	85	°C	
PD (Power Dissipation)	100BASE-TX	---	115	mA	3.3V
	100BASE-FX	---	25	mA	3.3V
	10BASE-T TX	---	125	mA	3.3V
	10BASE-T idle	---	44	mA	3.3V
	Auto-negotiation	---	76	mA	3.3V

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VCC = 3.3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
TTL Inputs (TXD0~TXD3, TXCLK, MDC, MDIO, TXEN, TXER, RXEN, TESTMODE, RMII, OSCSEL, PHYAD0~4, OPMODE0-2, RPTR, BP4B5B, RESET#)						
V_{IL}	Input Low Voltage	---	---	0.8	V	
V_{IH}	Input High Voltage	2.0	---	---	V	
I_{IL}	Input Low Leakage Current	---	---	10	uA	V_{IN} = 0.4V
I_{IH}	Input High Leakage Current	---	---	-10	uA	V_{IN} = 2.7V
MII TTL Outputs (RXD0-RXD3, RXDV, RXER, CRS, COL, MDIO)						
V_{OL}	Output Low Voltage	---	---	0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	2.4	---	---	V	I_{OH} = -4mA
Non-MII TTL Outputs (LINKLED#, SPEEDLED#, FDXLED#, MDINTR#)						
V_{OL}	Output Low Voltage	---	---	0.4	V	I_{OL} = 1mA
V_{OH}	Output High Voltage	2.4	---	---	V	I_{OH} = -0.1mA
Receiver						
V_{ICM}	RX+/RX- Common mode Input Voltage	---	0.9	---	V	100 Ω Termination Across
Transmitter						
V_{TD}100	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
V_{TD}10	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
I_{TD}100	100TX+/- Differential Output Current	• 19•	• 20•	• 21•	mA	
I_{TD}10	10TX+/- Differential Output Current	• 44•	• 50•	• 19•	mA	
V_{OH}	PECL Output Voltage – High	V_{CC}-1.05		V_{CC}-0.88	V	
V_{OL}	PECL Output Voltage – Low	V_{CC}-1.81		V_{CC}-1.62	V	
I_{FD}100	100FX+/- Differential Output Current	• 17•	• 18•	• 19•	mA	

AC Electrical Characteristics & Timing Waveforms

TP Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$t_{TR/F}$	100TX+/- Differential Rise/Fall Time	3.0	---	5.0	ns	
t_{TM}	100TX+/- Differential Rise/Fall Time Mismatch	0	---	0.5	ns	
t_{TDC}	100TX+/- Differential Output Duty Cycle Distortion	0	---	0.5	ns	
$t_{T/T}$	100TX+/- Differential Output Peak-to-Peak Jitter	0	---	1.4	ns	
XOST	100TX+/- Differential Voltage Overshoot	0	---	5	%	

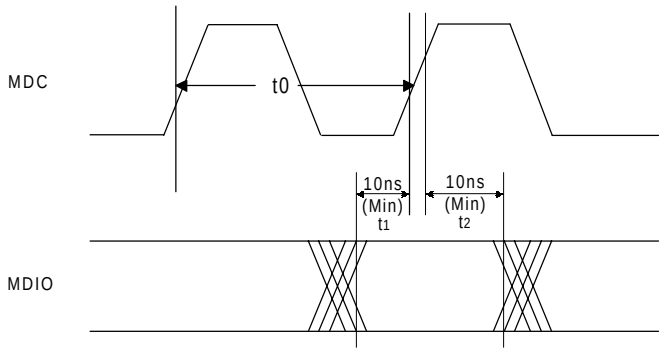
Oscillator/Crystal Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CKC}	OSC Cycle Time	39.998	40	40.002	ns	50ppm
t_{PWH}	OSC Pulse Width High	16	20	24	ns	
t_{PWL}	OSC Pulse Width Low	16	20	24	ns	

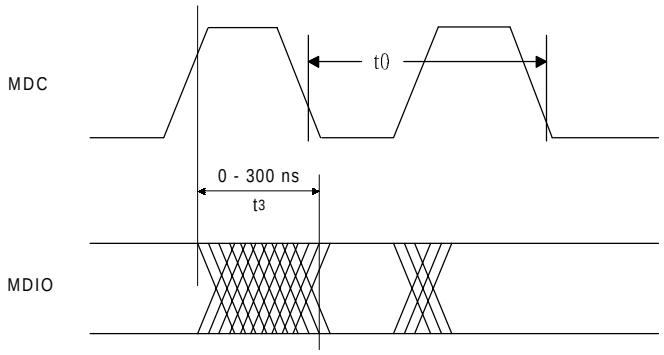
MDC/MDIO Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_0	MDC Cycle Time	80	---	---	ns	
t_1	MDIO Setup Before MDC	10	---	---	ns	When OUTPUT By STA
t_2	MDIO Hold After MDC	10	---	---	ns	When OUTPUT By STA
t_3	MDC To MDIO Output Delay	0	---	300	ns	When OUTPUT By DM9131

MDIO timing when OUTPUT by STA



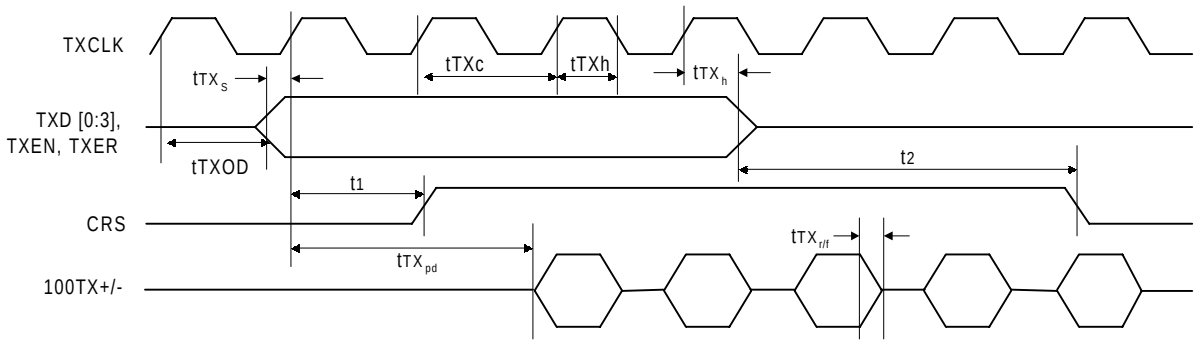
MDIO timing when OUTPUT by DM9131



100BASE-TX Transmit Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{TXc}	TXCLK Cycle Time	39.996	40	40.004	ns	
t_{TXh}, t_{TXl}	TXCLK High/Low Time	16	20	24	ns	
t_{TX_s}	TXD[0:3], TXEN, TXER Setup To TXCLK High	15	---	---	ns	
t_{TX_h}	TXD[0:3], TXEN, TXER Hold From TXCLK High	15	---	---	ns	
t_{TXOD}	TXCLK to Output Delay			25	ns	
t_1	TXEN Sampled To CRS Asserted	---	4	---	BT	
t_2	TXEN Sampled To CRS De-asserted	---	4	---	BT	
$t_{TX_{pd}}$	TXEN Sampled To TX+/- Out(Tx Latency)	---	8	---	BT	
$t_{TX_{r/f}}$	100TX Driver Rise/Fall Time	3	4	5	ns	90% To 10%, Into 100ohm Differential
1. Typical values are at 25℃and are for design aid only; not guaranteed and not subject to production testing.						

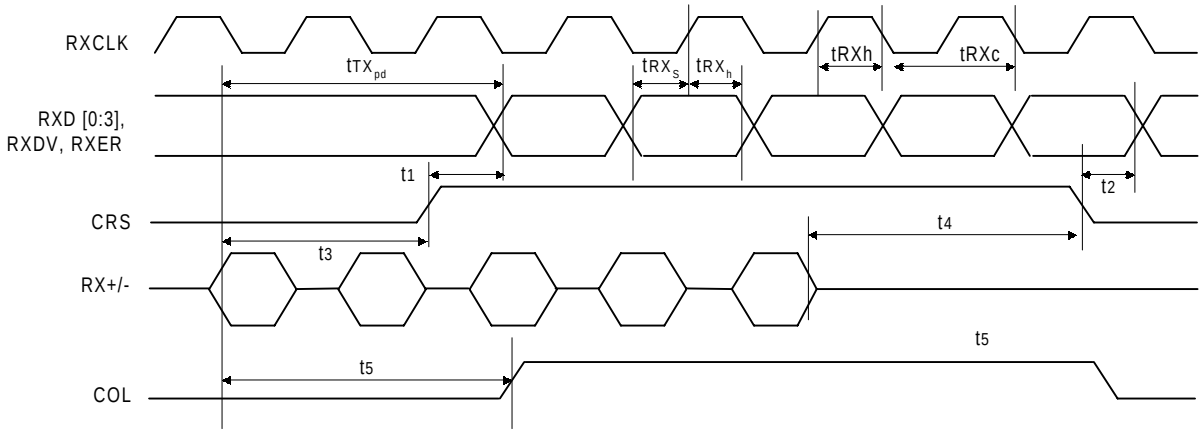
100BASE-TX Transmit Timing Diagram



100BASE-TX Receive Timing Parameter

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{RXc}	RXCLK Cycle Time	39.996	40	40.004		
t_{RXh}, t_{RXl}	RXCLK High/Low Time	16	20	24		
t_{RX_s}	RXD[0:3), RXDV, RXER Setup To RXCLK High	10	-	-	ns	
t_{RX_h}	RXD[0:3], RXDV, RXER Hold From RXCLK High	10	-	-	ns	
$t_{RX_{pd}}$	RX+/- In To RXD[0:3] Out (Rx Latency)	-	15	-	BT	
t_1	CRS Asserted To RXD[0:3], RXDV, RXER	-	4	-	BT	
t_2	CRS De-asserted To RXD[0:3], RXDV, RXER	-	0	-	BT	
t_3	RX+/- In To CRS Asserted	10	-	14	BT	
t_4	RX+/- Quiet To CRS De-asserted	14	-	18	BT	
t_5	RX+/- In To COL De-Asserted	14	-	18	BT	
1. Typical values are at 25℃and are for design aid only; not guaranteed and not subject to production testing.						

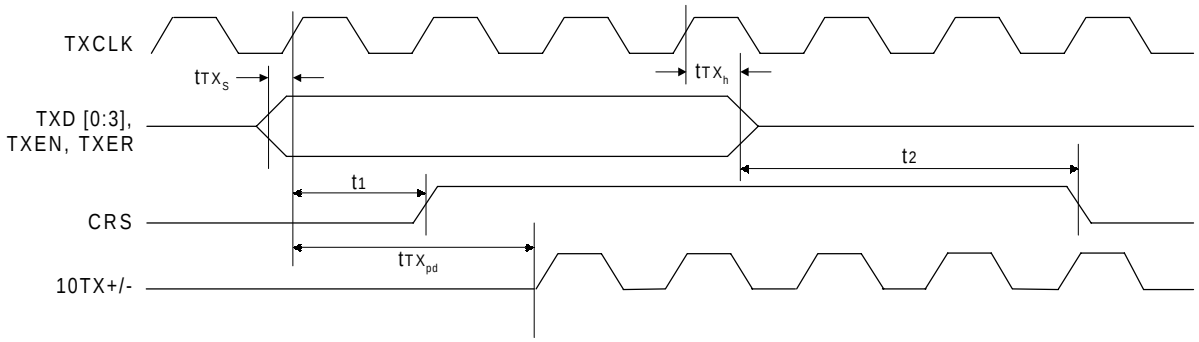
MII 100BASE-TX Receive Timing Diagram



MII 10BASE-T Nibble Transmit Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
TTX_S	TXD[0:3), TXEN, TXER Setup To TXCLK High	5	---	---	ns	
TTX_h	TXD[0:3], TXEN, TXER Hold From TXCLK High	5	---	---	ns	
t1	TXEN Sampled To CRS Asserted	---	2	4	BT	
t2	TXEN Sampled To CRS De-asserted	---	15	20	BT	
TTX_{pd}	TXEN Sampled To 10TXO Out (Tx Latency)	---	2	4	BT	

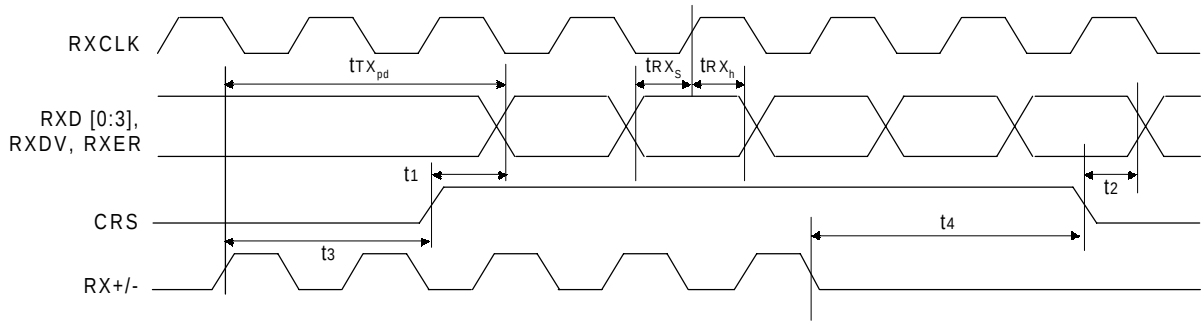
MII 10BASE-T Nibble Transmit Timing Diagram



MII 10BASE-T Receive Nibble Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tRX_s	RXD[0:3), RXDV, RXER Setup To RXCLK High	5	---	---	ns	
tRX_h	RXD[0:3], RXDV, RXER Hold From RXCLK High	5	---	---	ns	
tRX_{pd}	RXI In To RXD[0:3] Out (Rx Latency)	---	7	---	BT	
t1	CRS Asserted To RXD[0:3], RXDV, RXER	1	14	20	BT	
t2	CRS De-asserted To RXD[0:3], RXDV, RXER	---	---	3	BT	
t3	RXI In To CRS Asserted	1	2	4	BT	
t4	RXI Quiet To CRS De-asserted	1	10	15	BT	

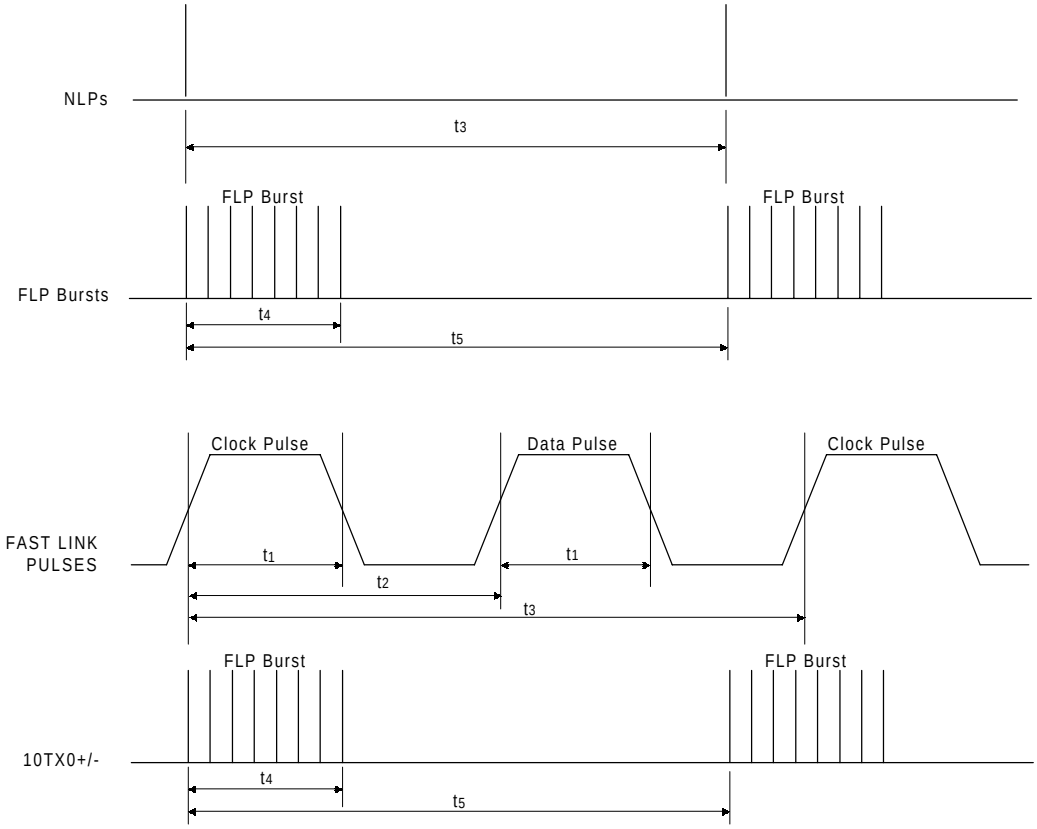
MII 10BASE-T Receive Nibble Timing Diagram



Auto-negotiation and Fast Link Pulse Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t1	Clock/Data Pulse Width	---	100	---	ns	
t2	Clock Pulse To Data Pulse Period	55.5	62.5	69.5	us	DATA = 1
t3	Clock Pulse To Clock Pulse Period	111	125	139	us	
t4	FLP Burst Width	-	2	-	ms	
t5	FLP Burst To FLP Burst Period	8		24	ms	
-	Clock/Data Pulses in a Burst	17		33	pulse	

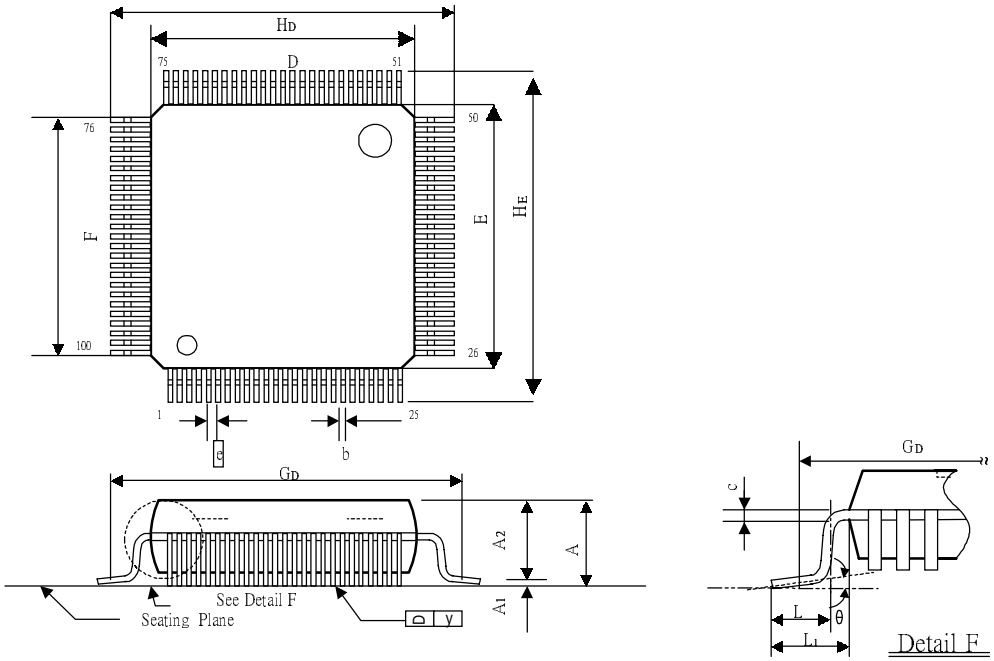
Auto-negotiation and Fast Link Pulse Timing Diagram



Package Information

LQFP 100L Outline Dimensions

Unit: Inches/mm



Symbol	Dimensions In Inches	Dimensions In mm
A	0.063 Max.	1.60 Max.
A_1	0.004 ± 0.002	0.1 ± 0.05
A_2	0.055 ± 0.002	1.40 ± 0.05
b	0.009 ± 0.002	0.22 ± 0.05
c	0.006 ± 0.002	0.15 ± 0.05
D	0.551 ± 0.005	14.00 ± 0.13
E	0.551 ± 0.005	14.00 ± 0.13
e	0.020 BSC.	0.50 BSC.
F	0.481 NOM.	12.22 NOM.
G_D	0.606 NOM.	15.40 NOM.
H_D	0.630 ± 0.006	16.00 ± 0.15
H_E	0.630 ± 0.006	16.00 ± 0.15
L	0.024 ± 0.006	0.60 ± 0.15
L_1	0.039 Ref.	1.00 Ref.
y	0.004 Max.	0.1 Max.
θ	0° ~ 12°	0° ~ 12°

Note: 1. Dimension D & E do not include resin fins.
2. Dimension GD is for PC Board surface mount pad pitch design reference only.
3. All dimensions are based on metric system.

Ordering Information

Part Number	Pin Count	Package
DM9131	100	LQFP

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DAVICOM Semiconductor, Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that re the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

Products

We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards.

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WARNING
Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.