3.3V Super I/O Controller with Infrared Support for Portable Applications

FEATURES

- PC 99 Compliant
- 3.3 Volt Operation (5V Tolerant)
- Intelligent Auto Power Management
- 16 Bit Address Qualification
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
  - Supports One Floppy Drive Directly
  - Configurable Open Drain/Push-Pull Output Drivers
  - Supports Vertical Recording Format
  - 16 Byte Data FIFO
  - 100% IBM Compatibility
  - Detects All Overrun and Underrun Conditions
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Power-Down Modes for Reduced Power Consumption
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - Swap Drives A and B
  - Non-Burst Mode DMA Option
  - 48 Base I/O Address, 15 IRQ and 4 DMA Options
  - Forceable Write Protect and Disk Change Controls
- Floppy Disk Available on Parallel Port Pins
  ACPI Compliant
- Enhanced Digital Data Separator
  - 2Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Serial Ports
  - Two High Speed NS16C550 Compatible UARTs with Send/Receive 16 Byte FIFOs
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
- Infrared Communications Controller
  - IrDA v1.1 (4Mbps), HPSIR, ASKIR, Consumer IR Support
  - 2 IR Ports
  - 96 Base I/O Address, 15 IRQ Options and 4 DMA Options
- Multi-Mode Parallel Port with ChiProtect
  - Standard Mode
  - IBM PC/XT, PC/AT, and PS/2 Compatible Bi-directional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible
  - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - Enhanced Capabilities Port (ECP) Compatible (IEEE 1284 Compliant)
  - Incorporates ChiProtect Circuitry for Protection Against Damage Due to Printer Power-On
  - 192 Base I/O Address, 15 IRQ and 4 DMA Options
- Game Port Select Logic
  - 48 Base I/O Addresses
- General Purpose Address Decoder
  - 16-Byte Block Decode

ORDERING INFORMATION

Order Number: FDC37N3869-MD
for 100 Pin TQFP Package

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GENERAL DESCRIPTION

The SMSC FDC37N3869 is a 3.3v PC 99-compliant Super I/O Controller with Infrared support. The FDC37N3869 utilizes SMSC's proven SuperCell technology and is optimized for motherboard applications. The FDC37N3869 incorporates SMSC's true CMOS 765B floppy disk controller, advanced digital data separator, 16-byte data FIFO, two 16C550 compatible UARTs, one Multi-Mode parallel port with ChiProtect circuitry plus EPP and ECP support, game port chip select logic and one floppy direct drive support. The FDC37N3869 does not require any external filter components, is easy to use and offers lower system cost and reduced board area. The FDC37N3869 is software and register compatible with SMSC's proprietary 82077AA core.

The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures and provides data overflow and underflow protection. The SMSC advanced digital data separator incorporates SMSC's patented data separator technology allowing for ease of testing and use. The FDC37N3869 supports both 1Mbps and 2Mbps data rates and vertical recording operation at 1Mbps Data Rate.

The FDC37N3869 also features a full 16-bit internally decoded address bus, a Serial IRQinterface with PCI nCLKRUN support, relocatable configuration ports and four DMA channel options.

Both on-chip UARTs are compatible with the NS16C550. One UART includes additional support for a Serial Infrared Interface that complies with IrDA v1.2 (Fast IR), HPSIR, and ASKIR formats (used by Sharp, Apple Newton, and other PDAs), as well as Consumer IR.

The parallel port and the game port select logic are compatible with IBM PC/AT architectures. The parallel port ChiProtect circuitry prevents damage caused by an attached powered printer when the FDC37N3869 is not powered.

The FDC37N3869 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes. The FDC37N3869 also features Software Configurable Logic (SCL) for ease of use. SCL allows programmable system configuration of key functions such as the FDC, parallel port, and UARTs.

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PIN CONFIGURATION

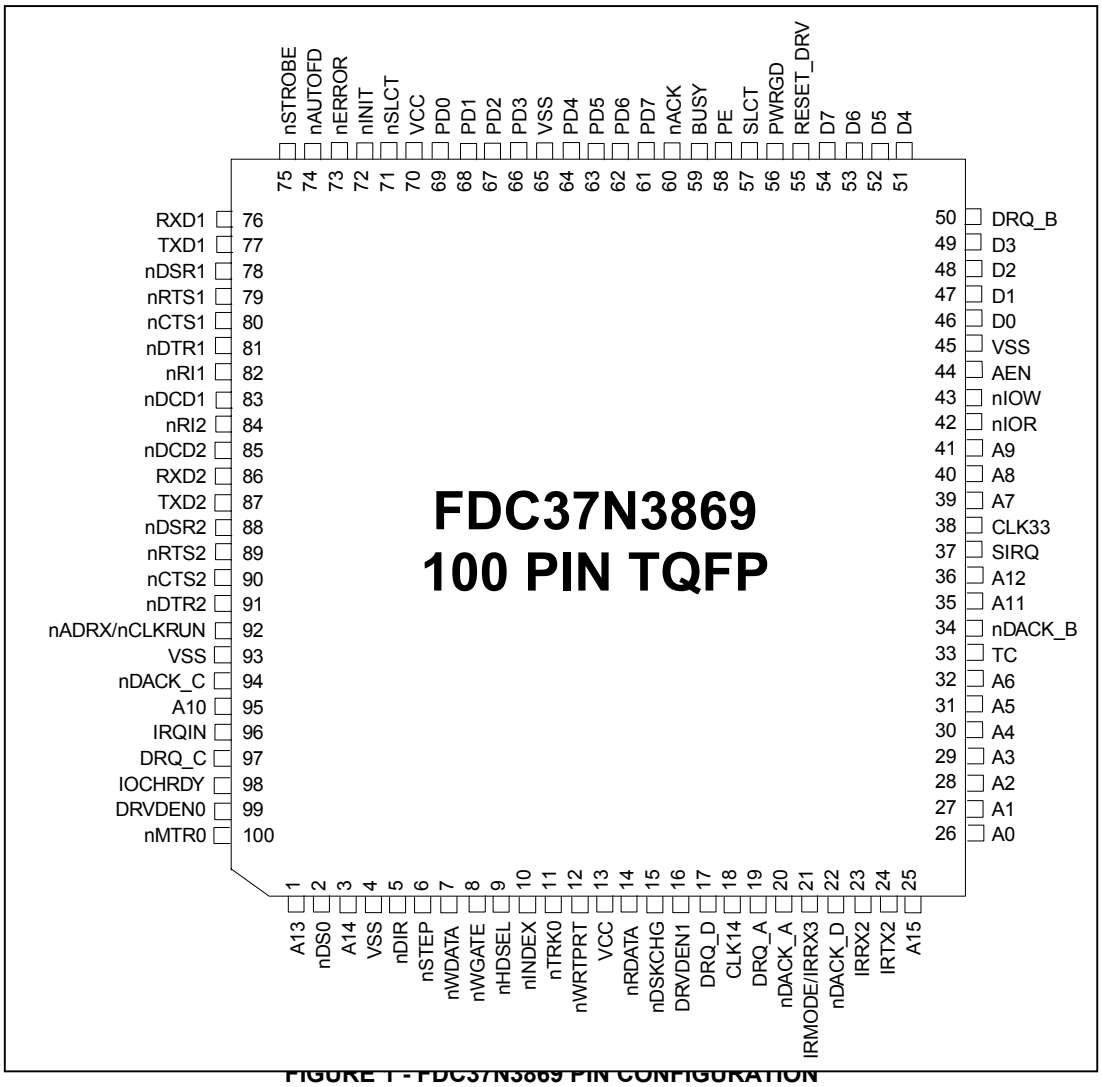


FIGURE 1 - FDC37N3869 PIN CONFIGURATION

PIN DESCRIPTION

Buffer Type Per Pin

Table 1 - Description Of Pin Functions

TQFP PIN #	NAME	SYMBOL	BUFFER MODE[6]	DESCRIPTION
HOST PROCESSOR INTERFACE				
46-49 51-54	Data Bus 0-7	D0-D7	IO12	The data bus connection used by the host microprocessor to transmit data to and from the chip. These pins are in a high-impedance state when not in the output mode.
42	nI/O Read	nIOR	IS	This active low signal is issued by the host microprocessor to indicate an I/O read operation.
43	nI/O Write	nIOW	IS	This active low signal is issued by the host microprocessor to indicate an I/O write operation.
44	Address Enable	AEN	IS	Active high Address Enable indicates DMA operations on the host data bus. Used internally to qualify appropriate address decodes.
26-32 39-41, 95,35, 36,1, 3,25	Address Bus	A0-A15	I	These host address bits determine the I/O address to be accessed during nIOR and nIOW cycles. These bits are latched internally by the leading edge of nIOR and nIOW. All internal address decodes use the full A0 to A15 address bits.
19,50, 97,17	DMA Request A, B, C, D	DRQ_A DRQ_B DRQ_C DRQ_D	O12	These active high outputs are the DMA request for byte transfers of data between the host and the chip. These signals are cleared on the last byte of the data transfer by the nDACK signal going low (or by nIOR going low if nDACK was already low as in demand mode).
20,34, 94,22	nDMA Acknowl-edge A, B, C, D	nDACK_A nDACK_B nDACK_C nDACK_D	IS	These are active low inputs acknowledging the request for a DMA transfer of data between the host and the chip. These inputs enable the DMA read or write internally.
33	Terminal Count	TC	IS	This signal indicates that DMA data transfer is complete. TC is only accepted when nDACK_x is low. In AT and PS/2 model 30 modes, TC is active high and in PS/2 mode, TC is active low.
37	Serial IRQ	SIRQ	IO12	Serial IRQ pin used with the CLK33 pin to transfer FDC37N3869 interrupts to the host.
38	PCI Clock	CLK33	ICLK	33MHz PCI clock input, used with the SIRQ and the nCLKRUN pins to serially transfer FDC37N3869 interrupts to the host.
55	Reset	RESET_ DRV	IS	This active high signal resets the chip and must be valid for 500ns minimum. The effect on the internal registers is described in the appropriate section. The configuration registers are not affected by this reset.
98	I/O Channel Ready (Note[4])	IOCHRDY	OD12	This pin is pulled low to extend the read/write command. IOCHRDY can used by the IRCC and by the Parallel Port in EPP mode.
FLOPPY DISK INTERFACE				
14	nRead Disk Data	nRDATA	IS	Raw serial bit stream from the disk drive, low active. Each falling edge represents a flux transition of the encoded data.

TQFP PIN #	NAME	SYMBOL	BUFFER MODE[6]	DESCRIPTION
8	nWrite Gate	nWGATE	(O12/ OD12)	This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette.
7	nWrite Data	nWDATA	(O12/ OD12)	This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media.
9	nHead Select	nHDSEL	(O12/ OD12)	This high current output selects the floppy disk side for reading or writing. A logic “1” on this pin means side 0 will be accessed, while a logic “0” means side 1 will be accessed.
5	Direction Control	nDIR	(O12/ OD12)	This high current low active output determines the direction of the head movement. A logic “1” on this pin means outward motion, while a logic “0” means inward motion.
6	nStep Pulse	nSTEP	(O12/ OD12)	This active low high current driver issues a low pulse for each track-to-track movement of the head.
15	Disk Change	nDSKCHG	IS	This input senses that the drive door is open or that the diskette has possibly been changed since the last drive selection. This input is inverted and read via bit 7 of I/O address 3F7H. The nDSKCHG bit also depends upon the state of the Force Disk Change bits in the Force FDD Status Change configuration register (see section **CR17** on page 107).
2	nDrive Select 0	nDS0	(O12/ OD12)	Active low output selects drive 0.
100	nMotor On 0	nMTR0	(O12/ OD12)	These active low output selects motor drive 0.
99	Drive Density 0	DRVDEN0	(O12/ OD12)	Indicates the drive and media selected. Refer to configuration registers CR03, CR0B, CR1F.
12	nWrite Protected	nWRTPRT	IS	This active low Schmitt Trigger input senses from the disk drive that a disk is write protected. Any write command is ignored. The nWRPRT bit also depends upon the state of the Force Write Protect bit in the Force FDD Status Change configuration register (see section **CR17** on page 107).
11	wTrack 00	nTRK0	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.
10	nIndex	nINDEX	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
16	Drive Density 1	DRVDEN 1	(O12/ OD12)	Indicates the drive and media selected. Refer to configuration registers CR03, CR0B, CR1F.
SERIAL PORTS INTERFACE				
86	Receive Data 2	RXD2	IS	Receiver serial data input for port 2. IR Receive Data
87	Transmit Data 2 (Note[5])	TXD2	O12PD	Transmit serial data output for port 2. IR transmit data.
76	Receive Data 1	RXD1	I	Receiver serial data input for port 1.
77	Transmit Data 1	TXD1	O12	Transmit serial data output for port 1.

TQFP PIN #	NAME	SYMBOL	BUFFER MODE[6]	DESCRIPTION
79,89	nRequest to Send (System Option)	nRTS1 nRTS2 (SYSOPT)	O6	Active low Request to Send outputs for the Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of the Modem Control Register (MCR). The hardware reset will reset the nRTS signal to inactive mode (high). nRTS is forced inactive during loop mode operation. At the trailing edge of hardware reset the nRTS2 inputs is latched to determine the configuration base address: 0 = INDEX Base I/O Address 3F0 Hex; 1 = INDEX Base I/O Address 370 Hex.
81,91	nData Terminal Ready	nDTR1 nDTR2	O6	Active low Data Terminal Ready outputs for the serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the nDTR signal to inactive mode (high). nDTR is forced inactive during loop mode operation.
80,90	nClear to Send	nCTS1 nCTS2	I	Active low Clear to Send inputs for the serial port. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of nCTS signal by reading bit 4 of Modem Status Register (MSR). A nCTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when nCTS changes state. The nCTS signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of nCTS.
78,88	nData Set Ready	nDSR1 nDSR2	I	Active low Data Set Ready inputs for the serial port. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of nDSR signal by reading bit 5 of Modem Status Register (MSR). A nDSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nDSR changes state. Note: Bit 5 of MSR is the complement of nDSR.
83,85	nData Carrier Detect	nDCD1 nDCD2	I	Active low Data Carrier Detect inputs for the serial port. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of nDCD signal by reading bit 7 of Modem Status Register (MSR). A nDCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nDCD changes state. Note: Bit 7 of MSR is the complement of nDCD.

TQFP PIN #	NAME	SYMBOL	BUFFER MODE[6]	DESCRIPTION
82,84	nRing Indicator	nRI1 nRI2	I (Note[1])	Active low Ring Indicator inputs for the serial port. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of nRI signal by reading bit 6 of Modem Status Register (MSR). A nRI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nRI changes state. Note: Bit 6 of MSR is the complement of nRI.

TQFP PIN #	NAME	SYMBOL	BUFFER MODE[6]	DESCRIPTION
PARALLEL PORT INTERFACE (NOTE 2)				
71	nPrinter Select Input/FDC nStep Pulse (Note[3])	nSLCT nSTEP	(OD14/OP14)/OD12	This active low output selects the printer. This is the complement of bit 3 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
72	nInitiate Output/ FDC nDirection Control (Note[3])	nINIT nDIR	(OD14/OP14)/OD12	This output is bit 2 of the printer control register. This is used to initiate the printer when low. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
74	nAutofeed Output/ FDC nDensity Select (Note[3])	nAUTOFD nDENSEL	(OD14/OP14)/OD12	This output goes low to cause the printer to automatically feed one line after each line is printed. The nAUTOFD output is the complement of bit 1 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
75	nStrobe Output/ FDC nDrive Select 0 (Note[3])	nSTROBE nDS0	(OD14/OP14)/OD12	An active low pulse on this output is used to strobe the printer data into the printer. The nSTROBE output is the complement of bit 0 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
59	Busy/ FDC nMotor On 1	BUSY nMTR1	I/OD12	This is a status output from the printer, a high indicating that the printer is not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.

TQFP PIN #	NAME	SYMBOL	BUFFER MODE[6]	DESCRIPTION
60	nAcknowl-edge/FDC nDrive Select 1	nACK nDS1	I/OD12	A low active output from the printer indicating that it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the nACK input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
58	Paper End/ FDC nWrite Data	PE nWRDATA	I/OD12	Another status output from the printer, a high indicating that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
57	Printer Selected Status/ FDC nWrite Gate	SLCT nWGATE	I/OD12	This high active output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
73	nError/FDC nHead Select	nERROR nHDSEL	I/OD12	A low on this input from the printer indicates that there is a error condition at the printer. Bit 3 of the Printer Status register reads the nERR input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
69	Port Data 0/FDC nIndex	PD0 nINDEX	IOP14/IS	Port Data 0 See FDC Pin definition.
68	Port Data 1/FDC nTrack 0	PD1 nTRK0	IOP14/IS	Port Data 1 See FDC Pin definition.
67	Port Data 2/FDC nWrite Protected	PD2 nWRTPRT	IOP14/IS	Port Data 2 See FDC Pin definition.
66	Port Data 3/FDC nRead Disk Data	PD3 nRDATA	IOP14/IS	Port Data 3 See FDC Pin definition.
64	Port Data 4/FDC nDisk Change	PD4 nDSKCHG	IOP14/IS	Port Data 4 See FDC Pin definition.
63	Port Data 5	PD5	IOP14	Port Data 5
62	Port Data 6/FDC nMotor On 0	PD6 nMTR0	IOP14/ OD12	Port Data 6 See FDC Pin definition.
61	Port Data 7	PD7	IOP14	Port Data 7

TQFP PIN #	NAME	SYMBOL	BUFFER MODE[6]	DESCRIPTION
ALTERNATE IR PINS/MISC				
18	14.318 MHz Input Clock	CLK14	ICLK	The external connection to a single source 14.318 MHz clock.
23	IR Receive 2	IRRX2	IS	IR Receive input
24	IR Transmit 2 (Note[5])	IRTX2	O12PD	IR transmit output
92	Address X/ PCI Clock Controller	nADRX/ nCLKRUN	OD12/ IOD12	The active-low address decoder output nADRX can be asserted on 1, 8, or 16-byte address boundaries (an external pull-up is required). Refer to configuration registers CR03, CR08, and CR09 for more information. nCLKRUN is used to indicate the PCI clock status and to request that a stopped clock be started.
21	IR Mode/ IR Receive 3	IRMODE/ IRRX3	O6/IS	IR mode IR Receive 3
56	Power Good/ nGame Port Chip Select	PWRGD nGAMECS	I/O4	This active high input indicates that the power (VCC) is valid. For device operation PWRGD must be active. When PWRGD is inactive, all inputs are disconnected and put into a low power mode; all outputs are put into high impedance. The contents of all registers are preserved as long as VCC is valid. The output driver current drain when PWRGD is inactive mode drops to I_{STBY} - standby current. This is the Game Port Chip Select output - active low. It will go active when the I/O address, qualified by AEN, matches that selected in Configuration register CR1E.
96	External Interrupt Input	IRQIN	IS	This pin is used to steer an interrupt signal from an external device onto one of 15 IRQs.
POWER INTERFACE				
13,70	Power	VCC		Positive Supply Voltage. (3.3V)
4,45, 65,93	Ground	VSS		Ground Supply.

Note 1: nRI and the UART interrupts are active when PWRGD is active and the UARTS are either fully powered or in AUTOPOWER DOWN mode.

Note 2: The FDD output pins multiplexed in the PARALLEL PORT INTERFACE are OD drivers only and are not affected by the FDD Output Driver Controls (see section CR05 on page 102).

Note 3: Active (push-pull) output drivers are required on these pins in the enhanced parallel port modes.

Note 4: An external pull-up must be provided for IOCHRDY.

Note 5: The pull-down on this pin is always active including when the output driver is tristated and regardless of the state of PWRGD.

Note 6: Buffer Modes describe the pad driver properties per function. Buffer Modes on multiplexed pins are separated by a slash "/". For example, the Buffer Modes for a multiplexed pin with two functions where the primary function is an input and the secondary function is an 8mA bidirectional driver is "I/IO8". Buffer Modes in parenthesis represent multiple Buffer Modes for a single pin function.

Buffer Type Summary

Table 2 below describes the buffer types shown in Table 1. All values are specified at V_{cc} = +3.3v, ±10%

Table 2 - FDC37N3869 Buffer Type Summary (See Note)

BUFFER TYPE	DESCRIPTION
IO12	Input/Output. 12mA sink; 6mA source
O12	Output. 12mA sink; 6mA source
O12PD	Output. 12mA sink; 6mA source with 30µa pull-down
OD12	Open Drain. 12mA sink
O6	Output. 6mA sink; 3mA source
OD14	Open Drain. 14mA sink
OP14	Output. 14mA sink; 14mA source. Backdrive Protected
IOP14	Input/Output. 14mA sink; 14mA source. Backdrive Protected
O4	Output. 4mA sink; 2mA source
ICLK	Input to Crystal Oscillator Circuit (TTL levels)
I	Input TTL Compatible
IS	Input with Schmitt Trigger
IOD12	Input/Open Drain Output. 12mA sink

Note: These are minimum ratings guaranteed at 3.3V.

Output Drivers

Active output drivers in the FDC37N3869 will always achieve the minimum specified DC Electrical Characteristics shown in Table 120.

Note: If there is a pull-up on an external node driven by an active output driver the FDC37N3869 may sink current from the pull-up through the low impedance source.

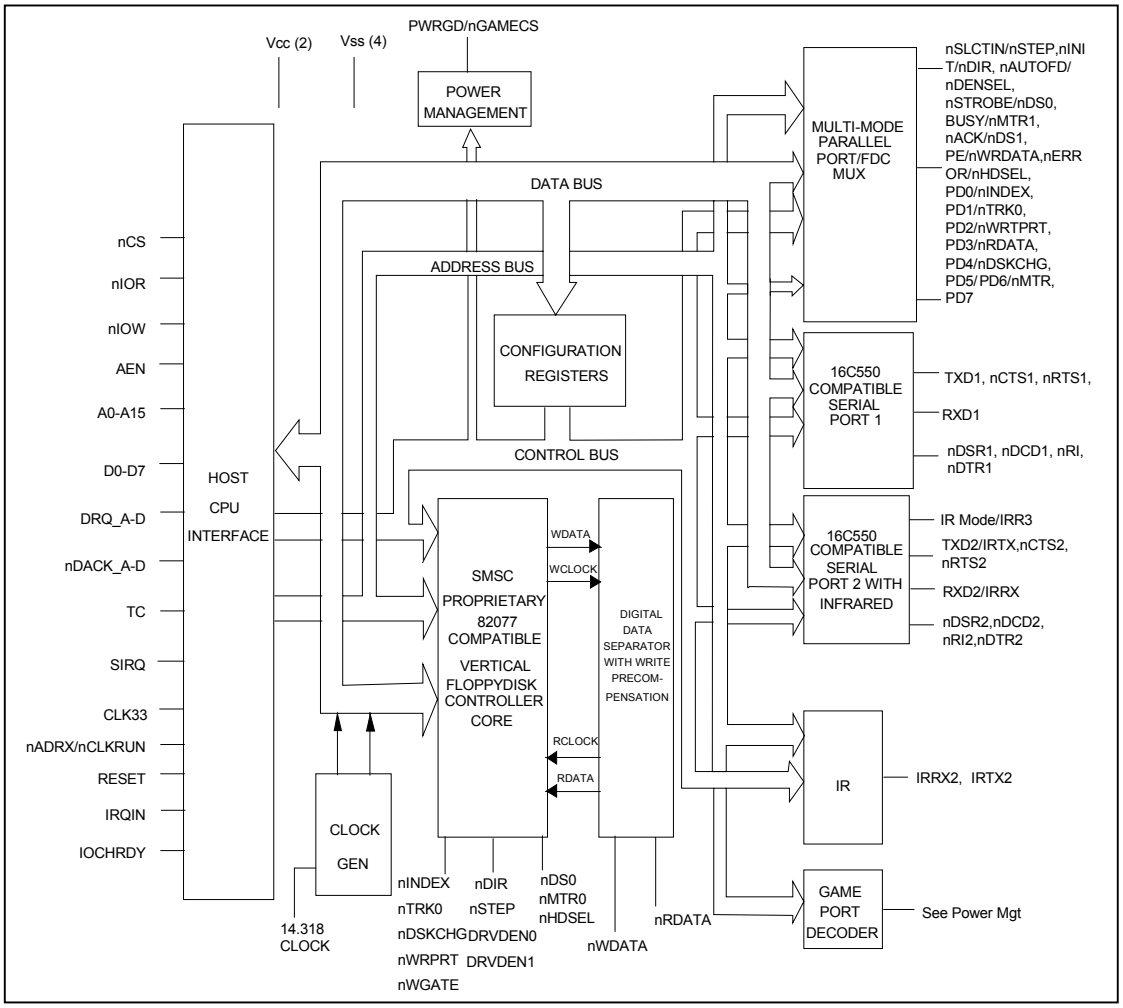


FIGURE 2 - FDC37N3869 BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

Super I/O Registers

Table 3 shows the addresses of the various device blocks of the Super I/O immediately after power up. The base addresses must be set in the configuration registers before accessing these devices. The base addresses of the FDC, Serial and Parallel Ports can be moved via the configuration registers.

Host Processor Interface

The host processor communicates with the FDC37N3869 using the Super I/O registers. Register access is accomplished through programmed I/O or DMA transfers. All registers are 8 bits wide. All host interface output buffers are capable of sinking a minimum of 12 mA.

Table 3 - FDC37N3869 Block Addresses

ADDRESS	BLOCK NAME	NOTES
3F0, 3F1 or 370, 371	Configuration	Write only; Note 1
Base +[0:7]	Floppy Disk	Disabled at power up; Note 2
Base +[0:7]	Serial Port Com 1	Disabled at power up; Note 2
Base1 +[0:7] Base2 +[0:7]	Serial Port Com 2	Disabled at power up; Note 2
Base +[0:3] all modes Base +[4:7] for EPP Base +[400:403] for ECP	Parallel Port	Disabled at power up; Note 2

Note 1: Configuration registers can only be modified in the configuration state, refer to section CONFIGURATION on page 96 for more information. All logical blocks in the FDC37N3869 can operate normally in the Configuration State.
Note 2: The base addresses must be set in the configuration registers before accessing device blocks.

FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC37N3869 is compatible with the 82077AA using SMSC's proprietary floppy disk controller core. For information about the floppy disk on the Parallel Port pins refer to section Parallel Port Floppy Disk Controller on page 54.

Modes Of Operation

The FDC37N3869 Floppy Disk Controller has two *Floppy* modes and three *Interface* modes. Each of the three Interface modes are available in each of the two Floppy modes.

FLOPPY MODES

The Floppy modes are used to select alternate configurations for the Tape Drive register. The active Floppy mode is determined by the *Enhanced Floppy Mode 2* bit in Configuration Register 3 (see section **CR03** on page 100). When the *Enhanced Floppy Mode 2* bit is 0 *Normal* Floppy mode is selected, otherwise *Enhanced Floppy Mode 2* (OS/2 mode) is selected. See section **TAPE DRIVE REGISTER (TDR)** on page 24 for the affects of the *Enhanced Floppy Mode 2* bit on the Tape Drive register.

INTERFACE MODES

The Interface modes are determined by the *MFM* and *IDENT* configuration bits in Configuration Register 3 (see section **CR03** on page 100).

PC/AT Interface Mode

When both IDENT and MFM are high the PC/AT register set is enabled, the DMA enable bit of the Digital Output Register becomes valid, FINTR and DRQ can be hi-Z, and TC and DENSEL become active high.

PS/2 Interface Mode

When IDENT is low and MFM is high PS/2 Interface mode is selected. This mode supports the PS/2 models 50/60/80 configuration and register set. The DMA bit of the Digital Output Register becomes a "don't care," FINTR and DRQ are always valid, TC and DENSEL become active low.

Model 30 Interface Mode

When both IDENT and MFM are low Model 30 Interface Mode is selected. This mode supports PS/2 Model 30 configuration and register set. The DMA enable bit of the Digital Output Register becomes valid, FINTR and DRQ can be hi-Z, TC is active high and DENSEL is active low.

Floppy Disk Controller Internal Registers

The Floppy Disk Controller contains eight internal registers that provide the interface between the host microprocessor and the floppy disk drives. Table 4 shows the addresses required to access these registers. Registers other than the ones shown are not supported.

Table 4 - Status, Data and Control Registers

BASE I/O ADDRESS		REGISTER	
+0	R	Status Register A	SRA
+1	R	Status Register B	SRB
+2	R/W	Digital Output Register	DOR
+3	R/W	Tape Drive Register	TDR
+4	R	Main Status Register	MSR
+4	W	Data Rate Select Register	DSR
+5	R/W	Data (FIFO)	FIFO
+6		Reserved	
+7	R	Digital Input Register	DIR
+7	W	Configuration Control Register	CCR

STATUS REGISTER A (SRA)

Status Register A (Base Address + 0) monitors the state of the FINTR pin and several disk interface pins in PS/2 interface mode (Table 5) and Model 30 interface mode (Table 6). SRA is read-only and can be accessed at any time when in these modes. During a read in the PC/AT interface mode the data bus pins D0 - D7 are held in a high impedance state.

PS/2 Interface Mode

Table 5 - SRA PS/2 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	nDRV2	STEP	nTRK0	HDSEL	nINDX	nWP	DIR
RESET CONDITION	0	1	0	N/A	0	N/A	N/A	0

Direction, Bit 0
Active high status indicating the direction of head movement. A logic "1" indicating inward direction, a logic "0" outward.

nWRITE PROTECT, Bit 1
Active low status of the WRITE PROTECT disk interface input. A logic "0" indicating that the disk is write protected. The nWRITE PROTECT bit also depends upon the state of the Force Write Protect bits in the Force FDD Status Change configuration register (see section CR17).

nINDEX, Bit 2
Active low status of the INDEX disk interface input.

Head Select, Bit 3
Active high status of the HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

nTRACK 0, Bit 4
Active low status of the TRK0 disk interface input.

Step, Bit 5
Active high status of the STEP output disk interface output pin.

nDRV2, Bit 6
The nDRV2 bit is always "1".

Interrupt Pending, Bit 7
Active high bit indicating the state of the Floppy Disk Interrupt output.

PS/2 Model 30 Interface Mode

Table 6 - SRA PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	DRQ	STEP F/F	TRK0	nHDSEL	INDX	WP	nDIR
RESET CONDITION	0	0	0	N/A	1	N/A	N/A	1

nDIRECTION, Bit 0
Active low status indicating the direction of head movement. A logic “0” indicating inward direction a logic “1” outward.

Write Protect, Bit 1
Active high status of the WRITE PROTECT disk interface input. A logic “1” indicating that the disk is write protected. The nWRITE PROTECT bit also depends upon the state of the Force Write Protect bits in the Force FDD Status Change configuration register (see section CR17 on page 109).

Index, Bit 2
Active high status of the INDEX disk interface input.

nHEAD SELECT, Bit 3
Active low status of the HDSEL disk interface input. A logic “0” selects side 1 and a logic “1” selects side 0.

Track, Bit 4
Active high status of the TRK0 disk interface input.

Step, Bit 5
Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

DMA Request, Bit 6
Active high status of the DRQ output pin. Interrupt Pending, Bit 7 Active high bit indicating the state of the Floppy Disk Interrupt output.

STATUS REGISTER B (SRB)

Status Register B (Base Address + 1) is read-only and monitors the state of several disk interface pins in PS/2 interface mode (Table 7) and Model 30 interface mode (Table 8). SRB can be accessed at any time when in these modes. During a read in PC/AT interface mode the data bus pins D0 - D7 are held in a high impedance state.

PS/2 Interface Mode

Table 7 - SRB PS/2 Mode

	7	6	5	4	3	2	1	0
	1	1	DRIVE SEL0	WDATA TOGGLE	RDATA TOGGLE	WGATE	MOT EN1	MOT EN0
RESET CONDITION	1	1	0	0	0	0	0	0

Motor Enable 0, Bit 0
Active high status of the MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

Motor Enable 1, Bit 1
Active high status of the MTR1 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

Write Gate, Bit 2
Active high status of the WGATE disk interface output.

Read Data Toggle, Bit 3
Every inactive edge of the RDATA input causes this bit to change state.

Write Data Toggle, Bit 4
Every inactive edge of the WDATA input causes this bit to change state.

Drive Select 0, Bit 5
Reflects the status of the Drive Select 0 bit of the DOR (address 3F2 bit 0). This bit is cleared after a hardware reset, it is unaffected by a software reset.

Reserved, Bits 6 - 7
Always read as a logic “1”.

PS/2 Model 30 Interface Mode

Table 8 - SRB PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	nDRV2	nDS1	nDS0	WDATA F/F	RDATA F/F	WGATE F/F	nDS3	nDS2
RESET CONDITION	N/A	1	1	0	0	0	1	1

nDRIVE SELECT 2, Bit 0
Active low status of the DS2 disk interface output.

nDRIVE SELECT 3, Bit 1
Active low status of the DS3 disk interface output.

Write Gate, Bit 2
Active high status of the latched WGATE output signal. This bit is latched by the active going edge of WGATE and is cleared by the read of the DIR register.

Read Data, Bit 3
Active high status of the latched RDATA output signal. This bit is latched by the inactive going edge of RDATA and is cleared by the read of the DIR register.

Write Data, Bit 4
Active high status of the latched WDATA output signal. This bit is latched by the inactive going edge of WDATA and is cleared by the read of the DIR register. This bit is not gated with WGATE.

nDRIVE SELECT 0, Bit 5
Active low status of the DS0 disk interface output.

nDRIVE SELECT 1, Bit 6
Active low status of the DS1 disk interface output.

nDRV2, Bit 7
The nDRV2 bit is always “1”.

DIGITAL OUTPUT REGISTER (DOR)

The Digital Output register (Base Address + 2) controls the drive select and motor enables of the disk interface outputs (Table 9 and Table 10). The DOR also contains the DMA logic enable and a software reset bit. The DOR is read/write and unaffected by a software reset.

Table 9 - Digital Output Register

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET CONDITION	0	0	0	0	0	0	0	0

DOR Bit Descriptions

DRIVE SELECT, Bits 0 - 1

These two bits are binary encoded for the four drive selects DS0-DS3, there by allowing only one drive to be selected at one time.

nRESET, Bit 2

A logic “0” written to this bit resets the Floppy disk controller. This reset will remain active until a logic “1” is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

DMAEN, Bit 3

PC/AT and Model 30 Interface Mode

In PC/AT and Model 30 mode writing this bit to logic “1” will enable the DRQ, nDACK, TC and FINTR outputs. This bit being a logic “0” will disable the nDACK and TC inputs, and hold the DRQ and FINTR outputs in a high impedance state. In PC/AT and Model 30 mode the DMAEN bit is a logic “0” after a reset.

PS/2 Interface Mode

In PS/2 mode the DRQ, nDACK, TC and FINTR pins are always enabled. During a reset the DRQ, nDACK, TC, and FINTR pins will remain enabled, but the DMAEN bit will be cleared to a logic “0”.

MOTOR ENABLE 0, Bit 4

This bit controls the MTR0 disk interface output. A logic “1” in this bit will cause the output pin to go active.

MOTOR ENABLE 1, Bit 5

This bit controls the MTR1 disk interface output. A logic “1” in this bit will cause the output pin to go active.

MOTOR ENABLE 2, Bit 6

The MOTOR ENABLE 2 bit controls the MTR2 disk interface output. A logic “1” in this bit will cause the output pin to go active.

MOTOR ENABLE 3, Bit 7

The MOTOR ENABLE 3 bit controls the MTR3 disk interface output. A logic “1” in this bit causes the output to go active.

Table 10 - Drive Activation Values

DRIVE	DOR VALUE
0	1CH
1	2DH
2	4EH
3	8FH

Table 11 - Internal 2 Drive Decode: Drives 0 and 1

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)			MOTOR ON OUTPUTS (ACTIVE LOW)		
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0		nDS1	nDS0		nMTR1	nMTR0
X	X	X	1	0	0		1	0		nBIT 5	nBIT 4
X	X	1	X	0	1		0	1		nBIT 5	nBIT 4
X	1	X	X	1	0		1	1		nBIT 5	nBIT 4
1	X	X	X	1	1		1	1		nBIT 5	nBIT 4
0	0	0	0	X	X		1	1		nBIT 5	nBIT 4

TAPE DRIVE REGISTER (TDR)

The Tape Drive register (Base Address + 3) is included for 82077 software compatibility and allows the user to assign tape support to a particular drive during initialization. Any future reference to that drive automatically invokes tape support. The Tape Select bits TDR.[1:0] determine the tape drive number. Table 12 illustrates the Tape Select bit encoding. Note that drive 0 is the boot device and cannot be assigned tape support.

The encoding of the TDR depends on the Floppy mode (see section **Floppy Modes** on page 17). The TDR is unaffected by a software reset.

Table 12 - Tape Select Bits

TAPE SEL1 (TDR.1)	TAPE SEL0 (TDR.0)	DRIVE SELECTED
0	0	NONE
0	1	1
1	0	2
1	1	3

Normal Floppy Mode

In *Normal* mode the TDR contains only bits 0 and 1 (Table 13). During a read in Normal mode TDR bits 2 - 7 are high impedance. The Tape Select Bits are Read/Write.

Table 13 - TDR Normal Floppy Mode

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
TDR	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tape Sel1	Tape Sel0

Enhanced Floppy Mode 2 (OS2)

The configuration of the TDR in the Enhanced Floppy Mode 2 (OS/2 mode) is shown in Table 14.

Table 14 - TDR Enhanced Floppy Mode 2

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
TDR	Reserved		Drive Type ID		Floppy Boot Drive		Tape Sel1	Tape Sel0

Reserved, Bits 6 - 7

Bits 6 and 7 are *RESERVED*. Reserved bits cannot be written and return 0 when read.

Drive Type ID, Bits 4 - 5
The Drive Type ID bits depend on the last drive selected in the Digital Output Register and the Drive Type IDs that are programmed in configuration register 6 (Table 15).

Table 15 - Drive Type ID

DIGITAL OUTPUT REGISTER		TDR - DRIVE TYPE ID	
Bit 1	Bit 0	Bit 5	Bit 4
0	0	CR6 - Bit 1	CR6 - Bit 0
0	1	CR6 - Bit 3	CR6 - Bit 2
1	0	CR6 - Bit 5	CR6 - Bit 4
1	1	CR6 - Bit 7	CR6 - Bit 6

Floppy Boot Drive, Bits 2 - 3
The Floppy Boot Drive bits come from Configuration Register 7: TDR Bit 3 = CR7 Bit 1; TDR Bit 2 = CR7 Bit 0.

Tape Drive Select, Bits 0 - 1
The Tape Drive Select bits are the same as in *Normal* mode. These bits are Read/Write.

MAIN STATUS REGISTER (MSR)

The Main Status Register (Base Address + 4: Read-only) indicates the status of the disk controller (Table 16). The Main Status Register is valid in all modes and can be read at any time. The MSR indicates when the disk controller is ready to receive data via the Data Register. It should be read before transferring each byte to or from the data register, except in DMA mode. No delay is required when reading the MSR after a data transfer.

Table 16 - Main Status Register

	7	6	5	4	3	2	1	0
MSR	RQM	DIO	NON DMA	CMD BUSY	DRV3 BUSY	DRV2 BUSY	DRV1 BUSY	DRV0 BUSY

DRVx Busy, Bits 0 - 3
These bits are set to a “1” when a drive is in the seek portion of a command, including implied and overlapped seeks and recalibrates.

Command Busy, Bit 4
This bit is set to a “1” when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (Seek, Recalibrate commands), this bit is returned to a “0” after the last command byte.

Non-DMA, Bit 5
This mode is selected in the SPECIFY command and will be set to a “1” during the execution phase of a command. This is for polled data transfers and helps to differentiate between the data transfer phase and the reading of result bytes.

DIO, Bit 6
Indicates the direction of a data transfer once an RQM is set. A “1” indicates a read and a “0” indicates a write is required.

RQM, Bit 7
Indicates that the host can transfer data if set to a “1”. No access is permitted if set to a “0”.

DATA RATE SELECT REGISTER (DSR)

The Data Rate Select Register (Base Address + 4: Write-only) is used to program the data rate, amount of write precompensation, power down status, and software reset (Table 17). Note: the data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and PS/2 Model 30 and Microchannel applications. Other applications can set the data rate in the DSR. The data rate of the floppy controller is the most recent write of either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and 250 Kbps.

Table 17 - Data Rate Select Register

	7	6	5	4	3	2	1	0
	S/W RESET	POWER DOWN	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
RESET CONDITION	0	0	0	0	0	0	1	0

Data Rate Select, Bits 0 - 1

These bits control the data rate of the floppy controller. See Table 19 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset and are set to 250 Kbps after a hardware reset.

Precompensation Select, Bits 2 - 4

These three bits select the value of write precompensation that will be applied to the WDATA output signal.
Table 18 shows the precompensation values for the combination of these bits settings. Track 0 is the default starting track number to start precompensation. The starting track number can be changed using the Configure command.

Undefined, Bit 5

Should be written as a logic “0”.

Low Power, Bit 6

A logic “1” written to this bit will put the floppy controller into Manual Low Power mode. The floppy controller clock and data separator circuits will be turned off. The controller will come out of manual low power mode after a software reset or following access to the Data Register or Main Status Register.

Software Reset, Bit 7

This active high bit has the same function as the DOR RESET (DOR bit 2) except that this bit is self clearing.

Table 18 - Precompensation Delays

PRECOMP SELECT			PRECOMPENSATION DELAY
4	**3**	**2**	
1	1	1	0.00 ns-DISABLED
0	0	1	41.67 ns
0	1	0	83.34 ns
0	1	1	125.00 ns
1	0	0	166.67 ns
1	0	1	208.33 ns
1	1	0	250.00 ns
0	0	0	Default (see Table 21)

Table 19 - Data Rates

DRIVE RATE SELECT (CR0B)		DATA RATE SELECT (DSR)		DATA RATE		DENSEL (Note 1)		DRATE	
DRT1	**DRT0**	**SEL1**	**SEL0**	**MFM**	**FM**	**IDENT=1**	**IDENT=0**	**1**	**0**
0	0	1	1	1Meg	---	1	0	1	1
0	0	0	0	500	250	1	0	0	0
0	0	0	1	300	150	0	1	0	1
0	0	1	0	250	125	0	1	1	0
0	1	1	1	1Meg	---	1	0	1	1
0	1	0	0	500	250	1	0	0	0
0	1	0	1	500	250	0	1	0	1
0	1	1	0	250	125	0	1	1	0
1	0	1	1	1Meg	---	1	0	1	1
1	0	0	0	500	250	1	0	0	0
1	0	0	1	2Meg	---	0	1	0	1
1	0	1	0	250	125	0	1	1	0

Note 1: This is for DENSEL in normal mode (see section CR05 on page 102). The DENSEL pin is set high after a hardware reset and is unaffected by the DOR and the DSR resets.

Table 20 - Drive Rate Table (Recommended)

DRIVE RATE		FORMAT
DRT1	**DRT0**	(see section **CR0B** on page 104 to program Drive Rate)
0	0	360K, 1.2M, 720K, 1.44M and 2.88M Vertical Format
0	1	3-Mode Drive
1	0	2 Meg Tape

Table 21 - Default Precompensation Delays

DATA RATE	PRECOMPENSATION DELAYS
2 Mbps	125 ns
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

DATA REGISTER (FIFO)

The Data Register (Base Address + 5) is used to transfer all command parameter information, disk data and result status between the host processor and the floppy disk controller. The Data Register is Read/Write. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The Data Register defaults to FIFO disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error.
Table 22 gives several examples of service delays with a FIFO. The data is based upon the following formula:

Threshold# × (8 ÷ Data Rate) - 1.5μS = DELAY

At the start of a command the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the command execution phase is entered, the FIFO is cleared of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

Table 22 - Example FIFO Service Delays

	EXAMPLE DATA RATES		
FIFO THRESHOLD EXAMPLES	**2Mbps**	**1Mbps**	**500Kbps**
1 byte	1 x 4μs - 1.5μs = 2.5μs	1 x 8μs - 1.5μs = 6.5μs	1 x 16μs - 1.5μs = 14.5μs
2 bytes	2 x 4μs - 1.5μs = 6.5μs	2 x 8μs - 1.5μs = 14.5μs	2 x 16μs - 1.5μs = 30.5μs
8 bytes	8 x 4μs - 1.5μs = 30.5μs	8 x 8μs - 1.5μs = 62.5μs	8 x 16μs - 1.5μs = 126.5μs
15 bytes	15 x 4μs - 1.5μs = 58.5μs	15 x 8μs - 1.5μs = 118.5μs	15 x 16μs - 1.5μs = 238.5μs

DIGITAL INPUT REGISTER (DIR)

The Digital Input Register (Bass Address + 7: Read-only) is read-only in all modes. Table 23 shows the DIR in PC/AT mode, Table 24 shows the DIR in PS/2 mode, and Table 25 shows the DIR in Model 30 mode.

PC-AT Interface Mode

Table 23 - DIR PC/AT Interface Mode

	7	6	5	4	3	2	1	0
	DSK CHG							
RESET CONDITION	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Undefined, Bits 0 - 6
The data bus outputs D0 - 6 will remain in a high impedance state during a read of this register.

DSK CHG, Bit 7
The DSK CHG bit monitors the state of the pin of the same name and reflects the opposite value seen on the disk cable. The DSK CHG bit also depends upon the Force Disk Change bits in the Force FDD Status Change register (see section CR17 on page 107).

PS/2 Interface Mode

Table 24 - DIR PS/2 Interface Mode

	7	6	5	4	3	2	1	0
	DSK CHG	1	1	1	1	DRATE SEL1	DRATE SEL0	nHIGH DENS
RESET CONDITION	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

nHIGH DENS, Bit 0
This bit is low whenever the 500 Kbps or 1 Mbps data rates are selected, and high when 250 Kbps and 300 Kbps are selected.

Data Rate Select, Bits 1 - 2
These bits control the data rate of the floppy controller. See Table 19 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

Undefined, Bits 3 - 6
Always read as a logic “1”

DSK CHG, Bit 7
The DSK CHG bit monitors the pin of the same name and reflects the opposite value seen on the disk cable. The DSK CHG bit also depends upon the Force Disk Change bits in the Force FDD Status Change register (see section CR17 on page 107).

Model 30 Interface Mode

Table 25 - DIR Model 30 Interface Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	DMAEN	NOPREC	DRATE SEL1	DRATE SEL0
RESET CONDITION	N/A	0	0	0	0	0	1	0

Data Rate Select, Bits 0 - 1
These bits control the data rate of the floppy controller. See Table 19 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250kb/s after a hardware reset

Noprec, Bit 2
This bit reflects the value of the NOPREC bit set in the CCR register.

DMAEN, Bit 3
This bit reflects the value of DMAEN bit set in the DOR register bit 3.

Undefined, Bits 4 - 6
Always read as a logic “0”

DSK CHG, Bit 7
The DSK CHG bit monitors the pin of the same name and reflects the opposite value seen on the pin. The DSK CHG bit also depends upon the Force Disk Change bits in the Force FDD Status Change register (see section CR17 on page 107).

CONFIGURATION CONTROL REGISTER (CCR)

The Configuration Control Register (Bass Address + 7: Write-only) is write-only in all modes. Table 26 shows the CCR in PC/AT mode and PS/2 mode. Table 27 shows the CCR in Model 30 mode.

PC/AT and PS/2 Interface Modes

Table 26 - CCR PC/AT and PS/2 Interface Modes

7	6	5	4	3	2	1	0

							DRATE SEL1	DRATE SEL0
RESET CONDITION	N/A	N/A	N/A	N/A	N/A	N/A	1	0

Data Rate Select, Bits 0 - 1
These bits determine the data rate of the floppy controller. See Table 19 for the appropriate values.

Reserved, Bits 2 - 7
Bits 2 to 7 are *RESERVED*. Reserved bits cannot be written and return 0 when read.

Model 30 Interface Mode

Table 27 - CCR Model 30 Interface Mode

	7	6	5	4	3	2	1	0
						NOPREC	DRATE SEL1	DRATE SEL0
RESET CONDITION	N/A	N/A	N/A	N/A	N/A	N/A	1	0

Data Rate Select, Bits 0 - 1
These bits determine the data rate of the floppy controller. See Table 19 for the appropriate values.

No Precompensation, Bit 2
This bit can be set by software, but it has no functionality. It can be read by bit 2 of the DSR when in Model 30 register mode. Unaffected by software reset.

Reserved, Bits 3 - 7
Bits 3 to 7 are *RESERVED*. Reserved bits cannot be written and return 0 when read.

Status Register Encoding

During the Result Phase of certain commands, the Data Register contains data bytes that give the status of the command just executed.

Table 28 - Status Register 0

BIT NO.	SYMBOL	NAME	DESCRIPTION
7,6	IC	Interrupt Code	00 - Normal termination of command. The specified command was properly executed and completed without error. 01 - Abnormal termination of command. Command execution was started, but was not successfully completed. 10 - Invalid command. The requested command could not be executed. 11 - Abnormal termination caused by Polling.
5	SE	Seek End	The FDC completed a Seek, Relative Seek or Recalibrate command (used during a Sense Interrupt Command).
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 80 step pulses in the Recalibrate command. 2. The Relative Seek command caused the FDC to step outward beyond Track 0.
3			Unused. This bit is always "0".
2	H	Head Address	The current head address.
1,0	DS1,0	Drive Select	The current selected drive.

Table 29 - Status Register 1

BIT NO.	SYMBOL	NAME	DESCRIPTION
7	EN	End of Cylinder	The FDC tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data command.
6			Unused. This bit is always "0".
5	DE	Data Error	The FDC detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the FDC does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3			Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. Read Data, Read Deleted Data command - the FDC did not find the specified sector. 2. Read ID command - the FDC cannot read the ID field without an error. 3. Read A Track command - the FDC cannot find the proper sector sequence.
1	NW	Not Writable	WP pin became a "1" while the FDC is executing a Write Data, Write Deleted Data, or Format A Track command.
0	MA	Missing Address Mark	Any one of the following: 1. The FDC did not detect an ID address mark at the specified track after encountering the index pulse from the IDX pin twice. 2. The FDC cannot detect a data address mark or a deleted data address mark on the specified track.

Table 30 - Status Register 2

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always “0”.
6	CM	Control Mark	Any one of the following: 1. Read Data command - the FDC encountered a deleted data address mark. 2. Read Deleted Data command - the FDC encountered a data address mark.
5	DD	Data Error in Data Field	The FDC detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3			Unused. This bit is always “0”.
2			Unused. This bit is always “0”.
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF hex, which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

Table 31 - Status Register 3

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always “0”.
6	WP	Write Protected	Indicates the status of the WP pin. The Write Protected bit also depends upon the state of the Force Write Protect bits in the Force FDD Status Change configuration register (see section **CR17** on page 109).
5			Unused. This bit is always “1”.
4	T0	Track 0	Indicates the status of the TRK0 pin.
3			Unused. This bit is always “1”.
2	HD	Head Address	Indicates the status of the HDSEL pin.
1,0	DS1,0	Drive Select	Indicates the status of the DS1, DS0 pins.

Reset

There are three sources of system reset on the FDC: the RESET pin of the FDC37N3869, a reset generated via a bit in the DOR, and a reset generated via a bit in the DSR. At power on, a Power On Reset initializes the FDC. All resets take the FDC out of the power down state.

All operations are terminated upon a RESET, and the FDC enters an idle state. A reset while a disk write is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the Configure command information, and the FDC waits for a new command. Drive polling will start unless disabled by a new Configure command.

RESET PIN (HARDWARE RESET)

The RESET pin is a global reset and clears all registers except those programmed by the Specify command. The DOR reset bit is enabled and must be cleared by the host to exit the reset state.

DOR RESET VS. DSR RESET (SOFTWARE RESET)

These two resets are functionally the same. Both will reset the FDC core, which affects drive status information and the FIFO circuits. The DSR reset clears itself automatically while the DOR reset requires the host to manually clear it. DOR reset has precedence over the DSR reset. The DOR reset is set automatically upon a pin reset. The user must manually clear this reset bit in the DOR to exit the reset state.

DMA Transfers

DMA transfers are enabled with the Specify command and are initiated by the FDC by activating the FDRQ pin during a data transfer command. The FIFO is enabled directly by asserting nDACK and addresses need not be valid.

Note that if the DMA controller (i.e. 8237A) is programmed to function in verify mode, a pseudo read is performed by the FDC based only on nDACK. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read. With the FIFO enabled, the FDC can perform the above operation by using the new Verify command; no DMA operation is needed.

Controller Phases

For simplicity, command handling in the FDC can be divided into three phases: Command, Execution, and Result. Each phase is described in the following sections.

COMMAND PHASE

After a reset, the FDC enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the FDC before the command phase is complete. (Refer to Table 33 for the command set descriptions). These bytes of data must be transferred in the order prescribed.

Before writing to the FDC, the host must examine the RQM and DIO bits of the Main Status Register. RQM and DIO must be equal to “1” and “0” respectively before command bytes may be written. RQM is set false by the FDC after each write cycle until the received byte is processed. The FDC asserts RQM again to request each parameter byte of the command unless an illegal command condition is detected. After the last parameter byte is received, RQM remains “0” and the FDC automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to provide for the proper handling of the “Invalid Command” condition.

EXECUTION PHASE

All data transfers to or from the FDC occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the Specify command.

After a reset, the FIFO is disabled. Each data byte is transferred by an FINT or FDRQ depending on the DMA mode. The Configure command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the FDC when service is requested from the host and ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a “fast” system. A high value of threshold (i.e. 12) is used with a “sluggish” system by affording a long latency period after a service request, but results in more frequent service requests.

Non-DMA Mode Transfers

FIFO to Host

The FINT pin and RQM bits in the Main Status Register are activated when the FIFO contains (16-<threshold>) bytes or the last bytes of a full sector have been placed in the FIFO. The FINT pin can be used for interrupt-driven systems,and RQM can be used for polled systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. The FDC will deactivate the FINT pin and RQM bit when the FIFO becomes empty. Host to FIFO The FINT pin and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The FINT pin and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has <threshold> bytes remaining in the FIFO. The FINT pin will also be deactivated if TC and nDACK both go inactive. The FDC enters the result phase after the last byte is taken by the FDC from the FIFO (i.e. FIFO empty condition).

DMA Mode Transfers

FIFO to Host

The FDC activates the DDRQ pin when the FIFO contains (16 - <threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The FDC will deactivate the DDRQ pin when the FIFO becomes empty. FDRQ goes inactive after nDACK goes active for the last byte of a data transfer (or on the active edge of nIOR, on the last byte, if no edge is present on nDACK). A data underrun may occur if FDRQ is not removed in time to prevent an unwanted cycle.

Host to FIFO

The FDC activates the FDRQ pin when entering the execution phase of the data transfer commands. The DMA controller must respond by activating the nDACK and nIOW pins and placing data in the FIFO. FDRQ remains active until the FIFO becomes full. FDRQ is again set true when the FIFO has <threshold> bytes remaining in the FIFO. The FDC will also deactivate the FDRQ pin when TC becomes true (qualified by nDACK), indicating that no more data is required. FDRQ goes inactive after nDACK goes active for the last byte of a data transfer (or on the active edge of nIOW of the last byte, if no edge is present on nDACK). A data overrun may occur if FDRQ is not removed in time to prevent an unwanted cycle.

Data Transfer Termination

The FDC supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer. If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the FDC will continue to complete the sector as if a hardware TC was received. The only difference between these implicit functions and TC is that they return “abnormal termination” result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the FDC, the internal sector count will be complete when the FDC reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the FDC to read the last 16 bytes from the FIFO. The host must tolerate this delay.

RESULT PHASE

The generation of FINT determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the FDC before the result phase is complete. These bytes of data must be read out for another command to start.

RQM and DIO must both equal “1” before the result bytes may be read. After all the result bytes have been read, the RQM and DIO bits switch to “1” and “0” respectively, and the CB bit is cleared, indicating that the FDC is ready to accept the next command.

Command Set/Descriptions

Commands can be written whenever the FDC is in the command phase. Each command has a unique set of needed parameters and status results. The FDC checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it is invalid, an interrupt is issued. The user sends a Sense Interrupt Status command which returns an invalid command error. Refer to Table 32 for explanations of the various symbols used. Table 33 lists the required parameters and the results associated with each command that the FDC is capable of performing.

Table 32 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
C	Cylinder Address	The currently selected address; 0 to 255.
D	Data Pattern	The pattern to be written in each sector data field during formatting.
D0, D1, D2, D3	Drive Select 0-3	Designates which drives are perpendicular drives on the Perpendicular Mode Command. A "1" indicates a perpendicular drive.
DIR	Direction Control	If this bit is "0", then the head will step out from the spindle during a relative seek. If set to a "1", the head will step in toward the spindle.
DS0, DS1	Disk Drive Select	**DS1** **DS0** **DRIVE** 0 0 Drive 0 0 1 Drive 1 1 0 Drive 2 1 1 Drive 3
DTL	Special Sector Size	By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.
EC	Enable Count	When this bit is "1" the "DTL" parameter of the Verify command becomes SC (number of sectors per track).
EFIFO	Enable FIFO	This active low bit when a 0, enables the FIFO. A "1" disables the FIFO (default).
EIS	Enable Implied Seek	When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.
EOT	End of Track	The final sector number of the current track.
GAP		Alters Gap 2 length when using Perpendicular Mode.
GPL	Gap Length	The Gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).
H/HDS	Head Address	Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	Head Load Time	The time interval that FDC waits after loading the head and before initializing a read or write operation. Refer to the Specify command for actual delays.
HUT	Head Unload Time	The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the Specify command for actual delays.
LOCK		Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE COMMAND can be reset to their default values by a "software Reset" (A reset caused by writing to the appropriate bits of either the DSR or DOR).
MFM	MFM/FM Mode Selector	A one selects the double density (MFM) mode. A zero selects single density (FM) mode.

SYMBOL	NAME	DESCRIPTION
MT	Multi-Track Selector	When set, this flag selects the multi-track operating mode. In this mode, the FDC treats a complete cylinder under head 0 and 1 as a single track. The FDC operates as this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the FDC finishes operating on the last sector under head 0.
N	Sector Size Code	This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16k. It is the user's responsibility to not select combinations that are not possible with the drive. **N** **SECTOR SIZE** 00 128bytes 01 256bytes 02 512bytes 07 16Kbytes
NCN	New Cylinder Number	The desired cylinder number.
ND	Non-DMA Mode Flag	When set to "1", indicates that the FDC is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the FDC operates in DMA mode, interfacing to a DMA controller by means of the DRQ and nDACK signals.
OW	Overwrite	The bits D0-D3 of the Perpendicular Mode Command can only be modified if OW is set to "1". OW id defined in the Lock command.
PCN	Present Cylinder Number	The current position of the head at the completion of Sense Interrupt Status command.
POLL	Polling Disable	When set, the internal polling routine is disabled. When clear, polling is enabled.
PRETRK	Precompensation Start Track Number	Programmable from track 00 to FFH.
R	Sector Address	The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	Relative Cylinder Number	Relative cylinder offset from present cylinder as used by the Relative Seek command.
SC	Number of Sectors Per Track	The number of sectors per track to be initialized by the Format command. The number of sectors per track to be verified during a Verify command when EC is set.
SK	Skip Flag	When set to "1", sectors containing a deleted data address mark will automatically be skipped during the execution of Read Data. If Read Deleted is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.
SRT	Step Rate Interval	The time interval between step pulses issued by the FDC. Programmable from 0.5 to 8 milliseconds in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Registers within the FDC which store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	Write Gate	Alters timing of WE to allow for pre-erase loads in perpendicular drives.

Instruction Set

Table 33 - Instruction Set

READ DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— C ———								Sector ID information prior to Command execution.
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data transfer between the FDD and system.
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								Sector ID information after Command execution.
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

READ DELETED DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— C ———								Sector ID information prior to Command execution.
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data transfer between the FDD and system.
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								Sector ID information after Command execution.
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

WRITE DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— C ———								Sector ID information prior to Command execution.
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data transfer between the FDD and system.
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								Sector ID information after Command execution.
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

WRITE DELETED DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— C ———								Sector ID information prior to Command execution.
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data transfer between the FDD and system.
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								Sector ID information after Command execution.
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

READ A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— C ———								Sector ID information prior to Command execution.
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data transfer between the FDD and system. FDC reads all of cylinders' contents from index hole to EOT.
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								Sector ID information after Command execution.
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

VERIFY										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	——— C ———								Sector ID information prior to Command execution.
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL/SC ———								
Execution										No data transfer takes place.
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								Sector ID information after Command execution.
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

VERSION										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

FORMAT A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— N ———								Bytes/Sector
	W	——— SC ———								Sectors/Cylinder
	W	——— GPL ———								Gap 3
	W	——— D ———								Filler Byte
Execution for Each Sector Repeat:	W	——— C ———								Input Sector Parameters
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
										FDC formats an entire cylinder
Result	R	——— ST0 ———								Status information after Command execution
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— Undefined ———								
	R	——— Undefined ———								
	R	——— Undefined ———								
	R	——— Undefined ———								

RECALIBRATE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt.

SENSE INTERRUPT STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	———— ST0 ————								Status information at the end of each seek operation.
	R	———— PCN ————								

SPECIFY										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	—— SRT ——				—— HUT ——				
	W	———— HLT ————							ND	

SENSE DRIVE STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	———— ST3 ————								Status information about FDD

SEEK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	———— NCN ————								
Execution										Head positioned over proper cylinder on diskette.

CONFIGURE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	—— FIFOTHR ——				
Execution	W	———— PRETRK ————								

RELATIVE SEEK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	———— RCN ————								

DUMPREG									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	*Note: Registers placed in FIFO
Execution										
Result	R	———— PCN-Drive 0 ————								
	R	———— PCN-Drive 1 ————								
	R	———— PCN-Drive 2 ————								
	R	———— PCN-Drive 3 ————								
	R	——— SRT ———					——— HUT ———			
	R	———— HLT ————							ND	
	R	———— SC/EOT ————								
	R	LOCK	0	D3	D2	D1	D0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL		——— FIFOTHR ———			
	R	———— PRETRK ————								

READ ID									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	———— ST0 ————								Status information after Command execution.
										Disk status after the Command has completed
	R	———— ST1 ————								
	R	———— ST2 ————								
	R	———— C ————								
	R	———— H ————								
	R	———— R ————								
	R	———— N ————								

PERPENDICULAR MODE			
		DATA BUS	

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Codes
		OW	0	D3	D2	D1	D0	GAP	WGATE	

INVALID CODES										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	——— Invalid Codes ———								Invalid Command Codes (NoOp - FDC37N3869 goes into Standby State)
Result	R	——— ST0 ———								ST0 = 80H

LOCK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

SC is returned if the last command that was issued was the Format command. EOT is returned if the last command was a Read or Write.

Note: These bits are used internally only. They are not reflected in the Drive Select pins. It is the user's responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

Data Transfer Commands

All of the Read Data, Write Data and Verify type commands use the same parameter bytes and return the same results information, the only difference being the coding of bits 0-4 in the first byte.

An implied seek will be executed if the feature was enabled by the Configure command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it will be reflected in the results status normally returned for a Read/Write Data command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

READ DATA

A set of nine bytes is required to place the FDC in the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the FDC reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of TC, or an implied TC (FIFO overrun/underrun), the FDC stops sending data but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector, terminate the Read Data Command. N determines the number of bytes per sector (see Table 34 below). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the FDC transfers the specified number of bytes to the host. For reads, it continues to read the entire 128-byte sector and checks for CRC errors. For writes, it completes the 128-byte sector by filling in zeros. If N is not set to 00 Hex, DTL should be set to FF Hex and has no impact on the number of bytes transferred.

Table 34 - Sector Sizes

N	SECTOR SIZE
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track) and N (number of bytes/sector).

The Multi-Track function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing the last sector of the same track at Side 1.
If the host terminates a read or write operation in the FDC, the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 38.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify command) has elapsed. If the host issues another command before the head unloads, then the head settling time may be saved between subsequent reads.

If the FDC detects a pulse on the nINDEX pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the Read Data Command.

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a CRC error occurs in the ID or data field, the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the Read Data Command. Table 36 describes the effect of the SK bit on the Read Data command execution and results. Except where noted in Table 36, the C or R value of the sector address is automatically incremented (see Table 38).

Table 35 - Affects of MT and N Bits

MT	N	MAXIMUM TRANSFER CAPACITY	FINAL SECTOR READ FROM DISK
0	1	256 x 26 = 6,656	26 at side 0 or 1
1	1	256 x 52 = 13,312	26 at side 1
0	2	512 x 15 = 7,680	15 at side 0 or 1
1	2	512 x 30 = 15,360	15 at side 1
0	3	1024 x 8 = 8,192	8 at side 0 or 1
1	3	1024 x 16 = 16,384	16 at side 1

Table 36 - Skip Bit vs. Read Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	No	Normal termination
0	Deleted Data	Yes	Yes	Address not incremented Next sector not searched for
1	Normal Data	Yes	No	Normal termination
1	Deleted Data	No	Yes	Normal termination. Sector not read ("skipped")

READ DELETED DATA

This command is the same as the Read Data command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.
Table 37 describes the effect of the SK bit on the Read Deleted Data command execution and results.

Except where noted in Table 37 the C or R value of the sector address is automatically incremented (see Table 38).

Table 37 - Skip Bit vs. Read Deleted Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	Yes	Address not incremented. Next sector not searched for.
0	Deleted Data	Yes	No	Normal termination.
1	Normal Data	No	Yes	Normal termination. Sector not read (“skipped”).
1	Deleted Data	Yes	No	Normal termination.

READ A TRACK

This command is similar to the Read Data command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the nINDEX pin, the FDC starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The FDC compares the ID information read from each sector with the specified value in the command and sets the ND flag of Status Register 1 to a “1” if there is no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (bits D7 and D5 of the first command byte respectively) should always be set to “0”.

This command terminates when the EOT specified number of sectors has not been read. If the FDC does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the IDX pin, then it sets the IC code in Status Register 0 to “01” (abnormal termination), sets the MA bit in Status Register 1 to “1”, and terminates the command.

Table 38 - Result Phase Table

MT	HEAD	FINAL SECTOR TRANSFERRED TO HOST	ID INFORMATION AT RESULT PHASE			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	LSB	01	NC

NC: No Change, the same value as the one at the beginning of command execution.
LSB: Least Significant Bit, the LSB of H is complemented.

WRITE DATA

After the Write Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the Specify command), and begins reading ID fields. When the sector address read from the diskette matches the sector address specified in the command, the FDC reads the data from the host via the FIFO and writes it to the sector's data field.

After writing data into the current sector, the FDC computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the FDC continues writing to the next data field. The FDC continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID fields, it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the Write Data command.

The Write Data command operates in much the same manner as the Read Data command. The following items are the same. Please refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command
- Definition of DTL when N = 0 and when N does not = 0

WRITE DELETED DATA

This command is almost the same as the Write Data command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

VERIFY

The Verify command is used to verify the data stored on a disk. This command acts exactly like a Read Data command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously-stored value.

Because data is not transferred to the host, TC (pin 25) cannot be used to terminate this command. By setting the EC bit to "1", an implicit TC will be issued to the FDC. This implicit TC will occur when the SC value has decremented to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0", DTL/SC should be programmed to 0FFH. Refer to Table 38 and Table 39 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:
Sectors Per Side = Number of formatted sectors per each side of the disk.
Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

Table 39 - Verify Command Result Phase Table

MT	EC	SC/EOT VALUE	TERMINATION RESULT
0	0	SC = DTL EOT £ # Sectors Per Side	Success Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC £ # Sectors Remaining AND EOT £ # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT £ # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC £ # Sectors Remaining AND EOT £ # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

Note: If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

FORMAT A TRACK

The Format command allows an entire track to be formatted. After a pulse from the IDX pin is detected, the FDC starts writing data on the disk including gaps, address marks, ID fields, and data fields per the IBM System 34 or 3740 format (MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID field for each sector is supplied by the host; that is, four data bytes per sector are needed by the FDC for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the FDC for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the FDC encounters a pulse on the IDX pin again and it terminates the command. Table 41 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

Table 40 - FORMAT FIELDS

SYSTEM 34 (DOUBLE DENSITY) FORMAT

GAP4a 80x 4E	SYNC 12x 00	IAM		GAP1 50x 4E	SYNC 12x 00	IDAM		CYL	HD	SEC	NO	CRC	GAP2 22x 4E	SYNC 12x 00	DATA AM		DATA	CRC	GAP3	GAP 4b
		3x C2	FC			3x A1	FE								3x A1	FB F8				

SYSTEM 3740 (SINGLE DENSITY) FORMAT

GAP4a 40x FF	SYNC 6x 00	IAM	GAP1 26x FF	SYNC 6x 00	IDAM	CYL	HD	SEC	NO	CRC	GAP2 11x FF	SYNC 6x 00	DATA AM	DATA	CRC	GAP3	GAP 4b
		FC			FE								FB or F8				

PERPENDICULAR FORMAT

GAP4a 80x 4E	SYNC 12x 00	IAM		GAP1 50x 4E	SYNC 12x 00	IDAM		CYL	HD	SEC	NO	CRC	GAP2 41x 4E	SYNC 12x 00	DATA AM		DATA	CRC	GAP3	GAP 4b
		3x C2	FC			3x A1	FE								3x A1	FB F8				

Table 41 - Typical Values for Formatting

	FORMAT	SECTOR SIZE	N	SC	GPL1	GPL2
5.25" Drives	FM	128	00	12	07	09
		128	00	10	10	19
		512	02	08	18	30
		1024	03	04	46	87
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
	MFM	256	01	12	0A	0C
		256	01	10	20	32
		512*	02	09	2A	50
		1024	03	04	80	F0
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
3.5" Drives	FM	128	0	0F	07	1B
		256	1	09	0F	2A
		512	2	05	1B	3A
	MFM	256	1	0F	0E	36
		512**	2	09	1B	54
		1024	3	05	35	74

GPL1 = suggested GPL values in Read and Write commands to avoid splice point between data field and ID field of contiguous sections.

GPL2 = suggested GPL value in Format A Track command.

*PC/AT values (typical)

**PS/2 values (typical). Applies with 1.0 MB and 2.0 MB drives.

Note: All values except sector size are in hex.

Control Commands

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete: Read ID, Recalibrate, and Seek. The other control commands do not generate an interrupt.

READ ID

The Read ID command is used to find the present position of the recording heads. The FDC stores the values from the first ID field it is able to read into its registers. If the FDC does not find an ID address mark on the diskette after the second occurrence of a pulse on the nINDEX pin, it then sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the Sense Interrupt Status command. Otherwise, valuable interrupt status information will be lost.

RECALIBRATE

This command causes the read/write head within the FDC to retract to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the nTR0 pin from the FDD. As long as the nTR0 pin is low, the DIR pin remains 0 and step pulses are issued. When the nTR0 pin goes high, the SE bit in Status Register 0 is set to "1" and the command is terminated. If the nTR0 pin is still low after 79 step pulses have been issued, the FDC sets the SE and the EC bits of Status Register 0 to "1" and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one Recalibrate command to return the head back to physical Track 0. The Recalibrate command does not have a result phase. The Sense Interrupt Status command must be issued after the Recalibrate command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the FDC is in the BUSY state, but during the execution

phase it is in a NON-BUSY state. At this time, another Recalibrate command may be issued, and in this manner parallel Recalibrate operations may be done on up to four drives at once.

Upon power up, the software must issue a Recalibrate command to properly initialize all drives and the controller.

SEEK

The read/write head within the drive is moved from track to track under the control of the Seek command. The FDC compares the PCN, which is the current head position, with the NCN and performs the following operation if there is a difference:

PCN < NCN: Direction signal to drive set to "1" (step in) and issues step pulses.
PCN > NCN: Direction signal to drive set to "0" (step out) and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN the SE bit in Status Register 0 is set to "1" and the command is terminated.

During the command phase of the seek or recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in the NON-BUSY state. At this time, another Seek or Recalibrate command may be issued, and in this manner, parallel seek operations may be done on up to four drives at once.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1) Seek command - Step to the proper track
2) Sense Interrupt Status command - Terminate the Seek command
3) Read ID - Verify head is on proper track
4) Issue Read/Write command.

The Seek command does not have a result phase. Therefore, it is highly recommended that the Sense Interrupt Status command be issued after the Seek command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return to a "0". When exiting POWERDOWN mode, the FDC clears the PCN value and the status information to zero. Prior to issuing the POWERDOWN command, it is highly recommended that the user service all pending interrupts through the Sense Interrupt Status command.

SENSE INTERRUPT STATUS

An interrupt signal on FINT pin is generated by the FDC for one of the following reasons:

1) Upon entering the Result Phase of:
   a) Read Data command
   b) Read A Track command
   c) Read ID command
   d) Read Deleted Data command
   e) Write Data command
   f) Format A Track command
   g) Write Deleted Data command
   h) Verify command
2) End of Seek, Relative Seek, or Recalibrate command
3) FDC requires a data transfer during the execution phase in the non-DMA mode

The Sense Interrupt Status command resets the interrupt signal and, via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt.

Table 42 - Interrupt Identification

SE	IC	INTERRUPT DUE TO
0	11	Polling
1	00	Normal termination of Seek or Recalibrate command
1	01	Abnormal termination of Seek or Recalibrate command

The Seek, Relative Seek, and Recalibrate commands have no result phase. The Sense Interrupt Status command must be issued immediately after these commands to terminate them and to provide verification of the head position

(PCN). The H (Head Address) bit in ST0 will always return a "0". If a Sense Interrupt Status is not issued, the drive will continue to be BUSY and may affect the operation of the next command.

SENSE DRIVE STATUS

Sense Drive Status obtains drive status information. It has not execution phase and goes directly to the result phase from the command phase. Status Register 3 contains the drive status information.

SPECIFY

The Specify command sets the initial values for each of the three internal times. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the read/write operation starts. The values change with the data rate speed selection and are documented in
Table 43. The values are the same for MFM and FM.

Table 43 - Drive Control Delays (ms)

	HUT					SRT				
	2M	**1M**	**500K**	**300K**	**250K**	**2M**	**1M**	**500K**	**300K**	**250K**
0	64	128	256	426	512	4	8	16	26.7	32
1	4	8	16	26.7	32	3.75	7.5	15	25	30
..	..	..	..	..	..	..	..	..	..	..
E	56	112	224	373	448	0.5	1	2	3.33	4
F	60	120	240	400	480	0.25	0.5	1	1.67	2

	HLT				
	2M	**1M**	**500K**	**300K**	**250K**
00	64	128	256	426	512
01	0.5	1	2	3.3	4
02	1	2	4	6.7	8
..	..	..	..	..	.
7F	63	126	252	420	504
7F	63.5	127	254	423	508

The choice of DMA or non-DMA operations is made by the ND bit. When this bit is "1", the non-DMA mode is selected, and when ND is "0", the DMA mode is selected. In DMA mode, data transfers are signaled by the FDRQ pin. Non-DMA mode uses the RQM bit and the FINT pin to signal data transfers.

CONFIGURE

The Configure command is issued to select the special features of the FDC. A Configure command need not be issued if the default values of the FDC meet the system requirements.
Configure Default Values:

EIS - No Implied Seeks
EFIFO - FIFO Disabled
POLL - Polling Enabled
FIFOTHR - FIFO Threshold Set to 1 Byte
PRETRK - Pre-Compensation Set to Track 0

EIS - Enable Implied Seek. When set to "1", the FDC will perform a Seek operation before executing a read or write command. Defaults to no implied seek.

EFIFO - A "1" disables the FIFO (default). This means data transfers are asked for on a byte-by-byte basis. Defaults to "1", FIFO disabled. The threshold defaults to "1".

POLL - Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a reset. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR - The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. A "00" selects one byte; "0F" selects 16 bytes.

PRETRK - Pre-Compensation Start Track Number. Programmable from track 0 to 255. Defaults to track 0. A “00” selects track 0; “FF” selects track 255.

VERSION

The Version command checks to see if the controller is an enhanced type or the older type (765A). A value of 90 H is returned as the result byte.

RELATIVE SEEK

The command is coded the same as for Seek, except for the MSB of the first byte and the DIR bit.

Table 44 - Head Step Direction Control

DIR	ACTION
0	Step Head Out
1	Step Head In

RCN - Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

The Relative Seek command differs from the Seek command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The Seek command is good for drives that support a maximum of 256 tracks. Relative Seeks cannot be overlapped with other Relative Seeks. Only one Relative Seek can be active at a time. Relative Seeks may be overlapped with Seeks and Recalibrates. Bit 4 of Status Register 0 (EC) will be set if Relative Seek attempts to step outward beyond Track 0. As an example, assume that a floppy drive has 300 useable tracks. The host needs to read track 300 and the head is on any track (0-255). If a Seek command is issued, the head will stop at track 255. If a Relative Seek command is issued, the FDC will move the head the specified number of tracks, regardless of the internal cylinder position register (but will increment the register). If the head was on track 40 (d), the maximum track that the FDC could position the head on using Relative Seek will be 295 (D), the initial track + 255 (D). The maximum count that the head can be moved with a single Relative Seek command is 255 (D).

The internal register, PCN, will overflow as the cylinder number crosses track 255 and will contain 39 (D). The resulting PCN value is thus (RCN + PCN) mod 256. Functionally, the FDC starts counting from 0 again as the track number goes above 255 (D). It is the user’s responsibility to compensate FDC functions (precompensation track number) when accessing tracks greater than 255. The FDC does not keep track that it is working in an “extended track area” (greater than 255). Any command issued will use the current PCN value except for the Recalibrate command, which only looks for the TRACK0 signal. Recalibrate will return an error if the head is farther than 79 due to its limitation of issuing a maximum of 80 step pulses. The user simply needs to issue a second Recalibrate command. The Seek command and implied seeks will function correctly within the 44 (D) track (299-255) area of the “extended track area”. It is the user’s responsibility not to issue a new track position that will exceed the maximum track that is present in the extended area. To return to the standard floppy range (0-255) of tracks, a Relative Seek should be issued to cross the track 255 boundary. A Relative Seek can be used instead of the normal Seek, but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a Read ID command to ensure that the head is physically on the track that software assumes it to be. Different FDC commands will return different cylinder results which may be difficult to keep track of with software without the Read ID command.

PERPENDICULAR MODE

The Perpendicular Mode command should be issued prior to executing Read/Write/Format commands that access a disk drive with perpendicular recording capability. With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives.
Table 45 describes the affects of the WGATE and GAP bits for the Perpendicular Mode command. Upon a reset, the FDC will default to the conventional mode (WGATE = 0, GAP = 0).

Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data Rate Select Register. The user must ensure that these two data rates remain consistent.

The Gap2 and VCO timing requirements for perpendicular recording type drives are dictated by the design of the read/write head. In the design of this head, a pre-erase head precedes the normal read/write head by a distance of 200 micrometers. This works out to about 38 bytes at a 1 Mbps recording density. Whenever the write head is enabled by the Write Gate signal, the pre-erase head is also activated at the same time. Thus, when the write head is initially turned on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-

erase head since it has not yet been activated. To accommodate this head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes. The format field shown on page 61 illustrates the change in the Gap2 field size for the perpendicular format.

On the read back by the FDC, the controller must begin synchronization at the beginning of the sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. But, when the controller operates in the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased Gap2 field size. For both cases, and approximate two-byte cushion is maintained from the beginning of the sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For the Write Data case, the FDC activates Write Gate at the beginning of the sync field under the conventional mode. The controller then writes a new sync field, data address mark, data field, and CRC as shown in Figure 4. With the pre-erase head of the perpendicular drive, the write head must be activated in the Gap2 field to insure a proper write of the new sync field. For the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), 38 bytes will be written in the Gap2 space. Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field for the 500 Kbps perpendicular mode (WGATE = 1, GAP =0).

It should be noted that none of the alterations in Gap2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. Once the Perpendicular Mode command is invoked, FDC software behavior from the user standpoint is unchanged.

The perpendicular mode command is enhanced to allow specific drives to be designated Perpendicular recording drives. This enhancement allows data transfers between Conventional and Perpendicular drives without having to issue Perpendicular mode commands between the accesses of the different drive types, nor having to change write pre-compensation values.

When both GAP and WGATE bits of the PERPENDICULAR MODE COMMAND are both programmed to “0” (Conventional mode), then D0, D1, D2, D3, and D4 can be programmed independently to “1” for that drive to be set automatically to Perpendicular mode. In this mode the following set of conditions also apply:

1) The GAP2 written to a perpendicular drive during a write operation will depend upon the programmed data rate.
2) The write pre-compensation given to a perpendicular mode drive will be 0ns.
3) For D0-D3 programmed to “0” for conventional mode drives any data written will be at the currently programmed write pre-compensation.

Note: Bits D0-D3 can only be overwritten when OW is programmed as a “1”.
If either GAP or WGATE is a “1” then D0-D3 are ignored.

Software and hardware resets have the following effect on the PERPENDICULAR MODE COMMAND:

1) “Software” resets (via the DOR or DSR registers) will only clear GAP and WGATE bits to “0”. D0-D3 are unaffected and retain their previous value.
2) “Hardware” resets will clear all bits (GAP, WGATE and D0-D3) to “0”, i.e. all conventional mode.

Table 45 - Affects of WGATE and GAP Bits

WGATE	GAP	MODE	LENGTH OF GAP2 FORMAT FIELD	PORTION OF GAP 2 WRITTEN BY WRITE DATA OPERATION
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500 Kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1 Mbps)	41 Bytes	38 Bytes

LOCK

In order to protect systems with long DMA latencies against older application software that can disable the FIFO the LOCK Command has been added. This command should only be used by the FDC routines, and application software should refrain from using it. If an application calls for the FIFO to be disabled then the CONFIGURE command should be used.

The LOCK command defines whether the EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to logic "1" all subsequent "software RESETS by the DOR and DSR registers will not change the previously set parameters to their default values. All "hardware" RESET from the RESET pin will set the LOCK bit to logic "0" and return the EFIFO, FIFOTHR, and PRETRK to their default values. A status byte is returned immediately after issuing a LOCK command. This byte reflects the value of the LOCK bit set by the command byte.

ENHANCED DUMPREG

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. To accommodate the LOCK command and the enhanced PERPENDICULAR MODE command the eighth byte of the DUMPREG command has been modified to contain the additional data from these two commands.

Compatibility

The FDC37N3869 was designed with software compatibility in mind. It is a fully backwards-compatible solution with the older generation 765A/B disk controllers. The FDC also implements on-board registers for compatibility with the PS/2, as well as PC/AT and PC/XT, floppy disk controller subsystems. After a hardware reset of the FDC, all registers, functions and enhancements default to a PC/AT, PS/2 or PS/2 Model 30 compatible operating mode, depending on how the IDENT and MFM bits are configured by the system BIOS.

Parallel Port Floppy Disk Controller

In this mode, the Floppy Disk Control signals are available on the parallel port pins. When this mode is selected, the parallel port is not available. There are two modes of operation, PPFD1 and PPFD2. These modes can be selected in Configuration Register 4. PPFD1 has only drive 1 on the parallel port pins; PPFD2 has drive 0 and 1 on the parallel port pins.

PPFD1: Drive 0 is on the FDC pins
Drive 1 is on the Parallel port pins
PPFD2: Drive 0 is on the Parallel port pins
Drive 1 is on the Parallel port pins

When the PPFDC is selected the following pins are set as follows:

1) nDACK: Assigned to the parallel port device during configuration.
2) PDRQ (assigned to the parallel port): not ECP = high-Z, ECP & dmaEn = 0, ECP & not dmaEn = high-Z
3) IRQ assigned to the parallel port: not active, this is hi-Z or Low depending on settings.

The following parallel port pins are read as follows by a read of the parallel port register:

1) Data Register (read) = last Data Register (write)
2) Control Register are read as "cable not connected" STROBE, AUTOFD and SLC = 0 and nINIT = 1;
3) Status Register reads: nBUSY = 0, PE = 0, SLCT = 0, nACK = 1, nERR = 1.

The following FDC pins are all in the high impedance state when the PPFDC is actually selected by the drive select register:

1) nWDATA, DENSEL, nHDSEL, nWGATE, nDIR, nSTEP, nDS1, nDS0, nMTRO, nMTR1.
2) If PPFDx is selected, then the parallel port can not be used as a parallel port until "Normal" mode is selected.

The FDC signals are muxed onto the Parallel Port pins as shown in Table 46.

Table 46 - FDC Parallel Port Pins

CONNECTOR PIN #	CHIP PIN #	SPP MODE	PIN DIRECTION	FDC MODE	PIN DIRECTION
1	75	nSTB	I/O	(nDS0)	I/(0)[1]
2	69	PD0	I/O	nINDEX	I
3	68	PD1	I/O	nTRK0	I
4	67	PD2	I/O	nWP	I
5	66	PD3	I/O	nRDATA	I
6	64	PD4	I/O	nDSKCHG	I
7	63	PD5	I/O		

CONNECTOR PIN #	CHIP PIN #	SPP MODE	PIN DIRECTION	FDC MODE	PIN DIRECTION
8	62	PD6	I/O	(nMTR0)	I/(0) [1]
9	61	PD7	I/O		
10	60	nACK	I	nDS1	0
11	59	BUSY	I	nMTR1	0
12	58	PE	I	nWDATA	0
13	57	SLCT	I	nWGATE	0
14	74	nAFD	I/O	nDENSEL	0
15	73	nERR	I	nHDSEL	0
16	72	nINIT	I/O	nDIR	0
17	71	nSLIN	I/O	nSTEP	0

Note[1]: These pins are outputs in mode PPFD2. Inputs in mode PPFD1

For ACPI compliance the FDD pins that are multiplexed onto the Parallel Port must function independently of the state of the Parallel Port controller. For example, if the FDC is enabled onto the Parallel Port the multiplexed FDD Interface should function normally regardless of the Parallel Port Power control CR01.2. Table 47 illustrates this functionality.

Table 47 - Parallel Port FDD Control

PARALLEL PORT POWER	PARALLEL PORT FDC CONTROL		PARALLEL PORT FDC STATE	PARALLEL PORT STATE
CR01.2	CR04.3	CR04.2		
1	0	0	OFF	ON
0	0	0	OFF	OFF
X	1	X	ON	OFF[1]
	X	1		

Note[1]: The Parallel Port Control register reads as “Cable Not Connected” when the PP FDC is enabled; i.e., STROBE = AUTOFD = SLC = 0 and nINIT = 1

SERIAL PORT (UART)

The FDC37N3869 incorporates two full function UARTs. They are compatible with the NS16450, the 16450 ACE registers and the NS16550A. The UARTs perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 115.2K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs each contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UARTs are also capable of supporting the MIDI data rate. Refer to the FDC37N3869 Configuration Registers for information on disabling, powering down and changing the base address of the UARTs. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic "1". When OUT2 is a logic "0" the UART Interrupt is disabled.

Register Description

Addressing of the accessible registers of the Serial Port is shown below (
Table 48). The base addresses of the serial ports are defined by the configuration registers (see section CONFIGURATION on page 96). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The FDC37N3869 contains two serial ports, each of which contain a register set as described below.

Table 48 - Addressing the Serial Port

DLAB[1]	A2	A1	A0	REGISTER NAME
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write)

Note[1]: DLAB is Bit 7 of the Line Control Register

RECEIVE BUFFER REGISTER (RB)

The Receive Buffer register (Address Offset = 0H, DLAB = 0, READ ONLY) holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit character which is transferred to the Receive Buffer register. The shift register is not accessible.

TRANSMIT BUFFER REGISTER (TB)

The Transmit Buffer register (Address Offset = 0H, DLAB = 0, WRITE ONLY) contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data character to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

INTERRUPT ENABLE REGISTER (IER)

The lower four bits of the Interrupt Enable register (Address Offset = 1H, DLAB = 0, READ/WRITE) control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, by setting the appropriate bits of this register to a high selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the FDC37N3869. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

ERDAI, Bit 0

The ERDAI bit enables the Received Data Available Interrupt (and time-out interrupts in the FIFO mode) when set to logic "1".

ETHREI, Bit 1
The ETHREI bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

ELSI, Bit 2
The ELSI bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

EMSI, Bit 3
The EMSI bit enables the MODEM Status Interrupt when set to logic "1". An MSI is caused when one of the Modem Status Register bits changes state.

Reserved, Bits 4 - 7
Bits 4 to 7 are *RESERVED*. Reserved bits cannot be written and return 0 when read.

INTERRUPT IDENTIFICATION REGISTER (IIR)

By accessing the Interrupt Identification register (Address Offset = 2H, DLAB = X, READ), the host CPU can determine the highest priority interrupt and its source. Four levels of interrupt priority exist. They are in descending order of priority:

1) Receiver Line Status (highest priority)
2) Received Data Ready
3) Transmitter Holding Register Empty
4) MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to the Interrupt Control Table,
Table 49). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed.

Interrupt Pending, Bit 0
The Interrupt Pending bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

Interrupt ID, Bits 1 - 2
The Interrupt ID bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table (Table 49).

Time-Out, Bit 3
In non-FIFO mode, the Time-Out bit is a logic "0". In FIFO mode the Time-Out bit is set along with bit 2 when a time-out interrupt is pending.

Reserved, Bits 4 - 5
Bits 4 to 5 are *RESERVED*. Reserved bits cannot be written and return 0 when read.

FIFOs Enabled, Bits 6 - 7
The FIFOs Enabled bits are set when the FIFO CONTROL Register bit 0 equals 1.

Table 49 - Interrupt Control

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Time-out Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Character times and there is at least 1 character in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

FIFO CONTROL REGISTER (FCR)

The FIFO Control register (Address Offset = 2H, DLAB = X, WRITE) appears at the same location as the IIR. This register is used to enable and clear the FIFOs and set the RCVR FIFO trigger level. Note: DMA is not supported.

FIFO Enable, Bit 0

Setting the FIFO Enable bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

RCVR FIFO Reset, Bit 1

Setting the RCVR FIFO Reset bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

XMIT FIFO Reset, Bit 2

Setting the XMIT FIFO Reset bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

DMA Mode Select, Bit 3
Writing to the DMA Mode Select bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.

Reserved, Bits 4 - 5
Bits 4 to 5 are *RESERVED*. Reserved bits cannot be written and return 0 when read.

RCVR Trigger, Bits 6 - 7
The RCVR Trigger bits are used to set the trigger level for the RCVR FIFO interrupt (Table 50).

Table 50 - RCVR Trigger Encoding

RCVR TRIGGER		RCVR FIFO Trigger Level (BYTES)
Bit 7	**Bit 6**	
0	0	1
0	1	4
1	0	8
1	1	14

LINE CONTROL REGISTER (LCR)
The Line Control register (Address Offset = 3H, DLAB = 0, READ/WRITE) contains the formatting information for the serial line.

Word Length Select, Bits 0 - 1
The Word Length Select bits specify the number of bits in each transmitted or received serial character. Note: the *Start*, *Stop* and *Parity* bits are not included in the word length. The encoding of the Word Length bits is shown in Table 51.

Table 51 - Word Length Encoding

WORD LENGTH SELECT		WORD LENGTH (Bits)
Bit 1	**Bit 0**	
0	0	5
0	1	6
1	0	7
1	1	8

Stop Bits, Bit 2
The Stop Bits bit specifies the number of stop bits in each transmitted or received serial character. Table 52 describes the Stop Bits encoding.

Table 52 - STOP Bit Encoding

STOP BITS (Bit 2)	WORD LENGTH	NUMBER OF STOP BITS
0	-	1
0	5 Bits	1.5
1	6 Bits	2
1	7 Bits	2
1	8 Bits	2

Note: The receiver ignores stop bits beyond the first, regardless of the number of stop bits used in transmitting.

Parity Enable, Bit 3
When the Parity Enable bit is a logic “1” a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed.

Even Parity Select, Bit 4
When the Even Parity Select (EPS) bit is a logic "0" and the Parity Enable is a logic "1", an odd number of logic "1"'s is transmitted or checked in the data word and the parity bit. When the Parity Enable is a logic "1" and the EPS bit is a logic "1" an even number of bits is transmitted and checked.

Stick Parity, Bit 5
When the Stick Parity bit is a logic "1" and the Parity Enable is a logic "1", the parity bit is transmitted and then detected by the receiver in the opposite state indicated by the EPS bit.

Set Break, Bit 6
When the Set Break Control bit is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there until reset by a low level bit 6, regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

DLAB, Bit 7
The Divisor Latch Access Bit must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

MODEM CONTROL REGISTER (MCR)

The Modem Control register (Address Offset = 4H, DLAB = X, READ/WRITE) manages the interface for the MODEM, data set, or device emulating a MODEM.

Data Terminal Ready, Bit 0
The Data Terminal Ready bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic "1", the nDTR output is forced to a logic "0". When bit 0 is a logic "0", the nDTR output is forced to a logic "1".

Request To Send, Bit 1
The Request To Send bit controls the Request To Send (nRTS) output. . When bit 1 is set to a logic "1", the nRTS output is forced to a logic "0". When bit 1 is a logic "0", the nRTS output is forced to a logic "1".

OUT1, Bit 2
The OUT1 bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

OUT2, Bit 3
The OUT2 bit is used to enable the UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state; i.e, disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Loop, Bit 4
The Loop bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occurs:

1) The TXD is set to the Marking State (logic "1").
2) The receiver Serial Input (RXD) is disconnected.
3) The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4) All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5) The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI and DCD) respectively.
6) The Modem Control output pins are forced inactive.
7) Data that is transmitted is immediately received.

The Loopback feature allows the processor to verify the transmit and receive data paths of the Serial Port. The receiver and the transmitter interrupts are fully operational in loopback mode. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Reserved, Bits 5 - 7
Bits 5 to 7 are *RESERVED*. Reserved bits cannot be written and return 0 when read.

LINE STATUS REGISTER (LSR)

Address Offset = 5H, DLAB = X, READ/WRITE

Data Ready, Bit 0

Data Ready (DR) is set to a logic "1" whenever a complete received data character has been transferred into the Receiver Buffer Register or the FIFO. DR is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

Overrun Error, Bit 1

The Overrun Error (OE) bit indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely received in the shift register: the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition and reset whenever the Line Status Register is read.

Parity Error, Bit 2

The Parity Error (PE) bit indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

Framing Error, Bit 3

The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

Break Interrupt, Bit 4

The Break Interrupt (BI) bit is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received requires the serial data (RXD) to be logic "1" for at least ½ bit time.

Note: LSR Bits 1 through 4 produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Transmitter Holding Register Empty, Bit 5

The Transmitter Holding Register Empty (THRE) bit indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is read-only.

Transmitter Empty, Bit 6

The Transmitter Empty (TEMT) bit is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is read-only. In the FIFO mode this bit is set whenever the THR and TSR are both empty.

RCVR FIFO Error, Bit 7
The RCVR FIFO Error bit is permanently set to logic “0” in the 450 mode. In the FIFO mode this bit is set to a logic “1” when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

MODEM STATUS REGISTER (MSR)

The Modem Status register (Address Offset = 6H, DLAB = X, READ/WRITE) provides the current state of the control lines from the MODEM or peripheral device. In addition to this current state information, four bits of the MODEM Status Register provide state change information. These four bits are set to logic “1” whenever a control input from the MODEM changes state. They are reset to logic “0” whenever the MODEM Status Register is read.

Delta Clear To Send, Bit 0
The Delta Clear To Send (DCTS) bit indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

Delta Data Set Ready, Bit 1
The Delta Data Set Ready (DDSR) bit indicates that the nDSR input has changed state since the last time the MSR was read.

Trailing Edge Of Ring Indicator, Bit 2
The Trailing Edge of Ring Indicator (TERI) bit indicates that the nRI input has changed from logic “0” to logic “1”.

Delta Data Carrier Detect, Bit 3
The Delta Data Carrier Detect (DDCD) bit indicates that the nDCD input to the chip has changed state.

Note: Whenever bits 0, 1, 2, or 3 are set to a logic “1”, a MODEM Status Interrupt is generated.

Clear To Send, Bit 4
The Clear To Send bit is the complement of the Clear To Send input (nCTS). If the Loop bit of the MCR is set to logic “1”, this bit is equivalent to nRTS in the MCR.

Data Set Ready, Bit 5
The Data Set Ready bit is the complement of the Data Set Ready input (nDSR). If the Loop bit of the MCR is set to logic “1”, this bit is equivalent to DTR in the MCR.

Ring Indicator, Bit 6
The Ring Indicator bit is the complement of the Ring Indicator input (nRI). If the Loop bit of the MCR is set to logic “1”, this bit is equivalent to OUT1 in the MCR.

Data Carrier Detect, Bit 7
The Data Carrier Detect bit is the complement of the Data Carrier Detect input (nDCD). If the Loop bit of the MCR is set to logic “1”, this bit is equivalent to OUT2 in the MCR.

SCRATCHPAD REGISTER (SCR)

The Scratchpad register (Address Offset =7H, DLAB =X, READ/WRITE) has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

PROGRAMMABLE BAUD RATE GENERATOR DIVISOR LATCHES

The internal Baud Rate Generator (BRG) using the Programmable Baud Rate Generator Divisor Latches DDL and DDM (Address Offset = 0 and 1, DLAB = 1, READ/WRITE) is capable of taking any clock input (DC to 3 MHz) and dividing it by any divisor from 1 to 65535. The Baud Rate Generator output is 16x the baud rate. Two 8-bit latches store the divisor in 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the DDL and DDM registers the BRG clock is divided by 3. If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the clock is divided by 2 with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is a 1.8462 MHz clock.
Table 53 shows the baud rates possible with a 1.8462 MHz clock.

Table 53 - Baud Rates Using 1.8462 MHz Clock

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL*	CROC: BIT 7 OR 6
50	2307	0.03	X
75	1538	0.03	X
110	1049	0.005	X
134.5	858	0.01	X
150	769	0.03	X
300	384	0.16	X
600	192	0.16	X
1200	96	0.16	X
1800	64	0.16	X
2000	58	0.5	X
2400	48	0.16	X
3600	32	0.16	X
4800	24	0.16	X
7200	16	0.16	X
9600	12	0.16	X
19200	6	0.16	X
38400	3	0.16	X
57600	2	1.6	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

THE AFFECTS OF RESET ON THE UART REGISTERS

The RESET Function (Table 54) details the affects of RESET on each of the Serial Port registers.

Table 54 - RESET Function

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1 - 7 low
FIFO Control	RESET	All bits low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5 - 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4 - 7 input
TXD1, TXD2	RESET	High
INTRPT (RCVR errs)	RESET/Read LSR	Low

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/ReadIIR/Write THR	Low
OUT2B	RESET	High
RTSB	RESET	High
DTRB	RESET	High
OUT1B	RESET	High
RCVR FIFO	RESET/FCR1*FCR0/_FCR0	All bits low
XMIT FIFO	RESET/FCR1*FCR0/_FCR0	All bits low

FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = “1”, IER bit 0 = “1”), RCVR interrupts occur as follows:

1) The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.
2) The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.
3) The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.
4) The data ready bit (LSR bit 0)is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO time-out interrupts occur as follows:

1) A FIFO time-out interrupt occurs if all the following conditions exist:
   - at least one character is in the FIFO
   - The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay.)
   - The most recent CPU read of the FIFO was longer than 4 continuous character times ago.

2) This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12 bit character.
3) Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
4) When a time-out interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.
5) When a time-out interrupt has not occurred the time-out timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = “1”, IER bit 1 = “1”), XMIT interrupts occur as follows:

1) The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

2) The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character time-out and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO Polled Mode Operation

With FCR bit 0 = “1” resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user’s program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:

1) Bit 0=1 as long as there is one byte in the RCVR FIFO.
2) Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.
3) Bit 5 indicates when the XMIT FIFO is empty.
4) Bit 6 indicates that both the XMIT FIFO and shift register are empty.
5) Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or time-out condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Table 55 - Individual UART Channel Register Summary

REGISTER ADDRESS*	REGISTER NAME	REGISTER SYMBOL	BIT 0	BIT 1
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 1)	Data Bit 1
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	”0” if Interrupt Pending	Interrupt ID Bit
ADDR = 2	FIFO Control Register (Write Only)	FCR	FIFO Enable	RCVR FIFO Reset
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)
ADDR = 4	MODEM Control Register	MCR	Data Terminal Ready (DTR)	Request to Send (RTS)
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)
ADDR = 6	MODEM Status Register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)
ADDR = 7	Scratch Register (Note 4)	SCR	Bit 0	Bit 1
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9

*DLAB is Bit 7 of the Line Control Register (ADDR = 3).
Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
Note 2: When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Table 56 - Individual UART Channel Register Summary Continued

BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Enable Receiver Line Status Interrupt (ELSI)	Enable MODEM Status Interrupt (EMSI)	0	0	0	0
Interrupt ID Bit	Interrupt ID Bit (Note 5)	0	0	FIFOs Enabled (Note 5)	FIFOs Enabled (Note 5)
XMIT FIFO Reset	DMA Mode Select (Note 6)	Reserved	Reserved	RCVR Trigger LSB	RCVR Trigger MSB
Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
OUT1 (Note 3)	OUT2 (Note 3)	Loop	0	0	0
Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 2)	Error in RCVR FIFO (Note 5)
Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 3: This bit no longer has a pin associated with it.
Note 4: When operating in the XT mode, this register is not available.
Note 5: These bits are always zero in the non-FIFO mode.
Note 6: Writing a one to this bit has no effect. DMA modes are not supported in this chip.

Notes On Serial Port FIFO Mode Operation

GENERAL

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

TX AND RX FIFO OPERATION

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. **The UART will prevent loads to the Tx FIFO if it currently holds 16 characters.** Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. **Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt**

delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay.

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. **To prevent the software from having to check for this situation the chip incorporates a time-out interrupt.**

The time-out interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The time-out interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256K baud).

INFRARED INTERFACE

The FDC37N3869 infrared interface provides a two-way wireless communications port using infrared as the transmission medium. Several infrared protocols have been provided in this implementation including IrDA v1.1 (SIR/FIR), ASKIR, and Consumer IR (Figure 3). For more information consult the SMSC Infrared Communication Controller (IRCC) specification.

The IrDA v1.0 (SIR) and ASKIR formats are driven by the ACE registers found in UART2. The UART2 registers are described in section

SERIAL PORT (UART) starting on page 56. The base address for UART2 is programmed in CR25, the UART2 Base Address Register (see section CR25 on page 110).

The IrDA V1.2 (FIR) and Consumer IR formats are driven by the SCE registers. Descriptions of these registers can be found in the SMSC Infrared Communications Controller Specification. The Base Address for the SCE registers is programmed in CR2B, the SCE Base Address Register (see section CR28 on page 111).

IrDA SIR/FIR and ASKIR

IrDA SIR (v1.0) specifies asynchronous serial communication at baud rates up to 115.2Kbps. Each byte is sent serially LSB first beginning with a zero value start bit. A zero is signaled by sending a single infrared pulse at the beginning of the serial bit time. A one is signaled by the absence of an infrared pulse during the bit time. Please refer to section AC TIMING for the parameters of these pulses and the IrDA waveforms.

IrDA FIR (v1.2) includes IrDA v1.0 SIR and additionally specifies synchronous serial communications at data rates up to 4Mbps.

Data is transferred LSB first in packets that can be up to 2048 bits in length. IrDA v1.2 includes .576Mbps and 1.152Mbps data rates using an encoding scheme that is similar to SIR. The 4Mbps data rate uses a pulse position modulation (PPM) technique.

The ASKIR infrared allows asynchronous serial communication at baud rates up to 19.2Kbps. Each byte is sent serially LSB first beginning with a zero value start bit. A zero is signaled by sending a 500KHz carrier waveform for the duration of the serial bit time. A one is signaled by the absence of carrier during the bit time. Please refer to section AC TIMING for the parameters of the ASKIR waveforms.

Consumer IR

The FDC37N3869 Consumer IR interface is a general-purpose Amplitude Shift Keyed encoder/decoder with programmable carrier and bit-cell rates that can emulate many popular TV Remote encoding formats; including, 38KHz PPM, PWM and RC-5. The carrier frequency is programmable from 1.6MHz to 6.25KHz. The bit-cell rate range is 100KHz to 390Hz.

Hardware Interface

The FDC37N3869 IR hardware interface is shown in Figure 3. This interface supports two types of external FIR transceiver modules. One uses a mode pin (IR Mode) to program the data rate, while the other has a second Rx data pin (IRR3). The FDC37N3869 uses Pin 21 for these functions. Pin 21 has IR Mode and IRR3 as its first and second alternate function, respectively. These functions are selected through CR29 as shown in Table 57.

Table 57 - FIR Transceiver Module-Type Select

HP MODE[1]	FUNCTION
0	IR Mode
1	IRR3

Note[1]: HPMODE is CR29, BIT 4 (see section CR29 on page 112). Refer to the Infrared Interface Block Diagram on the following page for HPMODE implementation.

The FAST bit is used to select between the SIR mode and FIR mode receiver, regardless of the transceiver type. If FAST = 1, the FIR mode receiver is selected; if FAST = 0, the SIR mode receiver is selected (Table 58).

Table 58 - IR Rx Data Pin Selection

CONTROL SIGNALS		INPUTS	
FAST	HPMODE	RX1	RX2
0	X	RX1=RXD2	RX2=IRRX2
X	0	RX1=RXD2	RX2=IRRX2
1	1	RX1=IR Mode/IRR3	RX2=IR Mode/IRR3

IR Half Duplex Turnaround Delay Time

If the Half Duplex option is chosen there is an IR Half Duplex Time-out that constrains IRCC direction mode changes. This time-out starts as each bit is transferred and prevents direction mode changes until the time-out expires. The timer is restarted whenever new data arrives in the current direction mode. For example, if data is loaded into the transmit buffer while a character is being received, the transmission will not start until the last bit has been received and the time-out expires. If the start bit of another character is received during this time-out, the timer is restarted after the new character is received. The Half Duplex Time-out is programmable from 0 to 25.5ms in 100µs increments (see section CR2D on page 112).

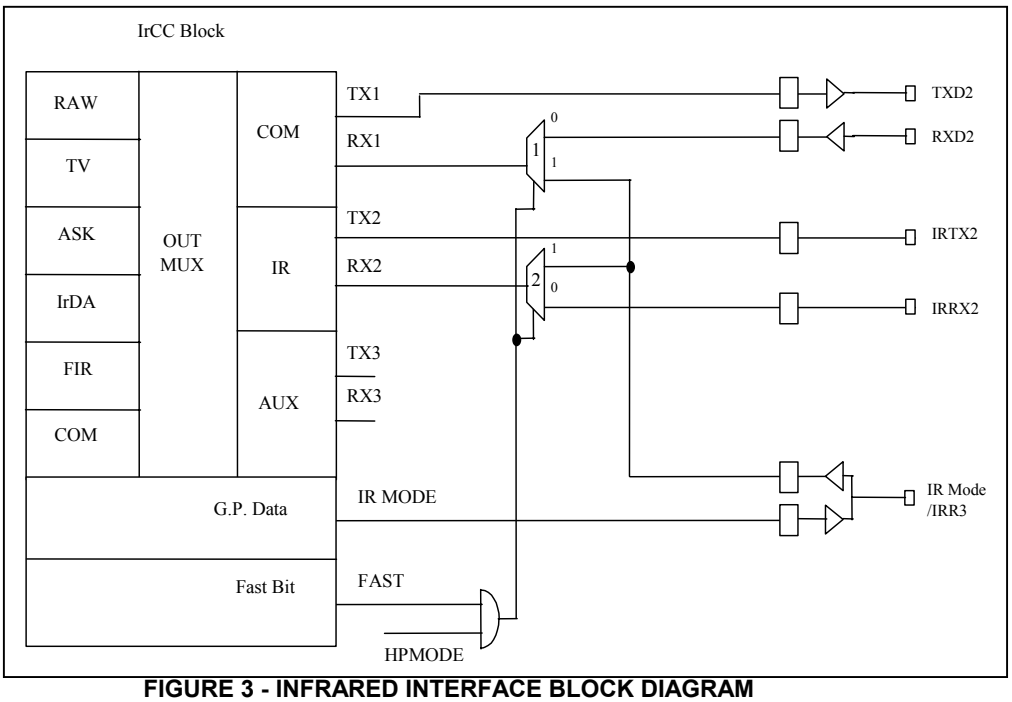


FIGURE 3 - INFRARED INTERFACE BLOCK DIAGRAM

PARALLEL PORT

The FDC37N3869 incorporates an IBM XT/AT compatible parallel port. The FDC37N3869 supports the optional PS/2 type bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) parallel port modes. Refer to the FDC37N3869 Configuration Registers and the following hardware configuration description for information on disabling, powering down, changing the base address, and selecting the mode of operation of the parallel port.

The FDC37N3869 also incorporates SMSC's ChiProtect circuitry, which prevents possible damage to the parallel port due to printer power-up.

The functionality of the Parallel Port is achieved through the use of eight addressable ports, with their associated registers and control gating. The control and data port are read/write by the CPU, the status port is read/write in the EPP mode. The address map and bit encoding of the Parallel Port registers is shown in Table 59; the Parallel Port Connector is shown in Table 63.

Table 59 - Parallel Port Registers

	BASE ADDRESS OFFSET	D0	D1	D2	D3	D4	D5	D6	D7
DATA PORT[1]	00H	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
STATUS PORT[1]	01H	TMOUT	0	0	nERR	SLCT	PE	nACK	nBUSY
CONTROL PORT[1]	02H	STROBE	AUTOFD	nINIT	SLC	IRQE	PCD	0	0
EPP ADDR PORT[2,3]	03H	PD0	PD1	PD2	PD3	PD4	PD5	PD6	AD7
EPP DATA PORT 0[2,3]	04H	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
EPP DATA PORT 1[2,3]	05H	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
EPP DATA PORT 2[2,3]	06H	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
EPP DATA PORT 3[2,3]	07H	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7

Note[1]: These registers are available in all modes.
Note[2]: These registers are only available in EPP mode.
Note[3]: For EPP mode, IOCHRDY must be connected to the ISA bus.

Table 60 - Parallel Port Connector

HOST CONNECTOR	PIN NUMBER	STANDARD	EPP	ECP
1	75	nStrobe	nWrite	nStrobe
2-9	69-66, 64-61	PData<0:7>	PData<0:7>	PData<0:7>
10	60	nAck	Intr	nAck
11	59	Busy	nWait	Busy, PeriphAck(3)
12	58	PE	(NU)	PError, nAckReverse(3)
13	57	Select	(NU)	Select
14	74	nAutofd	nDatastb	nAutoFd, HostAck(3)
15	73	nError	(NU)	nFault(1) nPeriphRequest(3)
16	72	nInit	(NU)	nInit(1) nReverseRqst(3)
17	71	nSelectin	nAddrstrb	nSelectIn(1,3)

(1) = Compatible Mode
(3) = High Speed Mode

Note: For the cable interconnection required for ECP support and the Slave Connector pin numbers, refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.09, Jan. 7, 1993. This document is available from Microsoft.

IBM Xt/At Compatible, Bi-Directional And Epp Modes

DATA PORT

ADDRESS OFFSET = 00H

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus with the rising edge of the nIOW input. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation in SPP mode, PD0 - PD7 ports are buffered (not latched) and output to the host CPU.

STATUS PORT

ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. The contents of this register are latched for the duration of an nIOR read cycle. The bits of the Status Port are defined as follows:

BIT 0 TMOUT - TIME OUT

This bit is valid in EPP mode only and indicates that a 10 usec time out has occurred on the EPP bus. A logic "0" means that no time out error has occurred; a logic "1" means that a time out error has been detected. This bit is cleared by a RESET. Writing a one to this bit clears the time out status bit. On a write, this bit is self clearing and does not require a write of a zero. Writing a zero to this bit has no effect.

BITS 1, 2 - are not implemented as register bits, during a read of the Printer Status Register these bits are a low level.

BIT 3 nERR - nERROR

The level on the nERROR input is read by the CPU as bit 3 of the Printer Status Register. A logic "0" means an error has been detected; a logic "1" means no error has been detected.

BIT 4 SLCT - PRINTER SELECTED STATUS

The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic "1" means the printer is on line; a logic "0" means it is not selected.

BIT 5 PE - PAPER END

The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic “1” indicates a paper end; a logic “0” indicates the presence of paper.

BIT 6 nACK - nACKNOWLEDGE
The level on the nACK input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the printer has received a character and can now accept another. A logic “1” means that it is still processing the last character or has not received the data.

BIT 7 nBUSY - nBUSY
The complement of the level on the nBUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic 0 in this bit means that the printer is busy and cannot accept a new character. A logic “1” means that it is ready to accept the next character.

CONTROL PORT

ADDRESS OFFSET = 02H
The Control Port is located at an offset of ‘02H’ from the base address. The Control Register is initialized by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the nSTROBE output.

BIT 1 AUTOFD – AUTOFEED
This bit is inverted and output onto the nAUTOFD output. A logic “1” causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 nINIT - nINITIATE OUTPUT
This bit is output onto the nINIT output without inversion.

BIT 3 SLCTIN - PRINTER SELECT INPUT
This bit is inverted and output onto the nSLCTIN output. A logic “1” on this bit selects the printer; a logic “0” means the printer is not selected.

BIT 4 IRQE - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going nACK input. When the IRQE bit is programmed low the IRQ is disabled.

BIT 5 PCD - PARALLEL CONTROL DIRECTION
Parallel Control Direction is valid in extended mode only (CR#1<3>=0). In printer mode, the direction is always out regardless of the state of this bit. In bi-directional mode, a logic “0” means that the printer port is in output mode (write); a logic “1” means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

EPP ADDRESS PORT

ADDRESS OFFSET = 03H
The EPP Address Port is located at an offset of ‘03H’ from the base address. The address register is cleared at initialization by RESET. During a WRITE operation, the contents of DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports, the leading edge of nIOW causes an EPP ADDRESS WRITE cycle to be performed, the trailing edge of IOW latches the data for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read, the leading edge of IOR causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the deassertion of ADDRSTB latches the PData for the duration of the IOR cycle. This register is only available in EPP mode.

EPP DATA PORT 0

ADDRESS OFFSET = 04H

The EPP Data Port 0 is located at an offset of '04H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the contents of DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports, the leading edge of nIOW causes an EPP DATA WRITE cycle to be performed, the trailing edge of IOW latches the data for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read, the leading edge of IOR causes an EPP READ cycle to be performed and the data output to the host CPU, the deassertion of DATASTB latches the PData for the duration of the IOR cycle. This register is only available in EPP mode.

EPP DATA PORT 1

ADDRESS OFFSET = 05H

The EPP Data Port 1 is located at an offset of '05H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP DATA PORT 2

ADDRESS OFFSET = 06H

The EPP Data Port 2 is located at an offset of '06H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP DATA PORT 3

ADDRESS OFFSET = 07H

The EPP Data Port 3 is located at an offset of '07H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP 1.9 Operation

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10μsec have elapsed from the start of the EPP cycle (nIOR or nIOW asserted) to nWAIT being deasserted (after command). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

During an EPP cycle, if STROBE is active, it overrides the EPP write signal forcing the PDx bus to always be in a write mode and the nWRITE signal to always be asserted.

SOFTWARE CONSTRAINTS

Before an EPP cycle is executed, the software must ensure that the control register bit PCD is a logic "0" (i.e. a 04H or 05H should be written to the Control port). If the user leaves PCD as a logic "1", and attempts to perform an EPP write, the chip is unable to perform the write (because PCD is a logic "1") and will appear to perform an EPP read on the parallel bus, no error is indicated.

EPP 1.9 WRITE

The timing for a write operation (address or data) is shown in timing diagram EPP 1.9 Write Data or Address cycle. IOCHRDY is driven active low at the start of each EPP write and is released when it has been determined that the write cycle can complete. The write cycle can complete under the following circumstances:

1) If the EPP bus is not ready (nWAIT is active low) when nDATASTB or nADDRSTB goes active then the write can complete when nWAIT goes inactive high.
2) If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of nDATASTB, nWRITE or nADDRSTB. The write can complete once nWAIT is determined inactive.

Write Sequence of Operation

1) The host selects an EPP register, places data on the SData bus and drives nIOW active.
2) The chip drives IOCHRDY inactive (low).
3) If WAIT is not asserted, the chip must wait until WAIT is asserted.
4) The chip places address or data on PData bus, clears PDIR, and asserts nWRITE.
5) Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
6) Peripheral deasserts nWAIT, indicating that any setup requirements have been satisfied and the chip may begin the termination phase of the cycle.
7) A) The chip deasserts nDATASTB or nADDRSTRB, this marks the beginning of the termination phase. If it has not already done so, the peripheral should latch the information byte now.
   B) The chip latches the data from the SData bus for the PData bus and asserts (releases) IOCHRDY allowing the host to complete the write cycle.
8) Peripheral asserts nWAIT, indicating to the host that any hold time requirements have been satisfied and acknowledging the termination of the cycle.
9) Chip may modify nWRITE and nPDATA in preparation for the next cycle.

EPP 1.9 READ

The timing for a read operation (data) is shown in timing diagram EPP Read Data cycle. IOCHRDY is driven active low at the start of each EPP read and is released when it has been determined that the read cycle can complete.

The read cycle can complete under the following circumstances:

1) If the EPP bus is not ready (nWAIT is active low) when nDATASTB goes active then the read can complete when nWAIT goes inactive high.
2) If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of WRITE or before nDATASTB goes active. The read can complete once nWAIT is determined inactive.

Read Sequence of Operation

1) The host selects an EPP register and drives nIOR active.
2) The chip drives IOCHRDY inactive (low).
3) If WAIT is not asserted, the chip must wait until WAIT is asserted.
4) The chip tri-states the PData bus and deasserts nWRITE.
5) Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
6) Peripheral drives PData bus valid.
7) Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
8) A) The chip latches the data from the PData bus for the SData bus, deasserts DATASTB or nADDRSTRB, this marks the beginning of the termination phase.

   B) The chip drives the valid data onto the SData bus and asserts (releases) IOCHRDY allowing the host to complete the read cycle.
9) Peripheral tri-states the PData bus and asserts nWAIT, indicating to the host that the PData bus is tri-stated.
10) Chip may modify nWRITE, PDIR and nPDATA in preparation for the next cycle.

EPP 1.7 Operation

When the EPP 1.7 mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than10usec have elapsed from the start of the EPP cycle (nIOR or nIOW asserted) to the end of the cycle nIOR or nIOW deasserted). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

SOFTWARE CONSTRAINTS

Before an EPP cycle is executed, the software must ensure that the control register bits D0, D1 and D3 are set to zero. Also, bit D5 (PCD) is a logic “0” for an EPP write or a logic “1” for and EPP read.

EPP 1.7 WRITE

The timing for a write operation (address or data) is shown in timing diagram EPP 1.7 Write Data or Address cycle. IOCHRDY is driven active low when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The write cycle can complete when nWAIT is inactive high.

Write Sequence of Operation

1) The host sets PDIR bit in the control register to a logic “0”. This asserts nWRITE.
2) The host selects an EPP register, places data on the SData bus and drives nIOW active.
3) The chip places address or data on PData bus.
4) Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
5) If nWAIT is asserted, IOCHRDY is deasserted until the peripheral deasserts nWAIT or a time-out occurs.
6) When the host deasserts nI0W the chip deasserts nDATASTB or nADDRSTRB and latches the data from the SData bus for the PData bus.
7) Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

EPP 1.7 READ

The timing for a read operation (data) is shown in timing diagram EPP 1.7 Read Data cycle. IOCHRDY is driven active low when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The read cycle can complete when nWAIT is inactive high.

Read Sequence of Operation

1) The host sets PDIR bit in the control register to a logic “1”. This deasserts nWRITE and tri-states the PData bus.
2) The host selects an EPP register and drives nIOR active.
3) Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
4) If nWAIT is asserted, IOCHRDY is deasserted until the peripheral deasserts nWAIT or a time-out occurs.
5) The Peripheral drives PData bus valid.
6) The Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
7) When the host deasserts nI0R the chip deasserts nDATASTB or nADDRSTRB.
8) Peripheral tri-states the PData bus.
9) Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

Table 61 - EPP Pin Descriptions

EPP SIGNAL	EPP NAME	TYPE	DESCRIPTION
nWRITE	nWrite	O	This signal is active low. It denotes a write operation.
PD<0:7>	Address/Data	I/O	Bi-directional EPP byte wide address and data bus.
INTR	Interrupt	I	This signal is active high and positive edge triggered. (Pass through with no inversion, Same as SPP).
WAIT	nWait	I	This signal is active low. It is driven inactive as a positive acknowledgment from the device that the transfer of data is completed. It is driven active as an indication that the device is ready for the next transfer.
DATASTB	nData Strobe	O	This signal is active low. It is used to denote data read or write operation.
RESET	nReset	O	This signal is active low. When driven active, the EPP device is reset to its initial operational mode.
ADDRSTB	nAddress Strobe	O	This signal is active low. It is used to denote address read or write operation.
PE	Paper End	I	Same as SPP mode.
SLCT	Printer Selected Status	I	Same as SPP mode.
NERR	Error	I	Same as SPP mode.
PDIR	Parallel Port Direction	O	This output shows the direction of the data transfer on the parallel port bus. A low means an output/write condition and a high means an input/read condition. This signal is normally a low (output/write) unless PCD of the control register is set or if an EPP read cycle is in progress.

Note 1: SPP and EPP can use 1 common register.

Note 2: nWrite is the only EPP output that can be over-ridden by SPP control port during an EPP cycle. For correct EPP read cycles, PCD is required to be a low.

Extended Capabilities Parallel Port

ECP provides a number of advantages, some of which are listed below. The individual features are explained in greater detail in the remainder of this section.

- High performance half-duplex forward and reverse channel
- Interlocked handshake, for fast reliable transfer
- Optional single byte RLE compression for improved throughput (64:1)
- Channel addressing for low-cost peripherals
- Maintains link and data layer separation
- Permits the use of active output drivers
- Permits the use of adaptive signal timing
- Peer-to-peer capability

VOCABULARY

The following terms are used in this document:

assert When a signal asserts it transitions to a "true" state, when a signal deasserts it transitions to a "false" state.
forward Host to Peripheral communication.
reverse Peripheral to Host communication.
Pword A port word; equal in size to the width of the ISA interface. For this implementation, PWord is always 8 bits.
1 A high level
0 A low level

These terms may be considered synonymous:

- PeriphClk, nAck
- HostAck, nAutoFd
- PeriphAck, Busy
- nPeriphRequest, nFault
- nReverseRequest, nInit
- nAckReverse, PError
- Xflag, Select
- ECPMode, nSelectIn
- HostClk, nStrobe

Reference Document:
IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev 1.09, Jan 7, 1993. This document is available from Microsoft. The bit map of the Extended Parallel Port registers is shown in Table 65.

Table 62 - ECP Registers

	D7	D6	D5	D4	D3	D2	D1	D0
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
ecpAFifo[2]	Addr/RLE	Address or RLE field						
dsr[1]	nBusy	nAck	PError	Select	nFault	0	0	0
dcr[1]	0	0	Direction	ackIntEn	SelectIn	nInit	autofd	strobe
cFifo[2]	Parallel Port Data FIFO							
ecpDFifo[2]	ECP Data FIFO							
tFifo[2]	Test FIFO							
cnfgA	0	0	0	1	0	0	0	0
cnfgB	compress	intrValue	IRQ Software Select			DMA Software Select		
ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty

Note[1]: These registers are available in all modes.
Note[2]: All FIFOs use one common 16 byte FIFO.

ISA IMPLEMENTATION STANDARD

This specification describes the standard ISA interface to the Extended Capabilities Port (ECP). All ISA devices supporting ECP must meet the requirements contained in this section or the port will not be supported by Microsoft. For a description of the ECP Protocol, please refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.09, Jan.7, 1993. This document is available from Microsoft.

DESCRIPTION

The port is software and hardware compatible with existing parallel ports so that it may be used as a standard LPT port if ECP is not required. The port is designed to be simple and requires a small number of gates to implement. It does not do any "protocol" negotiation, rather it provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward and reverse directions.

Small FIFOs are employed in both forward and reverse directions to smooth data flow and improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes deep. The port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The port also supports run length encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. Hardware support for compression is optional.

Table 63 - ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
nSTROBE	O	During write operations nSTROBE registers data or address into the slave on the asserting edge (handshakes with Busy).
Pdata 7:0	I/O	Contains address or data or RLE data.
nACK	I	Indicates valid data driven by the peripheral when asserted. This signal handshakes with nAUTOFD in reverse.
PeriphAck (Busy)	I	This signal deasserts to indicate that the peripheral can accept data. This signal handshakes with nStrobe in the forward direction. In the reverse direction this signal indicates whether the data lines contain ECP command information or data. The peripheral uses this signal to flow control in the forward direction. It is an "interlocked" handshake with nStrobe. PeriphAck also provides command information in the reverse direction.
Perror (nAckReverse)	I	Used to acknowledge a change in the direction the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. It is an "interlocked" handshake with nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select	I	Indicates printer on line.
nAUTOFD (HostAck)	O	Requests a byte of data from the peripheral when asserted, handshaking with nACK in the reverse direction. In the forward direction this signal indicates whether the data lines contain ECP address or data. The host drives this signal to flow control in the reverse direction. It is an "interlocked" handshake with nACK. HostAck also provides command information in the forward phase.
nFAULT (nPeriphRequest)	I	Generates an error interrupt when asserted. This signal provides a mechanism for peer-to-peer communication. This signal is valid only in the forward direction. During ECP Mode the peripheral is permitted (but not required) to drive this pin low to request a reverse transfer. The request is merely a "hint" to the host; the host has ultimate control over the transfer direction. This signal would be typically used to generate an interrupt to the host CPU.
nINIT	O	Sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. The peripheral is only allowed to drive the bi-directional data bus while in ECP Mode and HostAck is low and nSelectIn is high.
nSELECTIN	O	Always deasserted in ECP mode.

REGISTER DEFINITIONS

The register definitions are based on the standard IBM addresses for LPT. All of the standard printer ports are supported. The additional registers attach to an upper bit decode of the standard LPT port definition to avoid conflict

with standard ISA devices. The port is equivalent to a generic parallel port interface and may be operated in that mode. The port registers vary depending on the mode field in the ecr (Table 68). Table 67 lists these dependencies. Operation of the devices in modes other that those specified is undefined.

Table 64 - ECP Register Definitions

NAME	ADDRESS (Note 1)	ECP MODES	FUNCTION
data	+000h R/W	000-001	Data Register
ecpAFifo	+000h R/W	011	ECP FIFO (Address)
dsr	+001h R/W	All	Status Register
dcr	+002h R/W	All	Control Register
cFifo	+400h R/W	010	Parallel Port Data FIFO
ecpDFifo	+400h R/W	011	ECP FIFO (DATA)
tFifo	+400h R/W	110	Test FIFO
cnfgA	+400h R	111	Configuration Register A
cnfgB	+401h R/W	111	Configuration Register B
ecr	+402h R/W	All	Extended Control Register

Note 1: These addresses are added to the parallel port base address as selected by configuration register or jumpers.
Note 2: All addresses are qualified with AEN. Refer to the AEN pin definition.

Table 65 - Mode Descriptions

MODE	DESCRIPTION (Refer to ECR Register Description)
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the configuration registers)
101	(Reserved)
110	Test mode
111	Configuration mode

DATA and ecpAFifo PORT

ADDRESS OFFSET = 00H
Modes 000 and 001 (Data Port)
The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus on the rising edge of the nIOW input. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.

Mode 011 (ECP FIFO - Address/RLE)
A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is only defined for the forward direction (direction is 0). Refer to the ECP Parallel Port Forward Timing Diagram, located in the Timing Diagrams section of this data sheet.

Device Status Register (dsr)

ADDRESS OFFSET = 01H
The Status Port is located at an offset of '01H' from the base address. Bits 0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

BIT 3 nFault
The level on the nFault input is read by the CPU as bit 3 of the Device Status Register.

BIT 4 Select
The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

BIT 5 PError
The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

BIT 6 nAck
The level on the nAck input is read by the CPU as bit 6 of the Device Status Register.

BIT 7 nBusy
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

Device Control Register (dcr)

ADDRESS OFFSET = 02H
The Control Register is located at an offset of '02H' from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the nSTROBE output.

BIT 1 AUTOFD - AUTOFEED
This bit is inverted and output onto the nAUTOFD output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 nINIT - nINITIATE OUTPUT
This bit is output onto the nINIT output without inversion.

BIT 3 SELECTIN
This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 ackIntEn - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU due to a low to high transition on the nACK input.

Refer to the description of the interrupt under Operation, Interrupts.

BIT 5 DIRECTION
If mode=000 or mode=010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, Direction is valid and a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

BITS 6 AND 7
during a read are a low level, and cannot be written.

cFifo (Parallel Port Data FIFO)

ADDRESS OFFSET = 400h
Mode = 010
Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

ecpDFifo (ECP Data FIFO)

ADDRESS OFFSET = 400H
Mode = 011
Bytes written or DMAed from the system to this FIFO, when the direction bit is 0, are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

Data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO when the direction bit is 1. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

tFifo (Test FIFO Mode)

ADDRESS OFFSET = 400H
Mode = 110
Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction.

Data in the tFIFO will not be transmitted to the to the parallel port lines using a hardware protocol handshake. However, data in the tFIFO may be displayed on the parallel port data lines.

The tFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full tFIFO, the new data is not accepted into the tFIFO. If an attempt is made to read data from an empty tFIFO, the last data byte is re-read again. The full and empty bits must always keep track of the correct FIFO state. The tFIFO will transfer data at the maximum ISA rate so that software may generate performance metrics.

The FIFO size and interrupt threshold can be determined by writing bytes to the FIFO and checking the full and serviceIntr bits.

The writeIntrThreshold can be determined by starting with a full tFIFO, setting the direction bit to 0 and emptying it a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readIntrThreshold can be determined by setting the direction bit to 1 and filling the empty tFIFO a byte at a time until **serviceIntr** is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

Data bytes are always read from the head of tFIFO regardless of the value of the direction bit. For example if 44h, 33h, 22h is written to the FIFO, then reading the tFIFO will return 44h, 33h, 22h in the same order as was written.

cnfgA (Configuration Register A)

ADDRESS OFFSET = 400H
Mode = 111
This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation. (PWord = 1 byte)

cnfgB (Configuration Register B)

ADDRESS OFFSET = 401H
Mode = 111

BIT 7 compress
This bit is read only. During a read it is a low level. This means that this chip does not support hardware RLE compression. It does support hardware de-compression!

BIT 6 intrValue
Returns the value on the ISA iRq line to determine possible conflicts.

BITS 2:0 DMA Software Select
The DMA Software Select bits indicate the DMA channel number that has been allocated to the Parallel Port. The channel encoding is shown in Table 66. The DMA Software select bits shadow the ECP DMA Select bits in the ECP Software Select register CR22.

Table 66 - DMA Software Select Encoding

DMA SELECTED	DMA Software Select (cnfgB)		
	D2	D1	D0
3	0	1	1
2	0	1	0
1	0	0	1
Other	0	0	0

BITS 5:3 IRQ Software Select
The IRQ Software Select bits indicate the IRQ channel number that has been allocated to the Parallel Port. The IRQ encoding is shown in Table 67. The IRQ Software select bits shadow the ECP IRQ Select bits in the ECP Software Select register CR22.

Table 67 - IRQ Software Select Encoding

IRQ SELECTED	IRQ Software Select (cnfgB)		
	D5	D4	D3
15	1	1	0
14	1	0	1
11	1	0	0
10	0	1	1
9	0	1	0
7	0	0	1
5	1	1	1
Other	0	0	0

ecr (Extended Control Register)

ADDRESS OFFSET = 402H
Mode = all
This register controls the extended ECP parallel port functions (Table 69).

BITS 7,6,5
These bits are Read/Write and select the Mode.

BIT 4 nErrIntrEn
Read/Write (Valid only in ECP Mode)

1: Disables the interrupt generated on the asserting edge of nFault.
0: Enables an interrupt pulse on the high to low edge of nFault. Note that an interrupt will be generated if nFault is asserted (interrupting) and this bit is written from a "1" to a "0". This prevents interrupts from being lost in the time between the read of the ecr and the write of the ecr.

BIT 3 dmaEn
Read/Write

1: Enables DMA (DMA starts when serviceIntr is "0").
0: Disables DMA unconditionally.

BIT 2 serviceIntr
Read/Write

1: Disables DMA and all of the service interrupts.
0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred serviceIntr bit shall be set to a "1" by hardware, it must be reset to "0" to re-enable the interrupts. Writing this bit to a "1" will not cause an interrupt.

   case dmaEn=1:
   During DMA (this bit is set to a "1" when terminal count is reached).

   case dmaEn=0 direction=0:
   This bit shall be set to "1" whenever there are writeIntrThreshold or more bytes free in the FIFO.

   case dmaEn=0 direction=1:
   This bit shall be set to "1" whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.

BIT 1 full
Read only

1: The FIFO cannot accept another byte or the FIFO is completely full.
0: The FIFO has at least 1 free byte.

BIT 0 empty
Read only

1: The FIFO is completely empty.
0: The FIFO contains at least 1 byte of data.

Table 68 - Extended Control Register

R/W	MODE
000:	Standard Parallel Port mode. In this mode the FIFO is reset and common collector drivers are used on the control lines (nStrobe, nAutoFd, nInit and nSelectIn). Setting the direction bit will not tri-state the output drivers in this mode.
001:	PS/2 Parallel Port mode. Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. All drivers have active pull-ups (push-pull).
010:	Parallel Port FIFO mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull).
011:	ECP Parallel Port Mode. In the forward direction (direction is 0) bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. In the reverse direction (direction is 1) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. All drivers have active pull-ups (push-pull).
100:	Selects EPP Mode: In this mode, EPP is selected if the EPP supported option is selected in configuration register CR4. All drivers have active pull-ups (push-pull).
101:	Reserved
110:	Test Mode. In this mode the FIFO may be written and read, but the data will not be transmitted on the parallel port. All drivers have active pull-ups (push-pull).
111:	Configuration Mode. In this mode the confgA, confgB registers are accessible at 0x400 and 0x401. All drivers have active pull-ups (push-pull).

OPERATION

Mode Switching/Software Control

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

Once in an extended forward mode the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In this case all control signals will be deasserted before the mode switch. In an ECP reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001. Since the automatic hardware ECP reverse handshake only cares about the state of the FIFO it may have acquired extra data which will be discarded. It may in fact be in the middle of a transfer when the mode is changed back to 000 or 001. In this case the port will deassert nAutoFd independent of the state of the transfer. The design shall not cause glitches on the handshake signals if the software meets the constraints above.

ECP Operation

Prior to ECP operation the Host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol. This is a somewhat complex negotiation carried out under program control in mode 000. After negotiation, it is necessary to initialize some of the port bits. The following are required:

- Set Direction = 0, enabling the drivers.
- Set strobe = 0, causing the nStrobe signal to default to the deasserted state.
- Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.
- Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo respectively.

Note that all FIFO data transfers are byte wide and byte aligned. Address/RLE transfers are byte-wide and only allowed in the forward direction.

The host may switch directions by first switching to mode = 001, negotiating for the forward or reverse channel, setting direction to 1 or 0, then setting mode = 011. When direction is 1 the hardware shall handshake for each ECP read data byte and attempt to fill the FIFO. Bytes may then be read from the ecpDFifo as long as it is not empty .

ECP transfers may also be accomplished (albeit slowly) by handshaking individual bytes under program control in mode = 001, or 000.

Termination from ECP Mode

Termination from ECP Mode is similar to the termination from Nibble/Byte Modes. The host is permitted to terminate from ECP Mode only in specific well-defined states. The termination can only be executed while the bus is in the forward direction. To terminate while the channel is in the reverse direction, it must first be transitioned into the forward direction.

Command/Data

ECP Mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8 bit data or 8-bit commands (Table 70).

When in the forward direction, normal data is transferred when HostAck is high and an 8 bit command is transferred when HostAck is low.

The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address.

When in the reverse direction, normal data is transferred when PeriphAck is high and an 8 bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero. Reverse channel addresses are seldom used and may not be supported in hardware.

Table 69 - Forward Channel Commands (HostAck Low) Reverse Channel Commands (PeripAck Low) Data Compression

D7	D[6:0]
0	Run-Length Count (0-127) (mode 0011 0X00 only)
1	Channel Address (0-127)

The FDC37N3869 supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. A run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

Pin Definition

The drivers for nStrobe, nAutoFd, nInit and nSelectIn are open-collector in mode 000 and are push-pull in all other modes.

ISA Connections

The interface can never stall causing the host to hang. The width of data transfers is strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundary. (The PWord value can be obtained by reading Configuration Register A, cnfgA, described in the next section). Single byte wide transfers are always possible with standard or PS/2 mode using program control of the control signals.

Interrupts
The interrupts are enabled by **serviceIntr** in the **ecr** register.

serviceIntr = 1 Disables the DMA and all of the service interrupts.

serviceIntr = 0Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupt is generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

The interrupt generated is ISA friendly in that it must pulse the interrupt line low, allowing for interrupt sharing. After a brief pulse low following the interrupt event, the interrupt line is tri-stated so that other interrupts may assert.
An interrupt is generated when:

1) For DMA transfers: When **serviceIntr** is 0, dmaEn is 1 and the DMA TC is received.
2) For Programmed I/O:
   a. When **serviceIntr** is "0", dmaEn is "0", direction is "0" and there are writeIntrThreshold or more free bytes in the FIFO. Also, an interrupt is generated when **serviceIntr** is cleared to "0" whenever there are writeIntrThreshold or more free bytes in the FIFO.

   b(1) When **serviceIntr** is 0, dmaEn is 0, direction is "1" and there are readIntrThreshold or more bytes in the FIFO. Also, an interrupt is generated when **serviceIntr** is cleared to "0" whenever there are readIntr Threshold or more bytes in the FIFO.
3) When nErrIntrEn is "0" and nFault transitions from high to low or when nErrIntrEn is set from "1" to "0" and nFault is asserted.
4) When ackIntEn is "1" and the nAck signal transitions from a low to a high.

FIFO Operation
The FIFO threshold is set in the chip configuration registers. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. (FIFO test mode will be addressed separately.) After a reset, the FIFO is disabled. Each data byte is transferred by a Programmed I/O cycle or PDRQ depending on the selection of DMA or Programmed I/O mode.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.
A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

Dma Transfers

Note:
PDRQ - Currently selected Parallel Port DRQ channel
nPDACK - Currently selected Parallel Port DACK channel
PINTR - Currently selected Parallel Port IRQ channel

Typical DMA Mode Transfers
DMA transfers are always to or from the ecpDFifo, tFifo or CFifo. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets dmaEn to "1" and **serviceIntr** to "0". The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, disabling DMA. In order to prevent possible blocking of refresh requests dReq shall not be asserted for more than 32 DMA cycles in a row. The FIFO is enabled directly by asserting nPDACK and addresses need not be valid. PINTR is generated when a TC is received. PDRQ must not be asserted for more than 32 DMA cycles in a row. After the 32nd cycle, PDRQ must be kept unasserted until nPDACK is deasserted for a minimum of 350nsec. (Note: The only way to properly terminate DMA transfers is with a TC).

DMA may be disabled in the middle of a transfer by first disabling the host DMA controller. Then setting serviceIntr to 1, followed by setting dmaEn to 0, and waiting for the FIFO to become empty or full.

Restarting the DMA is accomplished by enabling DMA in the host, setting dmaEn to 1, followed by setting serviceIntr to 0.

DMA Mode - Transfers from the FIFO to the Host
(**Note:** In the reverse mode, the peripheral may not continue to fill the FIFO if it runs out of data to transfer, even if the chip continues to request more data from the peripheral).

The ECP activates the PDRQ pin whenever there is data in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The ECP will deactivate the PDRQ pin when the FIFO becomes empty or when the TC becomes true (qualified by nPDACK), indicating that no more data is required. PDRQ goes inactive after nPDACK goes active for the last byte of a data transfer (or on the active edge of nIOR, on the last byte, if no edge is present on nPDACK). If PDRQ goes inactive due to the FIFO going empty, then PDRQ is active again as soon as there is one byte in the FIFO. If PDRQ goes inactive due to the TC, then PDRQ is active again when there is one byte in the FIFO, and **serviceIntr** has been re-enabled. (Note: A data underrun may occur if PDRQ is not removed in time to prevent an unwanted cycle).

Programmed I/O Mode or Non-DMA Mode
The ECP or parallel port FIFOs may also be operated using interrupt driven programmed I/O. Software can determine the writeIntrThreshold, readIntrThreshold, and FIFO depth by accessing the FIFO in Test Mode.

Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. To use the programmed I/O transfers, the host first sets up the direction and state, sets dmaEn to 0 and **serviceIntr** to 0.

The ECP requests programmed I/O transfers from the host by activating the PINTR pin. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

Note: A threshold of 16 is equivalent to a threshold of 15. These two cases are treated the same.

Programmed I/O - Transfers from the FIFO to the Host
In the reverse direction an interrupt occurs when serviceIntr is 0 and readIntrThreshold bytes are available in the FIFO. If at this time the FIFO is full it can be emptied completely in a single burst, otherwise readIntrThreshold bytes may be read from the FIFO in a single burst.

readIntrThreshold =(16-<threshold>) data bytes in FIFO

An interrupt is generated when **serviceIntr** is 0 and the number of bytes in the FIFO is greater than or equal to (16-<threshold>). (If the threshold = 12, then the interrupt is set whenever there are 4-16 bytes in the FIFO.) The PINT pin can be used for interrupt-driven systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. If at this time the FIFO is full, it can be completely emptied in a single burst, otherwise a minimum of (16-<threshold>) bytes may be read from the FIFO in a single burst.

Programmed I/O - Transfers from the Host to the FIFO
In the forward direction an interrupt occurs when serviceIntr is 0 and there are writeIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit needs to be re-read. Otherwise it may be filled with writeIntrThreshold bytes.

writeIntrThreshold = (16-<threshold>) free bytes in FIFO

An interrupt is generated when **serviceIntr** is 0 and the number of bytes in the FIFO is less than or equal to <threshold>. (If the threshold = 12, then the interrupt is set whenever there are 12 or less bytes of data in the FIFO.) The PINT pin can be used for interrupt-driven systems. The host must respond to the request by writing data to the FIFO. If at this time the FIFO is empty, it can be completely filled in a single burst, otherwise a minimum of (16-<threshold>) bytes may be written to the FIFO in a single burst. This process is repeated until the last byte is transferred into the FIFO.

AUTO POWER MANAGEMENT

Power management is provided for the following FDC37N3869 logical devices: Floppy Disk, UART1, UART2 and the Parallel Port. For each logical device two types of power management are provided; direct powerdown and auto powerdown.

Direct powerdown is controlled by the powerdown bits in the configuration registers. One bit is provided for each logical device. Auto powerdown can be enabled for each logical device by setting the Auto Powerdown Enable bits in the configuration registers. In addition, a chip-level hardware powerdown function has been provided through the PWRGD pin. Refer to Table 1 and to other descriptions of the PWRGD function, for example section CONFIGURATION, for more information.

FDC Power Management

Direct FDC power management is controlled by *FDC Power* (bit 3) of Configuration Register 0 (see section CR00 on page 99). FDC auto power management is enabled by *Floppy Disk Enable* (bit 7) in CR7 (see section CR07 on page 103). An internal timer is activated as soon as auto power management is enabled. During the timer countdown any operation involving the MSR or the Data Register (FIFO) will re-initialize the timer. In auto powerdown mode the FDC enters the powerdown state when all of the following conditions have been met:

1) The motor enable pins of the DOR register are inactive (zero).
2) The FDC is idle; MSR=80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupts).
3) The internal head unload timer has expired.
4) The 10msec auto powerdown timer has lapsed.

Disabling the FDC auto power management cancels the internal timer and prevents any of the above conditions from re-enabling the powerdown state.

Note: At least 8us delay should be added when exiting FDC Auto Powerdown mode. If the operating environment is such that this delay cannot be guaranteed, the auto powerdown mode should not be used and Direct powerdown mode should be used instead. The Direct powerdown mode requires at least 8us delay at 250K bits/sec configuration and 4us delay at 500K bits/sec. The delay should be added so that the internal microcontroller can prepare itself to accept commands.

DSR FROM POWERDOWN

If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened from DSR powerdown, the auto powerdown will once again become effective.

WAKE UP FROM AUTO POWERDOWN

If the FDC enters the powerdown state through the auto powerdown mode, wake up will occur after a reset or by access to the specific registers shown below. If a hardware or software reset is used the part will follow the normal reset sequence. If wake up occurs as a result of access through selected registers the FDC37N3869 will resume normal operation as if the FDC had never powered-down.

The following register accesses will wake up the FDC:

1) Enabling any one of the motor enable bits in the DOR register (reading the DOR does not awaken the part).
2) A read from the MSR register.
3) A read or write to the Data register.

Once awake, the FDC37N3869 will reinitiate the auto powerdown timer for 10ms. The FDC will powerdown again when all of the powerdown conditions are met.

REGISTER BEHAVIOR

Table 70 reiterates the available FDC PC/AT and PS/2, including Model 30 mode, registers. In order to maintain software transparency, access to all the registers must be maintained regardless of the power state. As Table 70 shows, two kinds of registers are identified based on whether access results in the FDC remaining in the powerdown state or not.

Registers that will not awaken the FDC can be accessed during powerdown without changing the powerdown state but will reflect the true register status as shown in the FDC register description. For example, a write to one of these registers will result in the FDC retaining the data and subsequently using it appropriately when the block reawakens.

During powerdown accessing FDC registers that do not affect the power state may increase device power consumption, but only until the register access has been completed.

Table 70 - Available FDC PC/AT and PS/2 Registers

	AVAILABLE REGISTERS		
BASE + ADDRESS	**PC-AT**	**PS/2 (Model 30)**	**ACCESS PERMITTED**
Access to these registers DOES NOT wake up the FDC			
00H	----	SRA	R
01H	----	SRB	R
02H	DOR[1]	DOR[1]	R/W
03H	---	---	---
04H	DSR[1]	DSR[1]	W
06H	---	---	---
07H	DIR	DIR	R
07H	CCR	CCR	W
Access to these registers wakes up the FDC			
04H	MSR	MSR	R
05H	DATA	DATA	R/W

Note[1]: Writing to any of the motor enable bits in the DOR or doing a software reset via the DOR or DSR reset bits will wake up the FDC. Writing to any other DOR or DSR bits will not wake up the FDC.

PIN BEHAVIOR

The FDC37N3869 is specifically designed for portable PC systems where power conservation is a primary concern. Consequently, the behavior of the device pins during powerdown very important.

The pins of the FDC37N3869 FDC can be divided into two major categories: system interface and floppy disk drive interface. When the FDC is powered down, the floppy disk drive pins are disabled so that no power will be drawn through the part as a result of any voltage applied to the pin within the part's power supply range. Most of the system interface pins are left active to monitor system accesses that are intended to wake up the floppy controller.

System Interface Pins

Table 71 gives the state of the system interface pins in the powerdown state. Pins unaffected by the powerdown are labeled "Unchanged". Input pins are "Disabled" to prevent them from causing currents internal to the FDC37N3869 when they have indeterminate input values.

Table 71 - State of System Pins in Auto Powerdown

SYSTEM PINS	STATE IN AUTO POWERDOWN
Input Pins	
IOR	Unchanged
IOW	Unchanged
A[0:9]	Unchanged
D[0:7]	Unchanged
RESET	Unchanged
IDENT	Unchanged
DACK	Unchanged
TC	Unchanged
Output Pins	
FINTR	Unchanged (low)
DB[0:7]	Unchanged
FDRQ	Unchanged (low)

FDD Interface Pins

All pins in the FDD interface that can be connected directly to the floppy disk drive itself are either DISABLED or TRISTATED. Pins used for local logic control or part programming are unaffected.

Table 72 depicts the state of the floppy disk drive interface pins in the powerdown state.

Table 72 - State of FDC Interface Pins in Powerdown

FDD PINS	STATE IN AUTO POWERDOWN
Input Pins	
RDATA	Input
WP	Input
TRK0	Input
INDX	Input
DRV2	Input
DSKCHG	Input
Output Pins	
MOTEN[0:3]	Tristated
DS[0:3}	Tristated
DIR	Active
STEP	Active
WRDATA	Tristated
WE	Tristated
HDSEL	Active
DENSEL	Active
DRATE[0:1]	Active

UART Power Management

Direct UART power management is controlled by the UART1 and UART2 Power Down bits in Configuration Register 2. Refer to section CR02 on page 100 for more information.

UART Auto Power Management is enabled by the UART 1 and UART 2 Enable bits in Configuration Register 7 (see section CR07on page 103). When set, these bits enable the following auto power management features:

1) The transmitter enters auto powerdown when the transmit buffer and transmit shift register are empty.
2) The receiver enters powerdown when the following conditions are all met:
   - Receive FIFO is empty
   - The receiver is waiting for a start bit.

Note: While in the powerdown state, the Ring Indicator interrupts are still valid and are activated when the RI inputs change.

The UART transmitters exit the powerdown state on a write to the XMIT buffer. The UART receivers exit the auto powerdown state when RXDx changes state.

Parallel Port

Direct parallel port power management is controlled by the Parallel Port Power bit in Configuration Register 1. Refer to section CR01 on page 99 for more information.

Parallel port Auto Power Management is enabled by the Parallel Port Enable bit in Configuration Register 7 (see section CR07 on page 103). When set, this bit allows the ECP or EPP logical parallel port blocks to be placed into the powerdown state as follows:

The EPP logic is in powerdown under any of the following conditions:

1) EPP is not enabled in the configuration registers.
2) EPP is not selected through ecr while in ECP mode.

The ECP logic is in powerdown under any of the following conditions:

1) ECP is not enabled in the configuration registers.
2) SPP, PS/2 Parallel port or EPP mode is selected through ecr while in ECP mode.

The parallel port logic can change powerdown modes when the ECP mode is changed through the ecr register or when the parallel port mode is changed through the configuration registers.

Serial IRQ

INTRODUCTION

The FDC37N3869 provides a serial interrupt interface to the host. This scheme adheres to the *Serial IRQ Specification for PCI Systems*, Version 6.0. The CLK33, SIRQ, and nCLKRUN pins are required for this interface. The Serial IRQ Enable bit D7 in CR29 activates the serial interrupt interface.

The IRQ/Data serializer is a Wired-OR structure that simply passes the state of one or more device IRQs and/or Data to the Host Controller. The transfer can be initiated by either a device or the Host. Both high and low transitions are reported in this protocol.

A transfer, called an IRQSER Cycle, consists of three frame types:

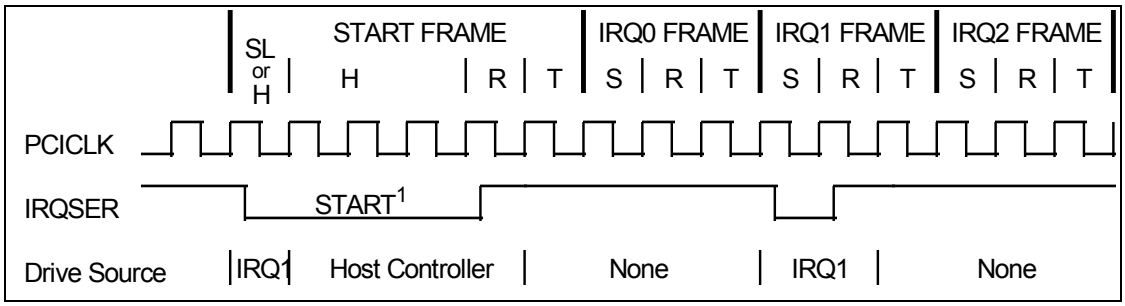
1) One *START* Frame
2) One or more *IRQ/DATA* Frames
3) One *STOP* Frame

The Serial IRQ protocol uses the PCI Clock as its clock source. The PCI clock conforms to the PCI bus electrical specification.

IRQSER CYCLE MODES

There are two modes of operation for IRQSER cycles: Quiet (Active) Mode and Continuous (Idle) Mode. In Quiet Mode any device may initiate an IRQSER cycle. In Continuous Mode only the host controller can initiate an IRQSER cycle (FIGURE 4).

Following a system reset the SIRQ bus defaults to Continuous Mode. IRQSER cycle mode transitions can only occur during the Stop Frame (
FIGURE 5). Slaves must continuously sample the pulse width of the Stop Frame to determine the mode of the next



IRQSER cycle (see the Stop Cycle Control section on page 94).

FIGURE 4 - START FRAME TIMING W/SOURCE SAMPLED LOW PULSE ON IRQ1

Notes:

H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

1) Start Frame pulse can be 4-8 clocks wide
2) PCICLK = CLK33 pin (33MHz PCI Clock input)
3) IRQSER = SIRQ pin

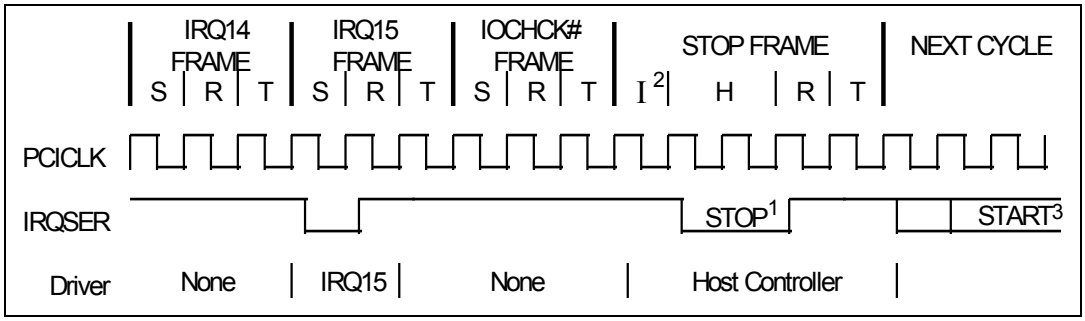


FIGURE 5 - STOP FRAME TIMING W/HOST USING 17 IRQSER SAMPLING PERIOD

Notes:

H=Host Control R=Recovery T=Turn-around S=Sample I= Idle

1) STOP pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.
2) There may be none, one or more Idle states during the Stop Frame.
3) The next IRQSER cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.
4) PCICLK = CLK33 pin (33MHz PCI Clock input)
5) IRQSER = SIRQ pin

Quiet (Active) Mode

In Quiet Mode any device may initiate a Start Frame by driving the IRQSER low for one clock while the IRQSER is Idle (FIGURE 4). After driving low for one clock, slaves must immediately tristate IRQSER without at any time driving high.

A Start Frame may not be initiated while the IRQSER is Active. The IRQSER is Idle between Stop and Start Frames. The IRQSER is Active between Start and Stop Frames. Quiet Mode operation allows the IRQSER to be idle when there are no IRQ/Data transitions.

Once a Start Frame has been initiated, the host controller will take over driving the IRQSER low in the next clock and will continue driving the IRQSER low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the host controller will drive the IRQSER back high for one clock, then tri-state.

Any IRQSER device (e.g., The FDC37N3869) which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the host controller unless the IRQSER is already in an IRQSER Cycle and the IRQ/Data transition can be delivered in that IRQSER Cycle.

Continuous (Idle) Mode

In Continuous Mode only the host controller can initiate a Start Frame to update IRQ/Data line information. All other IRQSER agents become passive and may not initiate a Start Frame. IRQSER Start Frame will be driven low for four to eight clocks by the Host Controller.

Continuous Mode has serves two purposes: it can be used to stop or idle the IRQSER, or the host controller can operate IRQSER continuously by initiating a Start Frame at the end of every Stop Frame.

IRQSER IRQ/DATA FRAMES

Once a Start Frame has been initiated, the FDC37N3869 will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames.

Each IRQ/Data Frame has three phases. Each phase takes one PCI clock: Sample phase, Recovery phase, and Turn-around phase. During the Sample phase the FDC37N3869 must drive the IRQSER (SIRQ pin) low if and only if the last detected IRQ/Data value was low. If the last detected IRQ/Data value was high IRQSER must be left tri-stated.

During the Recovery phase the FDC37N3869 must drive the SIRQ high if and only if it had driven the IRQSER low during the previous Sample Phase. During the Turn-around Phase the FDC37N3869 must tri-state SIRQ.

The FDC37N3869 will drive the IRQSER line low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the Start Frame.

The Sample Phase for each IRQ/Data Frame follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one. For example, the IRQ5 *Sample* Phase occurs on 17th clock after the rising edge of the Start Pulse because IRQ5 is the sixth IRQ/Data Frame ((6 x 3) - 1 = 17).

Table 73 - IRQSER Sampling Periods

IRQSER PERIOD	SIGNAL SAMPLED	# OF CLOCKS PAST START
1	Not Used	2
2	IRQ1	5
3	IRQ2	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47

The IRQSER IRQ/Data Frame will supports IRQ2 from a logical device. Previously, IRQSER Period 3 was reserved for use by the System Management Interrupt (nSMI). When using Period 3 for IRQ2 the user should mask off the SMI via the SMI Enable Register. Likewise, when using Period 3 for nSMI the user should not configure any logical devices as using IRQ2. Note: There is no SMI support in the FDC37N3869.

STOP CYCLE CONTROL

Once all IRQ/Data Frames have completed, the host controller will terminate IRQSER activity by initiating a Stop Frame. Only the host controller can initiate the Stop Frame.

A Stop Frame is indicated when the IRQSER is low for two or three clocks. If the Stop Frame is low for two clocks the next IRQSER Cycle operates in the Quiet mode and any IRQSER device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame pulse. If the Stop Frame is low for three clocks the next IRQSER Cycle operates in Continuous mode and only the host controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame pulse.

LATENCY

Latency for IRQ/Data updates over the IRQSER bus in bridge-less systems with the minimum IRQ/Data Frames of seventeen will range up to 96 clocks (3.84uS with a 25MHz PCI Bus or 2.88uS with a 33MHz PCI Bus).

If one or more PCI to PCI Bridges are added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

EOI/ISR READ LATENCY

Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault.

The host controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the IRQSER Cycle latency in order to ensure that these events do not occur out of order.

AC/DC SPECIFICATION ISSUE

All IRQSER agents must drive/sample IRQSER synchronously relative to the rising edge of the PCI bus clock. The IRQSER (SIRQ) pin uses the electrical specification of PCI bus.

RESET AND INITIALIZATION

The IRQSER bus uses RESET_DRV as its reset signal. The IRQSER pin is tri-stated by all agents while RESET_DRV is active. Following reset, IRQSER Slaves are put into Continuous (IDLE) mode. The host controller is responsible for starting the initial IRQSER cycle to collect the system's IRQ/Data default values.

The system then follows with the Continuous/Quiet mode protocol as determined by the Stop Frame pulse width for subsequent IRQSER Cycles. It is the responsibility of the host controller to provide the default values to 8259's and other system logic before the first IRQSER Cycle is performed.

For IRQSER system suspend, insertion, or removal application, the host controller should be programmed in Continuous (IDLE) mode first. This is to guarantee that the IRQSER bus is in the IDLE state before the system configuration changes.

Add PCI nCLKRUN Support

OVERVIEW

The FDC37N3869 supports the PCI nCLKRUN signal. nCLKRUN is used to indicate the PCI clock status as well as to request that a stopped clock be started. See Figure 6 for an example of a typical system implementation using nCLKRUN.

nCLKRUN support is required because the FDC37N3869 interrupt interface relies entirely on Serial IRQs. If an SIO interrupt occurs while the PCI clock is stopped, nCLKRUN must be asserted before the interrupt can be serviced.

If the FDC37N3869 SIRQ_EN signal is inactive, nCLKRUN support is also disabled. The FDC37N3869 nCLKRUN signal is multiplexed with nADRx on TQFP pin number 92. See Configuration Register CR03 for a description of the TQFP pin 92 multiplex controls.

nCLKRUN is an open drain output and an input. Refer to the *PCI Mobile Design Guide Rev 1.0* for a description of the nCLKRUN function.

USING NCLKRUN

If nCLKRUN is sampled "high", the PCI clock is stopped or stopping. If nCLKRUN is sampled "low", the PCI clock is starting or started (running). If a device in the FDC37N3869 asserts or de-asserts an interrupt and nCLKRUN is sample "high", the FDC37N3869 can request the restoration of the clock by asserting the nCLKRUN signal asynchronously Table 74). The FDC37N3869 holds nCLKRUN low until it detects two rising edges of the clock. After the second clock edge, the FDC37N3869 must disable the open drain driver (Figure 7).

The FDC37N3869 will not assert nCLKRUN under any conditions if SIRQ_EN is inactive ("0"). The SIRQ_EN bit is D7 in CR29.

The FDC37N3869 must not assert nCLKRUN if it is already driven low by the central resource; i.e., the PCI CLOCK GENERATOR in Figure 6. The FDC37N3869 must not assert nCLKRUN unless the line has been deasserted for two successive clocks; i.e., before the clock was stopped (Figure 7).

Table 74 - FDC37N3869 nCLKRUN Function

SIRQ_EN	INTERNAL (PARALLEL) INTERRUPTS	nCLKRUN	ACTION
1	X	X	None
0	NO CHANGE	X	None
	CHANGE[1]	0	None
		1	Assert nCLKRUN

Note[1]: "Change" means either-edge change on any or all parallel IRQs routed to the SIRQ block. The "change" detection logic must run asynchronously to the PCI Clock and regardless of the SIRQ mode; i.e., "continuous" or "quiet".

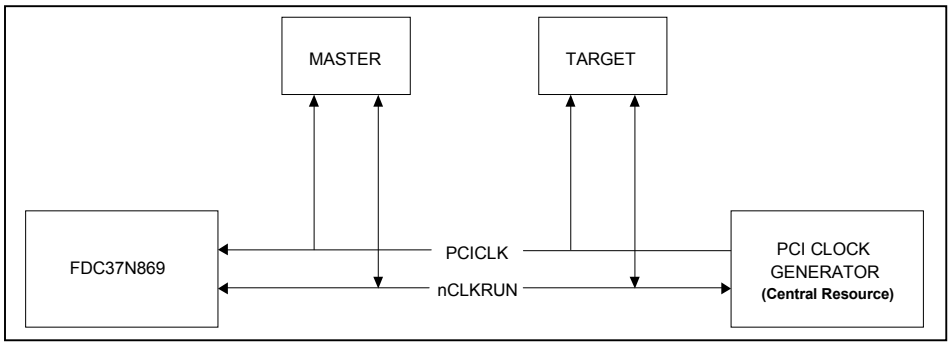


FIGURE 6 - nCLKRUN SYSTEM IMPLEMENTATION EXAMPLE

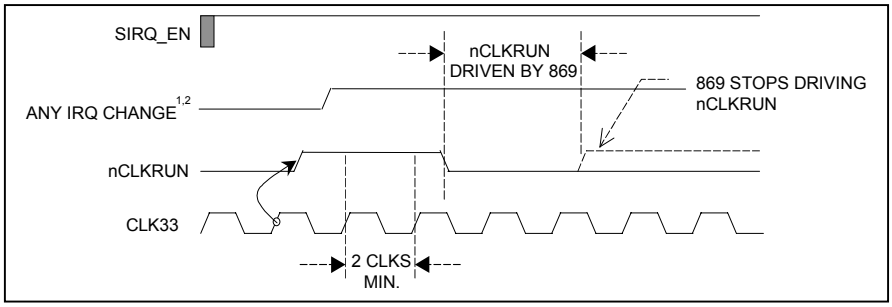


FIGURE 7 - CLOCK START ILLUSTRATION

Note 1: The signal "ANY IRQ CHANGE" is the same as "CHANGE" in Table 72.

Note 2: The FDC37N3869 must continually monitor the state of nCLKRUN to maintain the PCI Clock until an active "ANY IRQ CHANGE" condition has been transferred to the host in a Serial IRQ cycle. For example, if "ANY IRQ CHANGE" is asserted before nCLKRUN is de-asserted (not shown in Figure 7), the FDC37N3869 must assert nCLKRUN as needed until the Serial IRQ cycle has completed.

CONFIGURATION

The configuration of the FDC37N3869 is programmed through hardware selectable Configuration Access Ports that appear when the chip is placed into the configuration state. The FDC37N3869 logical device blocks, if enabled, will operate normally in the configuration state.

Configuration Access Ports

The Configuration Access Ports are the CONFIG PORT, the INDEX PORT, and the DATA PORT (Table 75). The base address of these registers is controlled by the nRTS2/SYSOPT pin (see Table 1) and by the Configuration Port Base Address registers CR12 and CR13. To determine the configuration base address at power-up, the state of the nRTS2/SYSOPT pin is latched by the falling edge of a hardware reset. If the latched state is a 0, the base address of the Configuration Access Ports is located at address 3F0H; if the latched state is a 1, the base address is located at address 370H.

Table 75 - Configuration Access Ports

PORT NAME	SYSOPT = 0	SYSOPT = 1	TYPE
CONFIG PORT	0x3F0	0x370	WRITE
INDEX PORT	0x3F0	0x370	READ/WRITE[1,2]
DATA PORT	INDEX PORT + 1		READ/WRITE[1]

Note[1]: The INDEX and DATA ports are active only when the FDC37N3869 is in the configuration state.

Note[2]: The INDEX PORT is only readable in the configuration state.

Configuration State

The configuration registers are used to select programmable chip options. The FDC37N3869 operates in two possible states: the run state and the configuration state. After power up by default the chip is in the run state. To program the configuration registers, the configuration state must be explicitly enabled. Programming the configuration registers typically follows this sequence:

1) Enter the Configuration State,
2) Program the Configuration Register(s),
3) Exit the Configuration State.

ENTERING THE CONFIGURATION STATE

To enter the configuration state write the Configuration Access Key to the CONFIG PORT. The Configuration Access Key is one byte of 55H data. The FDC37N3869 will automatically activate the Configuration Access Ports following this procedure.

CONFIGURATION REGISTER PROGRAMMING

The FDC37N3869 contains configuration registers CR00-CR2F. After the FDC37N3869 enters the configuration state, configuration registers can be programmed by first writing the register index number (00 - 2FH) to the Configuration Select Register (CSR) through the INDEX PORT and then writing or reading the configuration register contents through the DATA PORT. Configuration register access remains enabled until the configuration state is explicitly exited.

EXITING THE CONFIGURATION STATE

To exit the configuration state, write one byte of AAH data to the CONFIG PORT. The FDC37N3869 will automatically deactivate the Configuration Access Ports following this procedure, at which point configuration register access cannot occur until the configuration state is explicitly re-enabled.

PROGRAMMING EXAMPLE

The following is a configuration register programming example written in Intel 8086 assembly language.

```
;------------------------------.
; ENTER CONFIGURATION STATE   |
;------------------------------‘
MOV     DX,3F0H     ;SYSOPT = 0
MOV     AX,055H
OUT     DX,AL
;------------------------------.
; CONFIGURE REGISTERS CR0-CRx |
;------------------------------‘
MOV     DX,3F0H
MOV     AL,00H
OUT     DX,AL       ;Point to CR0
MOV     DX,3F1H
MOV     AL,3FH
OUT     DX,AL       ;Update CR0
;
MOV     DX,3F0H
MOV     AL,01H
OUT     DX,AL       ;Point to CR1
MOV     DX,3F1H
MOV     AL,9FH
OUT     DX,AL       ;Update CR1
;
; Repeat for all CRx registers
;
;------------------------------.
; EXIT CONFIGURATION STATE    |
;------------------------------‘
MOV     DX,3F0H
MOV     AX,AAH
OUT     DX,AL
```

CONFIGURATION SELECT REGISTER (CSR)

The Configuration Select Register can only be accessed when the FDC37N3869 is in the configuration state. The CSR is located at the INDEX PORT address and must be initialized with configuration register index before the register can be accessed using the DATA PORT.

Configuration Registers Description

The configuration registers are set to their default values at power up (Table 76) and are not affected by RESET, except where noted in the register descriptions that follow.

Table 76 - Configuration Registers

DEFAULT	INDEX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
28H	CR00	Valid	Reserved			FDC PWR	Reserved	Reserved	
9CH	CR01	Lock CRx	Reserved			PP MODE	PP PWR	Reserved	
88H	CR02	UART2 PWR	Reserved			UART1 PWR	Reserved		
70H	CR03	ADRX/ nCLKRUN	IDENT	MFM	DRV DEN 1	Reserved	ADRX/ nCLKRUN	Enhanced FDC Mode 2	PWRGD/ GAMECS
00H	CR04	Reserved	EPP Type	MIDI 2	MIDI 1	Parallel Port FDC		PP Ext. Modes	
00H	CR05	Reserved			DEN SEL		FDC DMA Mode	FDC Output Type Control	
FFH	CR06	FDD3 - ID		FDD2 - ID		FDD1 - ID		FDD0 - ID	
00H	CR07	Auto Power Management				Reserved		Floppy Boot Drive	
00H	CR08	ADRA7	ARDA6	ADRA5	ADRA4	0	0	0	0
00H	CR09	ADRx Config Cntrl		Reserved		ADRA11	ADRA10	ADRA9	ADRA8
00H	CR0A	IR Output MUX		Reserved		ECP FIFO Threshold			
00H	CR0B	FDD3-DRTx		FDD2-DRTx		FDD1-DRTx		FDD0-DRTx	
02H	CR0C	UART 2 Speed	UART 1 Speed	UART 2 Mode			UART 2 Duplex	UART 2 XMIT Polarity	UART 2 RCV Polarity
29H	CR0D	Device ID							
Revision	CR0E	Device Revision							
00H	CR0F	Test 7	Test 6	Test 5	Test 4	Test 3	Test 2	Test 1	Test 0
00H	CR10	Test 15	Test 14	Test 13	Test 12	Test 11	Test 10	Test 9	Test 8
80H	CR11	Test 23	Test 22	Test 21	Test 20	Test 19	Test 18	Test 17	Test 16
Note[1]	CR12	Configuration Ports Base Address [7:1]							0
Note[1]	CR13	Configuration Ports Base Address [10:8]							
-	CR14	Floppy Data Rate Select Shadow							
-	CR15	UART1 FIFO Control Shadow							
-	CR16	UART2 FIFO Control Shadow							
03H	CR17	Force FDD Status Change							
00H	CR18 - CR1D	Reserved							
80H	CR1E	GAMECS - ADR[9:4]						GAMECS CONFIG	
00H	CR1F	FDD3-DTx		FDD2-DTx		FDD1-DTx		FDD0-DTx	
3CH	CR20	FDC - ADR[9:4]						0	0
00H	CR21	Reserved							
00H	CR22	Reserved		Parallel Port ECP IRQ Select			Parallel Port ECP DMA Select		
00H	CR23	Parallel Port - ADR[9:2]							
00H	CR24	Serial Port 1 - ADR[9:3]							0
00H	CR25	Serial Port 2 - ADR[9:3]							0
00H	CR26	FDC DMA Select				Parallel Port DMA Select			
00H	CR27	FDC IRQ Select				Parallel Port IRQ Select			
00H	CR28	Serial Port 1 IRQ Select				Serial Port 2 IRQ Select			
00H	CR29	SIRQ_EN	Reserved		HPMODE	IRQIN IRQ Select			
00H	CR2A	Reserved							

DEFAULT	INDEX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
00H	CR2B	FIR Base I/O ADDR[10:3]							
0FH	CR2C	Reserved					Serial Port 2 DMA Select		
03H	CR2D	IR Half Duplex Time-Out							
00H	CR2E	Software Select A							
00H	CR2F	Software Select B							

Note[1]: Refer to sections CR12 - CR13 on page 106.

CR00

CR00 can only be accessed in the configuration state and after the CSR has been initialized to 00H. The default value of this register after power up is 28H (Table 77).

Table 77 - CR00

BIT NO.	BIT NAME	DESCRIPTION
0:2	Reserved	Read Only. A read returns 0
3	FDC Power [1]	A high level on this bit, supplies power to the FDC (default). A low level on this bit puts the FDC in low power mode.
4,5,6	Reserved	Read only. A read returns bit 5 as a 1 and bits 4 and 6 as a 0.
7	Valid	A high level on this software controlled bit can be used to indicate that a valid configuration cycle has occurred. The control software must take care to set this bit at the appropriate times. Set to zero after power up. This bit has no effect on any other hardware in the chip.

Note[1]: Power Down bits disable the respective logical device and associated pins, however the power down bit does not disable the selected address range for the logical device. To disable the host address registers the logical device's base address must be set below 100h. Devices that are powered down but still reside at a valid I/O base address will participate in Plug-and-Play range checking.

CR01

CR01 can only be accessed in the configuration state and after the CSR has been initialized to 01H. The default value of this register after power up is 9CH (Table 78).

Table 78 - CR01

BIT NO.	BIT NAME	DESCRIPTION
0,1	Reserved	Read Only. A read returns "0".
2	Parallel Port Power[1]	A high level on this bit, supplies power to the Parallel Port (Default). A low level on this bit puts the Parallel Port in low power mode.
3	Parallel Port Mode	Parallel Port Mode. A high level on this bit, sets the Parallel Port for Printer Mode (Default). A low level on this bit enables the Extended Parallel port modes. Refer to Bits 0 and 1 of CR4
4	Reserved	Read Only. A read returns "1".
5,6	Reserved	Read Only. A read returns "0".
7	Lock CRx	A high level on this bit enables the reading and writing of CR00 - CR2F (Default). A low level on this bit disables the reading and writing of CR00 - CR2F. Note: once the Lock Crx bit is set to "0", this bit can only be set to "1" by a hard reset or power-up reset.

Note[1]: Power Down bits disable the respective logical device and associated pins, however the power down bit does not disable the selected address range for the logical device. To disable the host address registers the logical device's base address must be set below 100h. Devices that are powered down but still reside at a valid I/O base address will participate in Plug-and-Play range checking.

CR02

CR02 can only be accessed in the configuration state and after the CSR has been initialized to 02H. The default value of this register after power up is 88H (Table 79).

Table 79 - CR02

BIT NO.	BIT NAME	DESCRIPTION
0:2	Reserved	Read Only. A read returns "0".
3	UART1 Power Down[1]	A high level on this bit, allows normal operation of the Primary Serial Port (Default). A low level on this bit places the Primary Serial Port into Power Down Mode.
4:6	Reserved	Read Only. A read returns "0".
7	UART2 Power Down[1]	A high level on this bit, allows normal operation of the Secondary Serial Port, including the SCE/FIR block (Default). A low level on this bit places the Secondary Serial Port including the SCE/FIR block into Power Down Mode.

Note[1]: Power Down bits disable the respective logical device and associated pins, however the power down bit does not disable the selected address range for the logical device. To disable the host address registers the logical device's base address must be set below 100h. Devices that are powered down but still reside at a valid I/O base address will participate in Plug-and-Play range checking.

CR03

CR03 can only be accessed in the configuration state and after the CSR has been initialized to 03H. The default value after power up is 70H (Table 80).

Table 80 - CR03

BIT NO.	BIT NAME	DESCRIPTION
0	PWRGD/ GAMECS	Bit 0 — Pin function 0 — PWRGD (default) 1 — GAMECS
1	Enhanced Floppy Mode 2	Bit 1 — Floppy Mode - Refer to the description of the TAPE DRIVE REGISTER (TDR) for more information on these modes. 0 — NORMAL Floppy Mode (Default) 1 — Enhanced Floppy Mode 2 (OS2)
3	Reserved	Reserved - Read as zero
4	DRVDEN1	Bit 4 — Pin DRVDEN1 Output[1] 0 — Output Programmed DRVDEN1 Value 1 — Force DRVDEN1 Output High (default)
5	MFM	IDENT is used in conjunction with MFM to define the FDC interface mode.
6	IDENT	**IDENT / MFM / MODE** 1 / 1 — AT Mode (Default) 1 / 0 — Reserved 0 / 1 — PS/2 0 / 0 — Model 30
7,2	nADRx/nCLKRUN	Bit - 7 / Bit - 2 — Pin 92 (TQFP) 0 / x — Reserved[2] 1 / 0 — nADRX 1 / 1 — nCLKRUN

Note[1]: See NOTE[2] in section **CR05** on page 102.
Note[2]: Pin 92 (TQFP) is tri-stated at power-up.

CR04

CR04 can only be accessed in the configuration state and after the CSR has been initialized to 04H. The default value after power up is 00H (Table 81).

Table 81 - CR04: Parallel and Serial Extended Setup Register

BIT NO.	BIT NAME	DESCRIPTION		
1,0	Parallel Port Extended Modes	Bit 1	Bit 0	If CR1 bit 3 is a low level then:
		0	0	Standard and Bi-directional Modes (SPP) (default)
		0	1	EPP Mode and SPP
		1	0	ECP Mode[2]
		1	1	ECP Mode & EPP Mode[1,2]
2,3	Parallel Port FDC	Refer to Parallel Port Floppy Disk Controller description.		
		Bit 3	Bit 2	
		0	0	Normal
		0	1	PPFD1
		1	0	PPFD2
		1	1	Reserved
4	MIDI 1[3]	Serial Clock Select Port 1: A low level on this bit, disables MIDI support, clock = divide by 13 (default). A high level on this bit enables MIDI support, clock = divide by 12.		
5	MIDI 2[3]	Serial Clock Select Port 2: A low level on this bit, disables MIDI support, clock = divide by 13 (default). A high level on this bit enables MIDI support, clock = divide by 12.		
6	EPP Type	0 = EPP 1.9 (default) 1 = EPP 1.7		
7	Reserved[4]	Reserved - Read as 0.		

Note[1]: In this mode, EPP can be selected through the ecr register of ECP as mode 100.

Note[2]: In these modes, 2 drives can be supported directly, 3 or 4 drives must use external 4 drive support. SPP can be selected through the ecr register of ECP as mode 000.

Note[3]: MIDI Support: The Musical Instrumental Digital Interface (MIDI) operates at 31.25Kbaud (+/-1%) which can be derived from 125KHz. (24 MHz/12=2 MHz, 2 MHz/16=125 kHz).

Note[4]: The function of this bit has been modified from the FDC37C669. This bit's former function, the selection of the pins for IR receive and transmit, has been moved to CR0A.

CR05

CR05 can only be accessed in the configuration state and after the CSR has been initialized to 05H. The default value after power up is 00H (Table 82).

Table 82 - CR05: Floppy Disk Setup Register

BIT NO.	BIT NAME	DESCRIPTION		
0[1]	FDC Output Type Control (R/W)	0 = FDC Outputs are open drain (default). 1 = FDC Outputs are push-pull.		
1[1,2]	FDC Output Control (R/W)	0 = FDC Outputs Active (default). 1 = FDC Outputs Tri-State.		
2	FDC DMA Mode	0 = Burst mode is enabled for the FDC FIFO execution phase data transfers (default). 1 = Non-Burst mode enabled. The FDRQ and FIRQ pins are strobed once for each byte transferred while the FIFO is enabled.		
4,3	DenSel	**BIT 4**	**BIT 3**	**DENSEL OUTPUT**
		0	0	Normal (default)
		0	1	Reserved
		1	0	1
		1	1	0
5-7	Reserved	Read Only. A read returns 0.		

Note[1]: Bits CR05[1:0] do not affect the Parallel Port FDC.

Note[2]: In the FDC37N3869, the behavior of the DRVDEN1 Control CR03.4 depends upon the FDC Output Control CR05.1 (Table 82). If the FDC Output Control is active DRVDEN1 will behave as described in the 669FR; i.e., if CR03.4 is 0 the DRVDEN1 output pin assumes the value of the DRVDEN1 function, if CR03.4 is 1 the DRVDEN1 output pin stays high. If the FDC Output Control is inactive the DRVDEN1 Control will have no affect on the DRVDEN1 output pin.

Table 83 - DRVDEN1 Control

FDC OUTPUT CONTROL	DRVDEN1 CONTROL	DRVDEN1	DESCRIPTION
(CR05.1)	**(CR03.4)**	**(PIN 18)**	
0	0	1/0	NORMAL DRVDEN1 FUNCTION
0	1	1	DRVDEN1 FORCED HIGH
1	X	TRISTATE	ALL FDD OUTPUT PINS ARE TRISTATED

CR06

CR06 can only be accessed in the configuration state and after the CSR has been initialized to 06H. The default value of this register after power up is FFH (Table 84). CR06 holds the floppy disk drive type IDs for up to four floppy disk drives (see section Drive Type ID, Bits 4 - 5 on page 25).

Table 84 - DR06: Drive Type ID Register

FDD3		FDD2		FDD1		FDD0	
D7	D6	D5	D4	D3	D2	D1	D0
ID31	ID30	ID21	ID20	ID11	ID10	ID01	ID00

CR07

CR07 can only be accessed in the configuration state and after the CSR has been initialized to 07H. The default value of this register after power up is 00H (Table 85). CR07 controls auto power management and the floppy boot drive.

Table 85 - CR07: Auto Power Management and Boot Drive Select

BIT NO.	BIT NAME	DESCRIPTION
0,1	Floppy Boot	This bit is used to define the boot floppy. 0 = Drive A (default) 1 = Drive B
2	Reserved	Read as 0.
3	Reserved	Read as 0.
4	Parallel Port Enable	This bit controls the AUTOPOWER DOWN feature of the Parallel Port. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by POR or a hardware reset.
5	UART 2 Enable	This bit controls the AUTOPOWER DOWN feature of the UART2. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by POR or a hardware reset.
6	UART 1 Enable	This bit controls the AUTOPOWER DOWN feature of the UART1. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by POR or a hardware reset.
7	Floppy Disk Enable	This bit controls the AUTOPOWER DOWN feature of the Floppy Disk. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled (See Note in the “FDC Power Management” section) This bit is reset to the default state by POR or a hardware reset.

CR08

CR08 can only be accessed in the configuration state and after the CSR has been initialized to 08H. The default value of this register after power up is 00H (Table 86). CR08 contains the lower 4 bits (ADRA7:4) for the ADRx address decoder. Bits D0 - D3 are Reserved. Reserved bits cannot be written and return 0 when read.

Table 86 - CR08: ADRx Lower Address Decode

D7	D6	D5	D4	D3	D2	D1	D0
ADRA7	ADRA6	ADRA5	ADRA4	Reserved			

CR09

CR09 can only be accessed in the configuration state and after the CSR has been initialized to 09H. The default value of this register after power up is 00H (Table 87). CR09 contains the upper 4 bits (ADRA11:8) of the ADRx address decoder and the ADRx Configuration Control Bits D[7:6]. The ADRx Configuration Control Bits configure the ADRx Address Decoder (
Table 88).

To activate the FDC37N3869 nADRx output, the system address bus bits A11 to A4 must match the values programmed in CR08 and CR09 and address bits A12 to A15 must be ‘0000b’.

Table 87 - CR09: ADRx Upper Address Decoder and Configuration

D7	D6	D5	D4	D3	D2	D1	D0
ADRx CONFIGURATION CONTROL		Reserved		ADRA11	ADRA10	ADRA9	ADRA8

Table 88 - ADRx Configuration Bits

ADRx CONFIGURATION CONTROL		DESCRIPTION
D7	D6	
0	0	ADRx disabled
0	1	1 Byte decode A[3:0]=0000b
1	0	8 Byte block decode A[3:0]=0XXXb
1	1	16 byte block decode A[3:0]=XXXXb

CR0A

CR0A can only be accessed in the configuration state and after the CSR has been initialized to 0AH. The default value of this register after power up is 00H (Table 88). CR0A defines the FIFO threshold for the ECP mode parallel port. Bits D[5:4] are Reserved. Reserved Bits cannot be written and return 0 when read. Bits D[7:6] are the IR OUTPUT MUX bits (Table 89) and are reset to the default state by a POR or a hardware reset.

Table 89 - CR0A

D7	D6	D5	D4	D3	D2	D1	D0
IR OUTPUT MUX (see Table 90)		RESERVED		ECP FIFO THRESHOLD			
				THR3	THR2	THR1	THR0

Table 90 - CR0A: IR OUTPUT MUX Bits

D7	D6	Mux Mode
0	0	Active device to COM port (Default). That is, use pins IRRX and IRTX (pins 88 and 89).
0	1	Active device to IR port. That is, use IRRX2, IRTX2 (pins 23, 24).
1	0	Reserved.
1	1	Outputs Inactive: IRTX and IRTX2 are High-Z.

Note: The function of the IR OUTPUT MUX bits and how they are reset has been modified from the FDC37C669. The first two options were previously selected through CR04.

CR0B

CR0B can only be accessed in the configuration state and after the CSR has been initialized to 0BH. The default value of this register after power up is 00H (Table 91). CR0B indicates the Drive Rate table used for each drive (see Table 20). Refer to section CR1F on page 108 for the Drive Type register.

Table 91 - CR0B

FDD3		FDD2		FDD1		FDD0	
D7	D6	D5	D4	D3	D2	D1	D0
DRT1	DRT0	DRT1	DRT0	DRT1	DRT0	DRT1	DRT0

CR0C

CR0C can only be accessed in the configuration state and after the CSR has been initialized to 0CH. The default value of this register after power up is 02H (Table 92). CR0C controls the operating mode of the UART. This register is reset to the default state by a POR or a hardware reset.

Table 92 - CR0C

BIT NO.	BIT NAME	DESCRIPTION
0	UART 2 RCV Polarity	0 = RX input active high (default). 1 = RX input active low.
1	UART 2 XMIT Polarity	0 = TX output active high. 1 = TX output active low (default).
2	UART 2 Duplex	This bit is used to define the FULL/HALF DUPLEX operation of UART 2. 1 = Half duplex 0 = Full duplex (default)
3, 4, 5	UART 2 MODE	UART 2 Mode 5 4 3 0 0 0 Standard (default) 0 0 1 IrDA (HPSIR) 0 1 0 Amplitude Shift Keyed IR @ 500kHz 0 1 1 Reserved 1 x x Reserved
6	UART 1 Speed	This bit enables the high speed mode of UART 1. 1 = High speed enabled 0 = Standard (default)
7	UART Speed	This bit enables the high speed mode of UART 2. 1 = High speed enabled 0 = Standard (default)

CR0D

CR0D can only be accessed in the configuration state and after the CSR has been initialized to 0DH. This register is read only. CR0D contains the FDC37N3869 Device ID. The default value of this register after power up is 29H.

CR0E

CR0E can only be accessed in the configuration state and after the CSR has been initialized to 0EH. This register is read only. CR0E contains the current FDC37N3869 Chip Revision Level starting at 00H.

CR0F

CR0F can only be accessed in the configuration state and after the CSR has been initialized to 0FH. The default value of this register after power up is 00H (Table 93). CR0F is a test control register and all bits must be treated as Reserved. Note: all test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 93 - CR0F

BIT NO.	BIT NAME	DESCRIPTION
0	Test 0	RESERVED FOR SMSC USE
1	Test 1	
2	Test 2	
3	Test 3	
4	Test 4	
5	Test 5	
6	Test 6	
7	Test 7	

CR10

CR10 can only be accessed in the configuration state and after the CSR has been initialized to 10H. The default value of this register after power up is 00H (Table 94). CR10 is a test control register and all bits must be treated as Reserved. **Note:** All test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 94 - CR10

BIT NO.	BIT NAME	DESCRIPTION
0	Test 8	RESERVED FOR SMSC USE
1	Test 9	
2	Test 10	
3	Test 11	
4	Test 12	
5	Test 13	
6	Test 14	
7	Test 15	

CR11

CR11 can only be accessed in the configuration state and after the CSR has been initialized to 11H. The default value of this register after power up is 80H (Table 95). CR11 is a test control register and all bits must be treated as Reserved. **Note:** all test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 95 - CR11

BIT NO.	BIT NAME	DESCRIPTION
0	Test 16	RESERVED FOR SMSC USE
1	Test 17	
2	Test 18	
3	Test 19	
4	Test 20	
5	Test 21	
6	Test 22	
7	Test 23	

CR12 - CR13

CR12 and CR13 are the FDC37N3869 Configuration Ports base address registers (Table 96). These registers are used to relocate the Configuration Ports base address beyond the power-up defaults determined by the SYSOP pin programming.

CR12 contains the Configuration Ports base address bits A[7:0]. CR13 contains the Configuration Ports base address bits A[10:8].

The Configuration Ports base address is relocatable on even-byte boundaries; i.e., A0 = ‘0’.

At power-up the Configuration Ports base address is determined by the SYSOP pin programming. To relocate the Configuration Ports base address after power-up, first write the lower address bits of the new base address to CR12 and then write the upper address bits to CR13. **Note:** Writing CR13 changes the Configuration Ports base address.

Table 96 - Configuration Ports Base Address Registers

INDEX	R/W	HARD RESET	VCC POR	CONFIGURATION PORTS BASE ADDRESS REGISTERS							
				D7	D6	D5	D4	D3	D2	D1	D0
0x12[2]	R/W	SYSOP=0: 0xF0 SYSOP=1: 0x70	SYSOP=0: 0xF0 SYSOP=1: 0x70	A7	A6	A5	A4	A3	A2	A1	"0"
0x13[1]	R/W	SYSOP=0: 0x03 SYSOP=1: 0x03	SYSOP=0: 0x03 SYSOP=1: 0x03	"0"	"0"	"0"	"0"	"0"	A10	A9	A8

Note[1]: Writing CR13 changes the Configuration Ports base address.
Note[2]: The Configuration Ports Base Address is relocatable on even-byte boundaries; i.e., A0 = "0".

CR14

CR14 can only be accessed in the configuration state and after the CSR has been initialized to 14H. CR14 shadows the bits in the write-only FDC run-time DSR register (Table 97).

Table 97 - CR14: DSR Shadow Register

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR 14	R	SOFT RESET	PWR DOWN	Res.	PRE-COMP 2	PRE-COMP 1	PRE-COMP 0	DATA RATE SELECT 1	DATA RATE SELECT 0	N/A

CR15

CR15 can only be accessed in the configuration state and after the CSR has been initialized to 15H. CR15 shadows the bits in the write-only UART1 run-time FCR register (Table 98).

Table 98 - CR15: UART1 FCR Shadow Register

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR15	R	RCVR TRIGGER MSB	RCVR TRIGGER LSB	Reserved		DMA MODE SELECT	XMIT FIFO RESET	RCVR FIFO RESET	FIFO ENABLE	N/A

CR16

CR161 can only be accessed in the configuration state and after the CSR has been initialized to 16H. CR16 shadows the bits in the write-only UART2 run-time FCR register (Table 99).

Table 99 - CR16: UART2 FCR Shadow Register

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR16	R	RCVR TRIGGER MSB	RCVR TRIGGER LSB	Reserved		DMA MODE SELECT	XMIT FIFO RESET	RCVR FIFO RESET	FIFO ENABLE	N/A

CR17

CR17 can only be accessed in the configuration state and after the CSR has been initialized to 17H. The default value of this register after power up is 003H (Table 100). CR17 is the Force FDD Status Change register.

Table 100 - CR17: Force FDD Status Change Register

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR 17	R/W	RESERVED				RESERVED	FORCE WRTPRT	FORCE DSKCHG1	FORCE DSKCHG0	0x03

Note: The controls in the Force FDD Status Change register (CR17) apply to the FDD Interface pins as well as to the Parallel Port FDC.

Force Disk Change, Bits 0 - 1

Setting either of the Force Disk Change bits active (1) forces the FDD nDSKCHG input active when the appropriate drive has been selected. FORCE DSKCHG1 and FORCE DSKCHG0 can be written to a 1 but are not clearable by software. FORCE DSKCHG1 is cleared on (nSTEP AND nDS1), FORCE DSKCHG0 is cleared on (nSTEP AND nDS0). Note: The DSK CHG bit in the Floppy DIR register, Bit 7 = (nDS0 AND FORCE DSKCHG0) OR (nDS1 AND FORCE DSKCHG1) OR nDSKCHG.

Force Write Protect, Bit 2

FORCE WRTPRT asserts the internal nWRTPRT input to the controller when the FORCE WRTPRT bit is active ("1") and a drive has been selected. The FORCE WRTPRT function applies to the nWRTPRT pin in the FDD Interface as well as the nWRTPRT pin in the Parallel Port FDC.

CR18 - CR1D

CR18 - CR1D registers are Reserved. Reserved registers cannot be written and return 0 when read. The default value of these registers after power up is 00H.

CR1E

CR1E register can only be accessed in the configuration state and after the CSR has been initialized to 1EH. The default value of this register after power up is 80H (Table 101). CR1E is used to select the base address of the Game Chip Select decoder (GAMECS). The GAMECS can be set to 48 locations on 16 byte boundaries from 100H-3F0H. To disable the GAMECS, set DB1 and DB0 to zero (Table 102).

Table 101 - CR1E

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	GAMECS CONFIG (see Table 100)	

Table 102 - GAMECS Configuration Bits

GAMECS CONFIGURATION		DESCRIPTION
DB1	DB0	
0	0	GAMECS disabled
0	1	1 Byte decode, ADR[3:0] = 0001b
1	0	8 Byte block decode, ADR[3:0] = 0XXXb
1	1	16 byte block decode, ADR[3:0] = XXXXb

Upper Address Decode requirements: nCS='0' and A10='0' are required to qualify the GAMECS output.
CR03.0, the PWRGD/GAMECS control bit, overrides the selection made by the GAMECS Configuration Bits.

CR1F

CR1F can only be accessed in the configuration state and after the CSR has been initialized to 1FH. The default value of this register after power up is 00H (Table 103). CR1F indicates the floppy disk Drive Type for each of four floppy disk drives. The floppy disk Drive Type is used to map the three FDC DENSEL, DRATE1 and DRATE0 outputs onto two Super I/O output pins DRVDEN1 and DRVDEN0 (Table 104).

Table 103 - CR1F

FDD3		FDD2		FDD1		FDD0	
D7	D6	D5	D4	D3	D2	D1	D0
DT0	DT1	DT0	DT1	DT0	DT1	DT0	DT1

Table 104 - Drive Type Encoding

DRIVE TYPE		DRVDEN0	DRVDEN1	
DT0	**DT1**			**DRIVE TYPE DESCRIPTION**
0	0	DENSEL	DRATE0	4/2/1 MB 3.5" 2/1 MB 5.25" FDDS 2/1.6/1 MB 3.5" (3-MODE)
0	1	DRATE1	DRATE0	
1	0	nDENSEL	DRATE0	PS/2
1	1	DRATE0	DRATE1	

CR20

CR20 can only be accessed in the configuration state and after the CSR has been initialized to 20H. The default value of this register after power up is 3CH (Table 105). CR20 is used to select the base address of the floppy disk controller (FDC). The FDC base address can be set to 48 locations on 16 byte boundaries from 100H - 3F0H. To disable the FDC set ADR9 and ADR8 to zero. Set CR20.[1:0] to 00b when writing the FDC Base Address.

FDC Address Decoding: nCS = '0' and A10 = '0' are required to access the FDC registers. A[3:0] are decoded as 0XXXb.

Table 105 - CR20: FDC Base Address Register

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	0	0

CR21

Register CR21 is Reserved. Reserved bits cannot be written and return 0 when read.

CR22

The ECP Software Select register CR22 contains the ECP IRQ Select bits and the ECP DMA Select bits (Table 106). CR22 is part of the ECP DMA/IRQ Software Indicators described in the ECP cnfgB register. CR22 is read/write. Note: all of the ECP DMA/IRQ Software Indicators, including CR22, are software-only. Writing these bits does not affect the ECP hardware DMA or IRQ channels that are configured in CR26 and CR27.

Table 106 - ECP Software Select Register (CR22)

INDEX	R/W	HARD RESET	VCC POR	DESCRIPTION							
				D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x22	R/W	0x00	0x00	Reserved		ECP IRQ Select			ECP DMA Select		

CR23

CR23 can only be accessed in the configuration state and after the CSR has been initialized to 23H. The default value of this register after power up is 00H (Table 107). CR23 is used to select the base address of the parallel port. If EPP is not enabled, the parallel port can be set to 192 locations on 4-byte boundaries from 100H - 3FCH; if EPP is enabled, the parallel port can be set to 96 locations on 8-byte boundaries from 100H - 3F8H (Table 108). To disable the parallel port, set ADR9 and ADR8 to zero.

Parallel Port Address Decoding: nCS = '0' and A10 = '0' are required to access the Parallel Port when in Compatible, Bi-directional, or EPP modes. A10 is active when in ECP mode.

Table 107 - CR23: Parallel Port Base Address Register

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2

Table 108 - Parallel Port Addressing Options

EPP ENABLED	ADDRESSING (LOW BITS) DECODE
No	A[1:0] = XXb
Yes	A[2:0] = XXXb

CR24

CR24 can only be accessed in the configuration state and after the CSR has been initialized to 24H. The default value of this register after power up is 00H (Table 109). CR24 is used to select the base address of Serial Port 1 (UART1). The serial port can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 1, set ADR9 and ADR8 to zero. Set CR24.0 to 0 when writing the UART1 Base Address.

Serial Port 1 Address Decoding: nCS = '0' and A10 = '0' are required to access UART1 registers. A[*2*:0] are decoded as XXXb.

Table 109 - CR24: UART1 Base Address Register

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	0

CR25

CR25 can only be accessed in the configuration state and after the CSR has been initialized to 25H. The default value of this register after power up is 00H (Table 110). CR25 is used to select the base address of Serial Port 2 (UART2). Serial Port 2 can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 2, set ADR9 and ADR8 to zero. Set CR25.0 to 0 when writing the UART2 Base Address.

Serial Port 2 Address Decoding: nCS = '0' and A10 = '0' are required to access UART2 registers. A[*2*:0] are decoded as XXXb.

Table 110 - CR25: UART2 Base Address Register

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	0

CR26

CR26 can only be accessed in the configuration state and after the CSR has been initialized to 26H. The default value of this register after power up is 00H (Table 111). CR26 is used to select the DMA for the FDC (Bits 4 - 7) and the Parallel Port (bits 0 - 3). Any unselected DMA Request output (DRQ) is in tristate.

Table 111 - CR26: FDC and PP DMA Selection Register

D3-D0 OR D7-D4	DMA SELECTED
0000	DMA_A
0001	DMA_B
0010	DMA_C
0011	DMA_D
0100	RESERVED
1111	NONE

CR27

CR27 can only be accessed in the configuration state and after the CSR has been initialized to 27H. The default value of this register after power up is 00H (Table 112). CR27 is used to select the IRQ for the FDC (Bits 4 - 7) and the Parallel Port (bits 3 - 0). Any unselected IRQ output (registers CR27 - CR29) is in tri-state.

Table 112 - CR27: FDC and PP IRQ Selection Register

D3-D0 OR D7-D4	IRQ SELECTED
0000	NONE
0001	IRQ_1
0010	IRQ_2
0011	IRQ_3
0100	IRQ_4
0101	IRQ_5
0110	IRQ_6
0111	IRQ_7
1000	IRQ_8
1001	IRQ_9
1010	IRQ_10
1011	IRQ_11
1100	IRQ_12
1101	IRQ_13
1110	IRQ_14
1111	IRQ_15

CR28

CR28 can only be accessed in the configuration state and after the CSR has been initialized to 28H. The default value of this register after power up is 00H. CR28 is used to select the IRQ for Serial Port 1 (bits 7 - 4) and for Serial Port 2 (bits 3 - 0). Refer to the IRQ encoding for CR27 (Table 113). Any unselected IRQ output (registers CR27 - CR29) is in tristate. Shared IRQs are not supported in the FDC37N3869.

Table 113 - UART Interrupt Operation

UART1		UART2		IRQ PINS	
UART1 OUT2 bit	UART1 IRQ Output State	UART2 OUT2 bit	UART2 IRQ Output State	UART1 Pin State	UART2 Pin State
0	Z	0	Z	Z	Z
1	asserted	0	Z	1	Z
1	de-asserted	0	Z	0	Z
0	Z	1	asserted	Z	1
0	Z	1	de-asserted	Z	0
1	asserted	1	asserted	1	1
1	asserted	1	de-asserted	1	0
1	de-asserted	1	asserted	0	1
1	de-asserted	1	de-asserted	0	0
It is the responsibility of the software to ensure that two IRQ's are not set to the same IRQ number. Potential damage to chip may result. Note: Z = Don't Care.					

CR29

CR29 can only be accessed in the configuration state and after the CSR has been initialized to 29H. The default value of this register after power up is 00H (Table 114). CR29 controls the HPMODE bit and is used to select the IRQ mapping (bits 0 - 3) for the IRQIN pin. Refer to IRQ encoding for CR27 (Table 109). Any unselected IRQ output (registers CR27 - CR29) is in tristate.

Table 114 - CR29

BIT NO.	NAME	DESCRIPTION	
0-3	IRQIN	Selects the IRQ for IRQIN	
4	HPMODE	See FIGURE 3 – INFRARED INTERFACE BLOCK DIAGRAM	
		0	Select IRMODE (default)
		1	Select IRR3
5	*RESERVED*	Not Writeable, Reads Return "0"	
7	SIRQ_EN	Serial IRQ enable bit. 0 = Enable (default) 1 = Disable	

CR2A

Register CR2A is reserved. The default value of this register after power up is 00H.

CR2B

CR2B can only be accessed in the configuration state and after the CSR has been initialized to 2BH. The default value of this register after power up is 00H (Table 115). CR2B is used to set the SCE (FIR) base address ADR[10:3]. The SCE base address can be set to 224 locations on 8-byte boundaries from 100H - 7F8H. To disable the SCE, set ADR10, ADR9 and ADR8 to zero.

SCE Address Decoding: nCS = '0' required to access SCE registers. A[2:0] are decoded as XXXb.

Table 115 - CR2B: SCE (FIR) Base Address Register

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
ADR10	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3

CR2C

CR2C can only be accessed in the configuration state and after the CSR has been initialized to 2CH. The default value of this register after power up is 00H (Table 116). Bits D[3:0] of this register are used to select the DMA for the SCE (FIR). Bits D[7:4] are Reserved. Reserved bits cannot be written and return 0 when read. Any unselected DMA Request output (DRQ) is in tristate.

Table 116 - CR2C: SCE (FIR) DMA Select Register

D3-D0 OR D7-D4	DMA SELECTED
0000	DMA_A
0001	DMA_B
0010	DMA_C
0011	DMA_D
0100	RESERVED
1111	NONE

CR2D

CR2D can only be accessed in the configuration state and after the CSR has been initialized to 2DH. The default value of this register after power up is 03H (Table 117). CR2D is used to set the IR Half Duplex Turnaround Delay Time for the IR port. This value is 0 to 10msec in 100µsec increments.

The IRCC v2.0 block includes an 8 bit IR Half Duplex Time-out register in SCE Register Block 5, Address 1 that interacts with configuration register CR2D. These two registers behave like the other IRCC Legacy controls where either source uniformly updates the value of both registers when either register is explicitly written using IOW or following a device-level POR. IRCC software resets do not affect these registers.

The IR Half Duplex Time-out is programmable from 0 to 25.5mS in 100μS increments, as follows:

IR HALF DUPLEX TIME-OUT = (CR2D) x 100μS

Table 117 - CR2D

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR2D	R/W	IR HALF DUPLEX TIME-OUT								0x03

CR2E

CR2E can only be accessed in the configuration state and after the CSR has been initialized to 2EH. The default value of this register after power up is 00H (Table 118). CR2E is directly connected to SCE Register Block Three, Address 0x05 in the IRCC v2.0 block.

Table 118 - CR2E

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR2E	R/W	Software Select A								0x00

CR2F

CR2F can only be accessed in the configuration state and after the CSR has been initialized to 2FH. The default value of this register after power up is 00H (Table 119). CR2F is directly connected to SCE Register Block Three, Address 0x06 in the IRCC v2.0 block.

Table 119 - CR2F

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR2F	R/W	Software Select B								0x00

OPERATIONAL DESCRIPTION

Maximum Guaranteed Ratings

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -55° to +150°C
Lead Temperature Range (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin, with respect to Ground ..... +Vcc+0.3V
Negative Voltage on any pin, with respect to Ground ..... -0.3V
Maximum V_{CC} ..... +5.5V

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC Electrical Characteristics

(T_A = 0°C - 70°C, V_{cc} = +3.3 V ± 10%)

Table 120 - DC Electrical Characteristics (T_A = 0°C - 70°C, V_{cc} = +3.3 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
I_{CLK} Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	2.2			V	
Input Leakage (All I and IS buffers except PWRGD)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{cc}
Input Current PWRGD	I_{OH}		75	150	µA	V_{IN} = 0
IO12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O12PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
O6 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -3mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
OD14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
OP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
IOP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
O4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 4mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -2mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
Supply Current Active	I_{CC}		15	20	mA	All outputs open.
Supply Current Standby	I_{CSBY}			100	µA	Note 3
ChiProtect (SLCT, PE, BUSY, nACK, nERROR)	I_{IL}			±10	µA	Chip in circuit: V_{CC} = 0V V_{IN} = 5.5V Max.
Backdrive Protect (nSLCTIN, nINIT, nAUTOFD, nSTROBE, PD[7:0])	I_{IL}			±10	µA	Chip in circuit: V_{CC} = 0V V_{IN} = 5.5V Max.

Note 1: Output leakage is measured with the current pins in high impedance as defined by the PWRGD pin.

Note 2: Output leakage is measured with the low driving output off, either for a high level output or a high impedance state defined by PWRGD.

Note 3: Defined by the device configuration with the PWRGD input low.

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC} = 3.3V

Table 121 - Clock Pin Loading

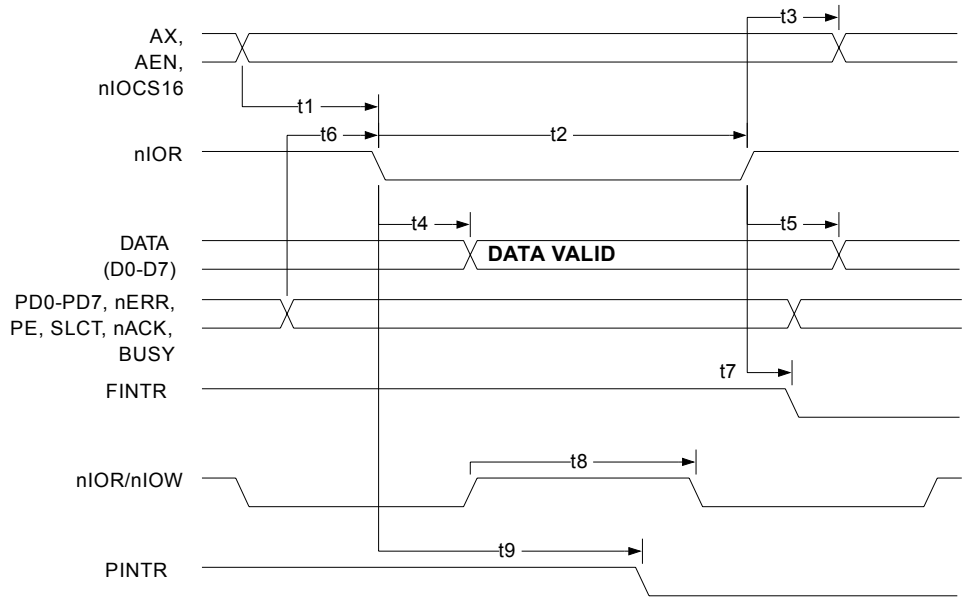
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Table 122 - Capacitive Loading per Output Pin

SIGNAL NAME	TOTAL CAPACITANCE (pF)
SD[0:7]	240
IOCHRDY	240
IRQs	120
DRQs	120
nWGATE	240
nWDATA	240
nHDSEL	240
nDIR	240
nSTEP	240
nDS[1:0]	240
nMTR[1:0]	240
DRVDEN[1:0]	240
TXD	100
nRTS	100
nDTR	100
PD[7:0]	240
nSLCTIN	240
nINIT	240
nALF	240
nSTB	240

AC TIMING

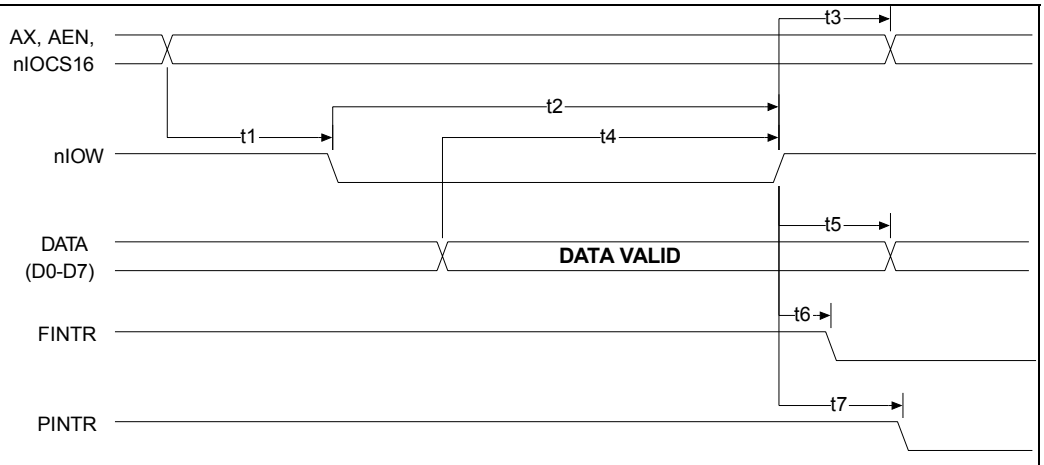
Host Timing



PINTR is the interrupt assigned to the Parallel Port
FINTR is the interrupt assigned to the Floppy Disk

	Parameter	min	typ	max	units
t1	A0-A9, AEN, nIOCS16 Set Up to nIOR Low	40			ns
t2	nIOR Width	150			ns
t3	A0-A9, AEN, nIOCS16 Hold from nIOR High	10			ns
t4	Data Access Time from nIOR Low			100	ns
t5	Data to Float Delay from nIOR High	10		60	ns
t6	Parallel Port Setup		20		ns
t7	Read Strobe to Clear FINTR		40	55	ns
t8	nIOR or nIOW Inactive for Transfers to and from ECP FIFO	150			ns
t9	nIOR Active to PINTR Inactive			260	ns

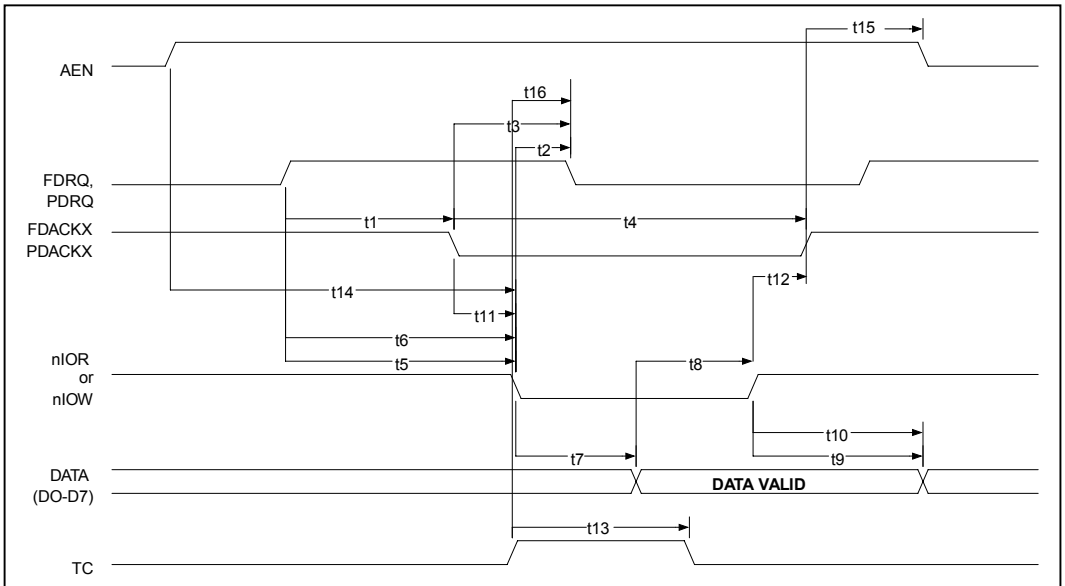
FIGURE 8 - MICROPROCESSOR READ TIMING



PINTR is the interrupt assigned to the Parallel Port
FINTR is the interrupt assigned to the Floppy Disk

	Parameter	min	typ	max	units
t1	A0-A9, AEN, nIOCS16 Set Up to nIOW Low	40			ns
t2	nIOW Width	150			ns
t3	A0-A9, AEN, nIOCS16 Hold from nIOW High	10			ns
t4	Data Set Up Time to nIOW High	40			ns
t5	Data Hold Time from nIOW High	10			ns
t6	Write Strobe to Clear FINTR		40	55	ns
t7	nIOW Inactive to PINTR Inactive			260	ns

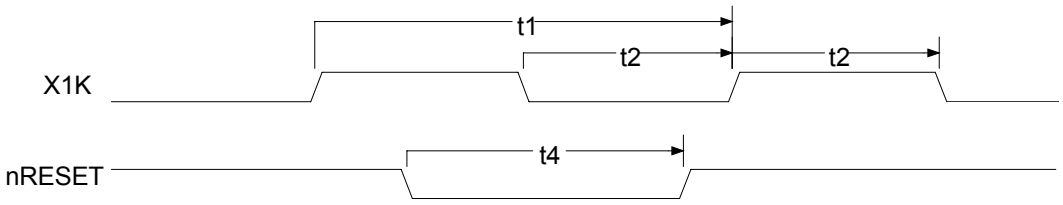
FIGURE 9 - MICROPROCESSOR WRITE TIMING



FDRQ refers to the DRQ assigned to the Floppy Disk
PDRQ refers to the DRQ assigned to the Parallel Port
FDACKX refers to the nDACK assigned to the to the Floppy Disk
PDACKX refers to the nDACK assigned to the Parallel Port

	Parameter	min	typ	max	units
t1	nDACK Delay Time from FDRQ High	0		100	ns
t2	DRQ Reset Delay from nIOR or nIOW			100	ns
t3	FDRQ Reset Delay from nDACK Low				ns
t4	nDACK Width	150			ns
t5	nIOR Delay from FDRQ High	0			ns
t6	nIOW Delay from FDRQ High	0		100	ns
t7	Data Access Time from nIOR Low				ns
t8	Data Set Up Time to nIOW High	40		60	ns
t9	Data to Float Delay from nIOR High	10			ns
t10	Data Hold Time from nIOW High	10			ns
t11	nDACK Set Up to nIOW/nIOR Low	5			ns
t12	nDACK Hold After nIOW/nIOR High	10			ns
t13	TC Pulse Width	60			ns
t14	AEN Set Up to nIOR/nIOW	40			ns
t15	AEN Hold from nDACK	10		100	ns
t16	TC Active to PDRQ Inactive				ns

FIGURE 10 - DMA TIMING

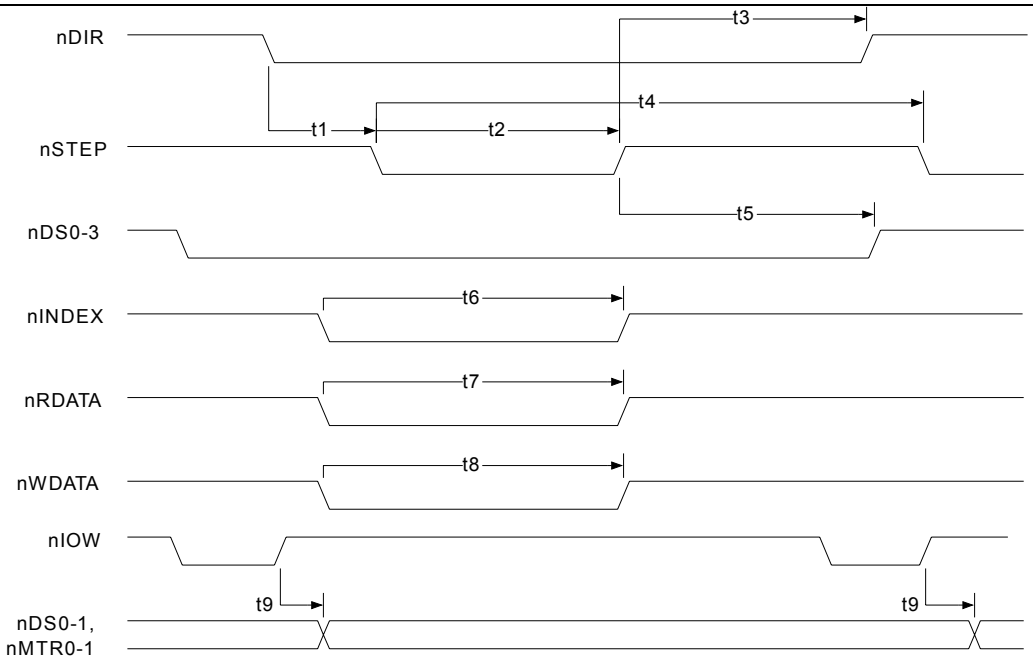


	Parameter	min	typ	max	units
t1	Clock CycleTime for 14.318MHz		70	65	ns
t2	Clock High Time/Low Time for 14.318MHz		35		ns
t1	Clock Cycle Time for 32kHz		31.25		us
t2	Clock High Time/Low Time for 32kHz		16.53		us
	Clock Rise Time/Fall Time (not shown)			5	ns
t4	nRESET Low Time	1.5			us

The nRESET low time is dependent upon the processor clock.
The nRESET must be active for a minimum of 1.5us.

FIGURE 11 - CLOCK TIMING

FDD Timing



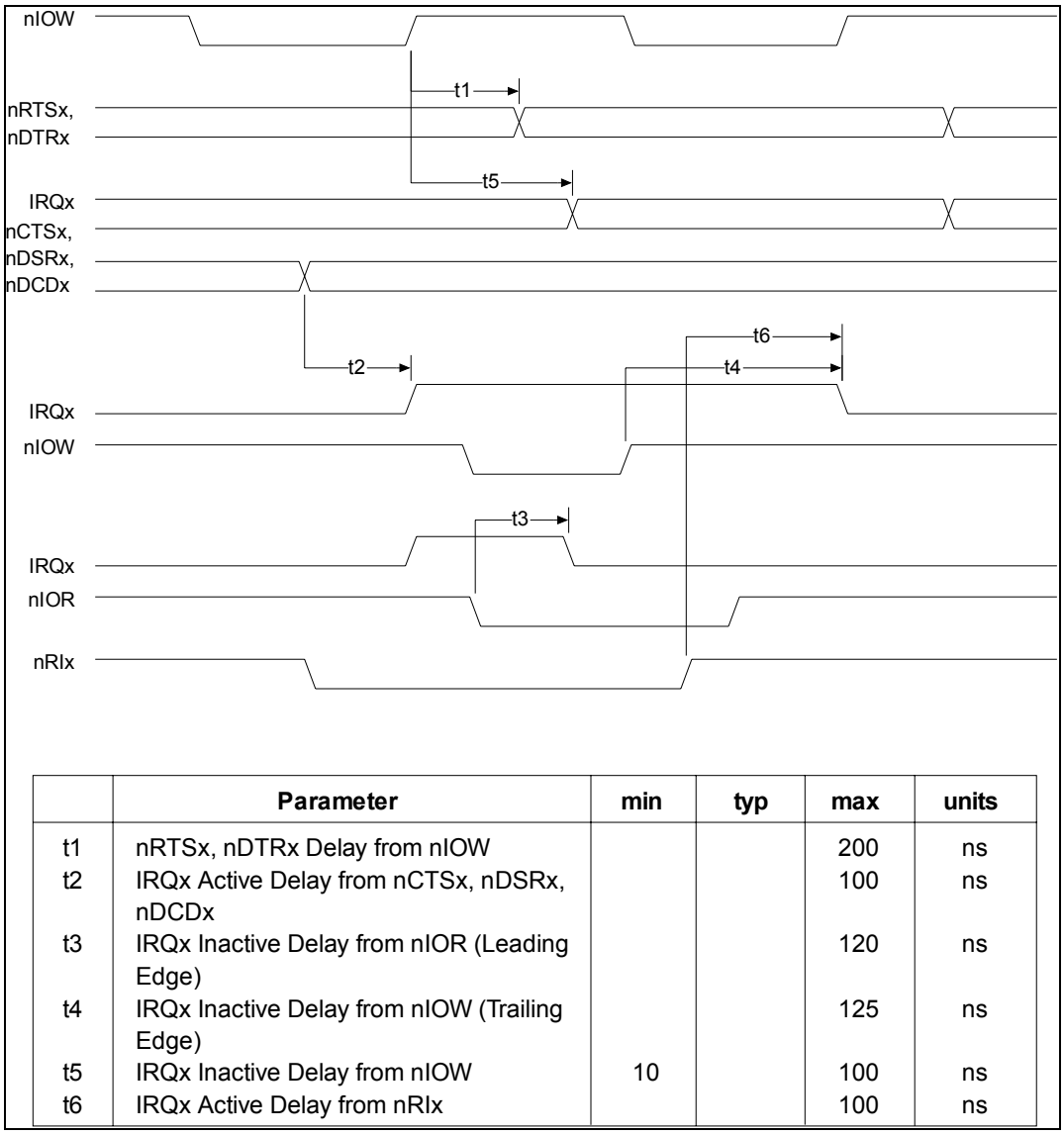
(AT Mode timing only)

	Parameter	min	typ	max	units
t1	nDIR Set Up to nSTEP Low		4		X*
t2	nSTEP Active Time Low		24		X*
t3	nDIR Hold Time After nSTEP		96		X*
t4	nSTEP Cycle Time		132		X*
t5	nDS0-1 Hold Time from nSTEP Low		20		X*
t6	nINDEX Pulse Width		2		X*
t7	nRDATA Active Time Low		40		ns
t8	nWDATA Write Data Width Low		.5		Y*
t9	nDS0-1, MTR0-1 from End of nIOW		25		ns

*X specifies one MCLK period and Y specifies one WCLK period.
MCLK = 16x Data Rate (at 500 Kbp/s MCLK = 8 MHz)
WCLK = 2x Data Rate (at 500 Kbp/s WCLK = 1 MHz)

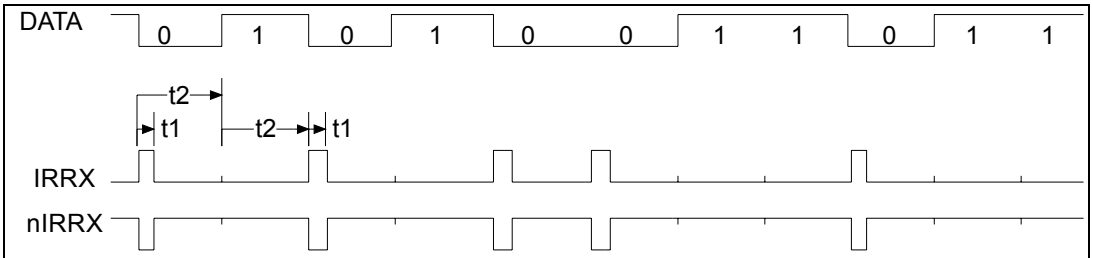
FIGURE 12 - DISK DRIVE TIMING

Serial Port Timing



	Parameter	min	typ	max	units
t1	nRTSx, nDTRx Delay from nIOW			200	ns
t2	IRQx Active Delay from nCTSx, nDSRx, nDCDx			100	ns
t3	IRQx Inactive Delay from nIOR (Leading Edge)			120	ns
t4	IRQx Inactive Delay from nIOW (Trailing Edge)			125	ns
t5	IRQx Inactive Delay from nIOW	10		100	ns
t6	IRQx Active Delay from nRIx			100	ns

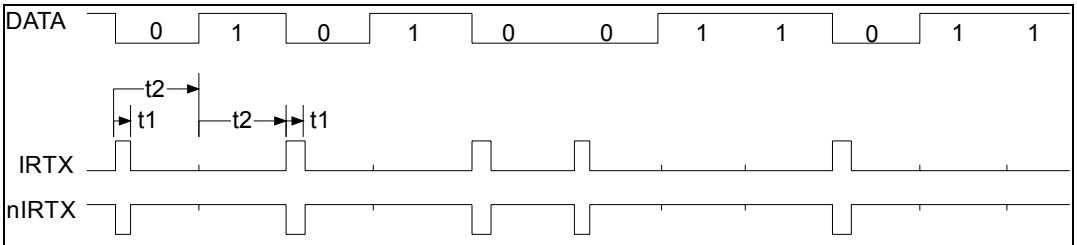
FIGURE 13 - SERIAL PORT TIMING



	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.4	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.4	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.4	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.4	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.4	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.4	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.4	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:
1. Receive Pulse Detection Criteria: A received pulse is considered detected if the received pulse is a minimum of 1.41µs.
2. IRRX: CRC Bit 0: 1 = RCV active low
   nIRRX: CRC Bit 0: 0 = RCV active high (default)

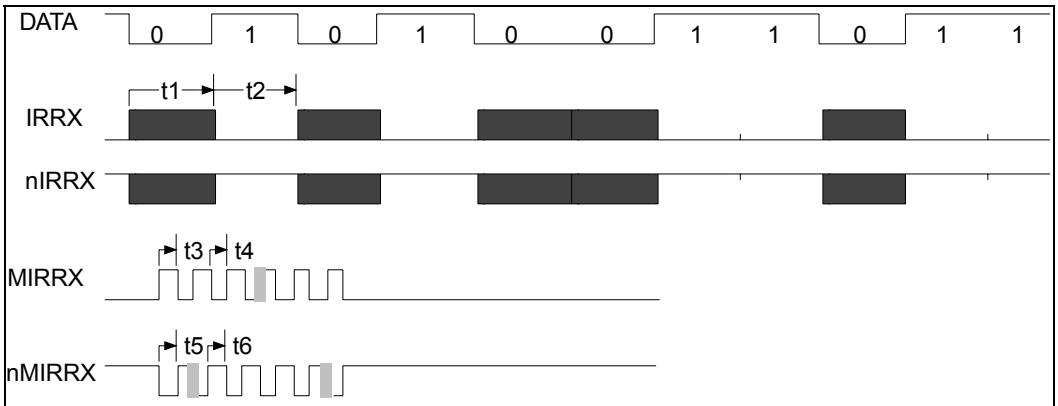
FIGURE 14 - IRDA SIR RECEIVE TIMING



	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.41	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.41	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.41	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.41	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.41	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.41	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.41	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:
1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. IRTX: CRC Bit 1: 1 = XMIT active low (default)
   nIRTX: CRC Bit 1: 0 = XMIT active high

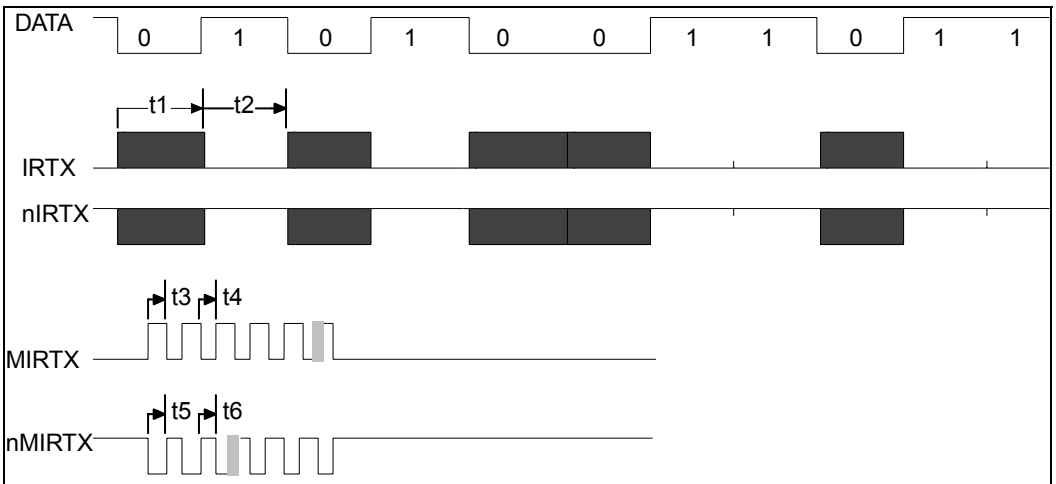
FIGURE 15 - IRDA SIR TRANSMIT TIMING



	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "On"	0.8	1	1.2	µs

Notes:
1. IRRX: CRC Bit 0: 1 = RCV active low
   nIRRX: CRC Bit 0: 0 = RCV active high (default)
   MIRRX, nMIRRX are the modulated outputs

FIGURE 16 - AMPLITUDE SHIFT KEYED IR RECEIVE TIMING

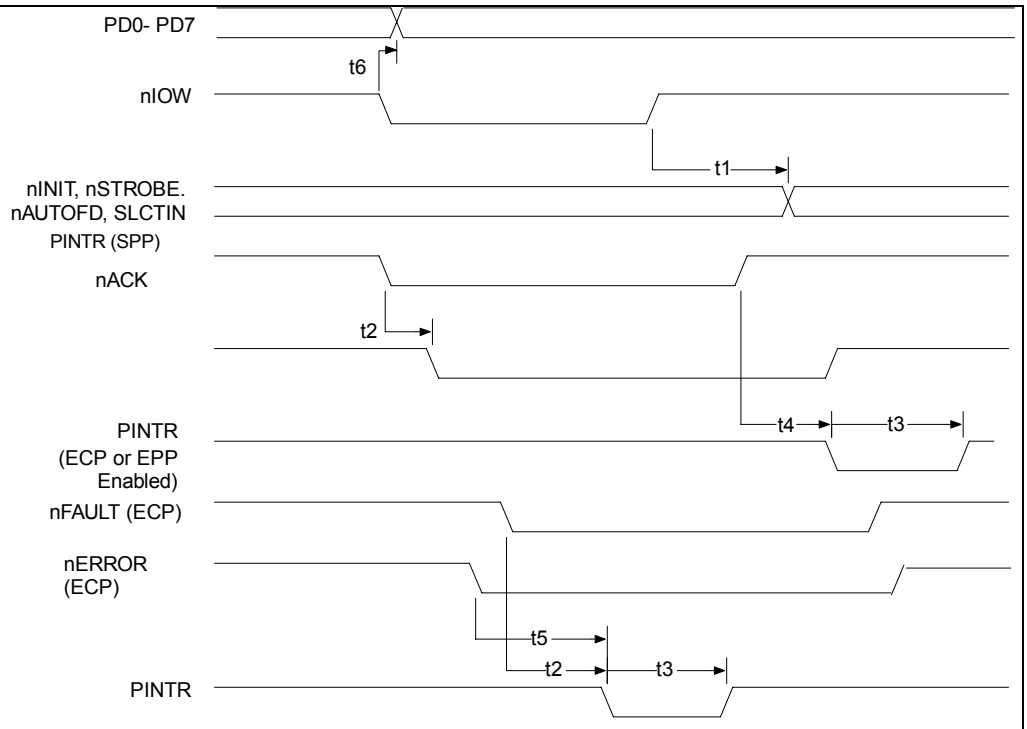


	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "On"	0.8	1	1.2	µs

Notes:
1. IRTX: CRC Bit 1: 1 = XMIT active low (default)
   nIRTX: CRC Bit 1: 0 = XMIT active high
   MIRTX, nMIRTX are the modulated outputs

FIGURE 17 - AMPLITUDE SHIFT KEYED IR TRANSMIT TIMING

Parallel Port Timing

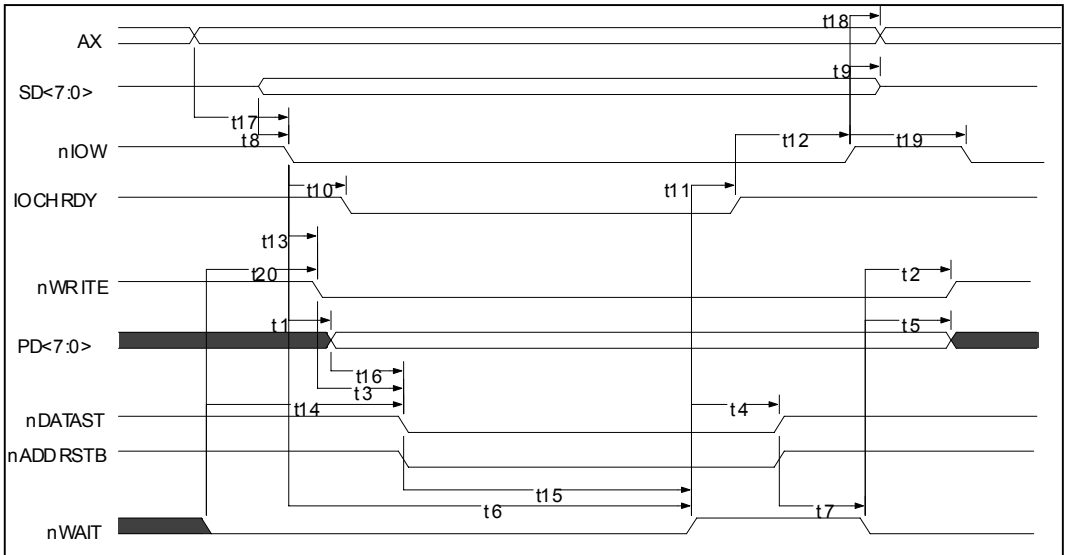


	Parameter	min	typ	max	units
t1	nINIT, nSTROBE, nAUTOFD Delay from nIOW Inactive			100	ns
t2	PINTR Delay from nACK, nFAULT			60	ns
t3	PINTR Active Low in ECP and EPP Modes	200		300	ns
t4	PINTR Delay from nACK			105	ns
t5	nERROR Active to PINTR Active			105	ns
t6	PD0-PD7 Delay from nIOW Active			100	ns

PINTR is the interrupt assigned to the Parallel Port

FIGURE 18 - PARALLEL PORT TIMING

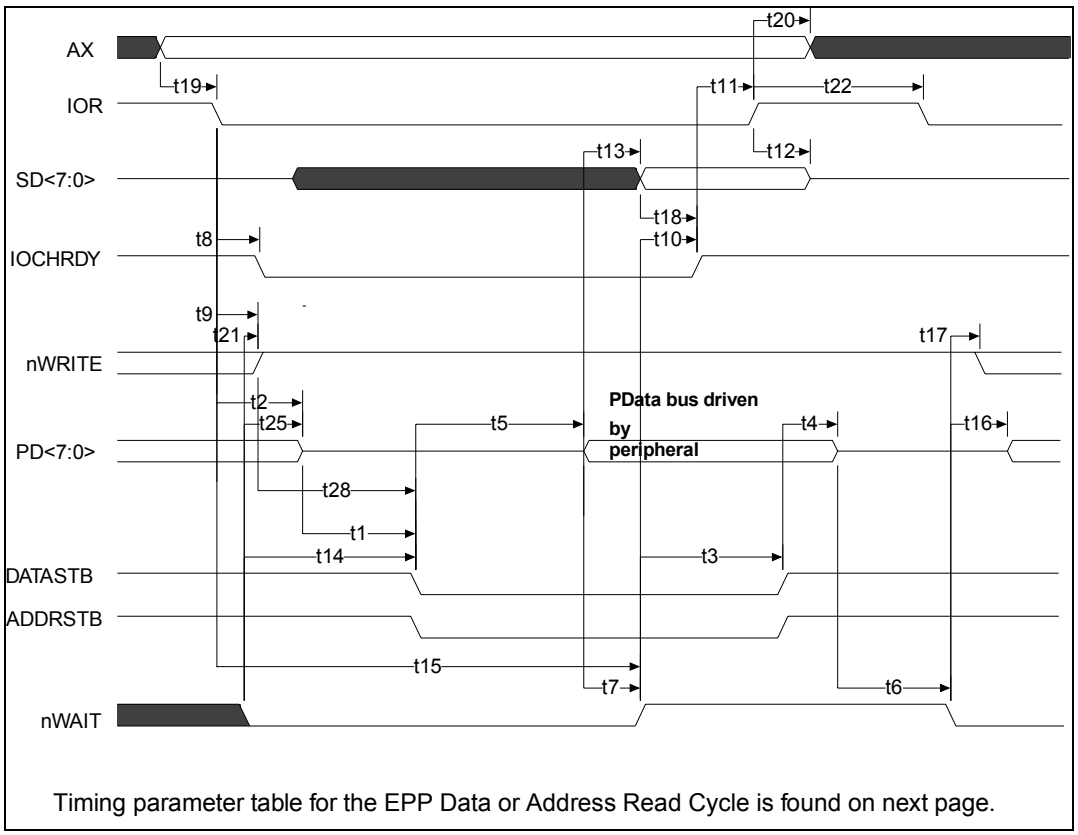
Parallel Port EPP Timing



	Parameter	min	max	units	Notes
t1	nIOW Asserted to PDATA Valid	0	50	ns	
t2	nWAIT Asserted to nWRITE Change	60	185	ns	1
t3	nWRITE to Command Asserted	5	35	ns	
t4	nWAIT Deasserted to Command Deasserted	60	190	ns	1
t5	nWAIT Asserted to PDATA Invalid	0		ns	1
t6	Time Out	10	12	µs	
t7	Command Deasserted to nWAIT Asserted	0		ns	
t8	SDATA Valid to IOW Asserted	10		ns	
t9	nIOW Deasserted to DATA Invalid	0		ns	
t10	nIOW Asserted to IOCHRDY Deasserted	0	24	ns	
t11	WAIT Deasserted to nIOCHRDY Asserted	60	160	ns	1
t12	IOCHRDY Deasserted to nIOW Asserted	10		ns	
t13	nIOW Asserted to nWRITE Asserted	0	70	ns	
t14	nWAIT Asserted to Command Asserted	60	210	ns	1
t15	Command Asserted to nWAIT Deasserted	0	10	µs	
t16	PDATA Valid to Command Asserted	10		ns	
t17	Ax Valid to nIOW Asserted	40		ns	
t18	nIOW Deasserted to Ax Invalid	10		ns	
t19	nIOW Deasserted to nIOW or nIOR Asserted	40		ns	
t20	nWAIT Asserted to nWRITE Asserted	60	185	ns	1

NOTE: WAIT must be filtered to compensate for ringing on the parallel bus cable. WAIT is considered to have settled after it does not transition for a minimum of 50 nsec.

FIGURE 19 - EPP 1.9 DATA OR ADDRESS WRITE CYCLE



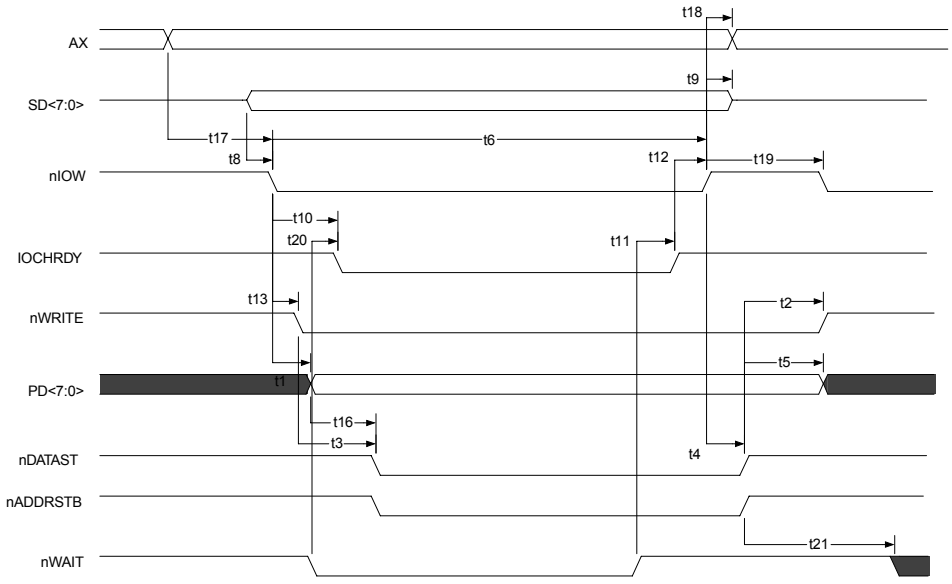
Timing parameter table for the EPP Data or Address Read Cycle is found on next page.

FIGURE 20 - EPP 1.9 DATA OR ADDRESS READ CYCLE

	Parameter	min	max	units	Notes
t1	PDATA Hi-Z to Command Asserted	0	30	ns	
t2	nIOR Asserted to PDATA Hi-Z	0	50	ns	
t3	nWAIT Deasserted to Command Deasserted	60	180	ns	1
t4	Command Deasserted to PDATA Hi-Z	0		ns	
t5	Command Asserted to PDATA Valid	0		ns	
t6	PDATA Hi-Z to nWAIT Deasserted	0		µs	
t7	PDATA Valid to nWAIT Deasserted	0		ns	
t8	nIOR Assertd to IOCHRDY Deasserted	0	24	ns	
t9	nWRITE Deasserted to nIOR Asserted	0		ns	2
t10	nWAIT Deasserted to IOCHRDY Asserted	60	160	ns	1
t11	IOCHRDY Deasserted to nIOR Asserted	0		ns	
t12	nIOR Deasserted to SDATA Hi-Z (Hold Time)	0	40	ns	
t13	PDATA Valid to SDATA Valid	0	75	ns	
t14	nWAIT Asserted to Command Asserted	0	195	ns	
t15	Time Out	10	12	µs	
t16	nWAIT Deasserted to PDATA Driven	60	190	ns	1
t17	nWAIT Deasserted to nWRITE Modified	60	190	ns	1,2
t18	SDATA Valid to IOCHRDY Asserted	0	85	ns	3
t19	Ax Valid to nIOR Asserted	40		ns	
t20	nIOR Deasserted to Ax Invalid	10		ns	
t21	nWAIT Asserted to nWRITE Deasserted	0	185	ns	
t22	nIOR Deasserted to nIOW or nIOR Asserted	40		ns	
t25	nWAIT Asserted to PDATA Hi-Z	60	180	ns	1
t28	WRITE Deasserted to Command	1		ns	

NOTES:
1. nWAIT is considered to have settled after it does not transition for a minimum of 50 ns.
2. When not executing a write cycle, EPP nWRITE is inactive high.
3. 85 is true only if t7 = 0.

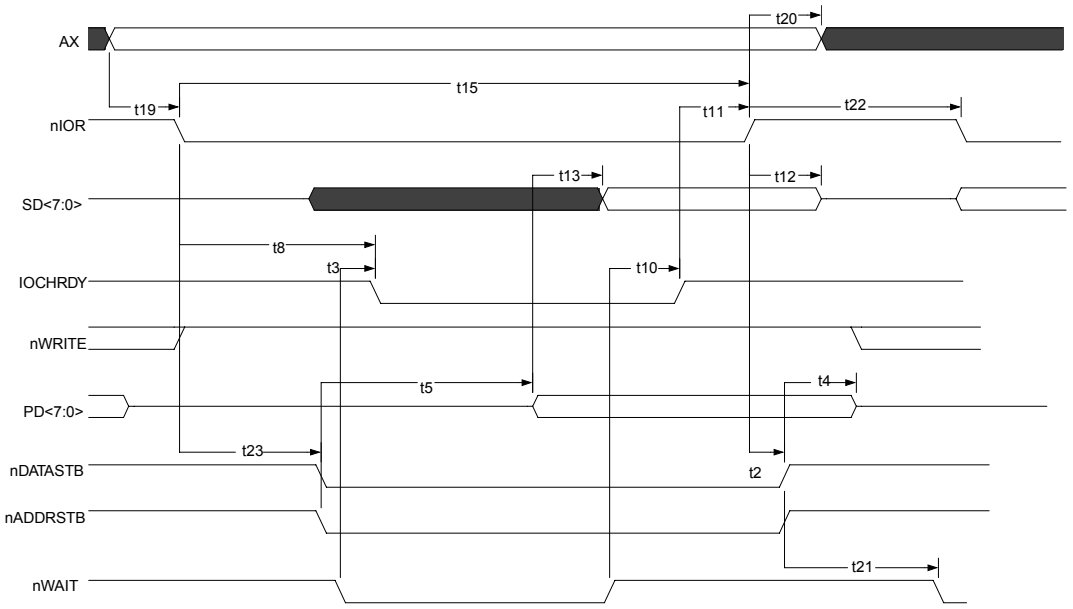
FIGURE 21 - EPP 1.9 DATA OR ADDRESS READ CYCLE TIMING PARAMETERS



	Parameter	min	max	units	Notes
t1	nIOW Asserted to PDATA Valid	0	50	ns	
t2	Command Dessserted to nWRITE Change	0	40	ns	
t3	nWRITE to Command	5	35	ns	
t4	nIOW Deasserted to Command Deasserted		50	ns	2
t5	Command Deasserted to PDATA Invalid	50		ns	
t6	Time Out	10	12	µs	
t8	SDATA Valid to nIOW Asserted	10		ns	
t9	nIOW Deasserted to DATA Invalid	0		ns	
t10	nIOW Asserted to IOCHRDY Deasserted	0	24	ns	
t11	nWAIT Deasserted to IOCHRDY Asserted		40	ns	
t12	IOCHRDY Deasserted to nIOW Deasserted	10		ns	
t13	nIOW Asserted to nWRITE Asserted	0	50	ns	
t16	PDATA Valid to Command Asserted	10	35	ns	
t17	Ax Valid to nIOW Asserted	40		ns	
t18	nIOW Deasserted to Ax Invalid	10		µs	
t19	nIOW Deasserted to nIOW or nIOR Asserted	100		ns	
t20	nWAIT Asserted to IOCHRDY Deasserted		45	ns	
t21	Command Deasserted to nWAIT Deasserted	0		ns	

NOTES:
1. WRITE is controlled by clearing the PDIR bit to "0" in the control register before performing an EPP Write.
2. This number is only valid if WAIT is active when nIOW goes active.

FIGURE 22 - EPP 1.7 DATA OR ADDRESS WRITE CYCLE



	Parameter	min	max	units	Notes
t2	nIOR Deasserted to Command Deasserted		50	ns	
t3	nWAIT Asserted to IOCHRDY Deasserted	0	40	ns	
t4	Command Deasserted to PDATA Hi-Z	0		ns	
t5	Command Asserted to PDATA Valid	0		ns	
t8	nIOR Asserted to IOCHRDY Deasserted		24	ns	
t10	nWAIT Deasserted to IOCHRDY Asserted		50	ns	
t11	nIOCHRDY Deasserted to nIOR Asserted	0		ns	
t12	nIOR Deasserted to SDATA High-Z (Hold Time)	0	40	ns	
t13	PData Valid to SDATA Valid		40	ns	
t15	Time Out	10	12	µs	
t19	Ax Valid to nIOR Asserted	40		ns	
t20	nIOR Deasserted to Ax Invalid	10		ns	
t21	Command Deasserted to nWAIT Deasserted	0		ns	
t22	nIOR Deasserted to nIOW or nIOR Asserted	40		ns	
t23	nIOR Asserted to Command Asserted		55	ns	

NOTE:

1. nWRITE is controlled by setting the PDIR bit to "1" in the control register before performing an EPP Read.

FIGURE 23 - EPP 1.7 DATA OR ADDRESS READ CYCLE

PARALLEL PORT ECP TIMING

Parallel Port FIFO (Mode 101)
The standard parallel port is run at or near the peak 500 Kbps allowed in the forward direction using DMA. The state machine does not examine nAck and begins the next transfer based on Busy. Refer to FIGURE 23.

ECP Parallel Port Timing
The timing is designed to allow operation at approximately 2.0Mbytes/sec over a 15ft cable. If a shorter cable is used then the bandwidth will increase.

Forward-Idle
When the host has no data to send it keeps HostClk (nStrobe) high and the peripheral will leave PeriphClk (Busy) low.

Forward Data Transfer Phase
The interface transfers data and commands from the host to the peripheral using an interlocked PeriphAck and HostClk. The peripheral may indicate its desire to send data to the host by asserting nPeriph Request.

The Forward Data Transfer Phase may be entered from the Forward-Idle Phase. While in the Forward Phase the peripheral may asynchronously assert the nPeriph Request (nFault) to request that the channel be reversed. When the peripheral is not busy it sets PeriphAck (Busy) low. The host then sets HostClk (nStrobe) low when it is prepared to send data. The data must be stable for the specified setup time prior to the falling edge of HostClk. The peripheral then sets PeriphAck (Busy) high to acknowledge the handshake. The host then sets HostClk (nStrobe) high. The peripheral then accepts the data and sets PeriphAck (Busy) low, completing the transfer. This sequence is shown in FIGURE 24.

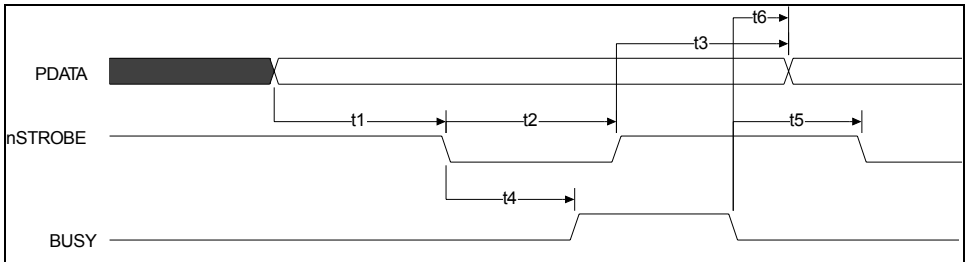
The timing is designed to provide 3 cable round-trip times for data setup if Data is driven simultaneously with HostClk (nStrobe).

Reverse-Idle Phase
The peripheral has no data to send and keeps PeriphClk high. The host is idle and keeps HostAck low.

Reverse Data Transfer Phase
The interface transfers data and commands from the peripheral to the host using an interlocked HostAck and PeriphClk.

The Reverse Data Transfer Phase may be entered from the Reverse-Idle Phase. After the previous byte has beed accepted the host sets HostAck (nAutoFd) low. The peripheral then sets PeriphClk (nAck) low when it has data to send. The data must be stable for the specified setup time prior to the falling edge of PeriphClk. When the host is ready it to accept a byte it sets. HostAck (nAutoFd) high to acknowledge the handshake. The peripheral then sets PeriphClk (nAck) high. After the host has accepted the data it sets HostAck (nAutoFd) low, completing the transfer. This sequence is shown in FIGURE 25.

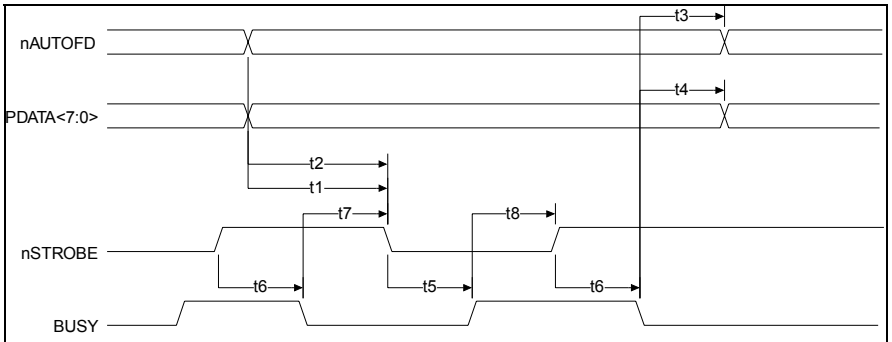
Output Drivers
To facilitate higher performance data transfer, the use of balanced CMOS active drivers for critical signals (Data, HostAck, HostClk, PeriphAck, PeriphClk) are used ECP Mode. Because the use of active drivers can present compatibility problems in Compatible Mode (the control signals, by tradition, are specified as open-collector), the drivers are dynamically changed from open-collector to totem-pole. The timing for the dynamic driverchange is specified in the IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14, July. 14, 1993, available from Microsoft. The dynamic driver change must be implemented properly to prevent glitching the outputs.



	Parameter	min	max	units	Notes
t1	DATA Valid to nSTROBE Active	600		ns	
t2	nSTROBE Active Pulse Width	600		ns	
t3	DATA Hold from nSTROBE Inactive	450		ns	1
t4	nSTROBE Active to BUSY Active		500	ns	
t5	BUSY Inactive to nSTROBE Active	680		ns	
t6	BUSY Inactive to PDATE Invalid	80		ns	1

NOTE:
1. The data is held until BUSY goes inactive or for time t3, whichever is longer. This only applies if another data transfer is pending. If no other data transfer is pending, the data is held indefinitely.

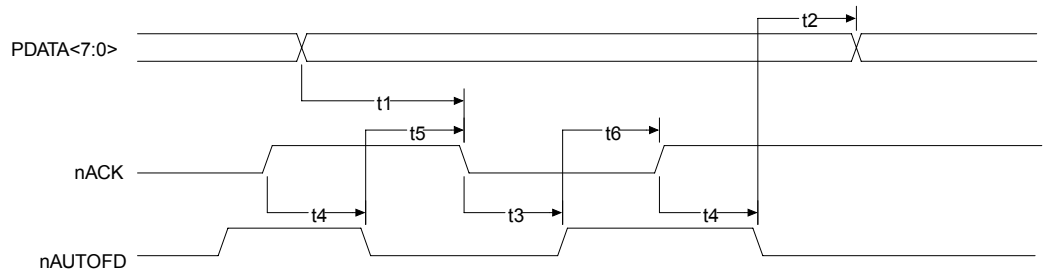
FIGURE 24 - PARALLEL PORT FIFO TIMING



	Parameter	min	max	units	Notes
t1	nAUTOFD Valid to nSTROBE Asserted	0	60	ns	
t2	PDATA Valid to nSTROBE Asserted	0	60	ns	
t3	BUSY Deasserted to nAUTOFD Changed	80	180	ns	1,2
t4	nBUSY Deasserted to PDATA Changed	80	180	ns	1,2
t5	nSTROBE Asserted to BUSY Asserted	0		ns	
t6	nSTROBE Deasserted to Busy Deasserted	0		ns	
t7	nBUSY Deasserted to nSTROBE Asserted	80	200	ns	1,2
t8	nBUSY Asserted to nSTROBE Deasserted	80	180	ns	2

NOTES:
1. Maximum value only applies if there is data in the FIFO waiting to be written out.
2. BUSY is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

FIGURE 25 - ECP PARALLEL PORT FORWARD TIMING

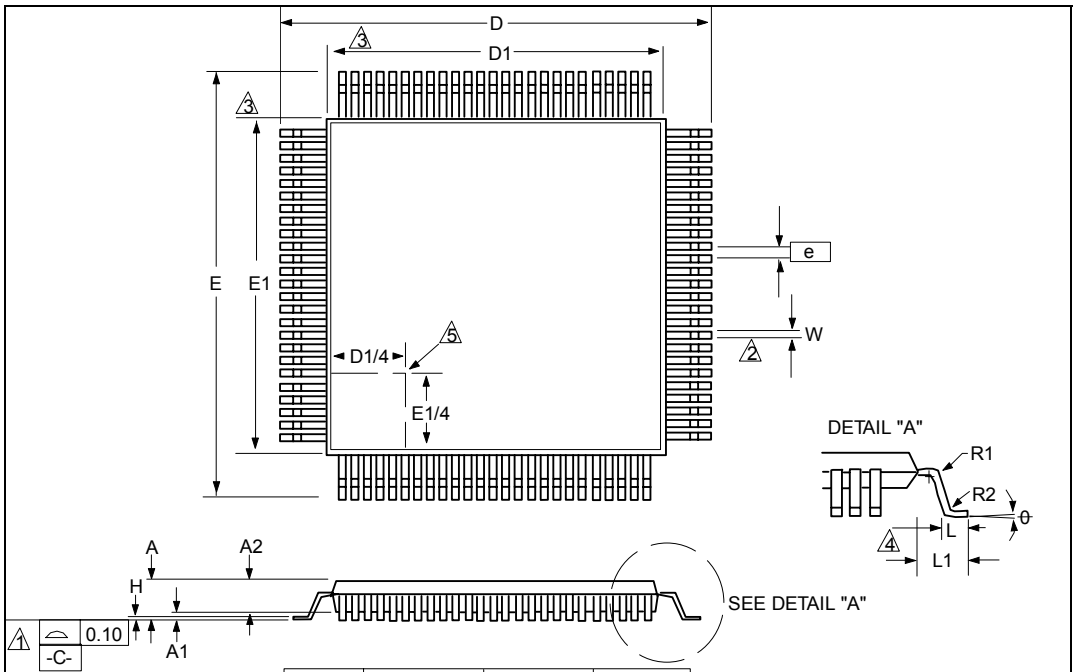


	Parameter	min	max	units	Notes
t1	PDATA Valid to nACK Asserted	0		ns	
t2	nAUTOFD Asserted to PDATA Changed	0		ns	
t3	nACK Asserted to nAUTOFD Deasserted	80	200	ns	1,2
t4	nACK Deasserted to nAUTOFD Asserted	80	200	ns	2
t5	nAUTOFD Asserted to nACK Asserted	0		ns	
t6	nAUTOFD Deasserted to nACK Deasserted	0		ns	

NOTES:
1. Maximum value only applies if there is room in the FIFO and a terminal count has not been received. ECP can stall by keeping nAUTOFD low.
2. nACK is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

FIGURE 26 - ECP PARALLEL PORT REVERSE TIMING

Package Outlines



DIM	MIN	NOM	MAX
A			1.6
A1	0.05		
A2	1.35	1.40	1.45
D	15.75	16.00	16.25
D1	13.90	14.00	14.10
E	15.75	16.00	16.25
E1	13.90	14.00	14.10
H			0.20
L	0.45	0.60	0.75
L1		1.00	
e		0.50 BSC	
θ	0°		8°
W		0.25	
R1		0.20	
R2		0.20	

Notes:
1. Coplanarity is 0.100mm maximum.
2. Tolerance on the position of the leads is 0.13mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25mm per side.
4. Dimension for foot length L are measured at the gauge plane 0.25mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.
6. Controlling dimension: millimeter

FIGURE 27 - 100 PIN TQFP PACKAGE OUTLINE