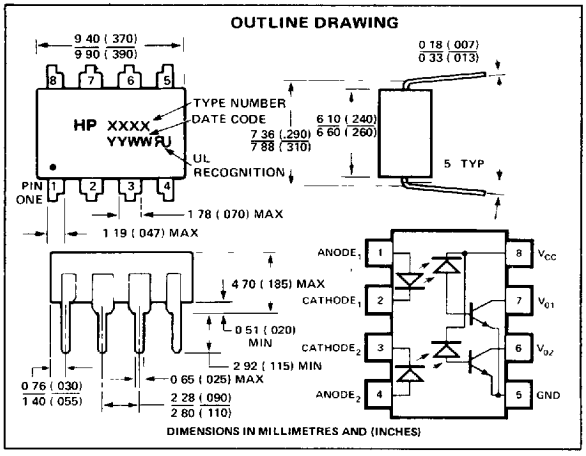
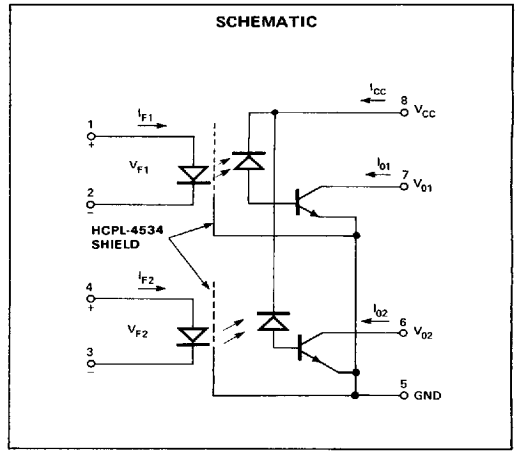
HEWLETT PACKARD

DUAL HIGH SPEED OPTOCOUPLER

HCPL-2530
HCPL-2531
HCPL-4534





Features

- **HIGH SPEED: 1 Mb/s**
- **TTL COMPATIBLE**
- **VERY HIGH COMMON MODE TRANSIENT IMMUNITY: 15000 V/μs @ V_{CM} = 1500 V GUARANTEED (HCPL-4534)**
- **HIGH DENSITY PACKAGING**
- **3 MHz BANDWIDTH**
- **OPEN COLLECTOR OUTPUTS**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE AND 5000 VAC, 1 MINUTE (OPTION 020) PENDING APPROVAL**
- **CSA APPROVED UNDER COMPONENT ACCEPTANCE NOTICE NO. 5 (FILE NO. LR88324)**
- **MIL-STD-1772 VERSION AVAILABLE (HCPL-5530/31)**

Description

These dual optocouplers contain a pair of light emitting diodes and integrated photo detectors with electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collectors increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

The HCPL-2530 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the -2530 is 7% minimum at I_F = 16 mA.

The HCPL-2531 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the -2531 is 19% minimum at I_F = 16 mA.

The HCPL-4534 is an HCPL-2531 with increased common mode transient immunity of 15000 V/μs minimum at V_{CM} = 1500 V guaranteed

Applications

- **Line Receivers** – High common mode transient immunity (>1000V/μs) and low input-output capacitance (0.6pF).
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Pulse Transformers** – Save board space and weight.
- **Analog Signal Ground Isolation** – Integrated photon detector provides improved linearity over phototransistor type.
- **Polarity Sensing.**
- **Isolated Analog Amplifier** – Dual channel packaging enhances thermal tracking.

Absolute Maximum Ratings

Storage Temperature	-55°C to +125°C
Operating Temperature	-55°C to +100°C
Lead Solder Temperature (1.6mm below seating plane)	260°C for 10s
Average Input Current – I_F (each channel)	25mA[1]
Peak Input Current – I_F (each channel) (50% duty cycle, 1 ms pulse width)	50mA[2]
Peak Transient Input Current – I_F (each channel) (≤1μs pulse width, 300pps)	1.0 A
Reverse Input Voltage – V_R (each channel)	5V
Input Power Dissipation (each channel)	45mW[3]
Average Output Current – I_O (each channel)	8mA
Peak Output Current – I_O (each channel)	16mA
Supply Voltage - V_{CC} (Pin 8-5)	- 0.5V to 30V
Output Voltage - V_O (Pin 7,6-5)	- 0.5V to 20V
Output Power Dissipation (each channel)	35mW[4]

See notes, following page

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. See note 13.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions			Fig.	Note
Current Transfer Ratio	CTR	HCPL-2530	7	18	50	%	T_A = 25°C	V_O = 0.5 V	I_F = 16 mA, V_{CC} = 4.5 V	1, 2 4	5, 6
			5					V_O = 0.5 V			
		HCPL-2531 HCPL-4534	19	24	50	%	T_A = 25°C	V_O = 0.5V			
			15					V_O = 0.5 V			
Logic Low Output Voltage	V_{OL}	HCPL-2530		0.1	0.4	V	T_A = 25°C	I_O = 1.1 mA	I_F = 16 mA, V_{CC} = 4.5 V	1	5
					0.5			I_O = 0.8 mA			
		HCPL-2531 HCPL-4534		0.1	0.4	V	T_A = 25°C	I_O = 3.0 mA			
					0.5			I_O = 2.4 mA			
Logic High Output Current	I_{OH}			0.003	0.5	µA	T_A = 25°C	V_O = V_{CC} = 5.5 V	I_F = 0 mA	6	5
							T_A = 25°C	V_O = V_{CC} = 15.0 V			
					50						
Logic Low Supply Current	I_{CCL}			100	400	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V				
Logic High Supply Current	I_{CCH}			0.05	4	µA	I_F = 0 mA, V_O = Open, V_{CC} = 15 V				
Input Forward Voltage	V_F			1.5	1.7	V	T_A = 25°C	I_F = 16 mA		3	5
					1.8						
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA				5
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16 mA				
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0 V				5
Input-Output Insulation Voltage	V_{ISO}		2500			V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C				7, 14
OPT 020 (PENDING)	V_{ISO}		5000								7, 15
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc				7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz				7
Input-Input Insulation Leakage Current	I_{I-I}			0.005		µA	45% Relative Humidity, t = 5 s V_{I-I} = 500 Vdc				8
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω	V_{I-I} = 500 Vdc				8
Capacitance (Input-Input)	C_{I-I}			0.25		pF	f = 1 MHz				8

*All typicals at 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA, unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	HCPL-2530		0.2	1.5	μs	T_A = 25°C	R_L = 4.1 kΩ	5, 9, 11	10, 11
					2.0					
		HCPL-2531 HCPL-4534		0.2	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Propagation Delay Time to Logic High at Output	t_{PLH}	HCPL-2530		1.3	1.5	μs	T_A = 25°C	R_L = 4.1 kΩ	5, 9, 11	10, 11
					2.0					
		HCPL-2531 HCPL-4534		0.6	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	HCPL-2530	1	10		KV/μs	R_L = 4.1 kΩ	I_F = 0 mA, T_A = 25°C, V_{CM} = 10 V_{P-P}	10	9, 10, 11
		HCPL-2531	1	10			R_L = 1.9 kΩ			
		HCPL-4534	15	30			R_L = 1.9 kΩ	I_F = 0 mA, T_A = 25°C, V_{CM} = 1500 V_{P-P}		
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	HCPL-2530	1	10		KV/μs	R_L = 4.1 kΩ	I_F = 16 mA, T_A = 25°C, V_{CM} = 10 V_{P-P}	10	9, 10, 11
		HCPL-2531	1	10			R_L = 1.9 kΩ			
		HCPL-4534	15	30			R_L = 1.9 kΩ	I_F = 16 mA, T_A = 25°C, V_{CM} = 1500 V_{P-P}		

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min.External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

Notes:

1 Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C
2 Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C
3 Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C
4 Derate linearly above 70°C free-air temperature at a rate of 1.0 mW/°C.
5 Each channel
6 CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
7 Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together
8 Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together
9 Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
10 The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor
11 The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull-up resistor
12 The frequency at which the ac output voltage is 3 dB below the low frequency asymptote
13 Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended
14 In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ μA)
15. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ μA).

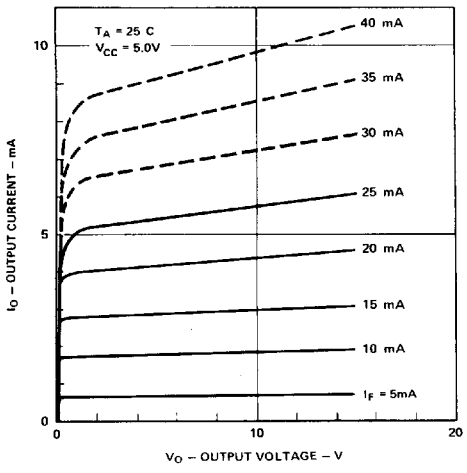


Figure 1. DC and Pulsed Transfer Characteristics.

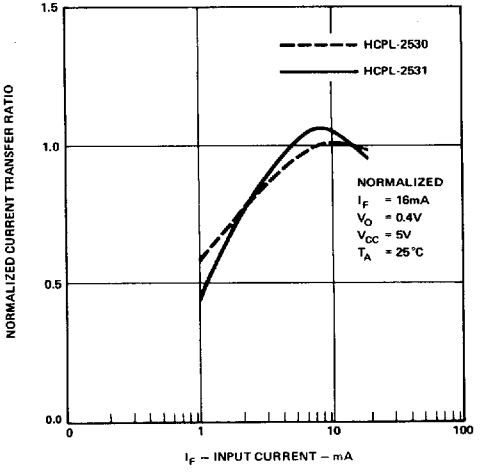


Figure 2. Current Transfer Ratio vs. Input Current.

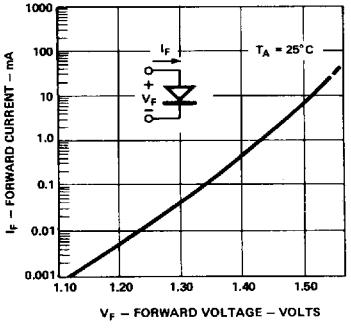


Figure 3. Input Current vs. Forward Voltage.

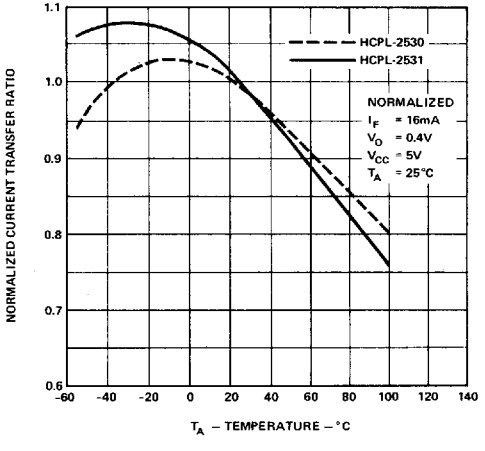


Figure 4. Current Transfer Ratio vs. Temperature.

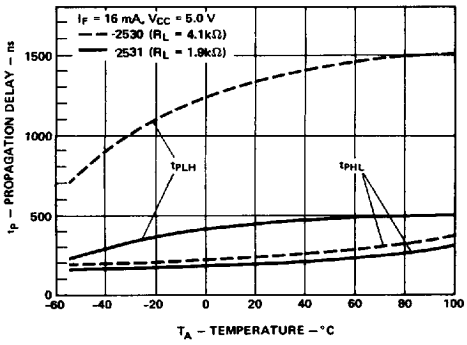


Figure 5. Propagation Delay vs. Temperature.

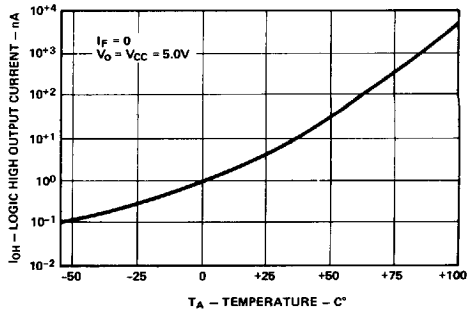


Figure 6. Logic High Output Current vs. Temperature.

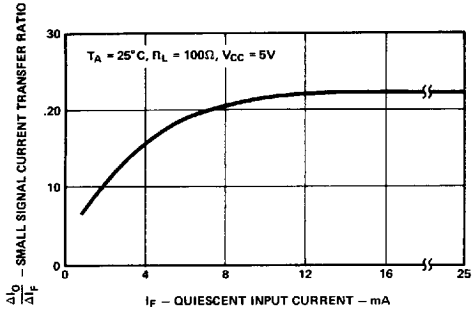
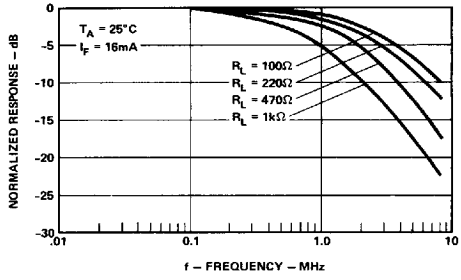


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.



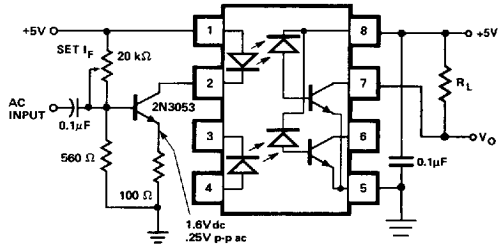


Figure 8. Frequency Response.

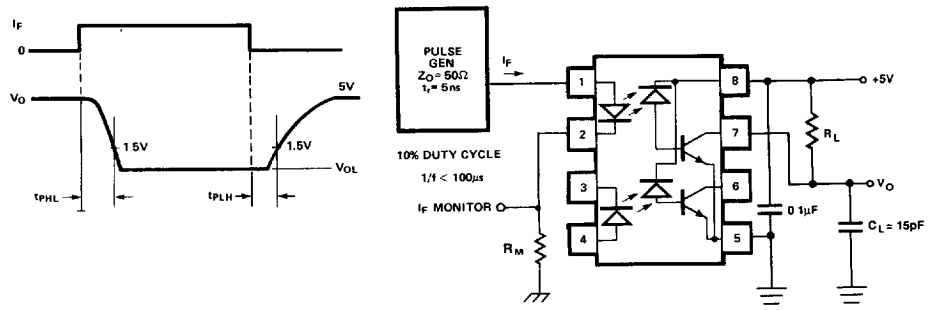


Figure 9. Switching Test Circuit.

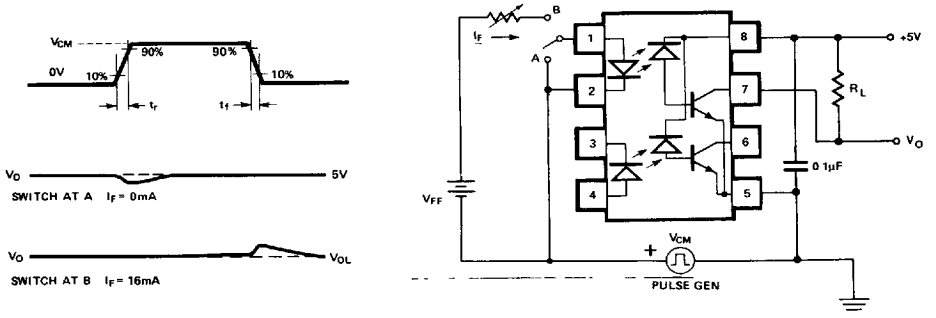


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

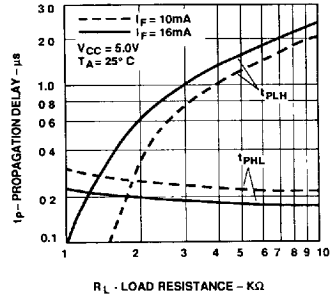


Figure 11. Propagation Delay Time vs. Load Resistance.

OPTO COUPLERS