DATA SHEET

SAA9042
Multi-standard Teletext IC for standard and features TV

Preliminary specification
Supersedes data of November 1990
File under Integrated Circuits, IC02

June 1995

PHILIPS

Multi-standard Teletext IC for standard and features TV

SAA9042

FEATURES

General

- Interfaces with analog and digital TV systems
- Multi-media compatible
- Directly interfaces up to 1 Mbit dynamic RAM
- Fully independent acquisition and display timing
- 3 display modes
  - normal (1H/1V)
  - progressive scan (2H/1V)
  - 100 Hz/120 Hz (2H/2V)
- I²C-bus controlled
- Single 5 V power supply.

Acquisition

- Simultaneous update of up to 8 pages
- Up to 100 page background memory capability
- Software selectable 625/525 line operation
- Full Level-One Features (FLOF) operation
- Table Of Pages (TOP) compatible
- VCR Programming via Teletext (VPT) and Program Delivery Control (PDC) compatible
- Vertical Blanking Interval (VBI) and full channel operation
- Extension packets 26/27/28/29 and 30 fully decoded.

Display

- Stable display by slaving from scan-related timing signals
- Automatic selection of six different languages
- Versions for Western and Eastern Europe and Turkey
- Storage of 192 characters (13 × 10 dot matrix)
- Software controlled RGB level removes the need for hardware adjustment
- Up to 27 display rows; 0 to 24 and up to 2 status rows.

GENERAL DESCRIPTION

The SAA9042 is a CMOS integrated circuit designed for reception, decoding and display of 625 and 525 line World System Teletext (WST).

It is used in conjunction with a teletext video processor (SAA5191) for data regeneration, and a single-chip 64K × 4-bit or 256K × 4-bit dynamic RAM page memory.

The SAA9042 acquires teletext packets defined at levels 1, 2 and 3 in the WST specification and produces a level 1 display.

The device is microcontroller controlled via the standard I²C-bus and is compatible with analog, digital and features TV.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current		–	100	–	mA
f_{clk}	clock frequency	625 line	–	6.9375	–	MHz
		525 line	–	5.7272	–	MHz
T_{amb}	operating ambient temperature		−20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9042	40	DIL	plastic	SOT129

BLOCK DIAGRAM

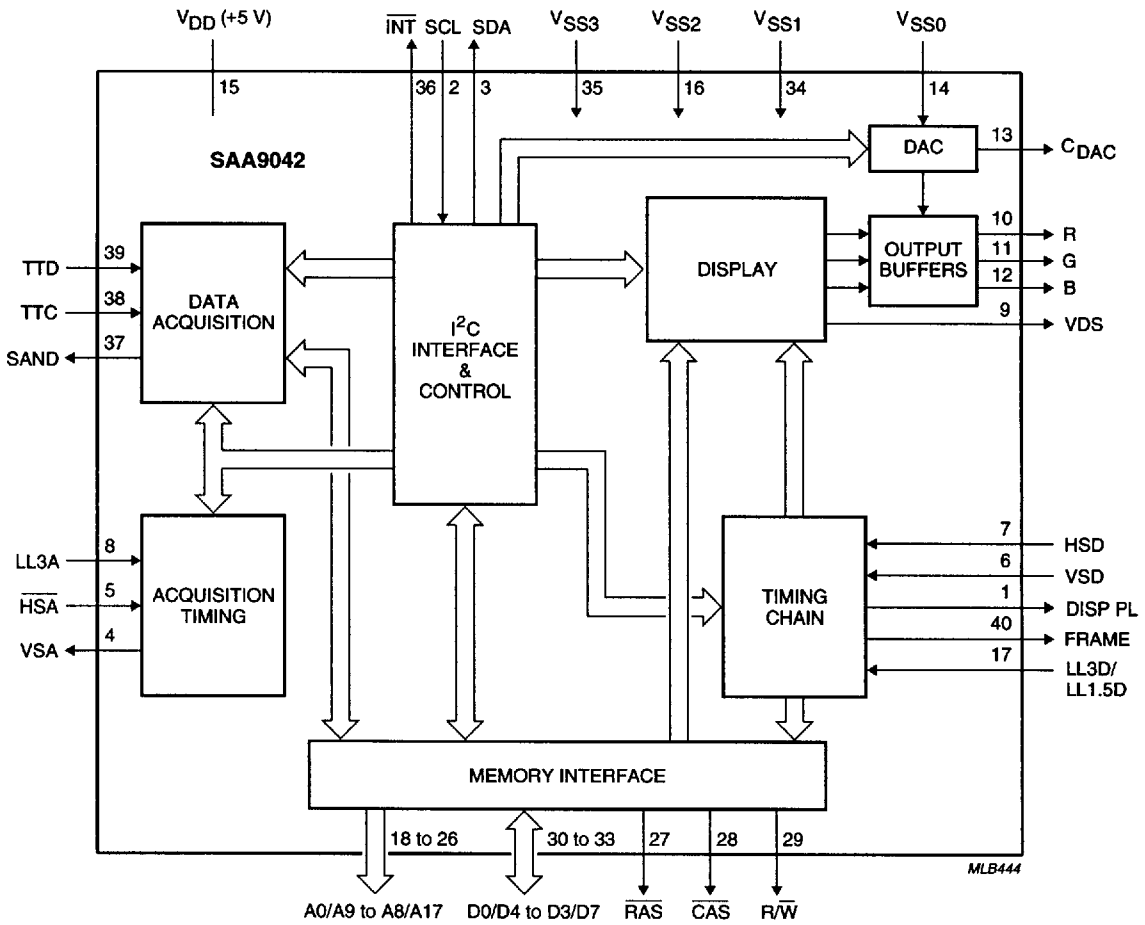


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DISP PL	1	Display PL: a programmable decode from the display-timing chain which can be used as a reference signal in an external PLL in scan-locked applications.
SCL	2	Serial Clock: input signal which is the I²C-bus clock from the microcontroller.
SDA	3	Serial Data: is the I²C-bus data line connected to the microcontroller. It is an input/output function with an open-drain output.
VSA	4	Vertical Synchronization Acquisition: synchronization signal from the SAA5191 (VCS), derived from the incoming video. This input enables field timing to be established in the acquisition section.
$\overline{HSA}$	5	Horizontal Synchronization Acquisition: horizontal synchronization signal derived from the incoming video e.g. burst gate pulse. This active LOW input enables line timing to be established in the acquisition section.
VSD	6	Vertical Synchronization Display: synchronization signal indicating the vertical position of the TV picture. This input allows field synchronization of the display section.
HSD	7	Horizontal Synchronization Display: synchronization signal indicating the horizontal position of the TV picture. This input allows line synchronization of the TV picture.
LL3A	8	Line-Locked system clock: 13.5 MHz system clock input for the acquisition section.
VDS	9	Video/Data Switch: push-pull active HIGH 3-state output which controls the switching between text (HIGH) and normal TV (LOW) picture for both normal text and superimposed displays.
R	10	Red: analog 3-state output which contains video character and background information for text display. The output level is adjustable over 16 steps and is controlled by V_{SS0}, V_{DD} and an internal register.
G	11	Green: analog 3-state output which contains video character and background information for text display. The output level is adjustable over 16 steps and is controlled by V_{SS0}, V_{DD} and an internal register.
B	12	Blue: analog 3-state output which contains video character and background information for text display. The output level is adjustable over 16 steps and is controlled by V_{SS0}, V_{DD} and an internal register.
C_{DAC}	13	DAC output: DAC output level, requires an external decoupling capacitor >1 μF.
V_{SS0}	14	Ground: ground connection 0 for video outputs.
V_{DD}	15	Power Supply: +5 V (typ.).
V_{SS2}	16	Ground: ground connection 2.
LL3D/LL1.5D	17	Line-Locked system clock: 13.5 MHz or 27 MHz system clock input for the display, memory interface and control sections.
A0/A9 to A8/A17	18 to 26	Address: multiplexed address outputs for the external nibble-wide dynamic RAM (DRAM). With a 256 kbit (64K × 4) DRAM the address pin A8 is not used.
$\overline{RAS}$	27	Row Address Strobe: active LOW output for the external DRAM.
$\overline{CAS}$	28	Column Address Strobe: active LOW output for the external DRAM.
R/$\overline{W}$	29	Read/Write: active LOW write enable signal for the external DRAM.
D3/D7 to D0/D4	30 to 33	Data: data inputs/outputs from the external nibble-wide DRAM.
V_{SS1}	34	Ground: ground connection 1.
V_{SS3}	35	Ground: ground connection 3.

SYMBOL	PIN	DESCRIPTION
$\overline{INT}$	36	Interrupt: open-drain active LOW output which provides an interrupt signal for a microcontroller indicating the arrival of a page or packet in any one of the acquisition channels, change in newsflash/subtitle status or power-on reset.
SAND	37	Sandcastle: 3-level output for the SAA5191 representing the PL/$\overline{CBB}$ signal, derived from the acquisition timing chain.
TTC	38	Teletext Clock: input from the SAA5191 supplied via an external coupling capacitor.
TTD	39	Teletext Data: input from the SAA5191 supplied via an external coupling capacitor, internally clamped to V_{SS} for 4 to 8 µs of each line to maintain the correct DC level.
FRAME	40	Frame: output for de-interlacing circuits. The signal is LOW for even fields and HIGH for odd fields when text but no picture is displayed. It is forced LOW when a TV picture is present.

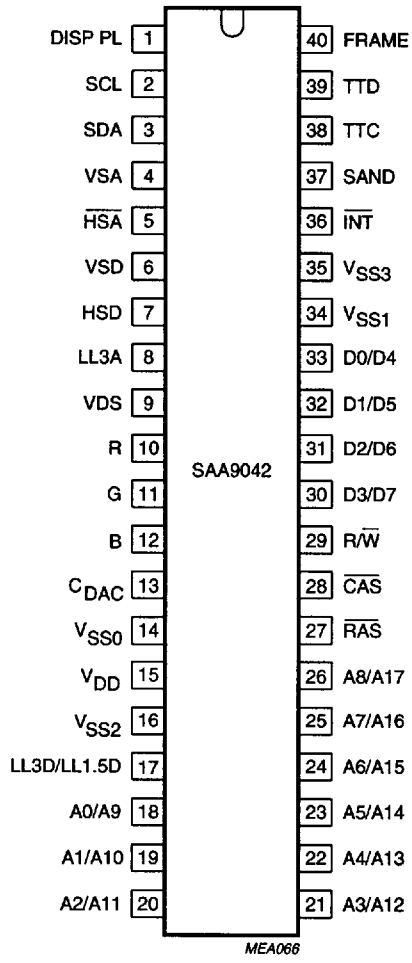


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). All voltages are with respect to VSS1/2/3. VSS0 is considered as an output.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	DC supply voltage		−0.5	+6.5	V
I_{DD}	DC supply current		tbf	tbf	mA
V_I	DC input voltage		−0.5	V_{DD} + 0.5	V
I_I	DC input current		−20	+20	mA
V_O	DC output voltage		−0.5	V_{DD} + 0.5	V
I_O	DC output current		−20	+20	mA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−20	+70	°C
V_{es}	electrostatic handling	note 1	−1000	+1000	V

Note

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; $V_{SS1/2/3}$ = 0 V; T_{amb} = −20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	DC supply voltage	note 1	4.5	5.0	5.5	V
I_{DD}	DC supply current		–	100	–	mA
Inputs; note 2						
TTD; NOTE 3						
$V_{I(p-p)}$	input voltage (peak-to-peak value)		2.0	–	5.0	V
C_{ext}	external coupling capacitor		–	22	50	nF
t_r, t_f	input rise and fall times	notes 4 and 26	10	–	80	ns
$t_{SU;DAT}$	input data set-up time	note 5	40	–	–	ns
$t_{HD;DAT}$	input data hold up time	note 5	40	–	–	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance	note 26	–	7	–	pF
t_{CLon}	clamp start time	note 6	3.5	4.0	4.5	µs
t_{CLoff}	clamp finish time	note 6	7.5	8.0	8.5	µs
I_{CL}	clamp output current	note 7	1.0	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TTC; NOTE 8						
$V_{I(p-p)}$	input voltage (peak-to-peak value)		2.0	–	5.0	V
C_{ext}	external coupling capacitor		–	10	10	nF
I_{IM}	peak input current		−10	–	+10	mA
V_{IM}	input voltage (peak value) relative to 50% duty factor		±0.2	–	±3.5	V
t_r, t_f	input rise and fall times	notes 4 and 26	10	–	80	ns
C_I	input capacitance	note 26	–	7	–	pF
V_{CL}	input clamp voltage		1.2	1.4	1.6	V
f_{clk}	clock frequency	625 line	–	6.9375	–	MHz
		525 line	–	5.7272	–	MHz
$\overline{HSA}$; NOTE 9						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
t_r, t_f	input rise and fall times	notes 4 and 26	–	–	500	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance	note 26	–	–	7	pF
VSA						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage	note 27	2.0	–	V_{DD}	V
t_r, t_f	input rise and fall times	notes 4 and 26	–	–	500	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance	note 26	–	–	7	pF
LL3A; TTL MODE; FIG.4						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
t_{CA}	LL3A cycle time	note 10	69	74	80	ns
t_{CAH}	LL3A HIGH time		28	–	–	ns
t_{CAL}	LL3A LOW time		28	–	–	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−100	–	+100	µA
C_I	input capacitance	note 26	–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LL3A; AC MODE; F = 13.5 MHz; SEE FIG.4						
V_{ACM}	mean voltage level	notes 25 and 26	−12	−	+12	V
$V_{AC(p-p)}$	AC voltage (peak-to-peak value)		1.0	−	3.0	V
V_{ACH}	voltage HIGH w.r.t. mean		0.3	−	2.0	V
V_{ACL}	voltage LOW w.r.t. mean		−2.0	−	−0.3	V
msr	input mark/space ratio w.r.t. mean t_{ACH}/t_{ACL} or t_{ACL}/t_{ACH}	note 28	30 : 70	−	70 : 30	
C_s	series capacitance		47	100	220	pF
Z_i	input impedance	notes 24 and 26	10	−	−	kΩ
SCL; NOTE 31						
V_{IL}	LOW level input voltage		0	−	1.5	V
V_{IH}	HIGH level input voltage		3.0	−	V_{DD}	V
t_r	input rise time	notes 4 and 26	−	−	1	µs
t_f	input fall time	notes 11 and 26	−	−	300	ns
I_{LI}	input leakage current	note 12; V_I = 0 to V_{DD}	−10	−	+10	µA
C_I	input capacitance	note 26	−	−	7	pF
HSD						
V_{IL}	LOW level input voltage		0	−	0.8	V
V_{IH}	HIGH level input voltage		2.0	−	V_{DD}	V
t_r, t_f	input rise and fall times	notes 4 and 26	−	50	500	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	−	+10	µA
C_I	input capacitance	note 26	−	−	7	pF
VSD						
V_{IL}	LOW level input voltage		0	−	0.8	V
V_{IH}	HIGH level input voltage		2.0	−	V_{DD}	V
t_r, t_f	input rise and fall times	notes 4 and 26	−	−	500	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	−	+10	µA
C_I	input capacitance	note 26	−	−	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LL3D/LL1.5D; TTL MODE						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
t_r, t_f	input rise and fall times	notes 4 and 26	–	–	10	ns
t_{CA}	LL3D/LL1.5D cycle time	13.5 MHz	69	74	80	ns
		27.0 MHz	35	37	40	ns
t_{CAH}	LL3D/LL1.5D HIGH time	13.5 MHz	28	–	–	ns
		27.0 MHz	14	–	–	ns
t_{CAL}	LL3D/LL1.5D LOW time	13.5 MHz	28	–	–	ns
		27.0 MHz	14	–	–	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−100	–	+100	µA
C_I	input capacitance	note 26	–	–	10	pF
LL3D/LL1.5D; AC MODE; f = 13.5 MHz OR 27 MHz; SEE FIG.4						
V_{ACM}	mean voltage level	notes 25 and 26	−12	–	+12	V
$V_{AC(p-p)}$	AC voltage		1.0	–	3.0	V
V_{ACH}	voltage HIGH w.r.t. mean		0.3	–	2.0	V
V_{ACL}	voltage LOW w.r.t. mean		−2.0	–	−0.3	V
msr	input mark/space ratio w.r.t. mean t_{ACH}/t_{ACL} or t_{ACL}/t_{ACH}	note 28	30 : 70	–	70 : 30	
C_s	series capacitance		47	100	220	pF
Z_i	input impedance	notes 24 and 26	10	–	–	kΩ
Inputs/outputs; note 13						
SDA; OPEN-DRAIN I/O; NOTE 31						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}	V
t_r	input rise time	notes 4 and 26	–	–	1	µs
t_f	input fall time	notes 11 and 26	–	–	300	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}; note 12; with output off	−10	–	+10	µA
C_I	input capacitance	note 26	–	–	7	pF
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.4	V
t_f	output fall time	notes 11 and 26	–	–	300	ns
C_L	load capacitance		–	–	400	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
D0/D4 TO D3/D7						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
I_{LI}	input leakage current	note 12; V_I = 0 to V_{DD}; with output off	−10	–	+10	μA
C_I	input capacitance	note 26	–	–	7	pF
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −200 μA	2.4	–	V_{DD}	V
t_r, t_f	output rise and fall times between 0.6 V and 1.8 V	note 26	–	–	10	ns
C_L	load capacitance	note 21	–	–	100	pF
Outputs; note 13						
SAND; NOTE 22						
V_{OL}	LOW level output voltage	I_{OL} = 0.2 mA	0	–	0.3	V
V_{OI}	intermediate level output voltage	I_{OI} = ±30 μA	1.3	–	2.7	V
V_{OH}	HIGH level output voltage	I_{OH} = 0 to −10 μA	4.0	–	V_{DD}	V
t_r	output rise time V_{OL} to V_{OI} between 0.4 V and 1.1 V	note 26	–	–	400	ns
t_r	output rise time V_{OL} to V_{OH} between 2.9 V and 4.0 V	note 26	–	–	200	ns
t_f	output fall time V_{OH} to V_{OL} between 4.0 V and 0.4 V	note 26	–	–	50	ns
C_L	load capacitance		–	–	30	pF
$\overline{INT}$; OPEN-DRAIN OUTPUT						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
I_{LO}	output leakage current	V_{PU} = 0 V to V_{DD}; with output off	−10	–	+10	μA
t_f	output fall time	notes 15 and 26	–	–	50	ns
C_L	load capacitance		–	–	100	pF
A0/A9 TO A8/A17						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −200 μA	2.4	–	V_{DD}	V
t_r, t_f	output rise and fall times between 0.6 V and 1.8 V	note 26	–	–	10	ns
C_L	load capacitance	note 23	–	–	100	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\overline{RAS}$, $\overline{CAS}$ AND R/$\overline{W}$						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –200 µA	2.4	–	V_{DD}	V
t_r, t_f	output rise and fall times between 0.6 V and 1.8 V	note 26	–	–	10	ns
C_L	load capacitance	note 23	–	–	100	pF
DISP PL AND FRAME						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –200 µA	2.4	–	V_{DD}	V
t_r, t_f	output rise and fall times	notes 16 and 26	–	–	200	ns
C_L	load capacitance		–	–	200	pF
R, G, B; 3-STATE; NOTE 29						
V_{OL}	LOW level output voltage	I_{OL} = 2.0 mA; note 17	V_{SS0}	–	V_{SS0} + 0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –2 mA; note 18	–	note 30	–	V
t_r, t_f	output rise and fall times between 0.6 V and 1.8 V	notes 4, 17 and 26	–	–	10	ns
C_L	load capacitance		–	–	30	pF
C_{off}	output capacitance	off state; note 26	–	–	10	pF
I_{off}	output leakage current	off state; V_I = 0 to V_{DD}	–10	–	+10	µA
VDS; 3-STATE; NOTE 29						
V_{OL}	LOW level output voltage	I_{OL} = 1.0 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –200 µA	1.1	–	2.8	V
t_r, t_f	output rise and fall times	note 26	–	–	10	ns
C_L	load capacitance		–	–	30	pF
I_{off}	output leakage current	off state; V_I = 0 to V_{DD}	–10	–	+10	µA
t_{skew}	skew delay between R, G, B and VDS outputs	note 19	–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
I²C-BUS; NOTE 20; FIG.3						
f_{SCL}	SCL clock frequency	note 31	0	–	100	kHz
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs
MEMORY INTERFACE; NOTE 14; FIGS 5 AND 6						
t_{CY}	cycle time		–	481	–	ns
t_T	transition time		–	–	10	ns
$t_{W;RAS}$	$\overline{RAS}$ pulse width		120	–	–	ns
$t_{PC;RAS}$	$\overline{RAS}$ precharge time		90	–	–	ns
$t_{HD;CAS}$	$\overline{CAS}$ hold time		120	–	–	ns
$t_{CY;PM}$	page mode cycle time		120	–	–	ns
t_d	$\overline{RAS}$ to $\overline{CAS}$ delay time		25	–	–	ns
$t_{W;CAS}$	$\overline{CAS}$ pulse width		60	–	–	ns
$t_{PC;CAS}$	$\overline{CAS}$ precharge time		50	–	–	ns
$t_{SU;ROW}$	row address set-up time		0	–	–	ns
$t_{HD;ROW}$	row address hold time		15	–	–	ns
$t_{SU;COL}$	column address set-up time		0	–	–	ns
$t_{HD;COL}$	column address hold time		20	–	–	ns
$t_{SU;RD}$	read command set-up time		0	–	–	ns
$t_{HD;RDC}$	read command hold time referenced to $\overline{CAS}$		0	–	–	ns
$t_{HD;RDR}$	read command hold time referenced to $\overline{RAS}$		10	–	–	ns
$t_{ACC;CAS}$	access time from $\overline{CAS}$		–	–	60	ns
$t_{W;WR}$	write command pulse width		50	–	–	ns
$t_{HD;WR}$	write command hold time		40	–	–	ns
$t_{SU;DATI}$	data input set-up time		0	–	–	ns
$t_{HD;DATI}$	data input hold time		40	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{ACC;RAS}$	access time from $\overline{RAS}$		–	–	120	ns
$t_{HD;RC}$	$\overline{RAS}$ hold time after $\overline{CAS}$		60	–	–	ns
$t_{PC;CR}$	$\overline{CAS}$ to $\overline{RAS}$ precharge time		20	–	–	ns
$t_{HD;COLR}$	column address hold time referenced to $\overline{RAS}$		80	–	–	ns
$t_{HD;DATIR}$	data input hold time referenced to $\overline{RAS}$		100	–	–	ns

Notes

1. The rise time of V_{DD} from 0 to 4.5 V must be >150 ns to ensure that the internal power-on reset triggers. For this circuit to reset the chip, V_{DD} must be initially <1.0 V or fall to <1.0 V for at least 100 ns. Spikes on V_{DD} are tolerable provided that V_{DD} is not reduced to <2.5 V.
2. All inputs are protected against static charge under normal handling.
3. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor.
4. Rise and fall times are measured between 10% and 90% levels.
5. Teletext input data set-up and hold times are measured with respect to 50% duty factor level of the rising edge of the teletext clock input (TTC). Data stable 1 ≥ 2.0 V, data stable 0 ≤ 0.8 V.
6. Clamp times measured from the line sync reference point, assuming acquisition timing is set correctly.
7. Clamping transistor on, $V_{TTD} - V_{SS1} \leq 0.1$ V.
8. The TTC input has an internal clamping diode.
9. $\overline{HSA}$ is falling edge triggered.
10. Minimum and maximum cycle times are ±7.1% of the typical value.
11. Fall time is measured between 3.0 V and 1.5 V.
12. Applies even when $V_{DD} = 0$ V.
13. All input/outputs and outputs are protected against static charge under normal handling.
14. For details of memory interface timings to and from external DRAM see Figs 5 and 6.
15. Output fall time measured between 4.0 V and 1.0 V levels with a 3.3 kΩ load to 5.0 V.
16. Output rise and fall times measured between 0.8 V and 2.0 V levels.
17. Measured with $I_{OL} = 2.0$ mA, $V_{SS0} = V_{SS1/2/3}$ and output voltage (C_{DAC}) = 1.5 V.
18. Measured with $I_{OH} = -2$ mA, $V_{SS0} = V_{SS1/2/3}$ and output voltage (C_{DAC}) = 0.5 to 1.5 V.
19. Skew delay time measured at 0.7 V levels.
20. For details of I^2C-bus timings see Fig.3; timings are referenced to $V_{IH} = 3.0$ V and $V_{IL} = 1.5$ V.
21. Load capacitance measured with two DRAM data inputs; 50 pF maximum.
22. A current of 1 μA flows out of the SAA5191 while its SAND input is in the range of 1 V to 3.5 V.
23. Load capacitance measured with eight DRAM data inputs; 80 pF maximum.
24. Through a 200 pF capacitor with a 13.5 MHz sinewave.
25. To be applied via a series capacitor only.
26. This specification point is included because of its importance to the application environment; it is not however guaranteed.
27. When connected to the SAA5191, it is acceptable for the clock frequency to initially attain ≤15 MHz in order to achieve synchronization.

28. When connected to the SAA5191, it is acceptable for the input voltage to attain V_{DD} + 0.9 V. The input current must be restricted as specified in the limiting values.
29. These outputs can be made 3-state via the I²C-bus.
30. Typical values adjustable over 0.5 to 1.5 V via the I²C-bus.
31. A standard (100 kHz) I²C interface is implemented. Fast mode (400 kHz) is not supported.

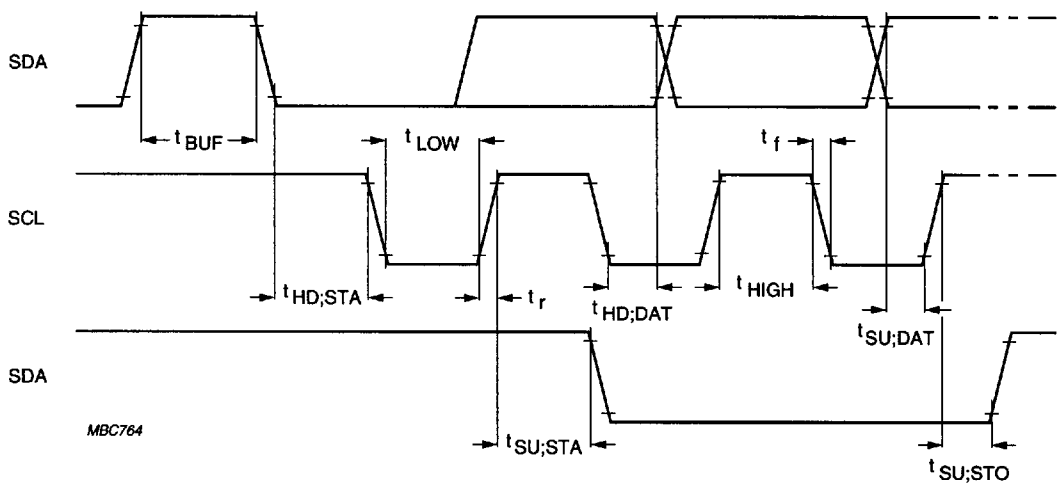


Fig.3 I²C-bus timing.

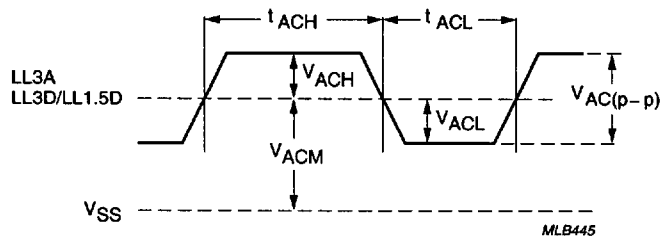


Fig.4 Line-locked system clock LL3A and LL3D/LL1.5D timing diagram.

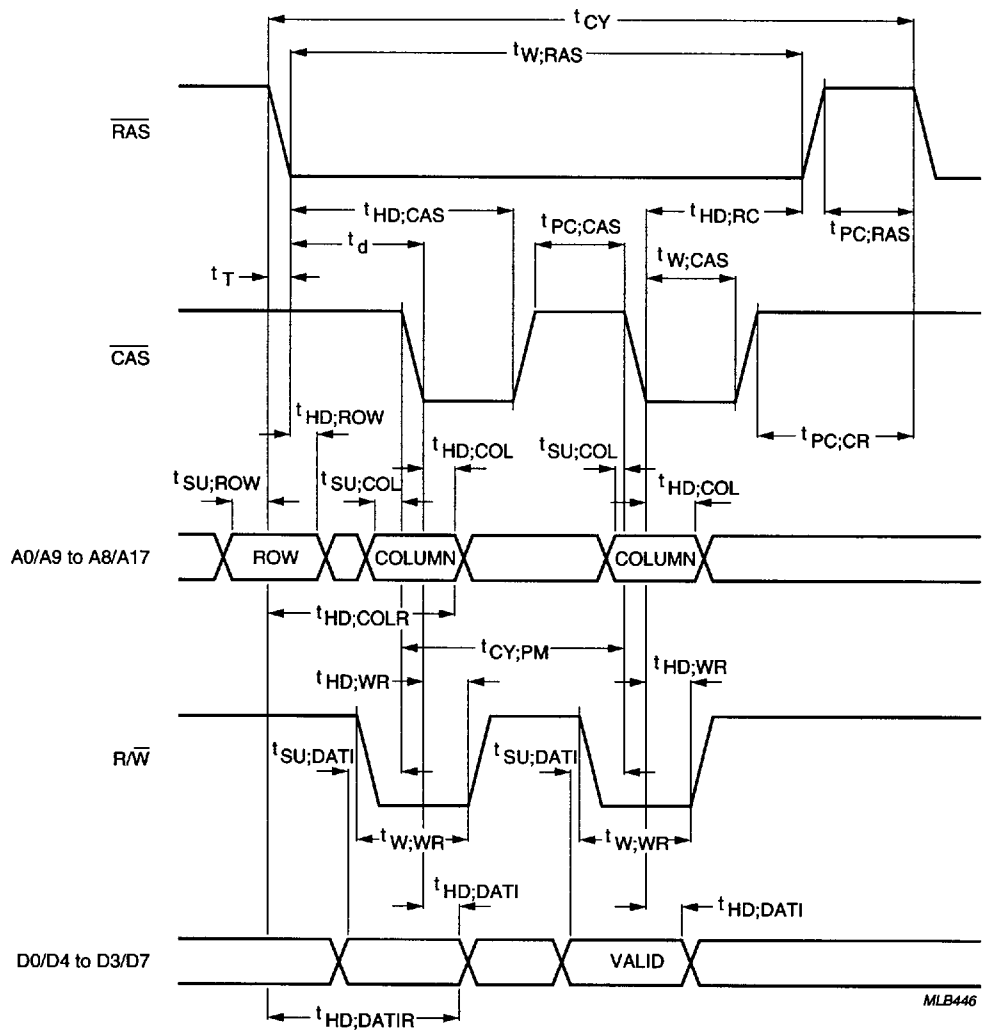


Fig.5 Memory interface timing for write cycle to external DRAM.

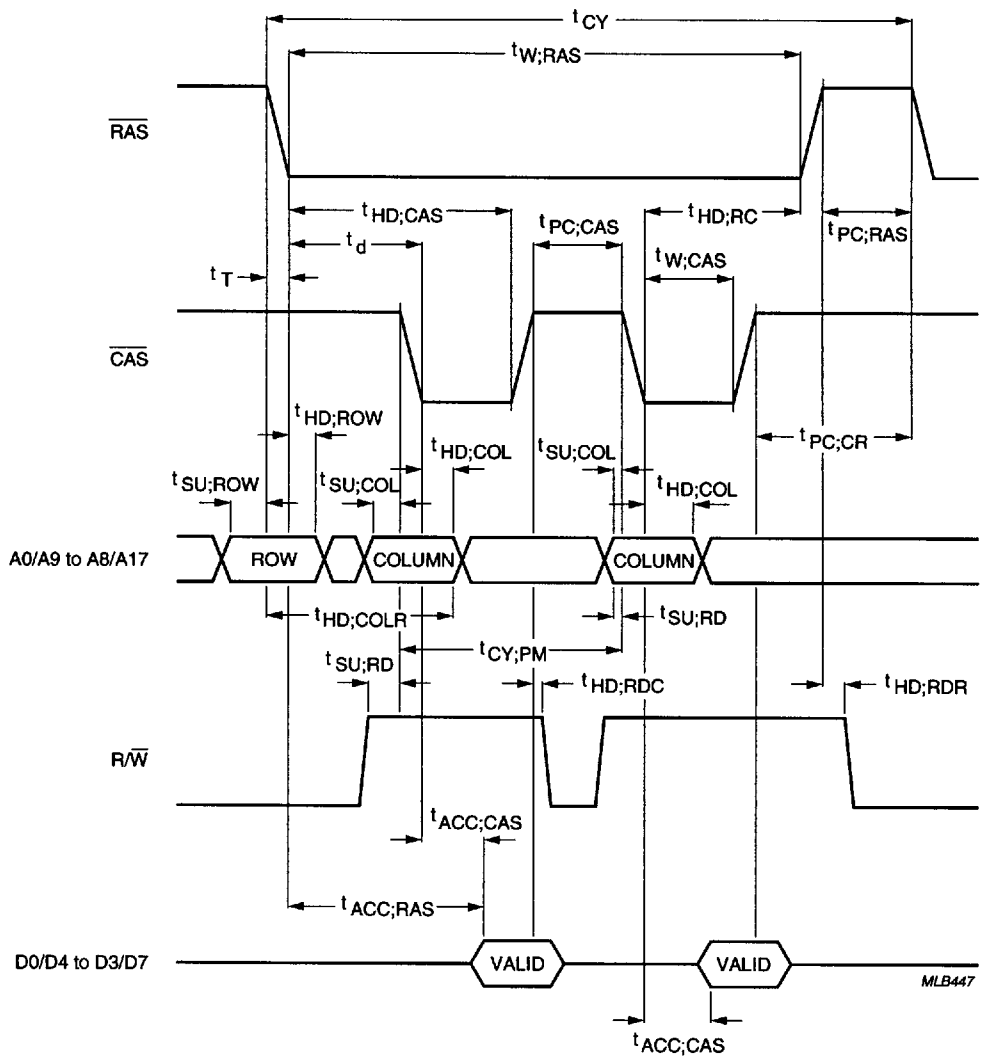
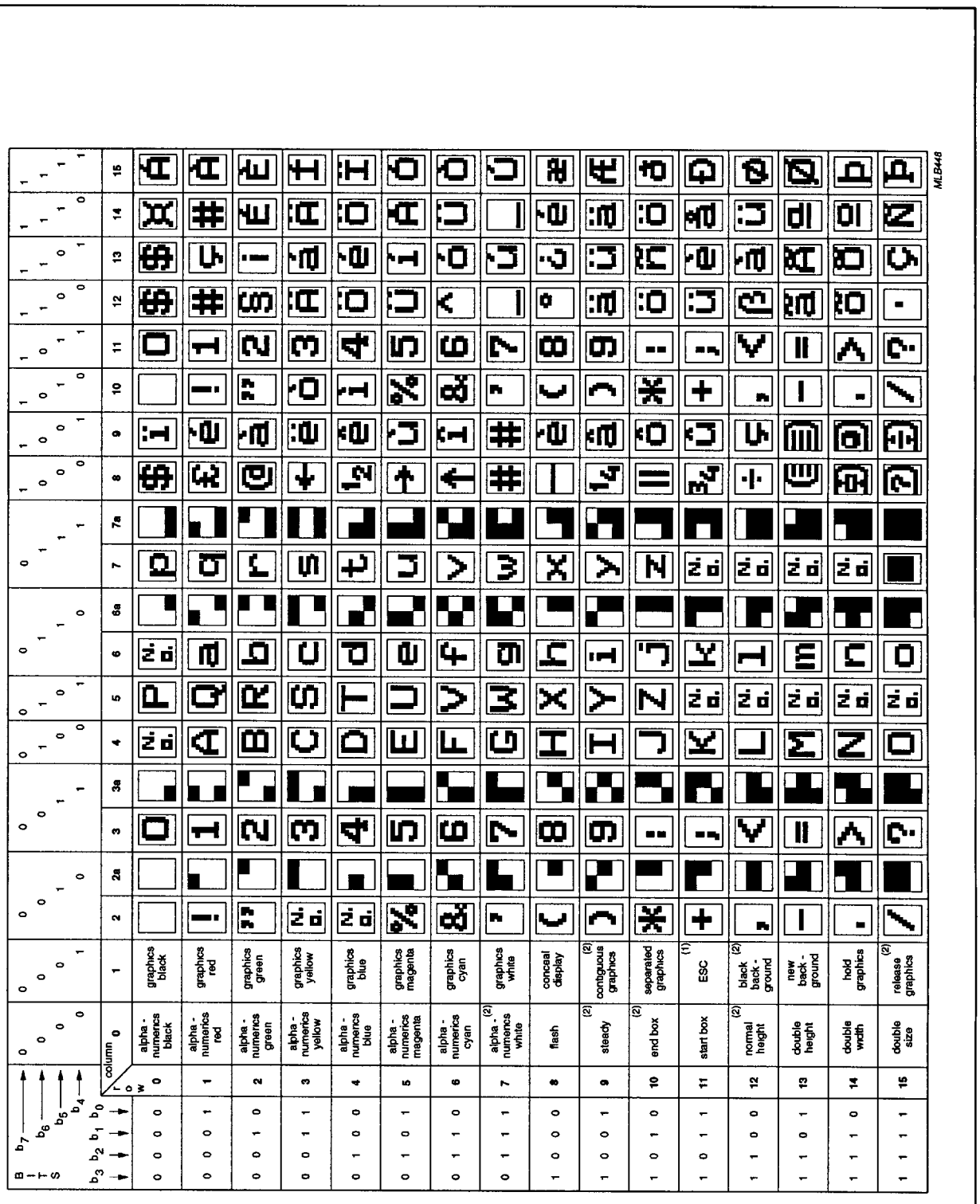


Fig.6 Memory interface timing for read cycle from external DRAM.

CHARACTER SETTINGS

The different character settings are explained in Tables 1 to 6.

Table 1 SAA9042A West European character set; for N.O. (national option character position) see Table 2.



Notes to Table 1

1. These control characters are reserved for compatibility with other data codes.
2. These control characters are presumed before each rows begins.

Table 2 SAA9042A West European national option sets.

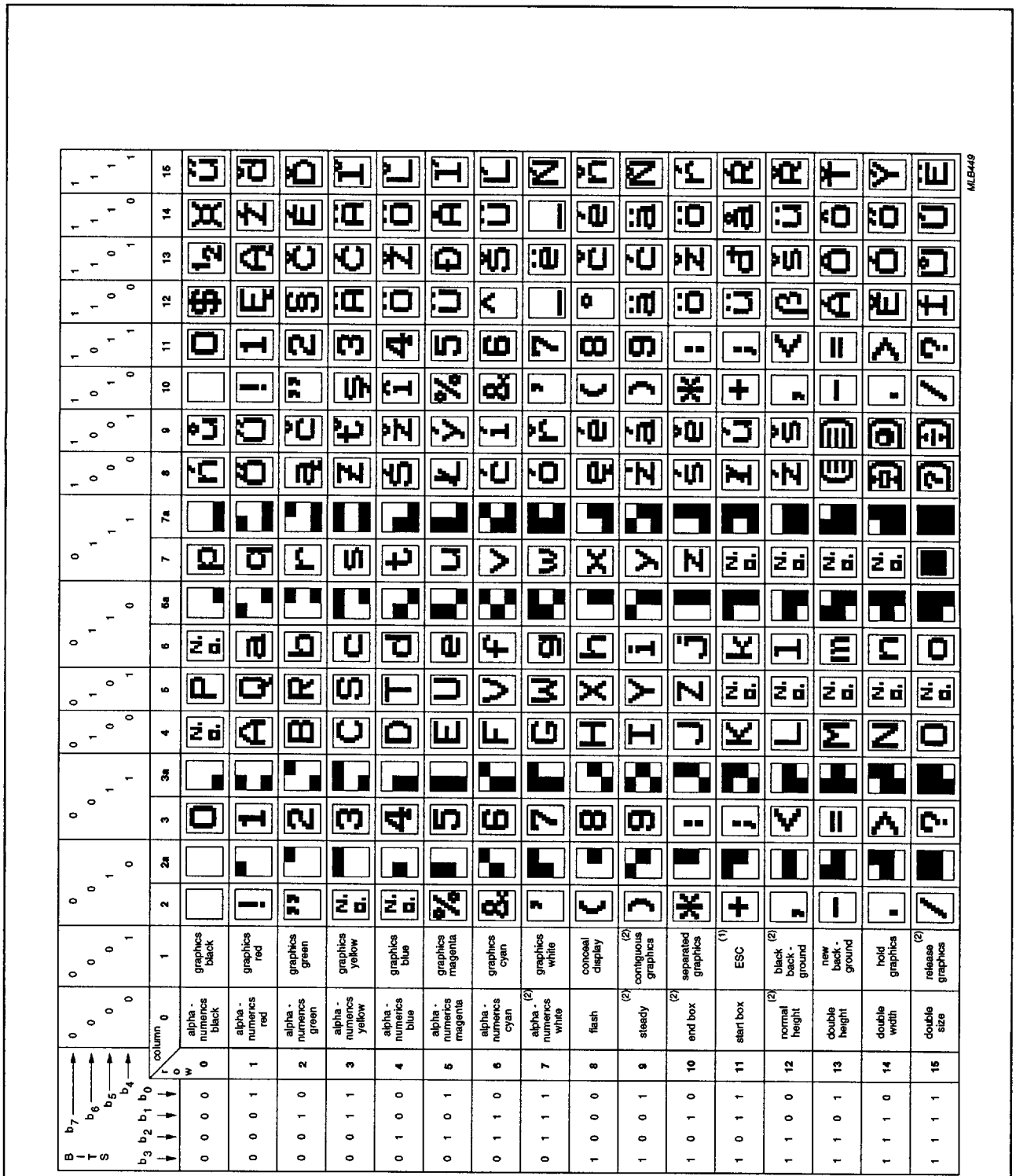
LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN (2)	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MEA559

Notes

1. Where PHCB are the Page Header Control Bits. Other combinations of PHCB default to English.
2. Basic character set is Italian. Selected when the force language bit (D5) in the display set-up register (R12) is set to logic 1.

Table 3 SAA9042B Eastern European character set; for N.O. (national option character position) see Table 4.



Notes to Table 3

1. These control characters are reserved for compatibility with other data codes.
2. These control characters are presumed before each rows begins.

Table 4 SAA9042B Eastern European national option sets.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
POLISH	0	0	0	#	ń	ą	Ż	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAK	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
ROMANIAN (2)	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

MLB450

Notes

1. Other combinations of C12, C13 and C14 default to German.
2. Basic character set is Romanian. Selected when the force language bit (D5) in the display set-up register (R12) is set to logic 1.

Table 5 SAA9042C Euro-Turkish character set; for N.O. (national option character position) see Table 6.

Notes to Table 5

1. These control characters are reserved for compatibility with other data codes.
2. These control characters are presumed before each rows begins.

Table 6 SAA9042C Euro-Turkish national option sets.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
ITALIAN (2)	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à
TURKISH	1	1	0	Ł	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü

MLB452

Notes

1. Other combinations of C12, C13 and C14 default to English.
2. Basic character set is Italian. Selected when the force language bit (D5) in the display set-up register (R12) is set to logic 1.

APPLICATION INFORMATION

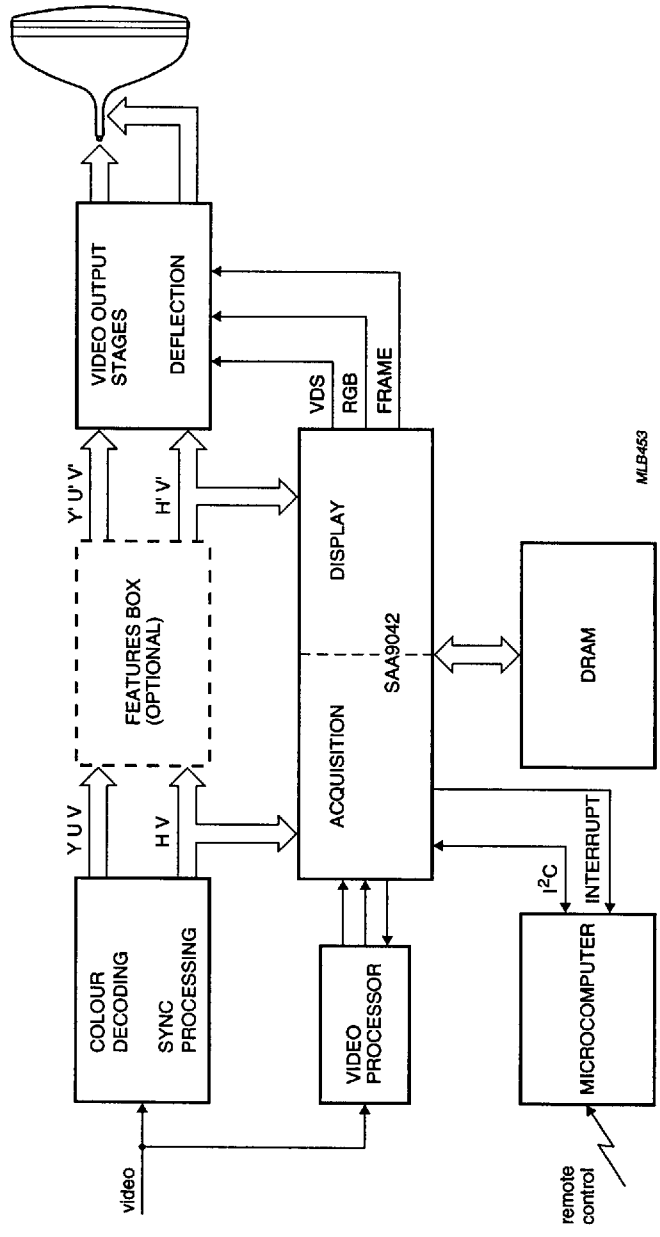
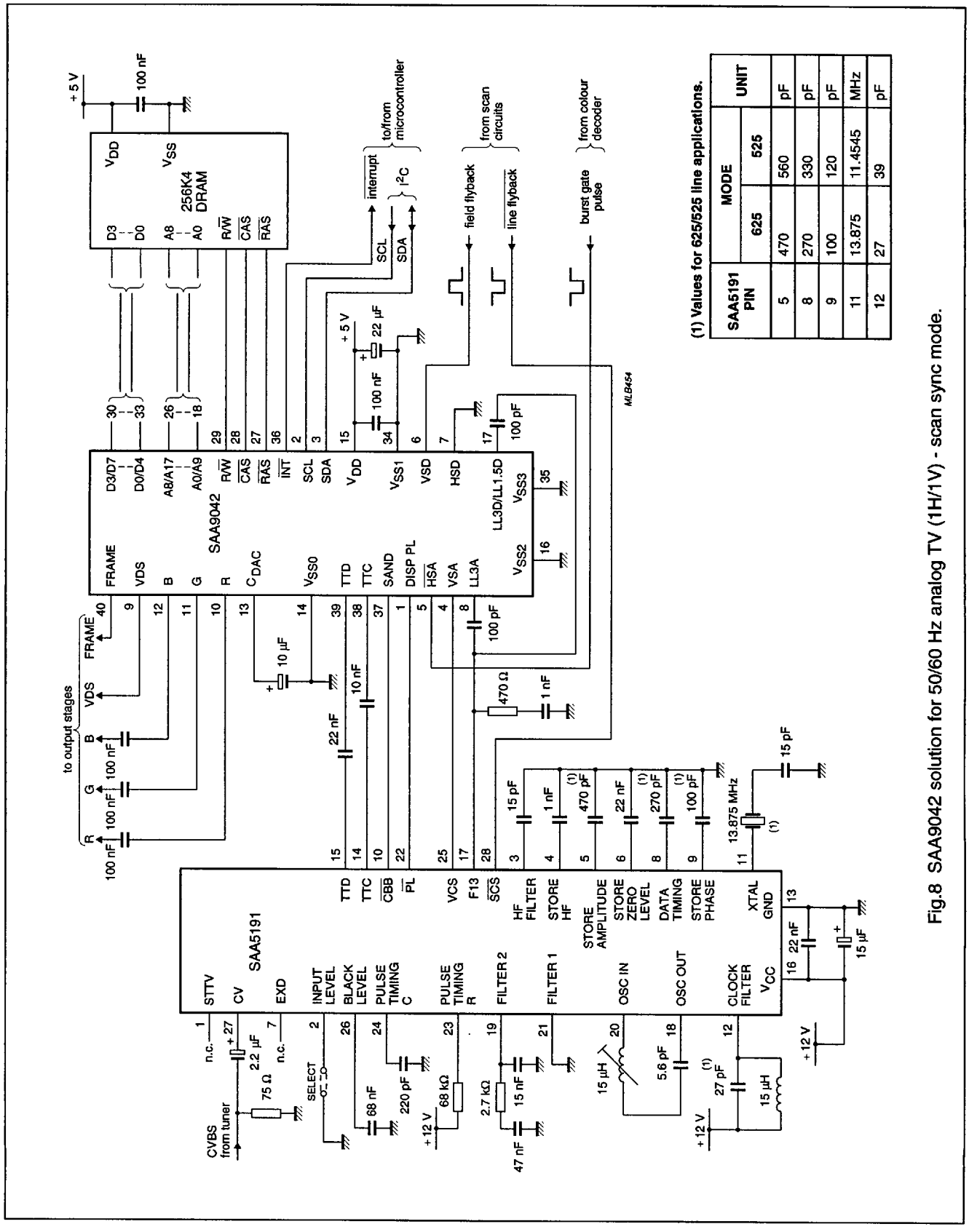


Fig.7 Basic system configuration.



(1) Values for 625/525 line applications.

SAA5191 PIN	MODE		UNIT
	625	525	
5	470	560	pF
8	270	330	pF
9	100	120	pF
11	13.875	11.4545	MHz
12	27	39	pF

Fig.8 SAA9042 solution for 50/60 Hz analog TV (1H/1V) - scan sync mode.

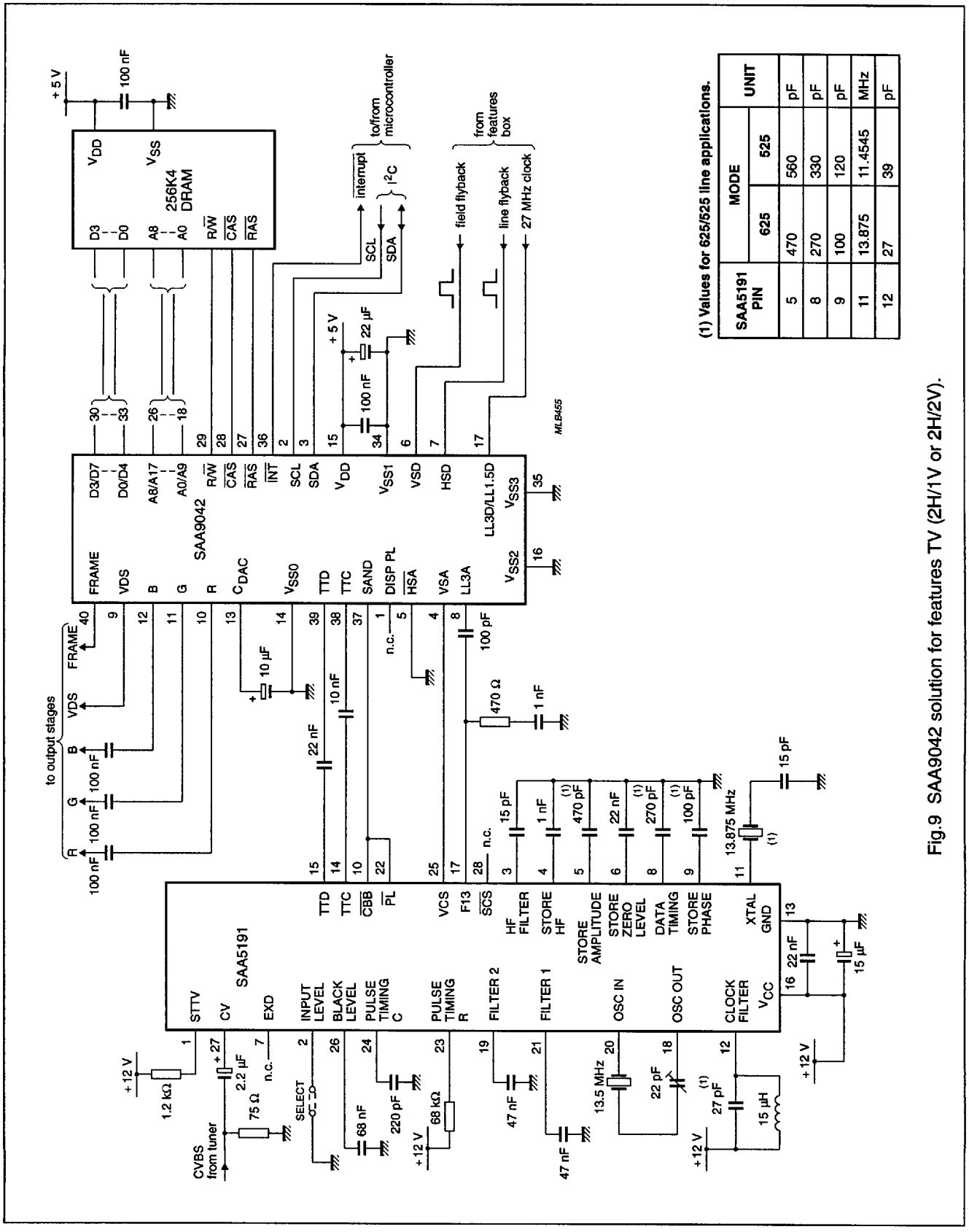
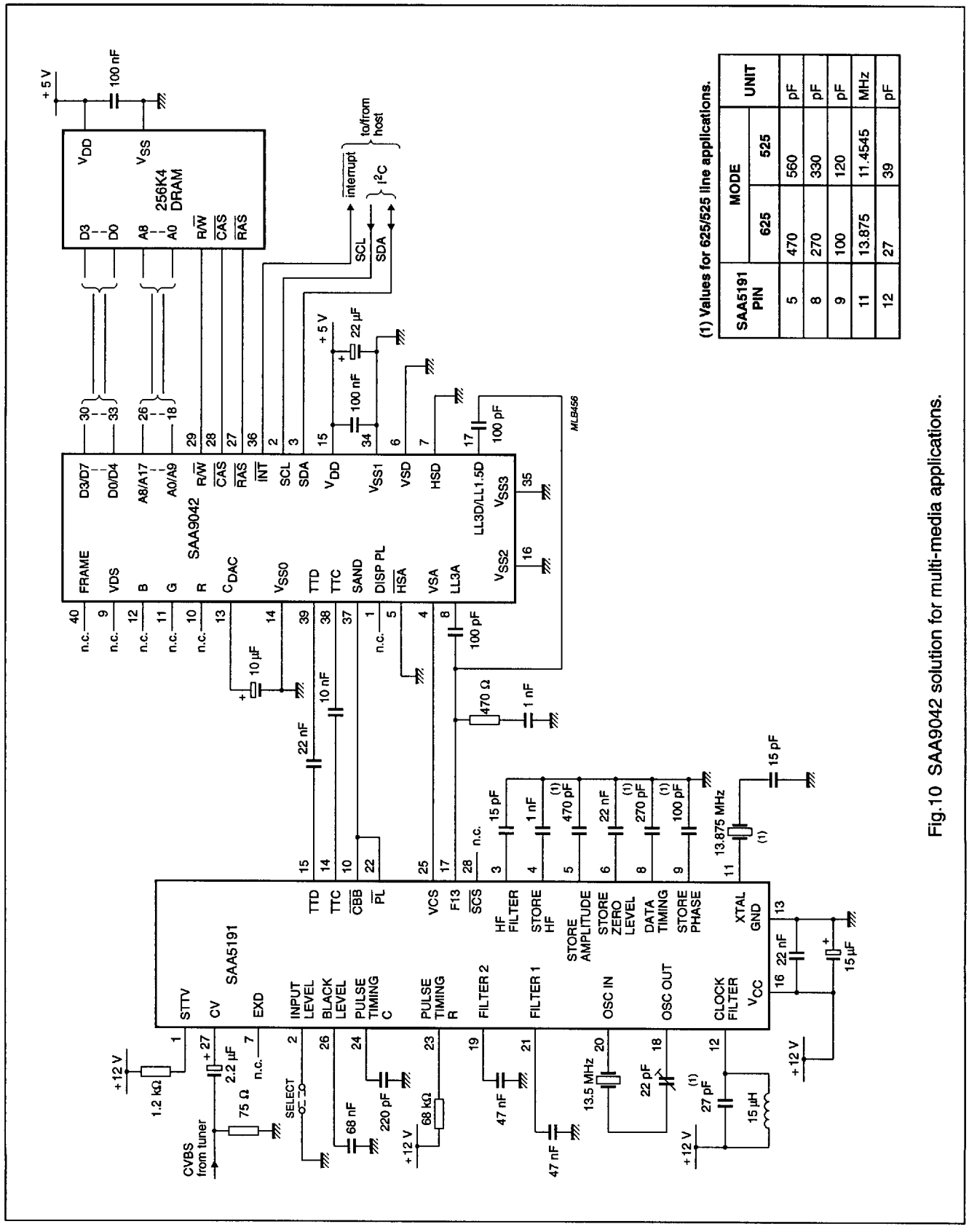


Fig.9 SAA9042 solution for features TV (2H/1V or 2H/2V).



(1) Values for 625/525 line applications.

SAA5191 PIN	MODE 625	MODE 525	UNIT
5	470	560	pF
8	270	330	pF
9	100	120	pF
11	13.875	11.4545	MHz
12	27	39	pF

Fig.10 SAA9042 solution for multi-media applications.

PACKAGE OUTLINE

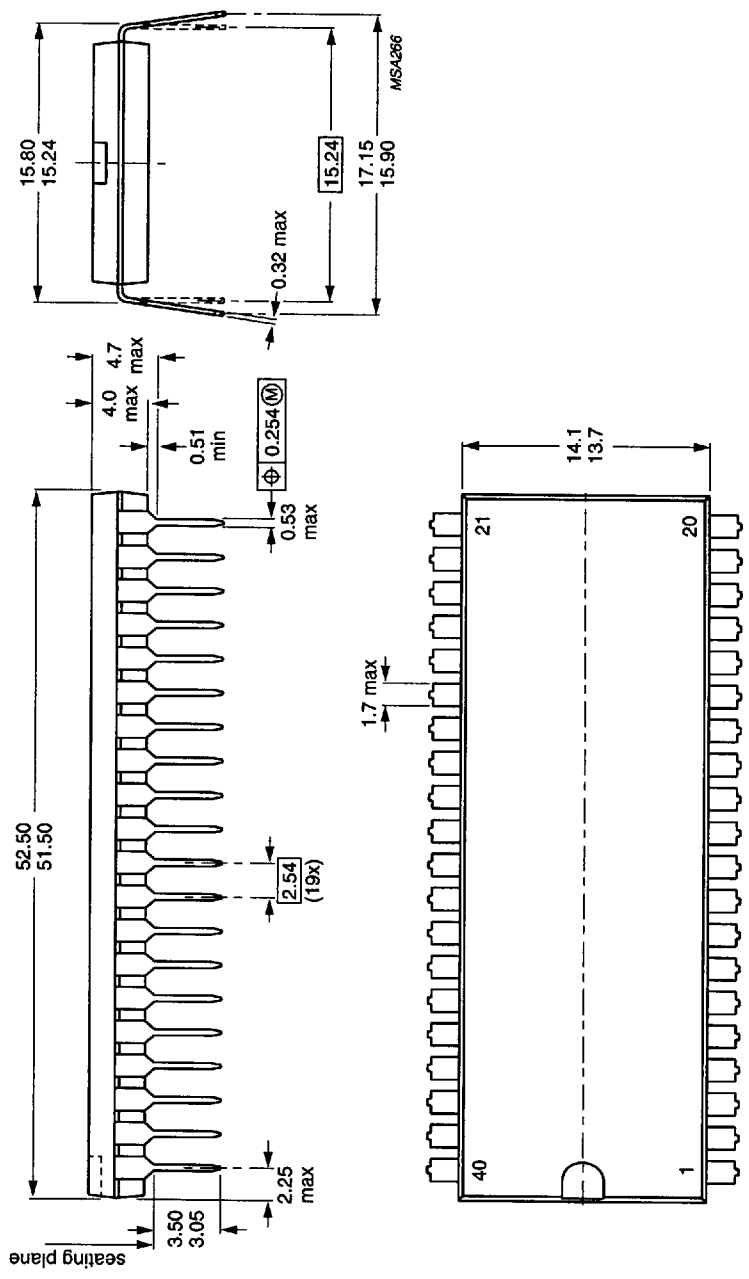


Fig.11 40-lead dual in-line; plastic (SOT129).

Dimensions in mm.

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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