1Mx8 CMOS SRAM MONOLITHIC

FEATURES

- 1 Meg x 8 bit CMOS Static
- Random Access Memory
  - Access Times 55 thru 100ns
  - Data Retention Function (EDI8F81027LP)
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- High Density Packaging
  - 32 Pin DIP, No.
- Single +5V (±10%) Supply Operation

DESCRIPTION

The EDI8F81027C is an 8 megabit CMOS Static RAM based on two 512Kx8 Static RAMs mounted on a multi-layered epoxy laminate (FR4) substrate.

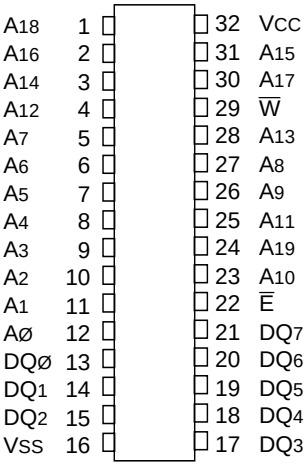
A low power version with data retention (EDI8F81027LP) is also available.

All inputs and outputs are TTL compatible and operate from a single 5V supply.

Fully asynchronous, the EDI8F81027C requires no clocks or refreshing for operation.

FIG. 1 PIN CONFIGURATION

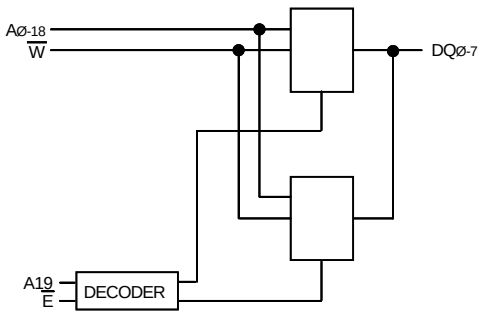
TOP VIEW



PIN DESCRIPTION

AØ-19	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
DQØ-7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	1 Watt
Output Current.	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	I_{CC2}, I_{CC3}
H	L	H	Output Deselect	High Z	I_{CC1}
L	L	H	Read	D_{OUT}	I_{CC1}
X	L	L	Write	D_{IN}	I_{CC1}

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	--	6.0	V
Input Low Voltage	V_{IL}	-0.3	--	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL =100pF

(Note: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF)

CAPACITANCE

(f = 1.0MHz, V_{IN} = V_{CC} or V_{SS})

Parameter	Symbol	Max	Unit
Address Lines	C_I	30	pF
Data Lines	$C_{D/Q}$	43	pF
Chip Enable Line	C_C	10	pF
Write and Output Enable Lines	C_W	32	pF

These parameters are sampled, not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	I_{CC1}	$\overline{W}$, $\overline{E}$ = V_{IL}, $I_{I/O}$ = 0mA, Min Cycle		--	85	175	mA
Standby (TTL) Power Supply Current	I_{CC2}	$\overline{E} \geq V_{IH}$, $V_{IN} \leq V_{IL}$ $V_{IN} \geq V_{IH}$		--	25	55	mA
Full Standby Power Supply Current (CMOS)	I_{CC3}	$\overline{E} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$	C	--	1.5	2	mA
			LP	--	190	300	µA
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}		-10	--	10	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = 0V to V_{CC}		-10	--	10	µA
Output High Voltage	V_{OH}	I_{OH} =-1.0mA		2.4	--	--	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		--	--	0.4	V

*Typical: T_A = 25°C, V_{CC} = 5.0V

AC CHARACTERISTICS - READ CYCLE

Parameter	Symbol JEDEC	Symbol Alt.	55ns Min	55ns Max	70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	Units
Read Cycle Time	t_{AVAV}	t_{RC}	55		70		85		100		ns
Address Access Time	t_{AVQV}	t_{AA}		55		70		85		100	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}		55		70		85		100	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	5		5		5		5		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}		25		30		35		40	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	5		5		5		5		ns

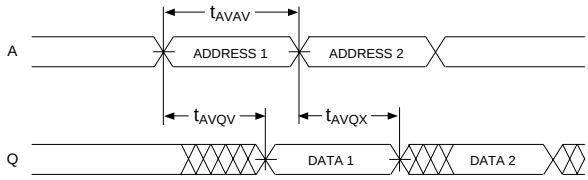
NOTE:
1. Parameter guaranteed, but not tested.

AC CHARACTERISTICS - WRITE CYCLE

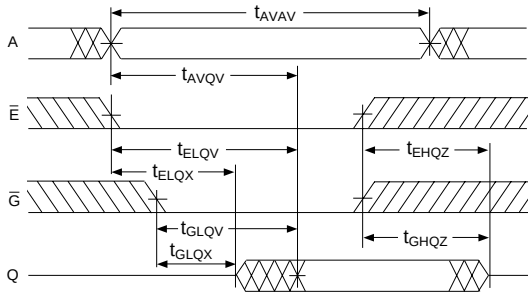
Write Cycle Parameter	Symbol JEDEC	Symbol Alt.	55ns Min	55ns Max	70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	Units
Write Cycle Time	t_{AVAV}	t_{WC}	55		70		85		100		ns
Chip Enable to End of Write	t_{ELWH}	t_{CW}	50		65		70		80		ns
	t_{ELEH}	t_{CW}	50		65		70		80		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		0		ns
	t_{AVEL}	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AVWH}	t_{AW}	50		65		70		80		ns
	t_{AVEH}	t_{AW}	50		65		70		80		ns
Write Pulse Width	t_{WLWH}	t_{WP}	45		65		70		80		ns
	t_{WLEH}	t_{WP}	45		65		70		80		ns
Write Recovery Time	t_{WHAX}	t_{WR}	5		5		5		5		ns
	t_{EHAX}	t_{WR}	5		5		5		5		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		ns
	t_{EHDX}	t_{DH}	0		0		0		0		ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	25	0	30	0	35	0	40	0	ns
Data to Write Time	t_{DVWH}	t_{DW}	25		30		35		40		ns
	t_{DVEH}	t_{DW}	25		30		35		40		ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	5		5		5		5		ns

NOTE:
1. Parameter guaranteed, but not tested.

FIG. 2
READ CYCLES

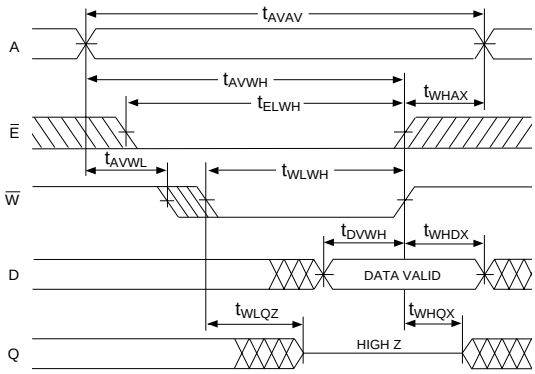


READ CYCLE 1 ($\overline{W}$ HIGH; $\overline{G}$, $\overline{E}$ LOW)



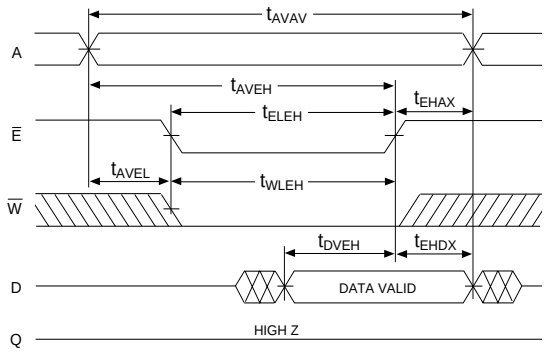
READ CYCLE 2 ($\overline{W}$ HIGH)

FIG. 3
WRITE CYCLE 1



WRITE CYCLE 1, $\overline{W}$ CONTROLLED

FIG. 4
WRITE CYCLE 2



WRITE CYCLE 2, $\overline{E}$ CONTROLLED

DATA RETENTION CHARACTERISTICS (LP VERSION ONLY)

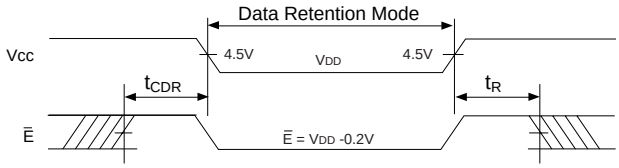
Characteristic	Sym	Test Conditions	V_{DD}	Min	Typ	Max		Unit
						70°C	85°C	
Data Retention Voltage	V_{DD}	$\overline{E} \geq V_{DD}$ -0.2V $V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq 0.2V$		2	--	--	--	V
Data Retention Quiescent Current	I_{CCDR}		2V	--		100	130	µA
			3V	--		160	210	µA
Chip Disable to Data Retention Time	t_{CDR}(1)			0	--	--	--	ns
Operation Recovery Time	t_R (1)			t_{AVAV}*	--	--	--	ns

NOTE:

1. Parameter guaranteed, but not tested

* Read Cycle Time

FIG. 5
DATA RETENTION - $\overline{E}$ CONTROLLED



DATA RETENTION, $\overline{E}$ CONTROLLED

ORDERING INFORMATION

Standard Power	Low Power with Data Retention	Speed (ns)	Package No.
EDI8F81027C55B6C	EDI8F81027LP55B6C	55	352
EDI8F81027C70B6C	EDI8F81027LP70B6C	70	352
EDI8F81027C85B6C	EDI8F81027LP85B6C	85	352
EDI8F81027C100B6C	EDI8F81027LP100B6C	100	352
EDI8F81027C70B6I		70	352
EDI8F81027C85B6I		85	352
EDI8F81027C100B6I		100	352

NOTE: To order an Industrial grade product substitute the letter C in the Suffix with the letter I, eg. EDI8F81027C70B6C becomes EDI8F81027C70B6I.

PACKAGE DESCRIPTION

PACKAGE NO. 352
32 PIN DIP