

# 64-Mbit (8M x 8) Static RAM

## Features

- High speed
  - $t_{AA} = 12 \text{ ns}$
- Low active power
  - $I_{CC} = 300 \text{ mA}$
- Low complementary metal oxide semiconductor (CMOS) standby power
  - $I_{SB2} = 100 \text{ mA}$
- Operating voltages of  $3.3 \pm 0.3 \text{ V}$
- 2.0-V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL)-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$  and  $CE_2$  features
- Available in Pb-free 48-ball fine ball grid array (FBGA) package

## Functional Description

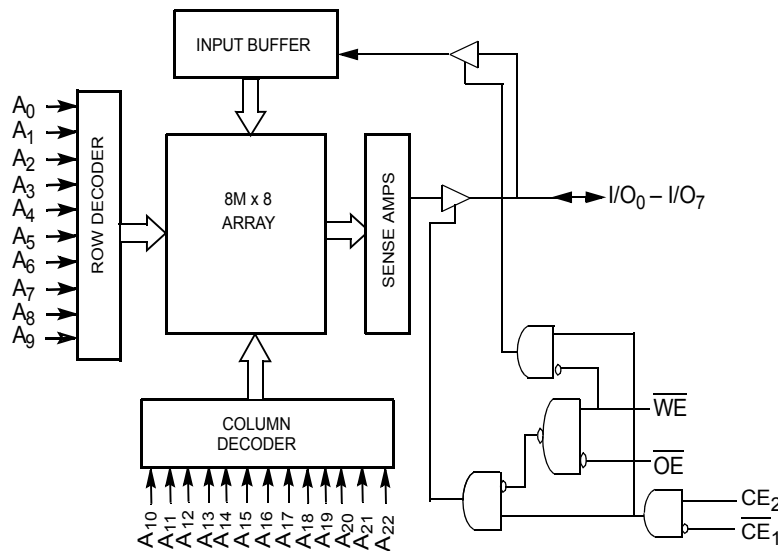
The CY7C1089DV33 is a high-performance CMOS static RAM organized as 8,388,608 words by 8 bits.

To write to the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) input LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{22}$ ).

To read from the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) LOW and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins. See [Truth Table](#) on page 9 for a complete description of Read and Write modes.

The input and output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  LOW or  $CE_2$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH and  $\overline{WE}$  LOW).

## Logic Block Diagram



## Selection Guide

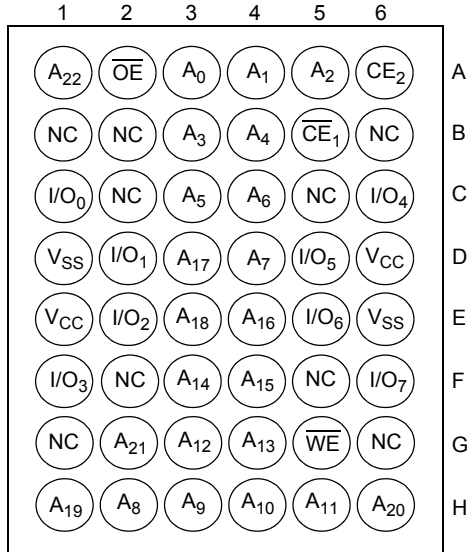
Description	-12	Unit
Maximum access time	12	ns
Maximum operating current	300	mA
Maximum CMOS standby current	100	mA

## Contents

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## Pin Configuration

Figure 1. 48-Ball FBGA (Top View) <sup>[1]</sup>



**Note**

1. NC pins are not connected to the die.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  relative to GND<sup>[2]</sup>..... -0.5 V to +4.6 V

DC voltage applied to outputs in high-Z state<sup>[2]</sup>..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage<sup>[2]</sup>..... -0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage..... >2001 V (MIL-STD-883, Method 3015)

Latch up current ..... >140 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Industrial	-40 °C to +85 °C	3.3V ± 0.3V

## DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-12		Unit
			Min	Max	
$V_{OH}$	Output HIGH voltage	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	-	V
$V_{OL}$	Output LOW voltage	$V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$	-	0.4	V
$V_{IH}$	Input HIGH voltage		2.0	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW voltage <sup>[2]</sup>		-0.3	0.8	V
$I_{IX}$	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-1	+1	μA
$I_{OZ}$	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$ , Output disabled	-1	+1	μA
$I_{CC}$	$V_{CC}$ operating supply current	$V_{CC} = \text{Max}, f = f_{MAX} = 1/t_{RC}, I_{OUT} = 0 \text{ mA CMOS levels}$	-	300	mA
$I_{SB1}$	Automatic CE power-down current — TTL inputs	Max $V_{CC}$ , $\overline{CE}_1 \geq V_{IH}$ , $CE_2 \leq V_{IL}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	-	120	mA
$I_{SB2}$	Automatic CE power-down current — CMOS inputs	Max $V_{CC}$ , $\overline{CE}_1 \geq V_{CC} - 0.3V$ , $CE_2 \leq 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V$ , $f = 0$	-	100	mA

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	FBGA	Unit
$C_{IN}$	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = 3.3 \text{ V}$	32	pF
$C_{OUT}$	I/O capacitance		40	pF

## Thermal Resistance

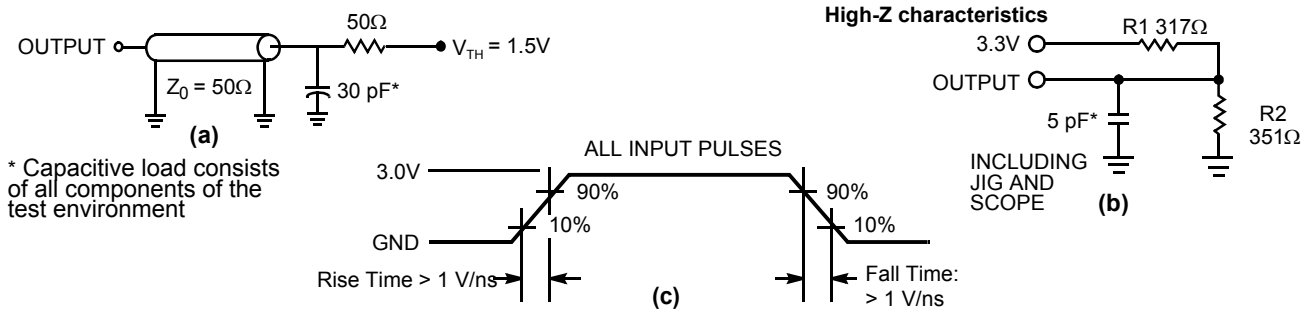
Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	FBGA	Unit
$\theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	55	°C/W
$\theta_{JC}$	Thermal resistance (junction to case)		23.04	°C/W

### Note

2.  $V_{IL}(\text{min}) = -2.0V$  and  $V_{IH}(\text{max}) = V_{CC} + 2V$  for pulse durations of less than 20 ns.

Figure 2. AC Test Loads and Waveforms<sup>[3]</sup>

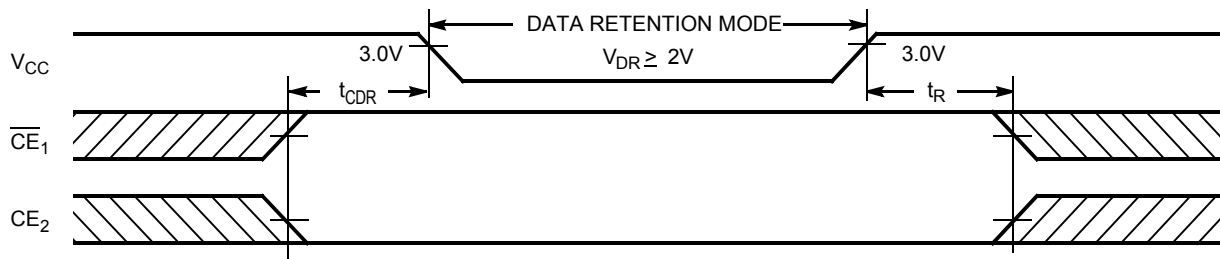


### Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		2	–	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = 2V$ , $\overline{CE}_1 \geq V_{CC} - 0.2V$ , $CE_2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	–	–	100	mA
$t_{CDR}^{[4]}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[5]}$	Operation recovery time		12	–	–	ns

Figure 3. Data Retention Waveform



**Notes**

- Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (3.0V). 100  $\mu s$  ( $t_{power}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation begins including reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ , 2.0V) voltage.
- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50 \mu s$  or stable at  $V_{CC(min.)} \geq 50 \mu s$ .

## AC Switching Characteristics

Over the Operating Range <sup>[6]</sup>

Parameter	Description	-12		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{\text{power}}$	$V_{\text{CC}}$ (typical) to the first access <sup>[7]</sup>	100	–	$\mu\text{s}$
$t_{\text{RC}}$	Read cycle time	12	–	ns
$t_{\text{AA}}$	Address to data valid	–	12	ns
$t_{\text{OHA}}$	Data hold from address change	3	–	ns
$t_{\text{ACE}}$	$\overline{\text{CE}}_1$ LOW and $\text{CE}_2$ HIGH to data valid	–	12	ns
$t_{\text{DOE}}$	$\overline{\text{OE}}$ LOW to data valid	–	7	ns
$t_{\text{LZOE}}$	$\overline{\text{OE}}$ LOW to low-Z	1	–	ns
$t_{\text{HZOE}}$	$\overline{\text{OE}}$ HIGH to high-Z <sup>[8]</sup>	–	7	ns
$t_{\text{LZCE}}$	$\overline{\text{CE}}_1$ LOW and $\text{CE}_2$ HIGH to low-Z <sup>[8]</sup>	3	–	ns
$t_{\text{HZCE}}$	$\overline{\text{CE}}_1$ HIGH and $\text{CE}_2$ LOW to high-Z <sup>[8]</sup>	–	7	ns
$t_{\text{PU}}$	$\overline{\text{CE}}_1$ LOW and $\text{CE}_2$ HIGH to power-up <sup>[9]</sup>	0	–	ns
$t_{\text{PD}}$	$\overline{\text{CE}}_1$ HIGH and $\text{CE}_2$ LOW to power-down <sup>[9]</sup>	–	12	ns
<b>Write Cycle</b> <sup>[10, 11]</sup>				
$t_{\text{WC}}$	Write cycle time	12	–	ns
$t_{\text{SCE}}$	$\overline{\text{CE}}_1$ LOW and $\text{CE}_2$ HIGH to write end	9	–	ns
$t_{\text{AW}}$	Address setup to write end	9	–	ns
$t_{\text{HA}}$	Address hold from write end	0	–	ns
$t_{\text{SA}}$	Address setup to write start	0	–	ns
$t_{\text{PWE}}$	$\overline{\text{WE}}$ pulse width	9	–	ns
$t_{\text{SD}}$	Data setup to write end	7	–	ns
$t_{\text{HD}}$	Data hold from write end	0	–	ns
$t_{\text{LZWE}}$	$\overline{\text{WE}}$ HIGH to low-Z <sup>[8]</sup>	3	–	ns
$t_{\text{HZWE}}$	$\overline{\text{WE}}$ LOW to high-Z <sup>[8]</sup>	–	7	ns

### Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and input pulse levels of 0 to 3.0V. Test conditions for the read cycle use output loading shown in part a) of [AC Test Loads and Waveforms](#)[3], unless specified otherwise.
- $t_{\text{POWER}}$  gives the minimum amount of time that the power supply is at typical  $V_{\text{CC}}$  values until the first memory access is performed.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ ,  $t_{\text{HZWE}}$ ,  $t_{\text{LZOE}}$ ,  $t_{\text{LZCE}}$ , and  $t_{\text{LZWE}}$  are specified with a load capacitance of 5 pF as in (b) of [AC Test Loads and Waveforms](#)[3].
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . Chip enables must be active and  $\overline{\text{WE}}$  must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 2 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

Switching Waveforms

Figure 4. Read Cycle No. 1 [12, 13, 14]

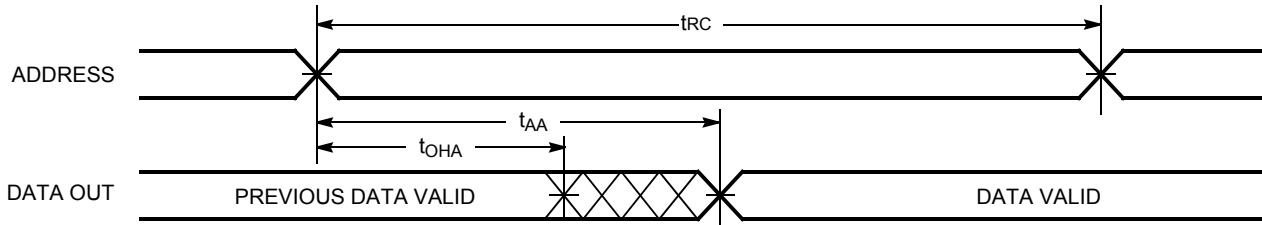
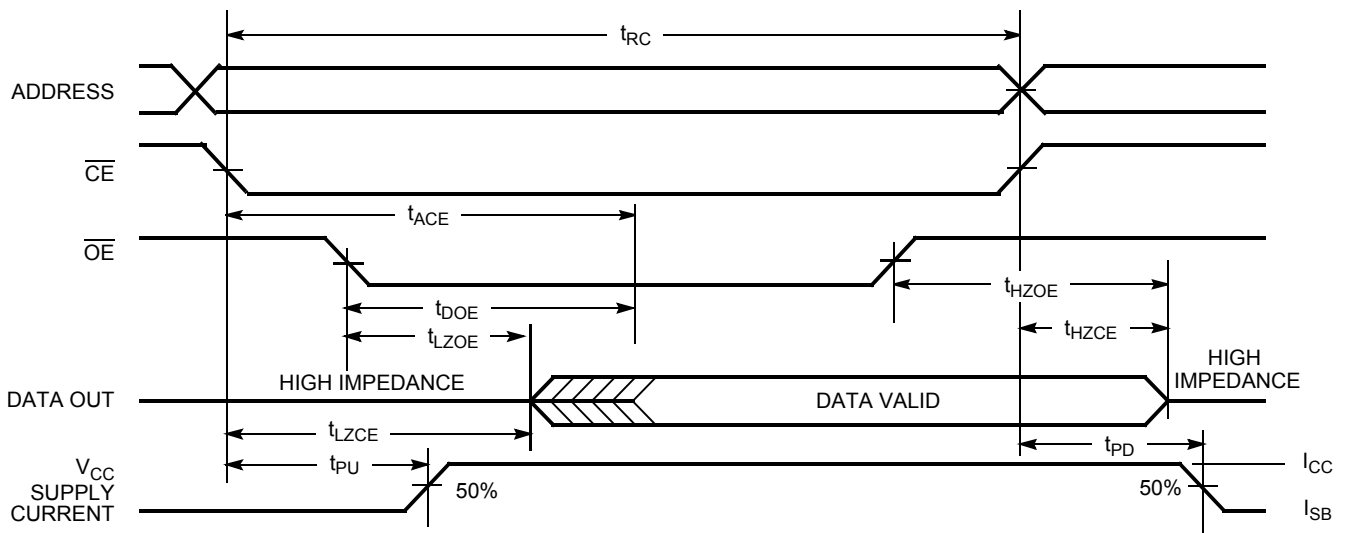


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [12, 14, 15]



Notes

- 12.  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $CE_2$  such that when  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW. For all other combinations,  $\overline{CE}$  is HIGH.
- 13. The device is continuously selected.  $\overline{CE} = V_{IL}$ .
- 14.  $\overline{WE}$  is HIGH for read cycle.
- 15. Address valid before or similar to  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [16, 17, 18]

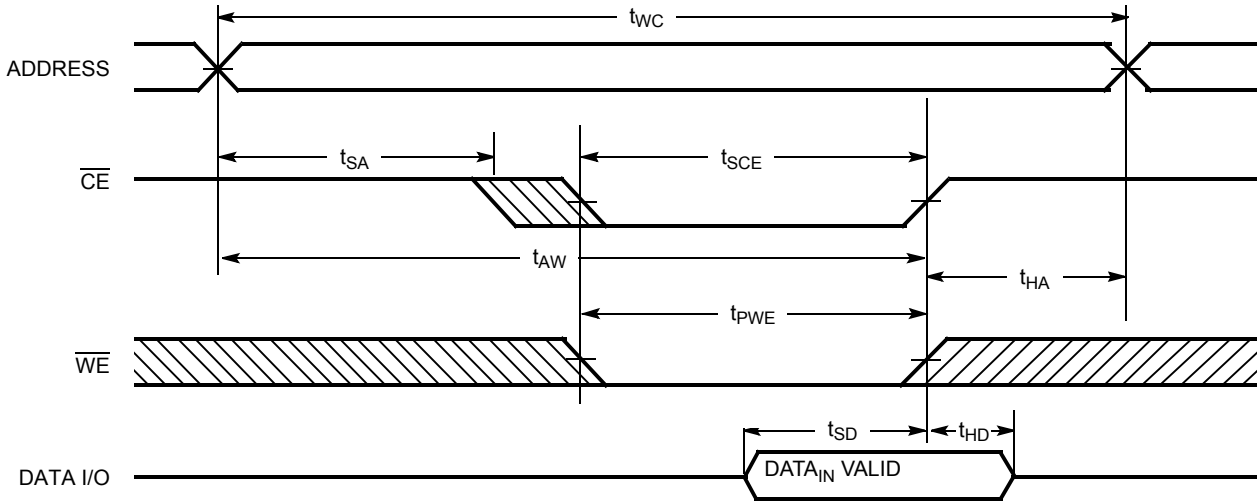
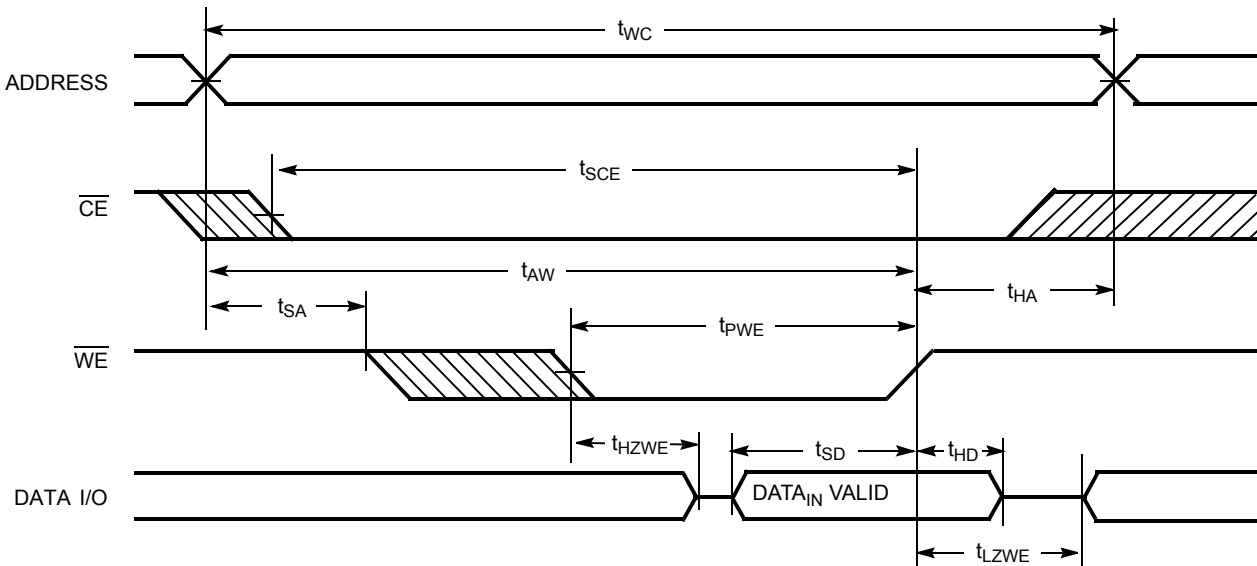


Figure 7. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [16, 17, 18]



Notes

- 16.  $\overline{\text{CE}}$  refers to the internal logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$  such that when  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW. For all other combinations,  $\overline{\text{CE}}$  is HIGH.
- 17. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
- 18. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high impedance state.



**Truth Table**

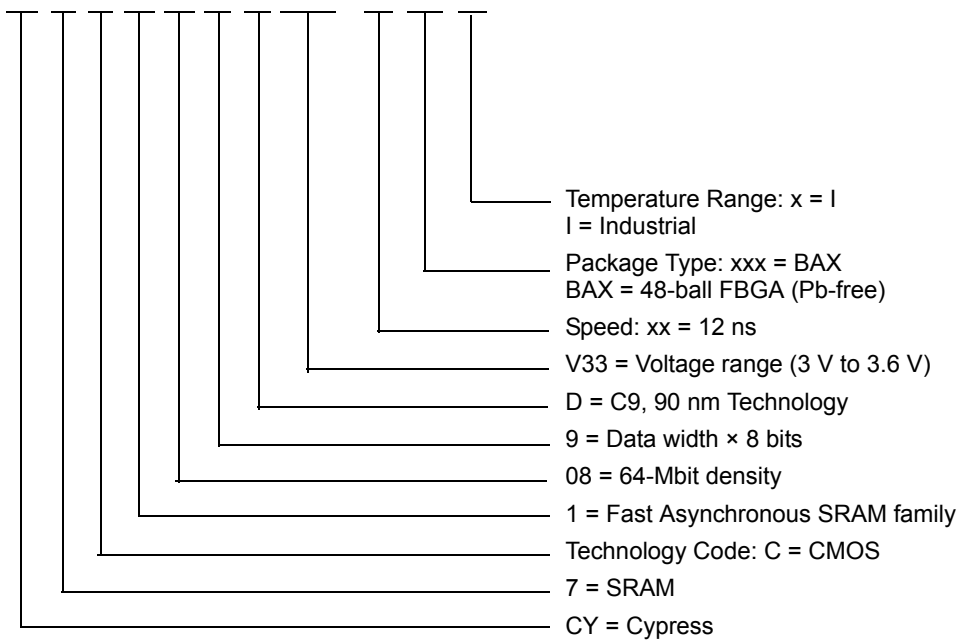
$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> – I/O <sub>7</sub>	Mode	Power
H	X	X	X	High-Z	Power down	Standby (I <sub>SB</sub> )
X	L	X	X	High-Z	Power down	Standby (I <sub>SB</sub> )
L	H	L	H	Data Out	Read all bits	Active (I <sub>CC</sub> )
L	H	X	L	Data In	Write all bits	Active (I <sub>CC</sub> )
L	H	H	H	High-Z	Selected, Outputs disabled	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1089DV33-12BAXI	001-50044	48-ball FBGA (8 × 9.5 × 1.4 mm) (Pb-free)	Industrial

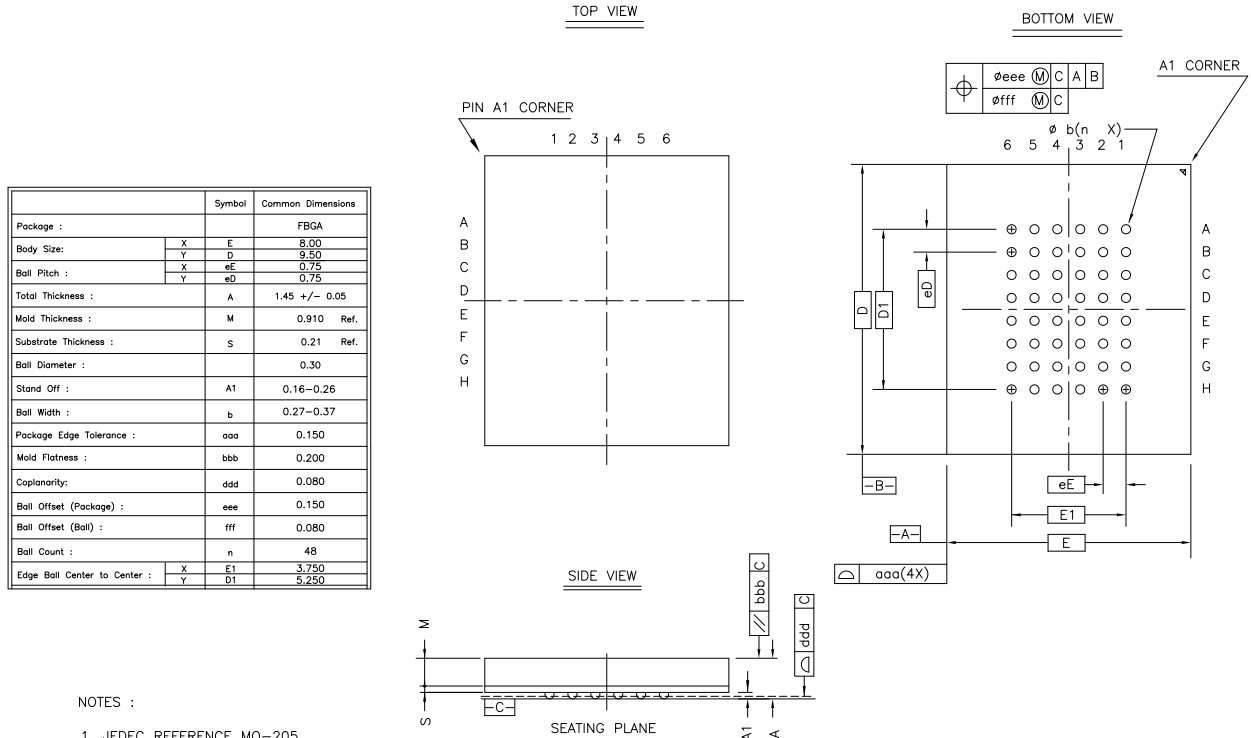
**Ordering Code Definition**

CY 7 C 1 08 9 D V33 - xx xxx x



## Package Diagram

Figure 8. 48-Ball FBGA (8 x 9.5 x 1.4 mm) (001-50044)



NOTES :

1. JEDEC REFERENCE MO-205
2. PACKAGE WEIGHT : 0.2409g
3. DIMENSIONS IN MILLIMETERS

001-50044 \*C

## Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
FBGA	fine ball grid array
I/O	input/output
SRAM	static random access memory
TTL	transistor-transistor logic

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μA	microamperes
mA	milliamperes
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

## Document History Page

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Document Number: 001-53993				
REV.	ECN NO.	Submission Date	Orig. of Change	Description of Change
**	2746867	07/31/2009	VKN/AESA	New Data sheet
*A	3100499	12/02/2010	PRAS	Updated Note 12. Changed datasheet status from Preliminary to Final. Updated <a href="#">Package Diagram</a> and <a href="#">Sales, Solutions, and Legal Information</a> . Added <a href="#">Acronyms</a> , <a href="#">Document Conventions</a> and <a href="#">Ordering Code Definition</a> .
*B	3178259	21/02/2011	PRAS	Post to external web.

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