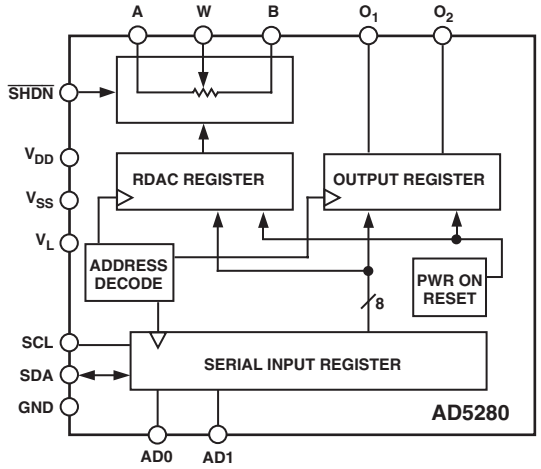
15 V, I²C Compatible 256-Position Digital Potentiometers

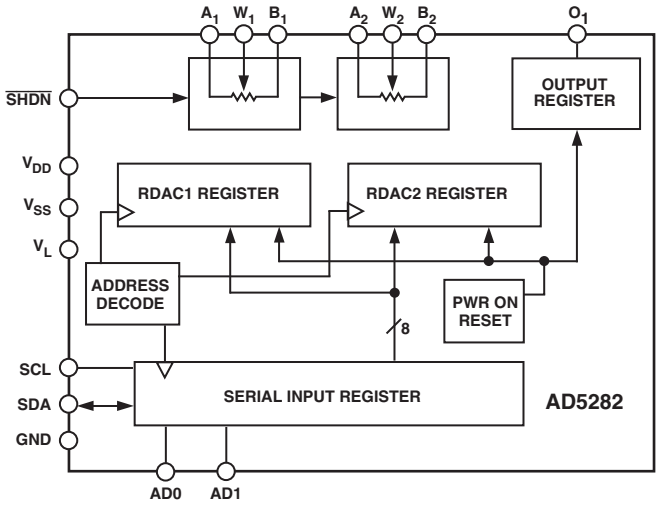
AD5280/AD5282*

FEATURES
256 Position
AD5280: 1-Channel
AD5282: 2-Channel (Independently Programmable)
Potentiometer Replacement
20 kΩ, 50 kΩ, 200 kΩ
Low Temperature Coefficient 30 ppm/°C
Internal Power-On Midscale Preset
5 V to 15 V Single-Supply; ±5.5 V Dual-Supply Operation
I²C Compatible Interface

APPLICATIONS
Multimedia, Video, and Audio
Communications
Mechanical Potentiometer Replacement
Instrumentation: Gain, Offset Adjustment
Programmable Voltage Source
Programmable Current Source
Line Impedance Matching

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The AD5280/AD5282 provides a single-/dual-channel, 256-position digitally controlled variable resistor (VR) device.[1] These devices perform the same electronic adjustment function as a potentiometer, trimmer, or variable resistor. Each VR offers a completely programmable value of resistance between the A terminal and the wiper or the B terminal and the wiper. The fixed A-to-B terminal resistance of 20 kΩ, 50 kΩ, or 200 kΩ has a 1% channel-to-channel matching tolerance. Nominal temperature coefficient of both parts is 30 ppm/°C. Another key feature of these parts is that they can operate up to +15 V or ±5 V.

Wiper position programming defaults to midscale at system power-on. Once powered, the VR wiper position is programmed by an I²C compatible 2-wire serial data interface. Both parts have additional programmable logic outputs that enable users to drive digital loads, logic gates, LED drivers, and analog switches in their system.

The AD5280/AD5282 are available in thin surface-mount 14-lead and 16-lead TSSOP packages. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +85°C. For 3-wire SPI compatible interface applications, see AD5260/AD5262 products.

*Patent Pending.
NOTE
[1]The terms digital potentiometer, VR, and RDAC are used interchangeably.

REV. 0

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AD5280/AD5282–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS 20 kΩ, 50 kΩ, 200 kΩ VERSION

(V_{DD} = +15 V, V_{SS} = 0 V or V_{DD} = +5 V, V_{SS} = –5 V; V_{LOGIC} = 5 V, V_A = +V_{DD}, V_B = 0 V; –40°C < T_A < +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS–RHEOSTAT MODE Specifications apply to all VRs						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = NC	–1	±1/4	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	–1	±1/4	+1	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	–30		+30	%
Resistance Temperature Coefficient	$R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = No Connect		30		ppm/°C
Wiper Resistance	R_W	I_W = V_{DD} /R, V_{DD} = 3 V or 5 V		60	150	Ω
DC CHARACTERISTICS–POTENTIOMETER DIVIDER MODE Specifications apply to all VRs						
Resolution	N		8			Bits
Integral Nonlinearity[4]	INL		–1	±1/4	+1	LSB
Differential Nonlinearity[4]	DNL		–1	±1/4	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 80_H		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = FF_H	–2	–1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	+1	+2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		V_{SS}		V_{DD}	V
Capacitance[6] A, B	$C_{A,B}$	f = 5 MHz, measured to GND, Code = 80_H		25		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 80_H		55		pF
Common-Mode Leakage	I_{CM}	V_A = V_B = V_W		1		nA
Shutdown Current	I_{SHDN}				5	µA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{LOGIC} = 3 V, V_{SS} = 0	2.1			V
Input Logic Low	V_{IL}	V_{LOGIC} = 3 V, V_{SS} = 0			0.6	V
Output Logic High (SDO)	V_{IH}		4.9			V
Output Logic Low (SDO)	V_{IL}				0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Logic Supply	V_{LOGIC}		2.7		5.5	V
Power Single-Supply Range	$V_{DD\ RANGE}$	V_{SS} = 0 V	5		15	V
Power Dual-Supply Range	$V_{DD/SS\ RANGE}$		±4.5		±5.5	V
Logic Supply Current	I_{LOGIC}	V_{LOGIC} = 5 V			60	µA
Positive Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		0.1	1	µA
Negative Supply Current	I_{SS}			0.1	1	µA
Power Dissipation[7]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = +5 V, V_{SS} = –5 V		0.2	0.3	mW
Power Supply Sensitivity	PSS			0.002	0.01	%/%
DYNAMIC CHARACTERISTICS[6, 8, 9]						
Bandwidth –3 dB	BW_20K	R_{AB} = 20 kΩ, Code = 80_H		310		kHz
	BW_50K	R_{AB} = 50 kΩ, Code = 80_H		150		kHz
	BW_200K	R_{AB} = 200 kΩ, Code = 80_H		35		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, R_{AB} = 20 kΩ V_B = 0 V DC, f = 1 kHz		0.014		%
V_W Settling Time	t_S	V_A = 5 V, V_B = 5 V, ±1 LSB error band		5		µs
Crosstalk	CT	V_A = V_{DD}, V_B = 0 V, Measure VW1 with Adjacent RDAC Making Full-Scale Code Change		15		nV-s
Analog Crosstalk	CTA	Measure V_{W1} with V_{W2} = 5 V p-p @ f = 10 kHz		–62		dB
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 20 kΩ, f = 1 kHz		18		nV/√Hz

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
INTERFACE TIMING CHARACTERISTICS Applies to all parts[6, 10]						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time between STOP and START	t_1		1.3			µs
$t_{HD:STA}$ Hold Time (Repeated START)	t_2	After this period, the first clock pulse is generated	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU:STA}$ Setup Time for START Condition	t_5		0.6			µs
$t_{HD:DAT}$ Data Hold Time	t_6				0.9	µs
$t_{SU:DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of Both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU:STO}$ Setup Time for STOP Condition	t_{10}		0.6			µs

NOTES

[1] Typicals represent average readings at 25°C, V_{DD} = +5 V, V_{SS} = –5 V.

[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

[3] V_{AB} = V_{DD}, Wiper (V_W) = No connect.

[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

[5] Resistor terminals A, B, W have no limitations on polarity with respect to each other.

[6] Guaranteed by design and not subject to production test.

[7] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.

[8] Bandwidth, noise, and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.

[9] All dynamic characteristics use V_{DD} = 5 V.

[10] See timing diagram for location of measured values.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND ..... –0.3 V, +15 V
V_{SS} to GND ..... 0 V, –7 V
V_{DD} to V_{SS} ..... 15 V
V_A, V_B, V_W to GND ..... V_{SS}, V_{DD}
$A_X – B_X$, $A_X – W_X$, $B_X – W_X$
Intermittent[2] ..... ±20 mA
Continuous ..... ±5 mA
V_{LOGIC} to GND ..... 0 V, 7 V
Output Voltage to GND ..... 0 V, 7 V
Operating Temperature Range ..... –40°C to +85°C
Thermal Resistance[3] θ_{JA},
TSSOP-14 ..... 206°C/W
TSSOP-16 ..... 150°C/W
Maximum Junction Temperature (T_J MAX) ..... 150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature
RU-14, RU-16 (Vapor Phase, 60 sec) ..... 215°C
RU-14, RU-16 (Infrared, 15 sec) ..... 220°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Maximum terminal current is bound by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[3]Package Power Dissipation (T_J MAX – T_A)/θ_{JA}

ORDERING GUIDE

Model	Number of Channels	R_{AB} (kΩ)	Temp	Package Description	Package Option	Parts Per Container	Branding Information*
AD5280BRU20	1	20	–40°C to +85°C	TSSOP-14	RU-14	96	AD5280B20
AD5280BRU20-REEL7	1	20	–40°C to +85°C	TSSOP-14	RU-14	1000	AD5280B20
AD5280BRU50	1	50	–40°C to +85°C	TSSOP-14	RU-14	96	AD5280B50
AD5280BRU50-REEL7	1	50	–40°C to +85°C	TSSOP-14	RU-14	1000	AD5280B50
AD5280BRU200	1	200	–40°C to +85°C	TSSOP-14	RU-14	96	AD5280B200
AD5280BRU200-REEL7	1	200	–40°C to +85°C	TSSOP-14	RU-14	1000	AD5280B200
AD5282BRU20	2	20	–40°C to +85°C	TSSOP-16	RU-16	96	AD5282B20
AD5282BRU20-REEL7	2	20	–40°C to +85°C	TSSOP-16	RU-16	1000	AD5282B20
AD5282BRU50	2	50	–40°C to +85°C	TSSOP-16	RU-16	96	AD5282B50
AD5282BRU50-REEL7	2	50	–40°C to +85°C	TSSOP-16	RU-16	1000	AD5282B50
AD5282BRU200	2	200	–40°C to +85°C	TSSOP-16	RU-16	96	AD5282B200
AD5282BRU200-REEL7	2	200	–40°C to +85°C	TSSOP-16	RU-16	1000	AD5282B200

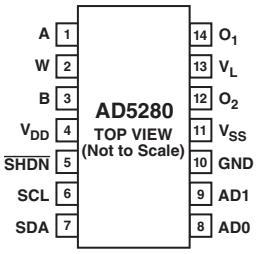
The AD5280/AD5282 die size is 75 mm × 120 mm, 9,000 sq. mm. Contains 3077 transistors.
*Line 1 contains model number, Line 2 contains ADI logo followed by the end-to-end resistance value, and line 3 contains date code YYWW.

CAUTION

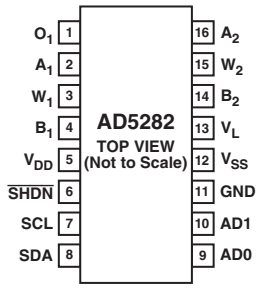
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5280/AD5282 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

AD5280 PIN CONFIGURATION



AD5282 PIN CONFIGURATION



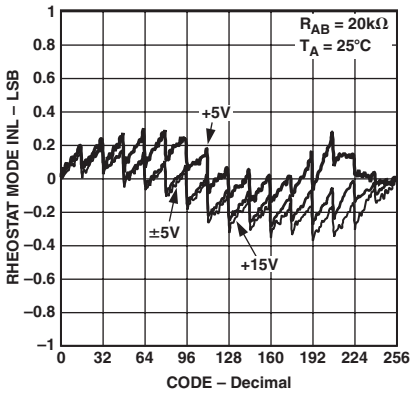
AD5280 PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	A	Resistor Terminal A
2	W	Wiper Terminal W
3	B	Resistor Terminal B
4	V_{DD}	Positive Power Supply. Specified for operation from 5 V to 15 V (Sum of $\|V_{DD}\| + \|V_{SS}\| \le 15$ V).
5	$\overline{SHDN}$	Active Low, Asynchronous Connection of the Wiper W to Terminal B and Open Circuit of Terminal A. RDAC Register contents unchanged. $\overline{SHDN}$ should tie to V_L if not used.
6	SCL	Serial Clock Input
7	SDA	Serial Data Input/Output
8	AD0	Programmable Address Bit 0 for Multiple Package Decoding. Bits AD0 and AD1 provide four possible addresses.
9	AD1	Programmable Address Bit 1 for Multiple Package Decoding. Bits AD0 and AD1 provide four possible addresses.
10	GND	Common Ground
11	V_{SS}	Negative Power Supply. Specified for operation from 0 V to –5 V (Sum of $\|V_{DD}\| + \|V_{SS}\| \le 15$ V).
12	O_2	Logic Output Terminal O_2
13	V_L	Logic Supply Voltage. Needs to be the same voltage as the digital logic controlling the AD5280.
14	O_1	Logic Output Terminal O_1

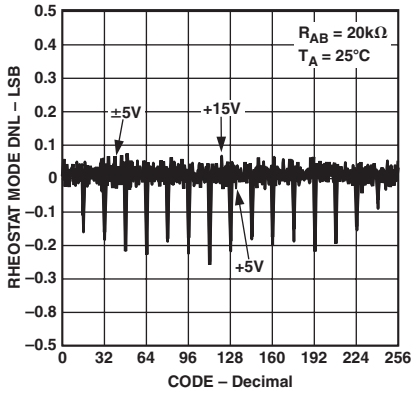
AD5282 PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	O_1	Logic Output Terminal O_1
2	A_1	Resistor Terminal A_1
3	W_1	Wiper Terminal W_1
4	B_1	Resistor Terminal B_1
5	V_{DD}	Positive Power Supply. Specified for operation from 5 V to 15 V (Sum of $\|V_{DD}\| + \|V_{SS}\| \le 15$ V).
6	$\overline{SHDN}$	Active Low, Asynchronous Connection of the Wiper W to Terminal B and Open Circuit of Terminal A. RDAC Register contents unchanged. $\overline{SHDN}$ should tie to V_L if not used.
7	SCL	Serial Clock Input
8	SDA	Serial Data Input/Output
9	AD0	Programmable Address Bit 0 for Multiple Package Decoding. Bits AD0 and AD1 provide four possible addresses.
10	AD1	Programmable Address Bit 1 for Multiple Package Decoding. Bits AD0 and AD1 provide four possible addresses.
11	GND	Common Ground
12	V_{SS}	Negative Power Supply. Specified for operation from 0 V to –5 V (Sum of $\|V_{DD}\| + \|V_{SS}\| \le 15$ V).
13	V_L	Logic Supply Voltage. Needs to be the same voltage as the digital logic controlling the AD5282.
14	B_2	Resistor Terminal B_2
15	W_2	Wiper Terminal W_2
16	A_2	Resistor Terminal A_2

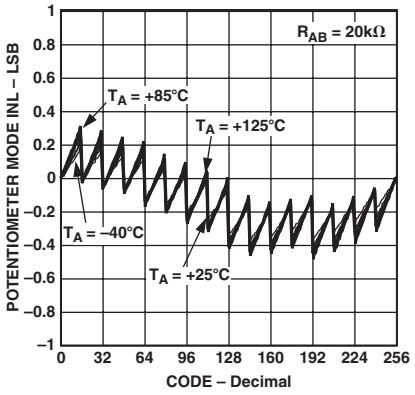
AD5280/AD5282–Typical Performance Characteristics



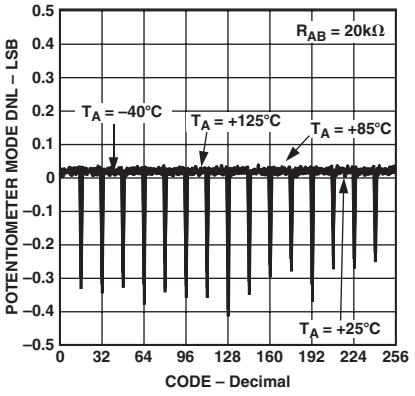
TPC 1. R-INL vs. Code vs. Supply Voltages



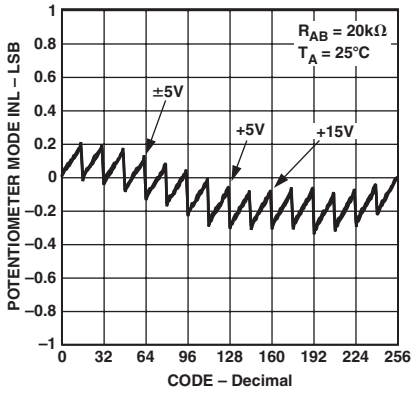
TPC 2. R-DNL vs. Code vs. Supply Voltages



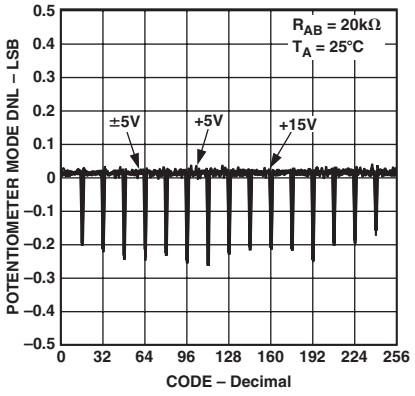
TPC 3. INL vs. Code, $V_{DD}/V_{SS} = \pm 5$ V



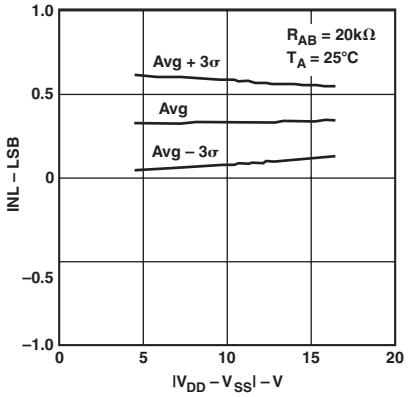
TPC 4. DNL vs. Code, $V_{DD}/V_{SS} = \pm 5$ V



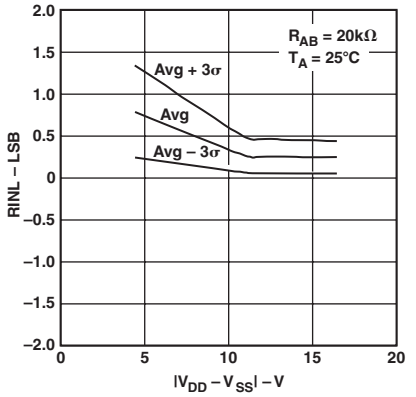
TPC 5. INL vs. Code vs. Supply Voltages



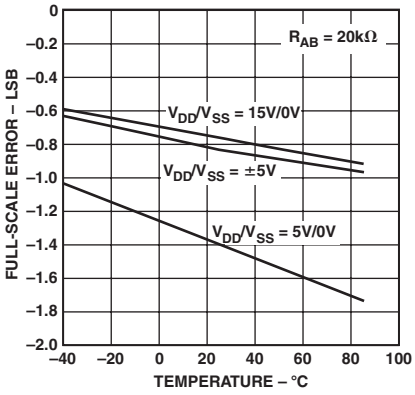
TPC 6. DNL vs. Code vs. Supply Voltages



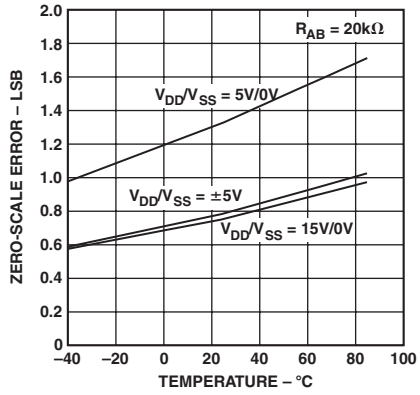
TPC 7. INL Over Supply Voltage



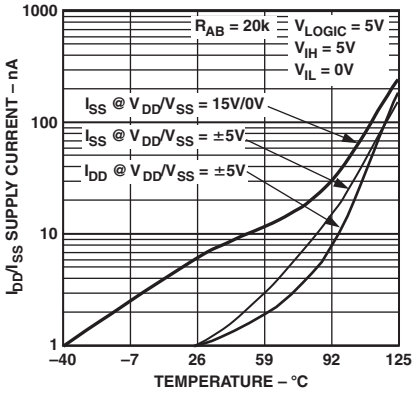
TPC 8. RINL Over Supply Voltage



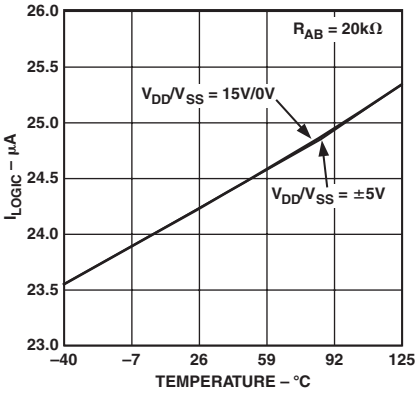
TPC 9. Full-Scale Error



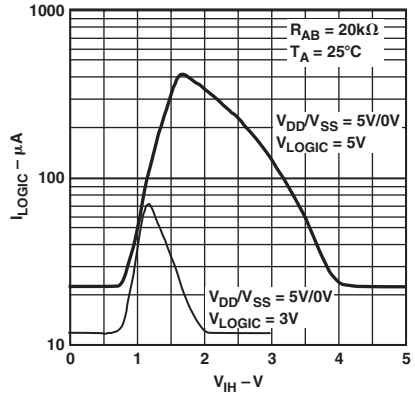
TPC 10. Zero-Scale Error



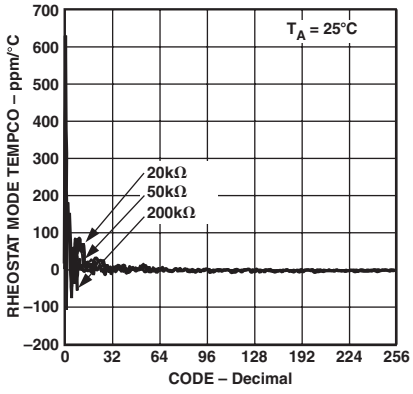
TPC 11. Supply Current vs. Temperature



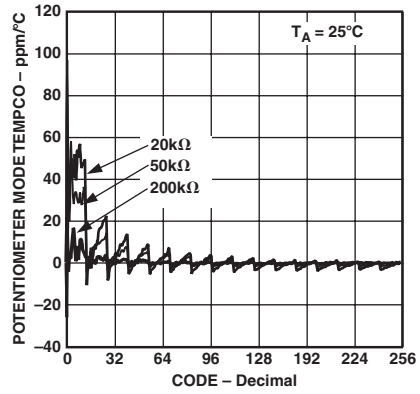
TPC 12. V_{LOGIC} Supply Current vs. Temperature



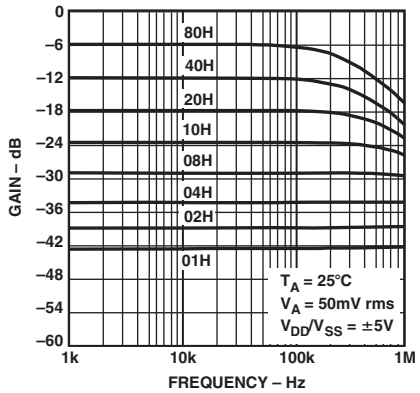
TPC 13. V_{LOGIC} Supply Current vs. Digital Input Voltage



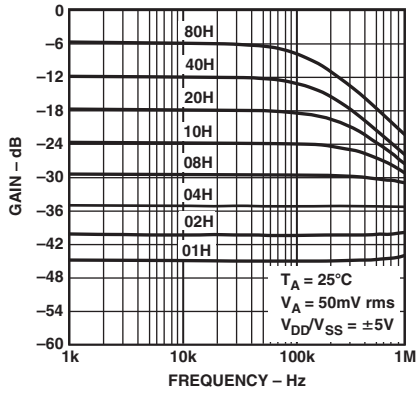
TPC 14. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code, $V_{DD}/V_{SS} = \pm 5$ V



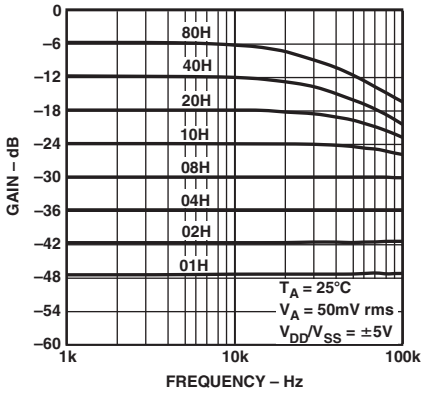
TPC 15. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code, $V_{DD}/V_{SS} = \pm 5$ V



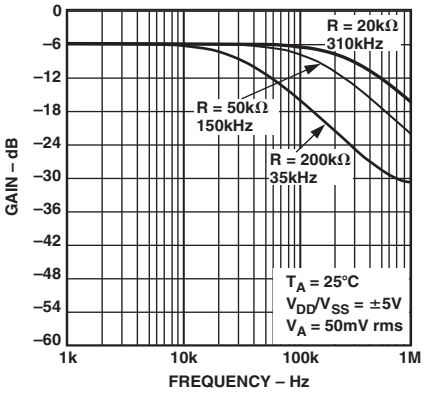
TPC 16. Gain vs. Frequency vs. Code, R_{AB} = 20 kΩ



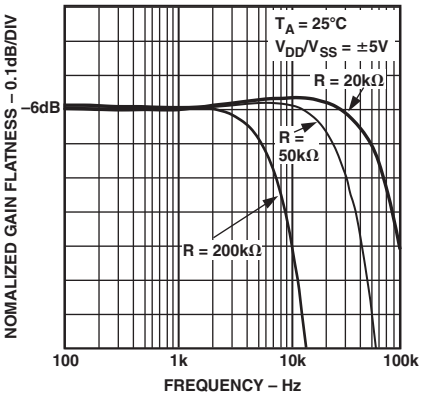
TPC 17. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ



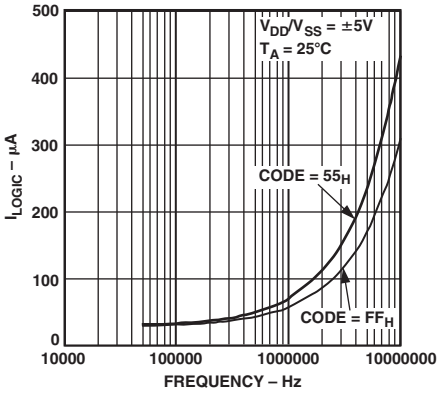
TPC 18. Gain vs. Frequency vs. Code, R_{AB} = 200 kΩ



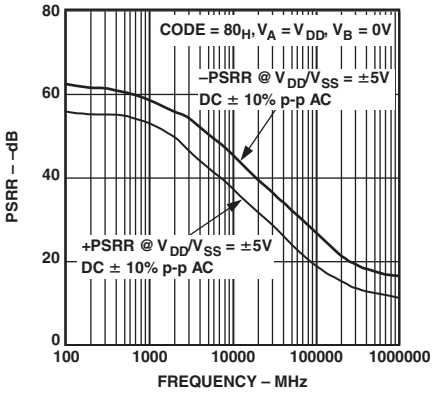
TPC 19. –3 dB Bandwidth



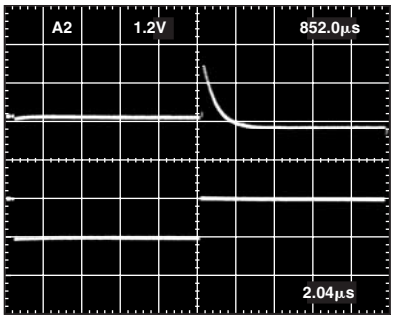
TPC 20. Normalized Gain Flatness vs. Frequency



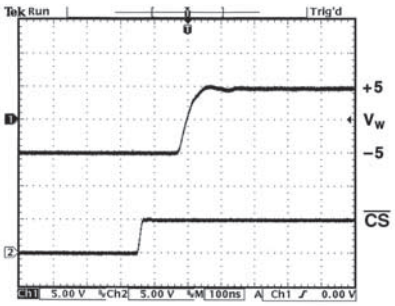
TPC 21. V_{LOGIC} Supply Current vs. Frequency



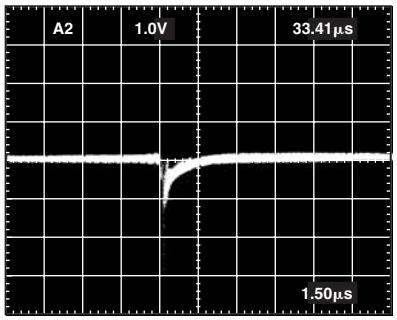
TPC 22. PSRR vs. Frequency



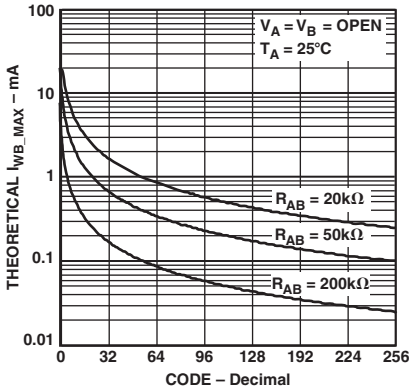
TPC 23. Midscale Glitch Energy Code 80_H to $7F_H$



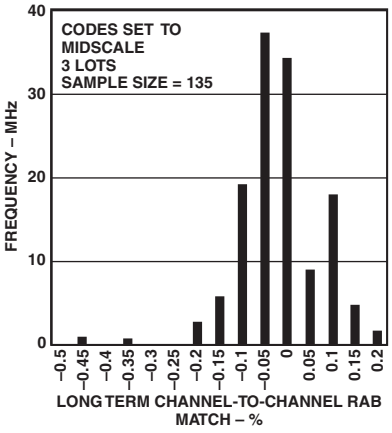
TPC 24. Large Signal Settling Time



TPC 25. Digital Feedthrough vs. Time



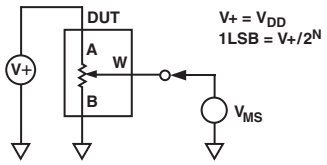
TPC 26. I_{MAX} vs. Code



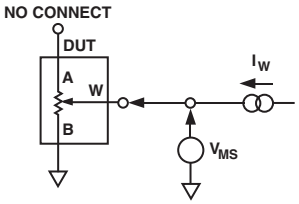
TPC 27. Channel-to-Channel Resistance Matching (AD5282)

TEST CIRCUITS

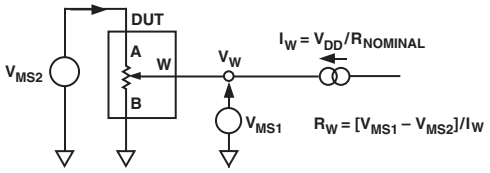
Test Circuits 1 to 11 define the test conditions used in the product specification table.



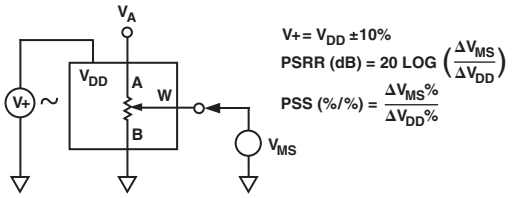
Test Circuit 1. Potentiometer Divider Nonlinearity Error (INL, DNL)



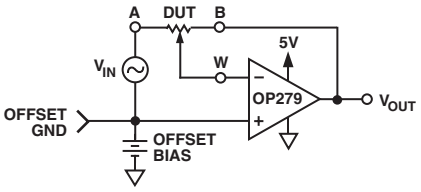
Test Circuit 2. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)



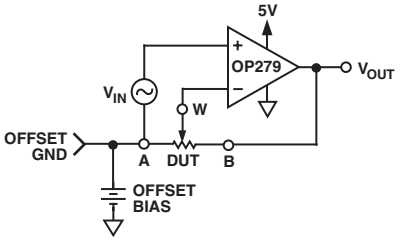
Test Circuit 3. Wiper Resistance



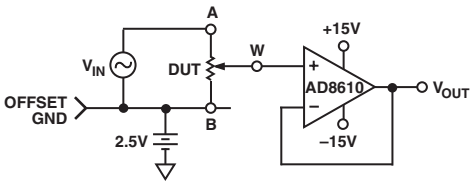
Test Circuit 4. Power Supply Sensitivity (PSS, PSSR)



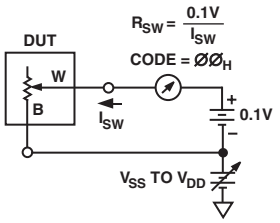
Test Circuit 5. Inverting Gain



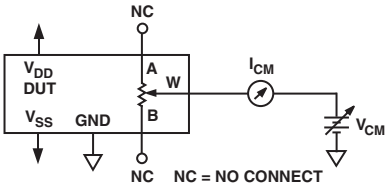
Test Circuit 6. Noninverting Gain



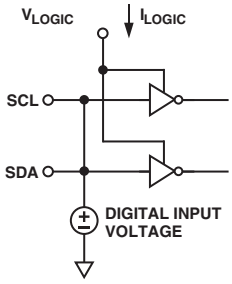
Test Circuit 7. Gain vs. Frequency



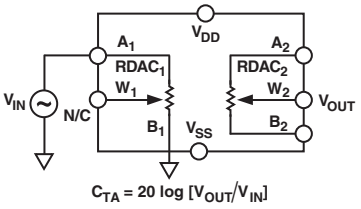
Test Circuit 8. Incremental On Resistance



Test Circuit 9. Common-Mode Leakage Current



Test Circuit 10. V_{LOGIC} Current vs. Digital Input Voltage



Test Circuit 11. Analog Crosstalk (AD5282 Only)

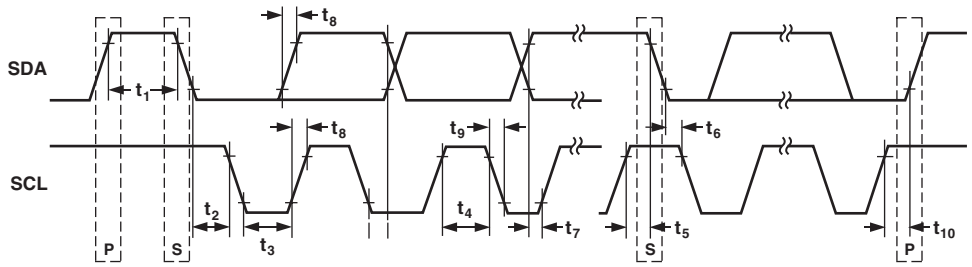


Figure 1. Detailed Timing Diagram

Data of AD5280/AD5282 is accepted from the I²C bus in the following serial format:

S	0 1 0 1 1 AD1 AD0 R/$\overline{W}$	A	$\overline{A}$/B RS SD O1 O2 X X X	A	D7 D6 D5 D4 D3 D2 D1 D0	A	P
	Slave Address Byte		Instruction Byte		Data Byte		

Where:

S = Start Condition
P = Stop Condition
A = Acknowledge
$\overline{A}$ = No Acknowledge
X = Don't Care
AD1, AD0 = Package Pin Programmable Address Bits
R/$\overline{W}$ = Read Enable at High and Write Enable at Low
$\overline{A}$/B = RDAC Subaddress Select. "Zero" for RDAC1 and "One" for RDAC2
RS = Midscale Reset, Active High (only affects selected channel)
SD = Shutdown. Same as $\overline{SHDN}$ pin operation except inverse logic (only affects selected channel)
O_2, O_1 = Output Logic Pin Latched Values, Default Logic 0
D7, D6, D5, D4, D3, D2, D1, D0 = Data Bits

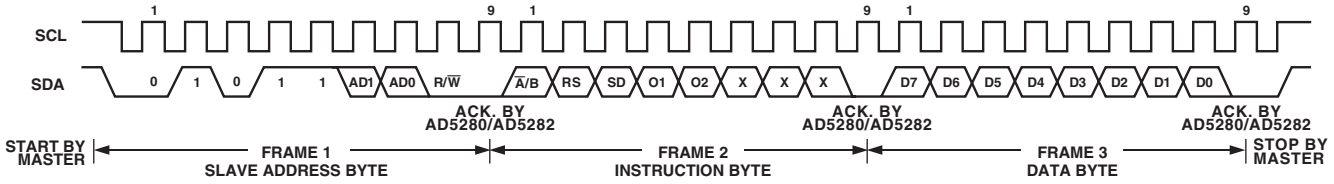


Figure 2. Writing to the RDAC Register

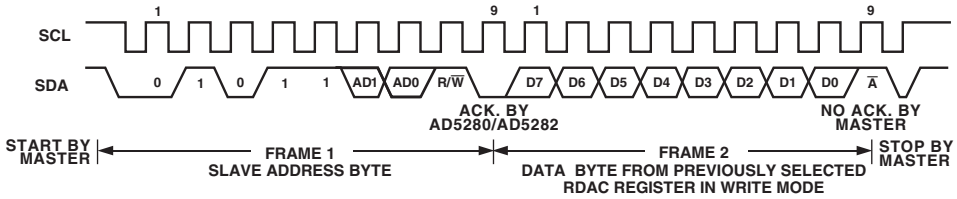


Figure 3. Reading Data from a Previously Selected RDAC Register in Write Mode

OPERATION

The AD5280/AD5282 provides a single-/dual-channel, 256-position, digitally controlled variable resistor (VR) device.

To program the VR settings, refer to the Digital Interface section. Both parts have an internal power-on preset that places the wiper at midscale during power-on, which simplifies the fault condition recovery at power-up. Operation of the power-on preset function also depends on the state of the V_L pin. In addition, the shutdown $\overline{SHDN}$ pin of the AD5280/AD5282 places the RDAC in an almost zero power consumption state where terminal A is open circuited and the wiper W is connected to terminal B, resulting in only leakage currents being consumed in the VR structure. During shutdown, the VR latch settings are maintained or new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting will be applied to the RDAC.

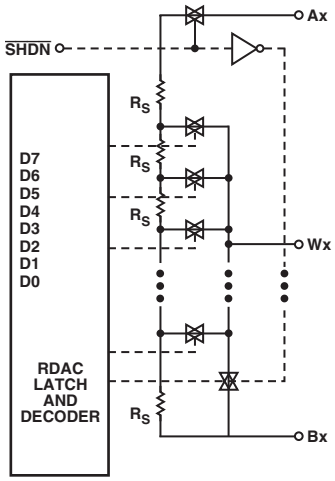


Figure 4. AD5280/AD5282 Equivalent RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between terminals A and B is available in 20 kΩ, 50 kΩ, and 200 kΩ. The final two or three digits of the part number determine the nominal resistance value, e.g., 20 kΩ = 20; 50 kΩ = 50; 200 kΩ = 200. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings. Assuming a 20 kΩ part is used, the wiper's first connection starts at the B terminal for data 00_H. Since there is a 60 Ω wiper contact resistance, such a connection yields a minimum of 60 Ω resistance between terminals W and B. The second connection is the first tap point that corresponds to 138 Ω (R_{WB} = R_{AB}/256 + R_W = 78 Ω + 60 Ω) for data 01_H. The third connection is the next tap point representing 216 Ω (78 × 2 + 60) for data 02_H, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 19982 Ω [R_{AB} – 1 LSB + R_W]. Figure 4 shows a simplified diagram of the equivalent RDAC circuit where the last resistor string will not be accessed; therefore, there is 1 LSB less of the nominal resistance at full scale in addition to the wiper resistance.

The general equation determining the digitally programmed output resistance between W and B is:

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad (1)$$

where:

D is the decimal equivalent of the binary code loaded in the 8-bit RDAC Register.

R_{AB} is the nominal end-to-end resistance.

R_W is the wiper resistance contributed by the on resistance of the internal switch.

Again, if R_{AB} = 20 kΩ and the A terminal is open circuited, the following output resistance values, R_{WB}, will be set for the following RDAC latch codes.

Table I. Codes and Corresponding Resistances

D (DEC)	R_{WB} (Ω)	Output State
255	19982	Full Scale (R_{AB} – 1 LSB + R_W)
128	10060	Midscale
1	138	1 LSB
0	60	Zero-Scale (Wiper Contact Resistance)

Note that in the zero-scale condition, a finite wiper resistance of 60 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is:

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \quad (2)$$

For R_{AB} = 20 kΩ and B terminal open circuited, the following output resistance, R_{WA}, will be set for the following RDAC latch codes.

Table II. Codes and Corresponding Resistances

D (DEC)	R_{WA} (Ω)	Output State
255	138	Full Scale
128	10060	Midscale
1	19982	1 LSB
0	20060	Zero Scale

The typical distribution of the nominal resistance, R_{AB}, from channel-to-channel matches within ±1%. Device-to-device matching is process lot dependent and is possible to have ±30% variation. Since the resistance element is processed in thin film technology, the change in R_{AB} with temperature has a very low 30 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A to be proportional to the input voltage at A-to-B. Unlike the polarity of V_{DD}–V_{SS}, which must be positive, voltage across A–B, W–A, and W–B can be at either polarity provided that V_{SS} is powered by a negative supply.

If ignoring the effect of the wiper resistance for approximation, connecting A terminal to 5 V and B terminal to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across A–B divided by the 256 positions of the potentiometer divider. Since AD5280/AD5282 can be supplied by dual supplies, the general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to terminals A and B is:

$$V_W(D) = \frac{D}{256}V_A + \frac{256 - D}{256}V_B \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance, V_W can be found as:

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}}V_A + \frac{R_{WA}(D)}{R_{AB}}V_B \quad (4)$$

Operation of the digital potentiometer in the Divider Mode results in a more accurate operation overtemperature. Unlike the Rheostat Mode, the output voltage is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB} and not on the absolute values; therefore, the temperature drift reduces to 5 ppm/°C.

DIGITAL INTERFACE

2-Wire Serial Bus

The AD5280/AD5282 are controlled via an I^2C compatible serial bus. The RDACs are connected to this bus as slave devices.

Referring to Figures 2 and 3, the first byte of AD5280/AD5282 is a Slave Address Byte. It has a 7-bit slave address and an R/$\overline{W}$ bit. The 5 MSBs are 01011 and the following two bits are determined by the state of the AD0 and AD1 pins of the device. AD0 and AD1 allow the user to place up to four of the I^2C compatible devices on one bus.

The 2-wire I^2C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 2). The following byte is the Slave Address Byte which consists of the 7-bit slave address followed by an R/$\overline{W}$ bit (this bit determines whether data will be read from or written to the slave device).

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the Acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master will read from the slave device. On the other hand, if the R/$\overline{W}$ bit is low, the master will write to the slave device.

2. A write operation contains an extra Instruction Byte more than a read operation. Such an Instruction Byte in Write Mode follows the Slave Address Byte. The MSB of the Instruction Byte labeled $\overline{A}$/B is the RDAC subaddress select. A "low" selects RDAC1 and a "high" selects RDAC2 for the dual-channel AD5282. Set $\overline{A}$/B to low for the AD5280.

   The second MSB, RS, is the midscale reset. A logic high on this bit moves the wiper of a selected channel to the center tap where $R_{WA} = R_{WB}$. This feature effectively writes over the contents of the register, and thus when taken out of reset mode, the RDAC will remain at midscale.

   The third MSB SD is a shutdown bit. A logic high causes the selected channel to open circuit at terminal A while shorting the wiper to terminal B. This operation yields almost 0 Ω in Rheostat Mode or 0 V in Potentiometer Mode. This SD bit serves the same function as the $\overline{SHDN}$ pin except that the $\overline{SHDN}$ pin reacts to active low. Also, the $\overline{SHDN}$ pin affects both channels (AD5282) as opposed to the SD bit, which only affects the channel that is being written to. It is important to note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting will be applied to the RDAC.

   The following two bits are O1 and O2. They are extra programmable logic outputs that can be used to drive other digital loads, logic gates, LED drivers, analog switches, and so on. The three LSBs are Don't Care (see Figure 2).

3. After acknowledging the Instruction Byte, the last byte in Write Mode is the Data Byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an Acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 2).

4. In the Read Mode, the Data Byte follows immediately after the acknowledgment of the Slave Address Byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference with the Write Mode, where there are eight data bits followed by an Acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 3).

5. When all data bits have been read or written, a Stop condition is established by the master. A Stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In Write Mode, the master will pull the SDA line high during the tenth clock pulse to establish a Stop condition, (see Figure 2). In Read Mode, the master will issue a No Acknowledge for the ninth clock pulse (i.e., the SDA line remains high). The master will then bring the SDA line low before the tenth clock pulse, which goes high to establish a Stop condition (see Figure 3).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. During the write cycle, each data byte will update the RDAC output. For example, after the RDAC has acknowledged its slave address and instruction bytes, the RDAC output will update after these two bytes. If another byte is written to the RDAC while it is still addressed to a specific slave device with the same instruction, this byte will update the output of the selected slave device. If different instructions are needed, the Write Mode has to start with a new Slave Address, Instruction, and Data Byte again. Similarly, a repeated read function of the RDAC is also allowed.

READBACK RDAC VALUE

AD5280/AD5282 allows the user to read back the RDAC values in the Read Mode. However, for the AD5282 dual-channel device, the channel of interest is the one that is previously selected in the Write Mode. In the case where users need to read the RDAC values of both channels in AD5282, they can program the first subaddress in Write Mode and then change to Read Mode to read the first channel value. After that, they can change back to Write Mode with the second subaddress and finally read the second channel value in Read Mode again. Note that it is not necessary for users to issue the Frame 3 data byte in Write Mode for subsequent readback operation. Users should refer to Figures 2 and 3 for the programming format.

ADDITIONAL PROGRAMMABLE LOGIC OUTPUT

AD5280/AD5282 features additional programmable logic outputs, O_1 and O_2, which can be used to drive a digital load, analog switches, and logic gates. O_1 and O_2 default to Logic 0. The logic states of O_1 and O_2 can be programmed in Frame 2 under the Write Mode (see Figure 2). These logic outputs have adequate current driving capability to sink/source milliamperes of load.

Users can also activate O_1 and O_2 in three different ways without affecting the wiper settings. They may do the following:

1. Start, Slave Address Byte, Acknowledge, Instruction Byte with O_1 and O_2 specified, Acknowledge, Stop.
2. Complete the write cycle with Stop, then Start, Slave Address Byte, Acknowledge, Instruction Byte with O_1 and O_2 specified, Acknowledge, Stop.
3. Do not complete the write cycle by not issuing the Stop, then Start, Slave Address Byte, Acknowledge, Instruction Byte with O_1 and O_2 specified, Acknowledge, Stop.

SELF-CONTAINED SHUTDOWN FUNCTION

Shutdown can be activated by strobing the $\overline{SHDN}$ pin or programming the SD bit in the Write Mode Instruction Byte. In addition, shutdown can even be implemented with the device digital output as shown in Figure 5. In this configuration, the device will be shut down during power-up, but users are allowed to program the device. Thus when O_1 is programmed high, the device will exit from Shutdown Mode and respond to the new setting. This self-contained shutdown function allows absolute shutdown during power-up, which is crucial in hazardous environments, without adding extra components.

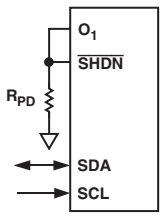


Figure 5. Shutdown by Internal Logic Output

MULTIPLE DEVICES ON ONE BUS

Figure 6 shows four AD5282 devices on the same serial bus. Each has a different slave address since the states of their AD0 and AD1 pins are different. This allows each RDAC within each device to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I^2C compatible interface.

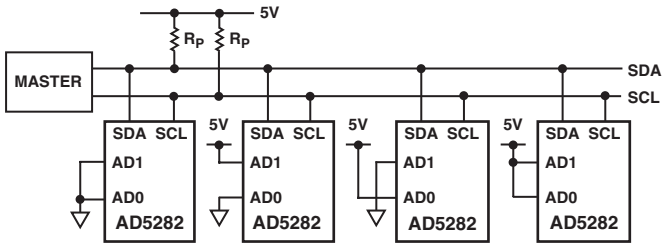


Figure 6. Multiple AD5282 Devices on One Bus

LEVEL SHIFT FOR BIDIRECTIONAL INTERFACE

While most old systems may be operated at one voltage, a new component may be optimized at another. When two systems operate the same signal at two different voltages, proper level shifting is needed. For instance, one can use a 3.3 V E^2PROM to interface with a 5 V digital potentiometer. A level shift scheme is needed to enable a bidirectional communication so that the setting of the digital potentiometer can be stored to and retrieved from the E^2PROM. Figure 7 shows one of the implementations. M1 and M2 can be any N-Ch signal FETs or low threshold FDV301N if V_{DD} falls below 2.5 V.

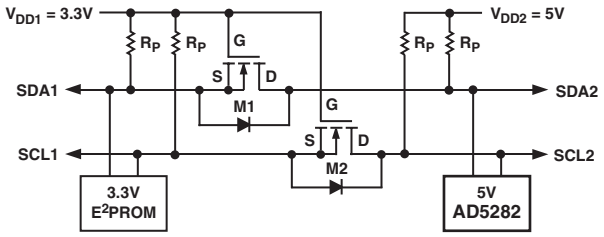


Figure 7. Level Shift for Different Potential Operation

LEVEL SHIFT FOR NEGATIVE VOLTAGE OPERATION

The digital potentiometer is popular in laser diode driver and certain telecommunications equipment level-setting applications. These applications are sometimes operated between ground and some negative supply voltage such that the systems can be biased at ground to avoid large bypass capacitors that may significantly impede the ac performance. Like most digital potentiometers, AD5280/AD5282 can be configured with a negative supply (see Figure 8).

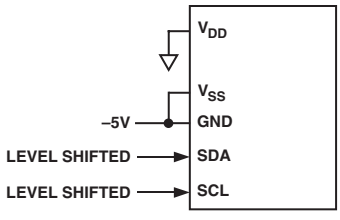


Figure 8. Biased at Negative Voltage

However, the digital inputs must also be level shifted to allow proper operation since the ground is now referenced to the negative potential. As a result, Figure 9 shows one implementation with a few transistors and a few resistors. When V_{IN} is below Q3's threshold value, Q3 is off, Q1 is off, and Q2 is on. In this state, V_{OUT} approaches 0 V. When V_{IN} is above 2 V, Q3 is on, Q1 is on, and Q2 is turned off. In this state, V_{OUT} is pulled down to V_{SS}. Beware that proper time shifting is also needed for successful communication with the device.

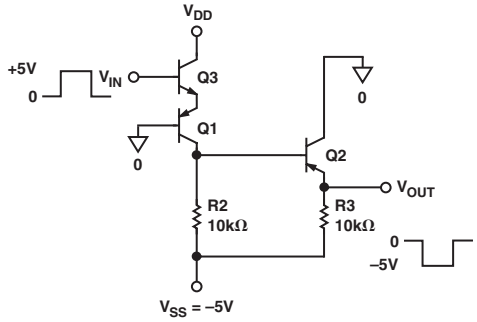


Figure 9. Level Shift for Bipolar Potential Operation

ESD PROTECTION

All digital inputs are protected with a series input resistor and parallel Zener ESD structures shown in Figure 10; applies to digital input pins, SDA, SCL, and $\overline{SHDN}$.

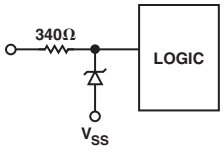


Figure 10a. ESD Protection of Digital Pins

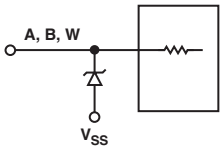


Figure 10b. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The AD5280/AD5282 positive V_{DD} and negative V_{SS} power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed V_{DD} or V_{SS} will be clamped by the internal forward biased diodes (see Figure 11).

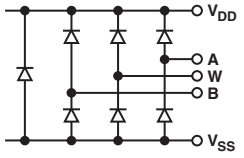


Figure 11. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

POWER-UP SEQUENCE

Since there are ESD protection diodes that limit the voltage compliance at terminals A, B, and W (see Figure 11), it is important to power V_{DD}/V_{SS} before applying any voltage to terminals A, B, and W. Otherwise, the diode will be forward biased such that V_{DD}/V_{SS} will be powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, V_{SS}, digital inputs, and $V_{A/B/W}$. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{DD}/V_{SS}.

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 µF to 0.1 µF disc or chip ceramics capacitors. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and filter low frequency ripple (see Figure 12). Notice the digital ground should also be joined remotely to the analog ground at one point to minimize the digital ground bounce.

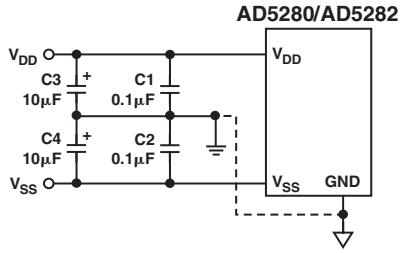


Figure 12. Power Supply Bypassing

APPLICATIONS

Bipolar DC or AC Operation from Dual Supplies

The AD5280/AD5282 can be operated from dual supplies enabling control of ground referenced ac signals or bipolar operation. The ac signal, as high as V_{DD}/V_{SS}, can be applied directly across terminals A–B with the output taken from terminal W. See Figure 13 for a typical circuit connection.

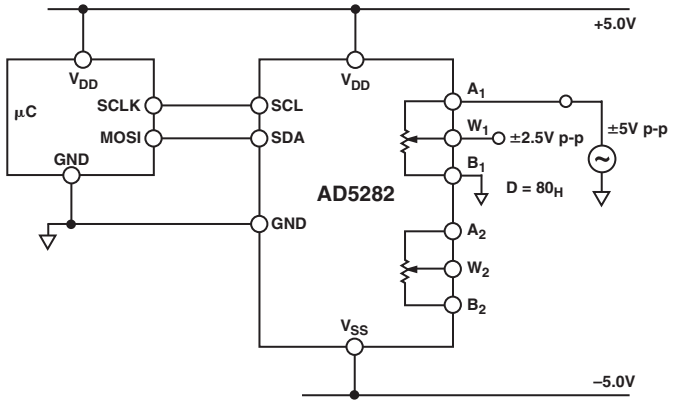


Figure 13. Bipolar Operation from Dual Supplies

Gain Control Compensation

The digital potentiometer is commonly used in gain control such as the noninverting gain amplifier shown in Figure 14.

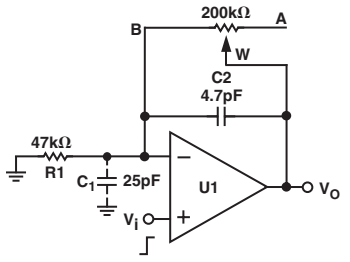


Figure 14. Typical Noninverting Gain Amplifier

Notice the RDAC B terminal parasitic capacitance is connected to the op amp noninverting node. It introduces a zero for the $1/\beta_o$ term with 20 dB/dec, whereas a typical op amp GBP has –20 dB/dec characteristics. A large R2 and finite C1 can cause this zero's frequency to fall well below the crossover frequency. Thus the rate of closure becomes 40 dB/dec and the system has 0° phase margin at the crossover frequency. The output may ring or oscillate if the input is a rectangular pulse or step function. Similarly, it is also likely to ring when switching between two gain values because this is equivalent to a step change at the input.

Depending on the op amp GBP, reducing the feedback resistor may extend the zero's frequency far enough to overcome the problem. A better approach is to include a compensation capacitor C2 to cancel the effect caused by C1. Optimum compensation occurs when R1 × C1 = R2 × C2. This is not an option because of the variation of R2. As a result, one may use the relationship above and scale C2 as if R2 is at its maximum value. Doing so may overcompensate and compromise the performance slightly when R2 is set at low values. However, it will avoid the gain peaking, ringing, or oscillation at the worst case. For critical applications, C2 should be found empirically to suit the need. In general, C2 in the range of a few pF to no more than a few tenths of pF is usually adequate for the compensation.

Similarly, there are W and A terminal capacitances connected to the output (not shown); fortunately their effect at this node is less significant and the compensation can be avoided in most cases.

Programmable Voltage Reference

For Voltage Divider Mode operation, Figure 15, it is common to buffer the output of the digital potentiometer unless the load is much larger than R_{WB}. Not only does the buffer serve the purpose of impedance conversion, it also allows a heavier load to be driven.

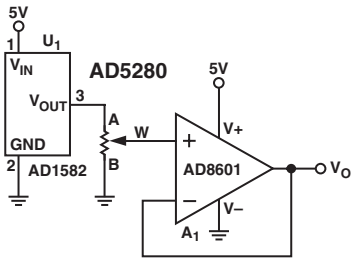


Figure 15. Programmable Voltage Reference

8-Bit Bipolar DAC

Figure 16 shows a low cost, 8-bit, bipolar DAC. It offers the same number of adjustable steps but not the precision as compared to the conventional DACs. The linearity and temperature coefficients, especially at low value codes, are skewed by the effects of the digital potentiometer wiper resistance. The output of this circuit is:

$$V_O = \left(\frac{2D}{256} - 1\right) \times V_{REF} \tag{5}$$

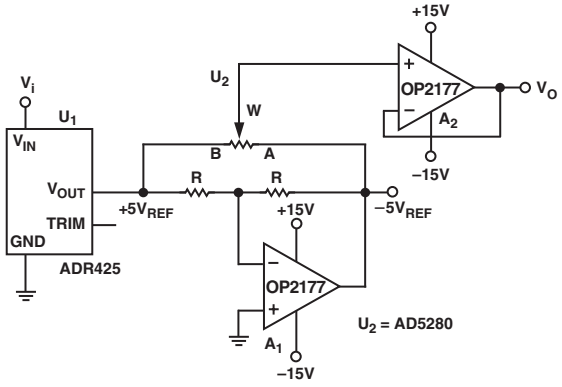


Figure 16. 8-Bit Bipolar DAC

Bipolar Programmable Gain Amplifier

For applications that require bipolar gain, Figure 17 shows one implementation similar to the previous circuit. The digital potentiometer, U_1, sets the adjustment range. The wiper voltage at W_2 can therefore be programmed between V_i and $-KV_i$ at a given U_2 setting. Configuring A_2 in the Noninverting Mode allows linear gain and attentuation. The transfer function is:

$$\frac{V_O}{V_i} = \left(1 + \frac{R2}{R1}\right) \times \left(\frac{D2}{256} \times (1 + K) - K\right) \tag{6}$$

where K is the ratio of R_{WB1}/R_{WA1} set by U_1.

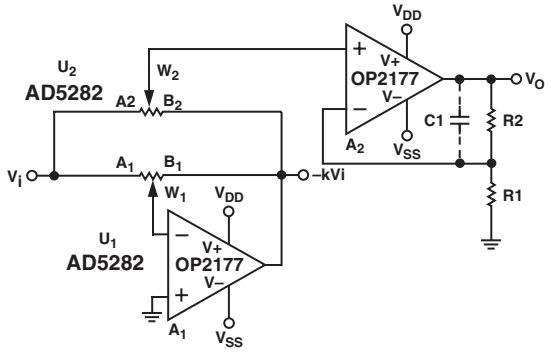


Figure 17. Bipolar Programmable Gain Amplifier

Similar to the previous example, in the simpler (and much more usual) case, where K = 1, a single digital potentiometer AD5280 is used and U_1 is replaced by a matched pair of resistors to apply V_i and $-V_i$ at the ends of the digital potentiometer. The relationship becomes:

$$V_O = \left(1 + \frac{R2}{R1}\right)\left(\frac{2D2}{256} - 1\right) \times V_i \tag{7}$$

If R2 is large, a few pF compensation capacitor may be needed to avoid any gain peaking.

Table III shows the result of adjusting D, with A2 configured as a unity gain, a gain of 2, and a gain of 10. The result is a bipolar amplifier with linearly programmable gain and 256-step resolution.

Table III. Result of Bipolar Gain Amplifier

D	R1 = ∞, R2 = 0	R1 = R2	R2 = 9R1
0	–1	–2	–10
64	–0.5	–1	–5
128	0	0	0
192	0.5	1	5
255	0.968	1.937	9.680

Programmable Voltage Source with Boosted Output
For applications that require high current adjustments such as a laser diode driver or tunable laser, a boosted voltage source can be considered (see Figure 18).

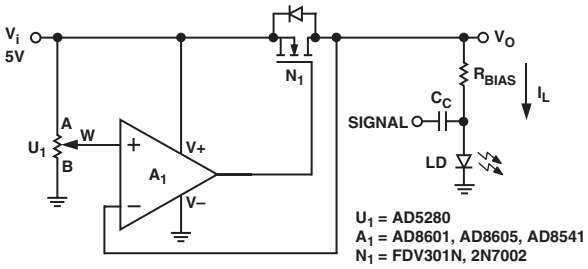


Figure 18. Programmable Booster Voltage Source

In this circuit, the inverting input of the op amp forces the V_{BIAS} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-Ch FET N1. N1's power handling must be adequate to dissipate $(V_i–V_O) \times I_L$ power. This circuit can source a maximum of 100 mA with a 5 V supply. A1 needs to be a rail-to-rail input type. Fore precision applications, a voltage reference such as ADR423, ADR292, or AD1584 can be applied at the input of the digital potentiometer.

Programmable 4 to 20 mA Current Source
A programmable 4 to 20 mA current source can be implemented with the circuit shown in Figure 19. REF191 is a unique, low supply headroom and high current handling precision reference that can deliver 20 mA at 2.048 V. The load current is simply the voltage across terminals B to W of the digital potentiometer divided by R_S:

$$I_L = \frac{V_{REF} \times D}{R_S \times 2^N} \quad (8)$$

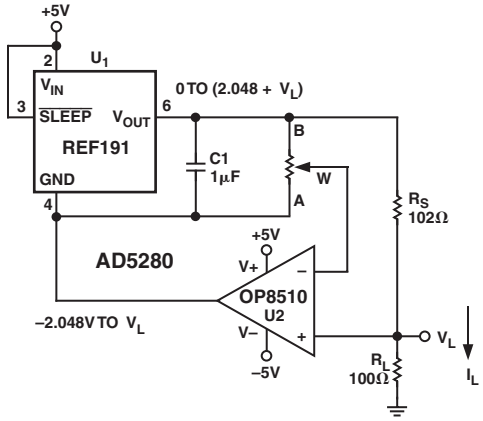


Figure 19. Programmable 4 to 20 mA Current Source

The circuit is simple, but beware of two things. First, dual supply op amps are ideal because the ground potential of REF191 can swing from –2.048 V at zero scale to V_L at full scale of the potentiometer setting. Although the circuit works under single supply, the programmable resolution of the system will be reduced.

For applications that demand higher current capabilities, a few changes to the circuit in Figure 19 will produce an adjustable current in the range of hundreds of mA. First, the voltage reference needs to be replaced with a high current, low dropout regulator, such as the ADP3333, and the op amp needs to be swapped with a high current dual-supply model, such as the AD8532. Depending on the desired range of current, an appropriate value for R_S must be calculated. Because of the high current flowing to the load, the user must pay attention to the load impedance so as not to drive the op amp beyond the positive rail.

Programmable Bidirectional Current Source
For applications that require bidirectional current control or higher voltage compliance, a Howland current pump can be a solution (see Figure 20). If the resistors are matched, the load current is:

$$I_L = \frac{\frac{(R2_A + R2_B)}{R1}}{R2_B} \times V_W \quad (9)$$

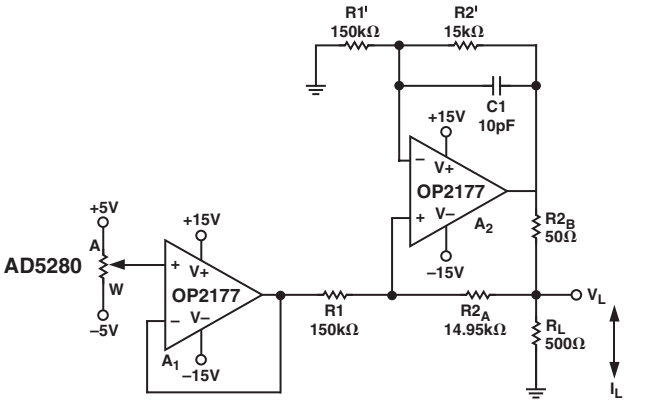


Figure 20. Programmable Bidirectional Current Source

$R2_B$ in theory can be made as small as needed to achieve the current needed within A_2's output current driving capability. In this circuit, OP2177 can deliver ±5 mA in either direction, and the voltage compliance approaches 15 V. It can be shown that the output impedance is:

$$Z_O = \frac{R1' \times R2_B(R1 + R2_A)}{R1 \times R2' - R1'(R2_A + R2_B)} \quad (10)$$

This output impedance can be infinite if resistors *R1*' and *R2*' match precisely with *R1* and $R2_A + R2_B$, respectively. On the other hand, it can be negative if the resistors are not matched. As a result, *C*1 in the range of 1 pF to 10 pF, is needed to prevent the oscillation.

Programmable Low-Pass Filter

In A/D conversion applications, it is common to include an antialiasing filter to band-limit the sampling signal. Dual-channel digital potentiometers can be used to construct a second order Sallen Key low-pass filter (see Figure 21). The design equations are:

$$\frac{V_O}{V_i} = \frac{\omega_o^{\,2}}{S^2 + \frac{\omega_o}{Q}S + \omega_o^{\,2}} \quad (11)$$

$$\omega_O = \sqrt{\frac{1}{R1R2C1C2}} \quad (12)$$

$$Q = \frac{1}{R1C1} + \frac{1}{R2C2} \quad (13)$$

Users can first select some convenient values for the capacitors. To achieve maximally flat bandwidth where Q = 0.707, let *C1* be twice the size of *C2* and let *R1* = *R2*. As a result, the user can adjust *R1* and *R2* to the same settings to achieve the desirable bandwidth.

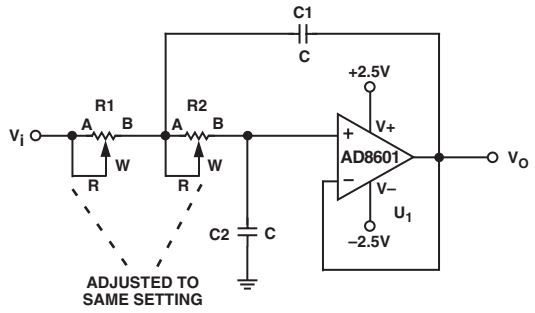


Figure 21. Sallen Key Low-Pass Filter

PROGRAMMABLE OSCILLATOR

In a classic Wien-bridge oscillator (Figure 22), the Wien network (R, R', C, C') provides positive feedback, while R1 and R2 provide negative feedback. At the resonant frequency, *fo*, the overall phase shift is zero, and the positive feedback causes the circuit to oscillate. With R = R', C = C', and $R2 = R2_A//(R2_B + R_{diode})$, the oscillation frequency is:

$$\omega_O = \frac{1}{RC} \quad or \quad f_O = \frac{1}{2\pi RC} \quad (14)$$

where *R* is equal R_{WA} such that:

$$R = \frac{256 - D}{256}R_{AB} \quad (15)$$

At resonance, setting:

$$\frac{R2}{R1} = 2 \quad (16)$$

balances the bridge. In practice, *R2*/*R1* should be set slightly larger than 2 to ensure the oscillation can start. On the other hand, the alternate turn-on of the diodes *D1* and *D2* ensures that *R2*/*R1* are smaller than 2 momentarily, and therefore stabilizes the oscillation.

Once the frequency is set, the oscillation amplitude can be tuned by $R2_B$ since:

$$\frac{2}{3}V_O = I_D R2_B + V_D \quad (17)$$

V_0, I_D, and V_D are interdependent variables. With proper selection of $R2_B$, an equilibrium will be reached such that V_O converges. $R2_B$ can be in series with a discrete resistor to increase the amplitude, but the total resistance cannot be too large to prevent saturation of the output.

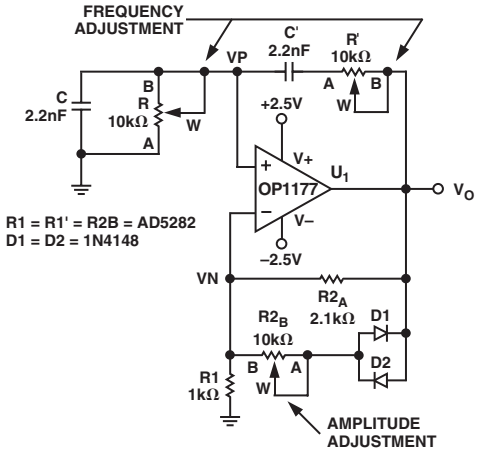


Figure 22. Programmable Oscillator with Amplitude Control

Resistance Scaling

AD5280/AD5282 offers 20 kΩ, 50 kΩ, and 200 kΩ nominal resistance. Users who need a lower resistance and the same number of step adjustments can place multiple devices in parallel. For example, Figure 23 shows a simple scheme of paralleling both channels of the AD5282. To adjust half of the resistance linearly per step, users need to program both channels to the same settings.

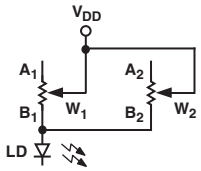


Figure 23. Reduce Resistance by Half with Linear Adjustment Characteristics

Applicable only to the Voltage Divider Mode, by paralleling a discrete resistor as shown in Figure 24, a proportionately lower voltage appears at terminal A. This translates into a finer degree of precision because the step size at terminal W will be smaller. The voltage can be found as:

$$V_W(D) = \frac{D}{256} \times \left(\frac{V_{DD}}{R3 + R_{AB} \,//\, R2} \right) \times (R_{AB} \,//\, R2) \quad (18)$$

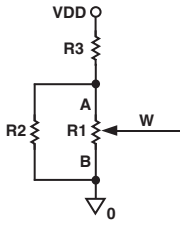


Figure 24. Lowering the Nominal Resistance

Figures 23 and 24 show that the digital potentiometers change steps linearly. On the other hand, log taper adjustment is usually preferred in applications like volume control. Figure 25 shows another way of resistance scaling. In this circuit, the smaller the R2 with respect to R_{AB}, the more the pseudo log taper characteristic behaves.

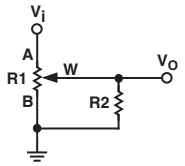


Figure 25. Resistor Scaling with Log Adjustment Characteristics

RDAC CIRCUIT SIMULATION MODEL

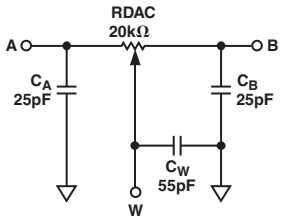


Figure 26. RDAC Circuit Simulation Model for RDAC = 20 kΩ

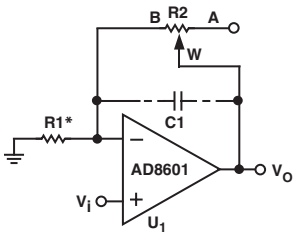
The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the RDACs. Configured as a potentiometer divider, the –3 dB bandwidth of the AD5280 (20 kΩ resistor) measures 310 kHz at half scale. TPC 19 provides the large signal BODE plot characteristics of the three available resistor versions—20 kΩ, 50 kΩ, and 200 kΩ. A parasitic simulation model is shown in Figure 26. A macro model net list for the 20 kΩ RDAC is provided.

Macro Model Net List for RDAC

```
.PARAM D=256, RDAC=20E3
*
.SUBCKT DPOT (A,W,B)
*
CA      A       0       25E-12
RWA     A       W       {(1-D/256)*RDAC+60}
CW      W       0       55E-12
RWB     W       B       {D/256*RDAC+60}
CB      B       0       25E-12
*
.ENDS DPOT
```

Resistance Tolerance, Drift, and Temperature Coefficient Mismatch Considerations

In a Rheostat Mode operation such as gain control, Figure 27, the tolerance mismatch between the digital potentiometer and the discrete resistor can cause repeatability issues among various systems. Because of the inherent matching of the silicon process, it is practical to apply the dual-channel device in this type of application. As such, R1 should be replaced by one of the channels of the digital potentiometer. R1 should be programmed to a specific value while R2 can be used for the adjustable gain. Although it adds cost, this approach minimizes the tolerance and temperature coefficient mismatch between R1 and R2. In addition, this approach also tracks the resistance drift over time. As a result, these nonideal parameters become less sensitive to the system variations.



*REPLACED WITH ANOTHER CHANNEL OF RDAC

Figure 27. Linear Gain Control with Tracking Resistance Tolerance and Drift

Notice the circuit in Figure 28 can also be used to track the tolerance, temperature coefficient, and drift in this particular application. However, the characteristics of the transfer function change from a linear to pseudo-logarithmic gain function.

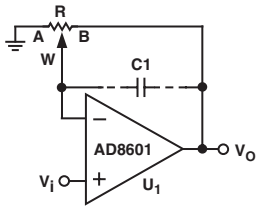
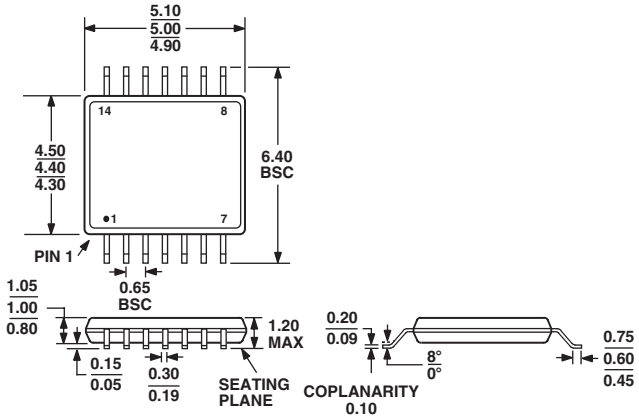


Figure 28. Nonlinear Gain Control with Tracking Resistance Tolerance and Drift

OUTLINE DIMENSIONS

14-Lead Thin Shrink Small Outline Package (TSSOP)
(RU-14)

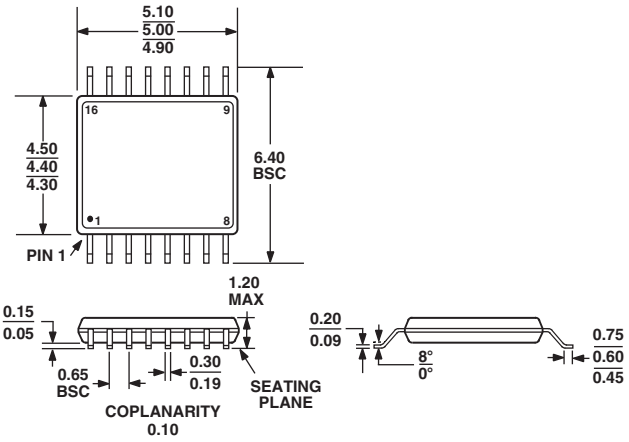
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AB-1

16-Lead Thin Shrink Small Outline Package (TSSOP)
(RU-16)

Dimensions shown in millimeters



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