

DUAL "D" - TYPE FLIP-FLOP

GENERAL DESCRIPTION

The MMC 4013 is a monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package.

The MMP 4013 consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and \bar{Q} outputs. These devices can be used for shift register applications, and, by connecting Q output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

FEATURES

- set-reset capability
- static flip-flop operation — retains state indefinitely with clock level either "high" or "low"
- medium-speed operation — 16 MHz (typ.) clock toggle rate at 10 V
- quiescent current specified to 20 V
- maximum input leakage of 1 μ A at 18 V (full package temperature range)
- standardized symmetrical output characteristics
- 5 V, 10 V, and 15 V parametric ratings

ABSOLUTE MAXIMUM RATINGS

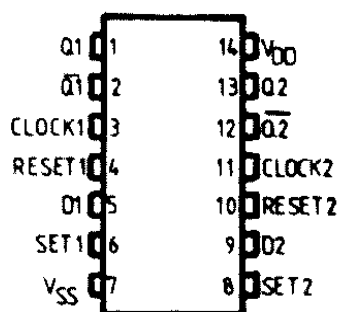
V_{DD}^*	Supply voltage: G and H types E and F types	-0.5 to -0.5 to -0.5 to	20 18 $V_{DD} + 0.5$	V V V
V_i	Input voltage			
I_i	DC input current (any one input)		± 10	mA
P_{tot}	Total power dissipation (per package) Dissipation per output transistor for T_A = full package-temperature range		200	mW
T_A	Operating temperature: G and H types E and F types	-55 to -40 to -65 to	125 85 150	$^{\circ}$ C $^{\circ}$ C $^{\circ}$ C
T_{stg}	Storage temperature			

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

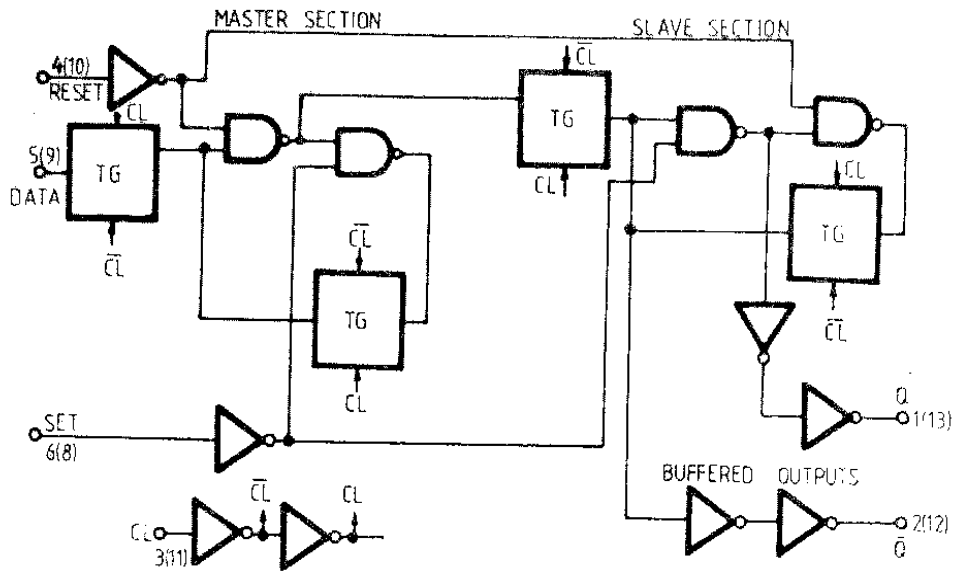
V_{DD}^*	Supply voltage: G and H types E and F types	3 to 3 to 0 to	18 15 V_{DD}	V V V
V_i	Input voltage			
T_A	Operating temperature: G and H types E and F types	-55 to -40 to	125 85	$^{\circ}$ C $^{\circ}$ C

CONNECTION DIAGRAM



LOGIC DIAGRAM

(one of two identical flip-flops)



N(N) = FF1/FF2 TERMINAL ASSIGNMENT

TRUTH TABLE

CL ●	D	R	S	Q	\bar{Q}
	0	0	0	0	1
	1	0	0	1	0
	X	0	0	Q	\bar{Q}
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

NO CHANGE

LOGIC 0 = LOW ● = LEVEL CHANGE
 LOGIC 1 = HIGH X = DON'T CARE

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES						UNIT		
		V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	T _{LOW}		25°C			T _{HIGH}			
						min.	max.	min.	typ	max.	min.		max.	
I _L	Quiescent current	G, H types	0/ 5			5		1	0.02	1		30	μ A	
			0/10			10		2	0.02	2		60		
			0/15			15		4	0.02	4		120		
			0/20			20		20	0.04	20		600		
		E, F types	0/ 5			5		4	0.02	4		30		
			0/10			10		8	0.02	8		60		
			0/15			15		16	0.02	16		120		
V _{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95		4.95		V	
			0/10		< 1	10	9.95		9.95		9.95			
			0/15		< 1	15	14.95		14.95		14.95			
V _{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		V	
			10/0		< 1	10		0.05			0.05			
			15/0		< 1	15		0.05			0.05			
V _{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5		3.5		V	
				1/9	< 1	10	7		7		7			
				1.5/13.5	< 1	15	11		11		11			
V _{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		V	
				9/1	< 1	10		3			3			
				13.5/1.5	< 1	15		4			4			
I _{OH}	Output drive current	G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15	mA	
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		E, F types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I _{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36	mA	
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I _{IH} , I _{IL}	Input leakage current	G, H types	0/18	Any input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μ A
		E, F types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
C _I	Input capacitance			Any input						5	7.5		p	

* T_{LOW} = -55°C for G, H devices; -40°C for E, F devices.* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V2 V min. with V_{DD} = 10 V2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ kohm}$, typical temperature coefficient for all $V_{DD} = 0.3\%/^\circ\text{C}$ values, all input rise and fall time = 20 ns)

PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES			UNIT
		min.	typ.	max.	
t_{PLH} , t_{PHL} Propagation delay time (clock to \bar{Q} or Q outputs)	5		150	300	ns
	10		65	130	
	15		45	90	
t_{PLH} , Propagation delay time (Set to Q or Reset to \bar{Q})	5		150	300	ns
	10		65	130	
	15		45	90	
t_{PHL} , Propagation delay time (Set to \bar{Q} or Reset to Q)	5		200	400	ns
	10		85	170	
	15		60	120	
t_{FLH} , t_{THL} Transition time	5		100	200	ns
	10		50	100	
	15		40	80	
f_{CL} ● Maximum clock frequency	5	3.5	7		MHz
	10	8	16		
	15	12	24		
t_W Clock pulse width	5	140	70		ns
	10	60	30		
	15	40	20		
t_r , t_f ●● Clock input rise or fall time	5			15	μs
	10			4	
	15			1	
t_W Set or reset pulse width	5	180	90		ns
	10	80	40		
	15	50	25		
t_{setup} Data setup time	5	40	20		ns
	10	20	10		
	15	15	7		

● Input t_r , $t_f = 5\text{ ns}$

●● If more than one unit is cascaded in a parallel clocked operation, t_r should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.