FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-20884-2E

FLASH MEMORY

CMOS

32M (4M × 8) BIT NAND-type

MBM30LV0032

■ DESCRIPTION

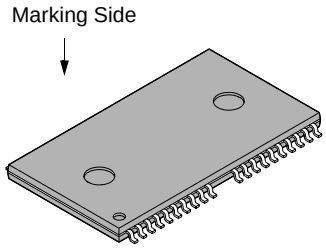
The MBM30LV0032 device is a single 3.3 V 4M × 8 bit NAND flash memory organized as 528 byte × 16 pages × 512 blocks. Each 528 byte page contains 16 bytes of optionally selected spare area which may be used to store ECC code(Specifications indicated are on condition that ECC system would be combined.). Program and read data is transferred between the memory array and page register in 528 byte increments. A 528 byte page can be programmed in 200 µs and an 8K byte block can be erased in 2 ms under typical conditions. An internal controller automates all program and erase operations including the verification of data margins. Data within a page can be read with a 50 ns cycle time per byte. The I/O pins are utilized for both address and data input/output as well as command inputs. The MBM30LV0032 is an ideal solution for applications requiring mass non-volatile storage such as solid state file storage, digital recording, image file memory for still cameras, and other uses which require high density and non-volatile storage.

■ PRODUCT LINE UP

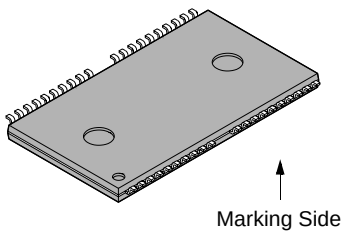
Part No.		MBM30LV0032
Operating Temperature		–40°C to +85°C
V_{CC}		+2.7 V to +3.6 V
Power Dissipation (Max.)	Read	72 mW
	Erase / Program	72 mW
	TTL Standby	3.6 mW
	CMOS Standby	0.18 mW

■ PACKAGES

44-pin plastic TSOP (II)



(FPT-44P-M07)
(Normal Bend)



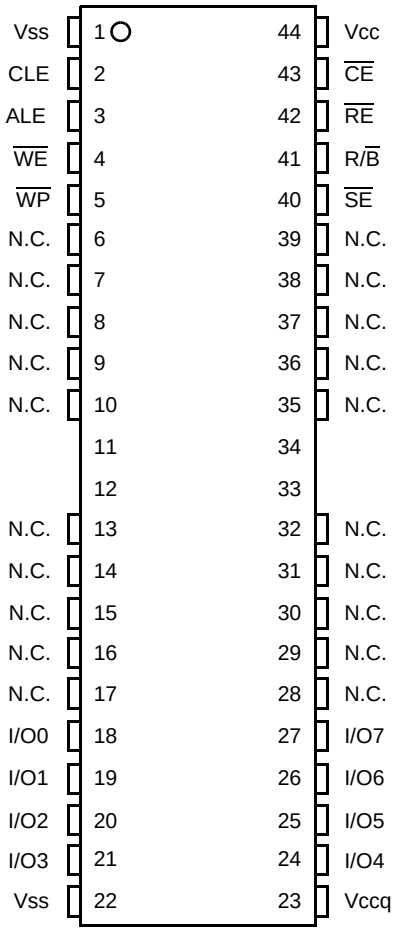
(FPT-44P-M08)
(Reverse Bend)

■ FEATURES

- **3.3 V-only operating voltage (2.7 V to 3.6 V)**
  Minimizes system level power requirements
- **Organization**
  Memory Cell Array : (4M + 128K) ×8 bit
  Data Register : (512 + 16) ×8 bit
- **Automatic Program and Erase**
  Page Program : (512 + 16) Byte
  Block Erase : (8K + 256) Byte
- **528 Byte Page Read Operation**
  Random Access : 7 µs (Max.)
  Serial Access : 35 ns (Max.)
- **Fast Program and Erase**
  Program Time : 200 µs (Typ.) / page
  Block Erase Time : 2 ms (Typ.) / block
- **Command/Address/Data Multiplexed I/O Port**
- **Hardware Data Protection**
- **1,000,000 write/erase cycle guaranteed (ECC system required)**
- **Command Register Operation**
- **Package**
  44(40)-pin TSOP Type II (0.8 mm pitch)
  Normal/Reverse Type
- **Data Retention: 10 years**

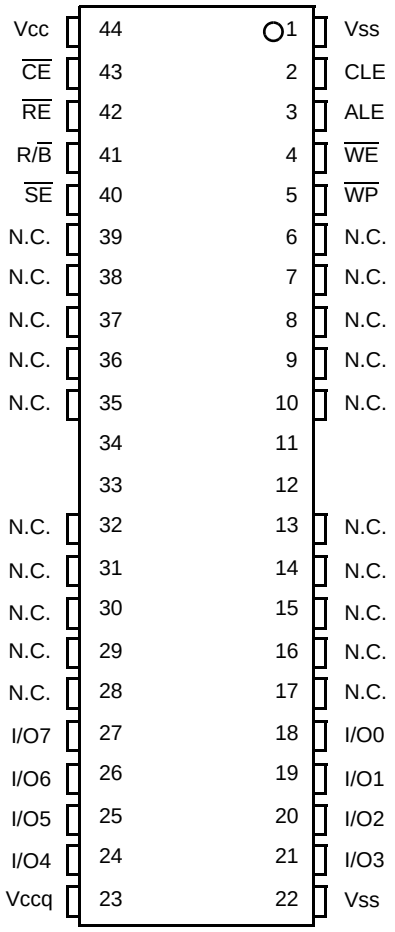
■ PIN ASSIGNMENTS

TOP VIEW



FPT-44P-M07

TOP VIEW

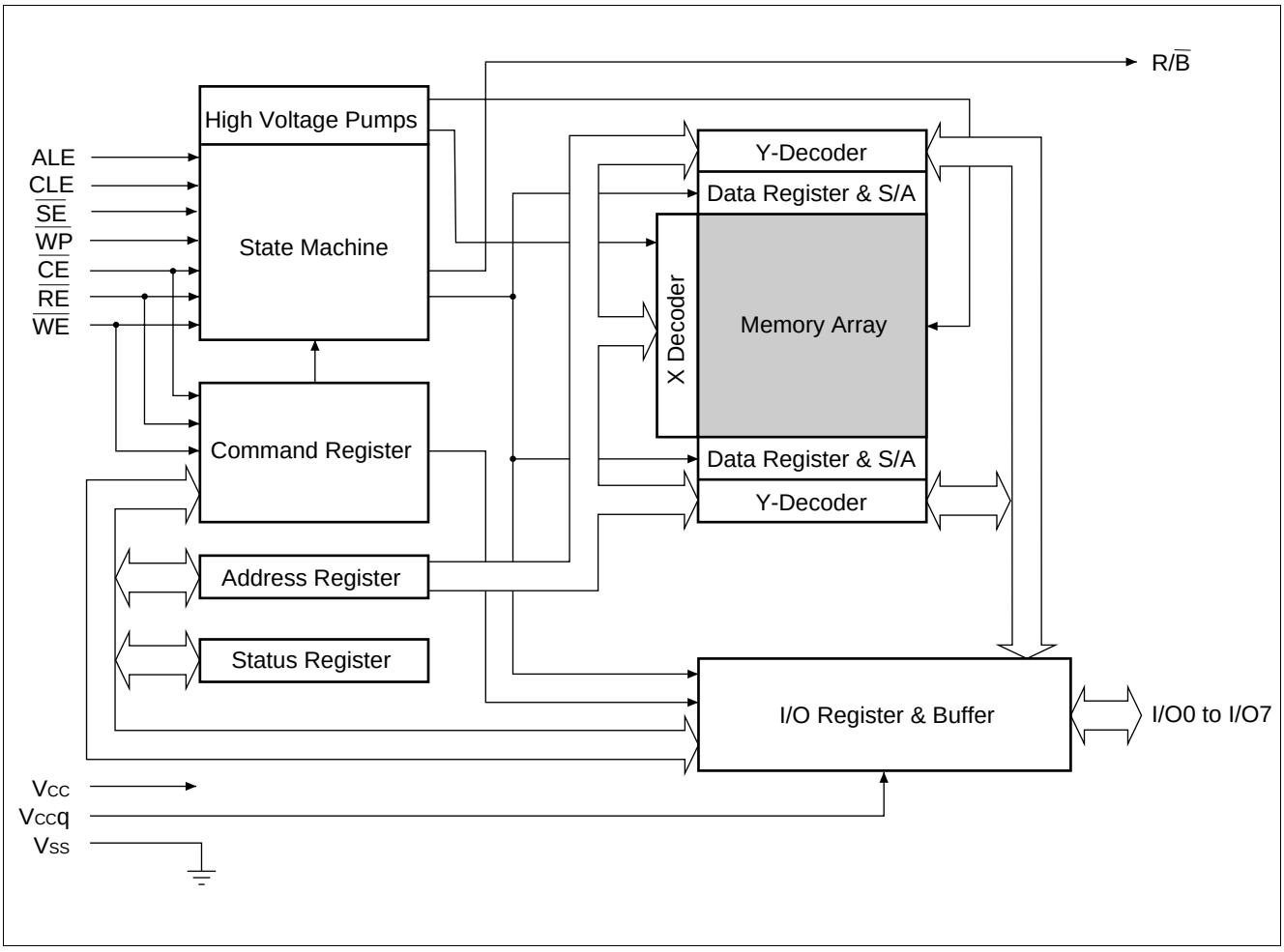


FPT-44P-M08

■ PIN DESCRIOTIONS

Pin Number	Pin Name	Descriptions
18 to 21 24 to 27	I/O0 to I/O7	Data Input/Output The I/O ports are used for transferring command, address, and input/output data into and out of the device. The I/O pins will be high impedance when the outputs are disabled or the device is not selected.
2	CLE	Command Latch Enable The CLE signal enables the acquisition of the made command into the internal command register. When CLE="H", command are latched into the command register from the I/O port upon the rising edge of the $\overline{WE}$ signal.
3	ALE	Address Latch Enable The ALE signal enables the acquisition of either address or data into the internal address/data register. The rising edge of $\overline{WE}$ latch in addresses when ALE is high and data when ALE is low.
43	$\overline{CE}$	Chip Enable The $\overline{CE}$ signal is used to select the device. When $\overline{CE}$ is high, the device enters a low power standby mode. If $\overline{CE}$ transitions high during a read operation, the standby mode will be entered. However, the $\overline{CE}$ signal is ignored if the device is in a busy state(R/$\overline{B}$=L) during a program or erase operation.
42	$\overline{RE}$	Read Enable The $\overline{RE}$ signal controls the serial data output. The falling edge of $\overline{RE}$ drives the data onto the I/O bus and increments the column address counter by one.
4	$\overline{WE}$	Write Enable The $\overline{WE}$ signal controls writes from the I/O port. Data, address, and commands on the I/O port are latched upon the rising of the $\overline{WE}$ pulse.
5	$\overline{WP}$	Write Protect The $\overline{WP}$ signal protects the device against accidental erasure or programming during power up/down by disabling the internal high voltage generators. $\overline{WP}$ should be kept low when the device powers up until V_{CC} is above 2.5 V. During power down, $\overline{WP}$ should be low when V_{CC} falls below 2.5 V.
40	$\overline{SE}$	Spare Area Enable The $\overline{SE}$ input enables the spare area during sequential data input, page program, and Read 1.
41	R/$\overline{B}$	Ready Busy Output The R/$\overline{B}$ output signal is used to indicate the operating status of the device. During program, erase, or read, R/$\overline{B}$ is low and will return high upon the completion of the operation. The output buffer for this signal is an open drain.
23	V_{CC}q	Output Buffer Power Supply The VCCq input supplies the power to the I/O interface logic. This power line is electrically isolated from V_{CC} for the purpose of supporting 5V tolerant I/O.
44	V_{CC}	Power Supply
1,22	V_{SS}	Ground
6 to 17 28 to 39	N.C.	No Connection

■ BLOCK DIAGRAM



■ SCHEMATIC CELL LAYOUT AND ADDRESS ASSIGNMENT

The Program operation is implemented in page units while the Erase operation is carried out in block units.

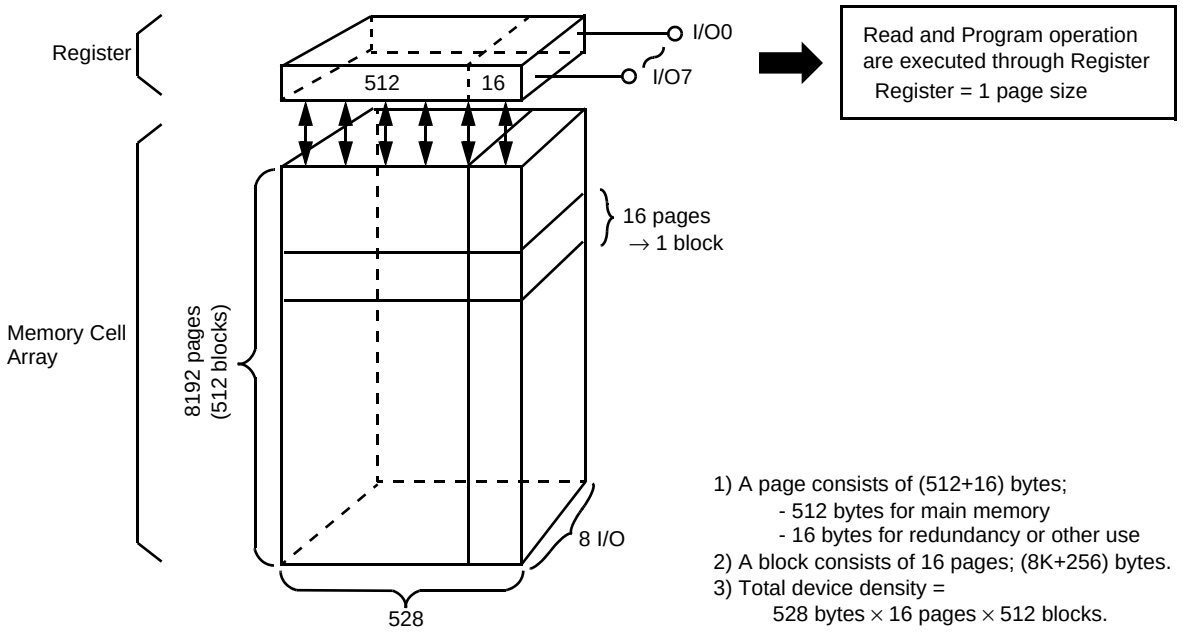


Figure 1 Schematic Cell Layout

Table 1 Addressing

	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
First Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
Second Cycle	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}
Third Cycle	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}	X*	X*	X*

A_0 to A_7 : column address

A_9 to A_{21} : page address { A_{13} to A_{21} : block address
A_9 to A_{12} : Page address in block

(A_8 is automatically set to “Low” or “High” by the “00h” command or the “01h” command in device inside.)

* : X = V_{IH} or V_{IL}

■ DEVICE BUS OPERATIONS

Table 2 Operation Table *1

Mode		CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{SE}$	$\overline{WP}$
Read Mode	Command Input	H	L	L	↑	H	X *4	X
	Address Input (3 clock)	L	H	L	↑	H	X *4	X
During Read (Busy)		L	L	L	H	H	L/H *3	X
Sequential Read & Data Output		L	L	L	H	↓	L/H *3	X
Program/ Erase Mode	Command Input	H	L	L	↑	H	X *4	H
	Address Input (2 or 3 clock)	L	H	L	↑	H	X *4	H
Data Input		L	L	L	↑	H	L/H *3	H
During Program (Busy)		X	X	X	X	X	L/H *3	H
During Erase (Busy)		X	X	X	X	X	X	H
Write Protect		X	X	X	X	X	X	L
Stand-by		X	X	H	X	X	0 V/V_{CC} *2	0 V/V_{CC} *2

*1: H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}

*2: $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

*3: When $\overline{SE}$ is high, spare area is deselected.

*4: If 50h command is input and read/program operation is executed only for spare area, $\overline{SE}$ must be low at the command/address input.

Table 3 Read Mode Operation Status *

Operation	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O0 to I/O7	Power
Output Select	L	L	L	H	L	Data Output	Active
Output Deselect	L	L	L	H	H	High Impedance	Active
Standby	X	X	H	X	X	High Impedance	Standby

*: H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}

■ COMMAND OPERATION

Table 4 Command Table

Function	1st Cycle	2nd Cycle	Acceptable Command During Busy State
Read (1)	00h *1	—	
Read (2)	01h *2	—	
Read (3)	50h *3	—	
Sequential Data Input	80h	—	
Page Program	10h	—	
Block Erase	60h	D0h	
Reset	FFh	—	○
Status Read	70h	—	○
ID Read	90h	—	

*1: The 00h Command defines starting Address on the 1st half Page.

*2: The 01h Command defines starting Address on the 2nd half Page.

*3: The 50h Command is valid only When $\overline{SE}$ is low level.

■ FUNCTIONAL DESCRIPTION

READ MODE

There are three distinct commands used for the read operation: 00h, 01h, and 50h. After the command cycle, three address cycles are used to input the starting address. Upon the rising edge of the final $\overline{WE}$ pulse, there is a 7 µs latency in which the 528 byte page is transferred to the data register. The R/$\overline{B}$ signal may be used to monitor the completion of the data transfer. In the read operation, the $\overline{CE}$ signal must stay “Low” after the third address input and during Busy state. If the $\overline{CE}$ signal goes High during this period, the read operation will be terminated and then the standby mode will be entered. Once the page of data has been loaded into the data register, it may be clocked out with consecutive 50 ns $\overline{RE}$ pulses. Each $\overline{RE}$ pulse will automatically advance the column address by one. Once the last column has been read, the page address will automatically increment by one and the data register will be updated with the new page after 7 µs.

The 00h Read command will set the pointer to the first half page of the array while the 01h Read command will set it in the second half. It may be logical to think of 00h as a command which sets $A_8 = 0$ while 01h sets $A_8 = 1$. The 50h command set the pointer to the spare area, consisting of columns 512 to 527. During this read mode, A_3 to A_0 is used to set the starting address of the spare area. As with the 00h and 01h operations, once the spare area page is loaded into the data register, it may be read out by $\overline{RE}$ pulses. Each $\overline{RE}$ pulse will increment the column address until the final column (527) is reached. At this time, the pointer will be reset to column 512 while the page address is incriminated and the data register is updated. The 00h or 01h command is required to move the pointer back into the main array area.

Read (1), (2): 00h/01h

The Read (1), (2) mode is invoked by latching the 00h or 01h command into the command register. This mode (00h) will be automatically selected when the device powers up.

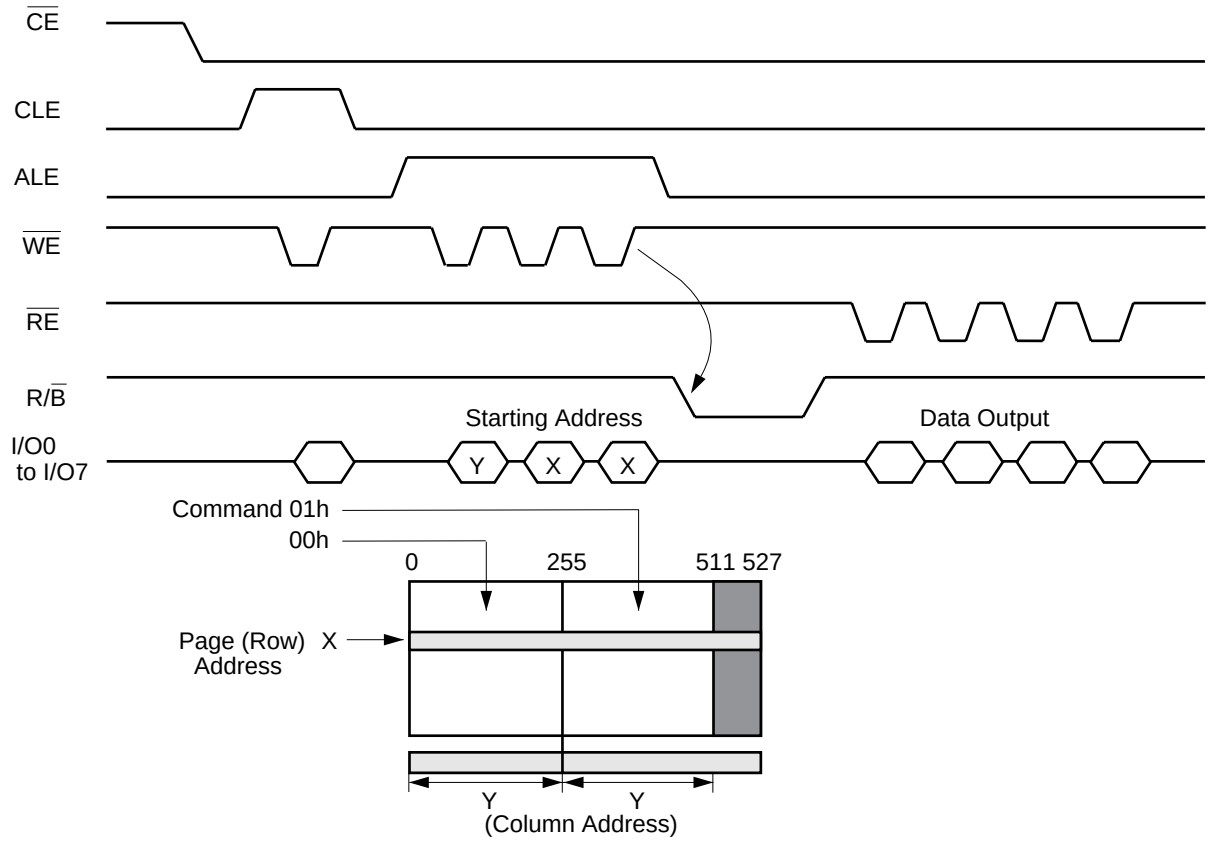


Figure 2 Read Mode (1), (2) Operation

Read (3): 50h

The Read (3) mode has identical timing to that of Read (1) and (2). However, while Read (1) and (2) are used to access the array, Read (3) is used to access the 16 byte spare area. When the 50h command is executed, the pointer will be set to an address space between columns 512 and 527. The values of Y will complete the address decoding. During this operation, only address bits A_3 to A_0 are used to determine the starting column address; A_7 to A_4 are ignored. A_{21} to A_9 are used to determine the starting row address.

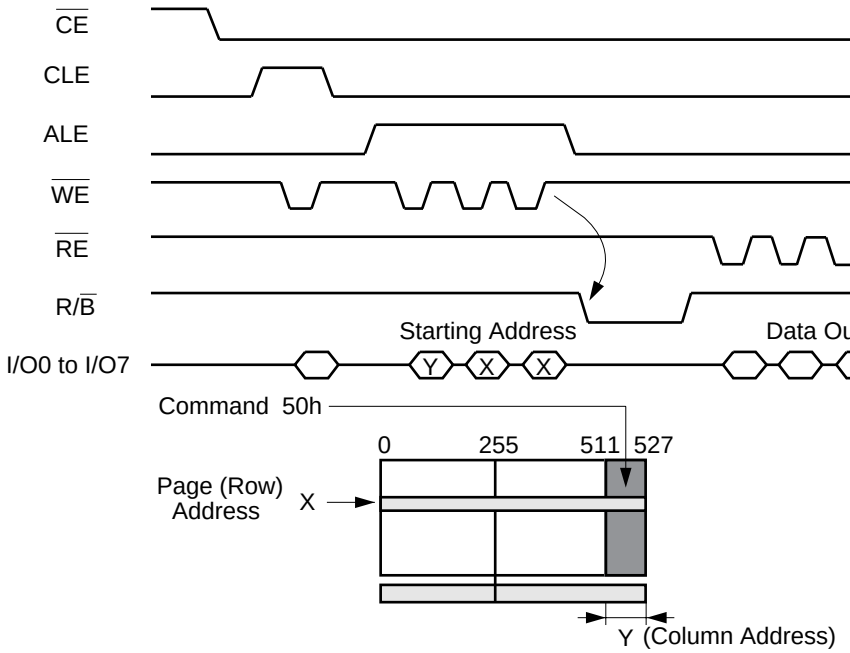


Figure 3 Read Mode (3) Operation

Sequential Read

Each $\overline{RE}$ pulse used to output data from the data register will cause the column address pointer to increment by one. When the final column has been reached, the next page will be automatically loaded into the data register. The R/$\overline{B}$ signal may be used to monitor the completion of the data transfer.

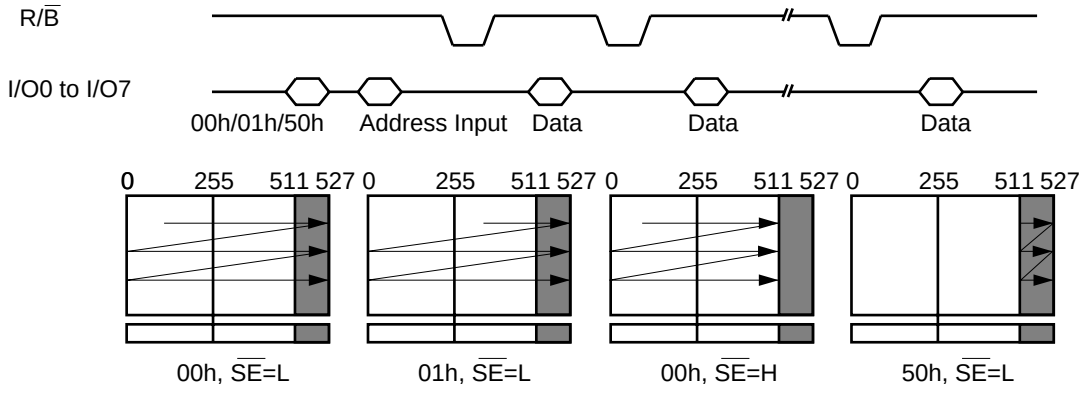


Figure 4 Sequential Read

Page Program: 80h, 10h

The device is programmed either by the page or partial page. Programming is done by issuing the 80h command followed by three address cycles then serial data input. The 80h command may be preceded by either 00h, 01h or 50h to set the pointer to either the first half page, second half page, or spare area respectively. If the pointer command is not specifically issued, its location is determined by its previous use (see Application Note (2)). After the serial data input, any column address which did not receive new data will not be programmed. This enables a page to be partially programmed. After the data has been entered, the 10h command will initiate the embedded programming process. If the 10h command is issued without loading any new data, programming will not be initiated. A given page may not be partially programmed more than ten consecutive times without an intervening erase operation. During the programming cycle, the R/$\overline{B}$ pin or Status Register bit I/O6 may be used to monitor the completion of the programming cycle. Only the Reset and Read Status commands are valid while programming is in progress. After programming, the Status Register bit I/O0 should be checked to verify whether the procedure was successful or not.

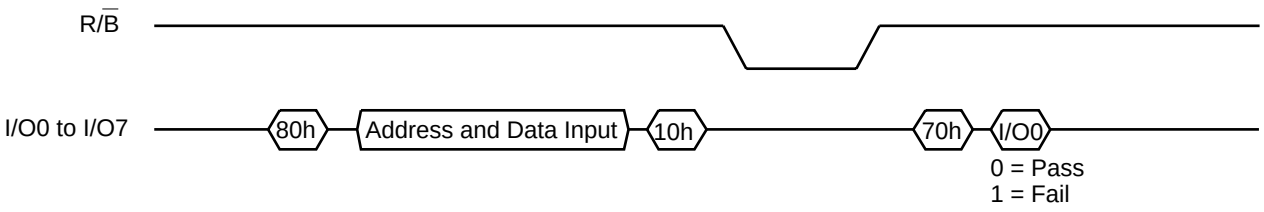


Figure 5 Page Program

Block Erase: 60h

The device data is erased in a block consisting of sixteen pages. The erase operation begins with the 60h command followed by two address cycles in which the block to be erased is entered. While the two address cycles require A_{21} to A_9 to be entered, A_{12} to A_9 are don't care bits. Once the block address is successfully loaded, the D0h command is entered to initiate the erase operation. The R/$\overline{B}$ signal may be used to monitor the completion of the cycle. Upon completion, the Status Register bit I/O0 should be used to verify a successful erase.

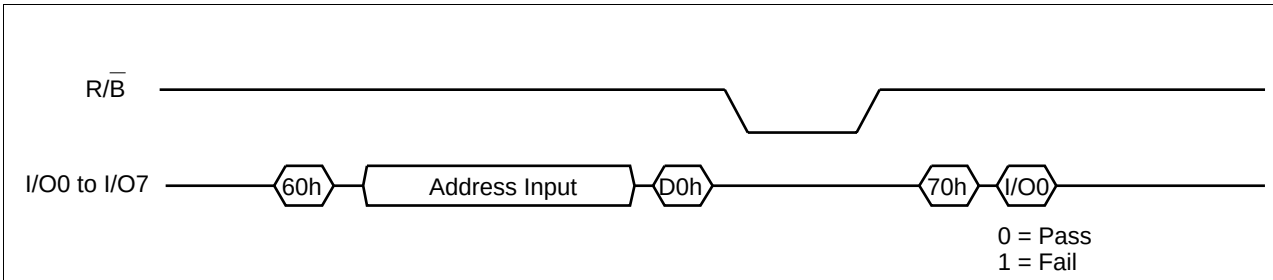


Figure 6 Block Erase

Read ID: 90h

This mode allows the identification of the manufacturer and product. After the 90h command cycle, one address cycle follows in which 00h is entered. The next two $\overline{RE}$ pulses will output the manufacturer and device code respectively.

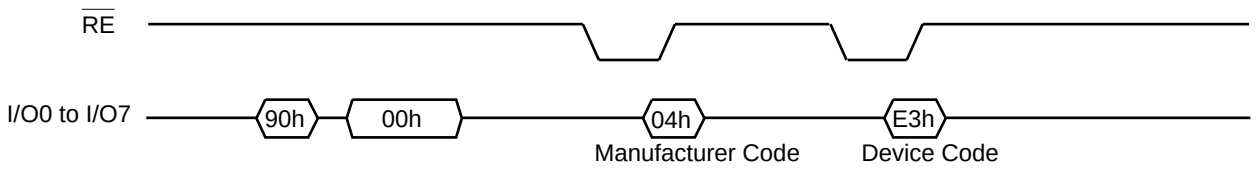


Figure 7 Read ID Operation

Table 5 Code Table

	I/O7	I/O 6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Code
Manufacturer	0	0	0	0	0	1	0	0	04h
Device	1	1	1	0	0	0	1	1	E3h

Status Read: 70h

The Status Register may be used to determine if the device is ready, in the write protect mode, or passed program/erase operations. After the 70h command is entered, the more recent falling edge of either $\overline{CE}$ or $\overline{RE}$ will output the contents of the status register to I/O0 to 7. The status register is continually updated and does not require either $\overline{CE}$ or $\overline{RE}$ to be toggled. By utilizing the $\overline{CE}$ pin, multiple devices with R/$\overline{B}$ pins wired together may be polled to determine their specific status.

Table 6 Status Output Table

	Status	Description
I/O0	Program/Erase	0 = Pass; 1 = Fail
I/O1	Not Used	
I/O2	Not Used	
I/O3	Not Used	
I/O4	Not Used	
I/O5	Not Used	
I/O6	Ready/Busy	0 = Busy; 1 = Ready
I/O7	Write Protect	0 = Protected; 1 = Unprotected

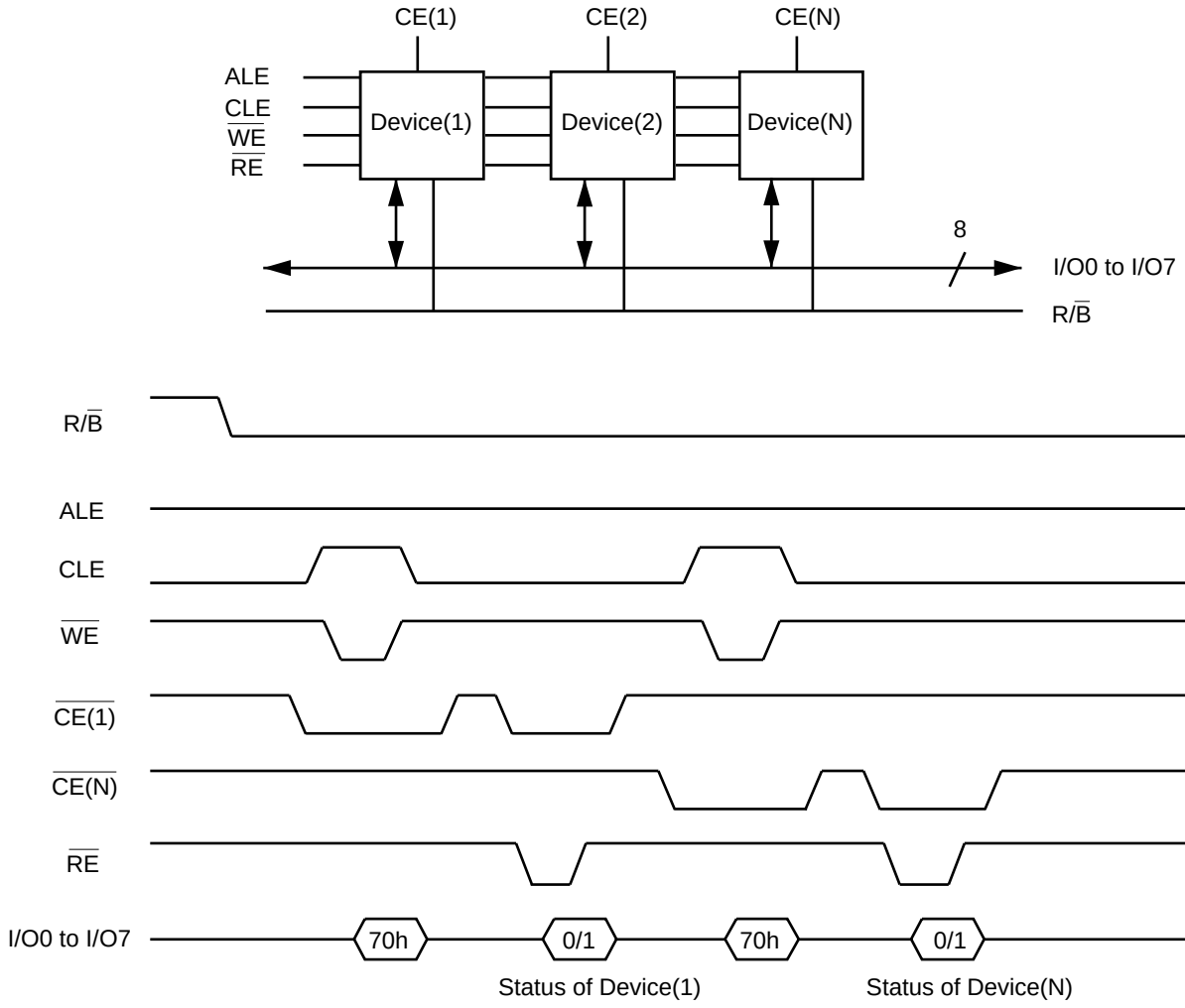
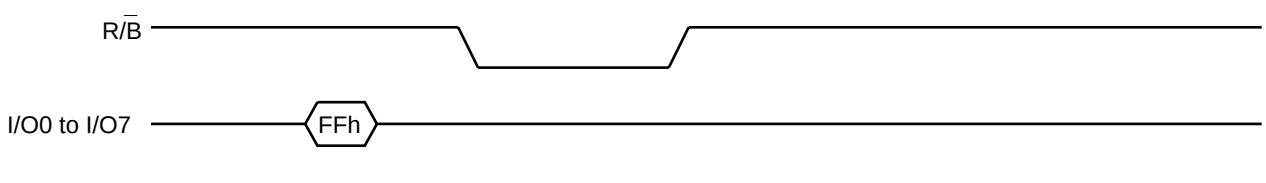


Figure 8 Status Read

Reset

When the device is busy during program, erase, or read, it can be reset by entering the command FFh. If $\overline{WP}$ = 1, the Status Register will be set to C0h. If a reset command is issued while the device is in the reset state, the command will be ignored. If the device is reset during the program or erase operations, the internal high voltages will be discharged before R/$\overline{B}$ goes high.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Ambient Temperature with Power Applied	T_A	–40	+85	°C
Storage Temperature	Tstg	–55	+125	°C
Voltage on a I/O pin with respect to Ground *	$V_{I/O}$	–0.6	$V_{CC}q$ +0.5	V
Voltage on a pin except I/O with respect to Ground *	V_{IN}	–0.6	V_{CC} +0.5	V
Power Supply Voltage	V_{CC}	–0.6	+5.5	V
	$V_{CC}q$	–0.6	+6.0	

*: Minimum DC voltage on input or I/O pins is –0.5V. During voltage transitions, inputs may undershoot Vss to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input pins is V_{CC} + 0.5 V and on I/O pins are $V_{CC}q$ + 0.5 V. During voltage transitions,input pins may overshoot to V_{CC} + 2.0 V for periods of up to 20ns and I/O pins may overshoot to $V_{CC}q$ + 2.0 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min.	Max.	
Supply Voltages	V_{CC}	+2.7	+3.6	V
Supply Voltages	$V_{CC}q$ *	+2.7	+5.5	V
Voltages	V_{SS}	0		V
Ambient Temperature	T_A	–40	+85	°C

*: $V_{CC}q$ = 5.0 V ± 10% can be guaranteed on $V_{CC} \geq$ 3.0 V.

Note: Operating ranges define those limits between which the functionality of the device is quaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Sequential Read Current	I_{CC1}	t_{CYCLE} = 50 ns, $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA	—	10	20	mA
Command Address Input Current	I_{CC3}	t_{CYCLE} = 50 ns, $\overline{CE}$ = V_{IL}	—	10	20	mA
Data Input Current	I_{CC4}	—	—	10	20	mA
Program Current	I_{CC6}	—	—	10	20	mA
Erase Current	I_{CC7}	—	—	10	20	mA
Stand-by Current (TTL)	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{WP}$ = $\overline{SE}$ = 0 V/V_{CC}	—	—	1	mA
Stand-by Current (CMOS)	I_{SB2}	$\overline{CE}$ = V_{CC} –0.2 V, $\overline{WP}$ = $\overline{SE}$ = 0 V/ V_{CC}	—	10	50	µA
Input Leakage Current	I_{LI}	V_{IN} = 0 to 3.6 V	—	—	±10	µA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to 3.6 V	—	—	±10	µA
Input High Voltage	V_{IH}	I/O pins	2.0	—	V_{CC}q +0.3	V
		Except I/O pins	2.0	—	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	—	–0.3	—	0.8	V
Output High Voltage Level	V_{OH}	I_{OH} = –400 µA	2.4	—	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Output Low Current (R/$\overline{B}$)	I_{OL}	V_{OL} = 0.4 V	8	10	—	mA

2. AC Characteristics (Note 1)

Parameter	Symbol	Value		Unit
		Min.	Max.	
CLE Setup Time	t_{CLS}	0	—	ns
CLE Hold Time	t_{CLH}	10	—	ns
$\overline{CE}$ Setup Time	t_{CS}	0	—	ns
$\overline{CE}$ Hold Time	t_{CH}	10	—	ns
Write Pulse Width	t_{WP}	25	—	ns
ALE Setup Time	t_{ALS}	0	—	ns
ALE Hold Time	t_{ALH}	10	—	ns
Data Setup Time	t_{DS}	20	—	ns
Data Hold Time	t_{DH}	10	—	ns
Write Cycle Time	t_{WC}	50	—	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	—	ns
$\overline{WP}$ High to $\overline{WE}$ Low	t_{WW}	100	—	ns
Ready to $\overline{RE}$ Falling Edge	t_{RR}	20	—	ns
Read Pulse Width	t_{RP}	30	—	ns
Read Cycle Time	t_{RC}	50	—	ns
$\overline{RE}$ Access Time (Serial Data Access)	t_{REA}	—	35	ns
$\overline{CE}$ High Time for the Last Address in Serial Read Cycle (Note 3)	t_{CEH}	100	—	ns
$\overline{RE}$ Access Time (ID Read)	t_{READID}	—	35	ns
$\overline{RE}$ High to Output High Impedance	t_{RHZ}	15	30	ns
$\overline{CE}$ High to Output High Impedance	t_{CHZ}	—	20	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	—	ns
Output High Impedance to $\overline{RE}$ Falling Edge	t_{IR}	0	—	ns
$\overline{RE}$ Access Time (Status Read)	t_{RSTO}	—	35	ns
$\overline{CE}$ Access Time (Status Read)	t_{CSTO}	—	45	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	—	ns
ALE Low to $\overline{RE}$ Low (ID Read)	t_{AR1}	100	—	ns
$\overline{CE}$ Low to $\overline{RE}$ Low (ID Read)	t_{CR}	100	—	ns
Data Transfer from Memory Cell Array to Register	t_{R}	—	7	µs
$\overline{WE}$ High to Busy	t_{WB}	—	100	ns

(Continued)

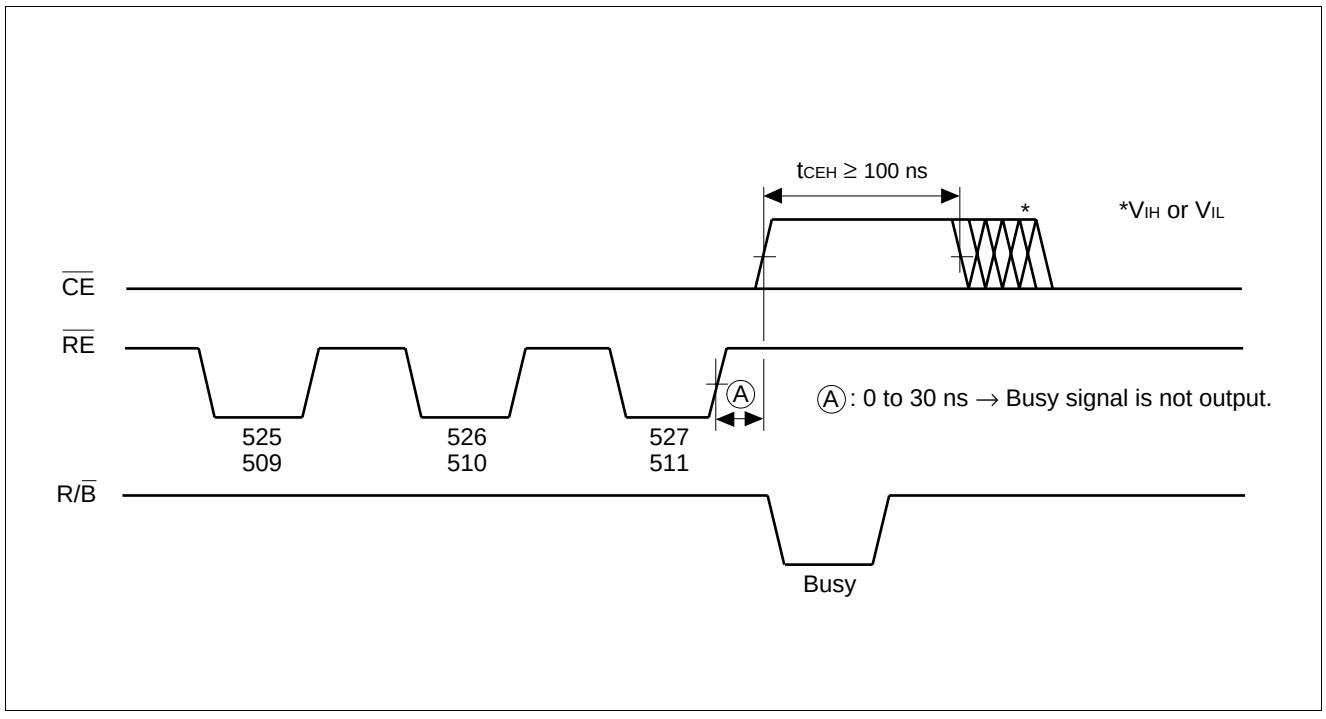
(Continued)

Parameter	Symbol	Value		Unit
		Min.	Max.	
ALE Low to $\overline{RE}$ Low (Read Cycle)	t_{AR2}	50	—	ns
$\overline{RE}$ Last Clock Rising Edge to Busy (in Sequential Read)	t_{RB}	—	100	ns
$\overline{CE}$ High to Ready (in Case of Interception by $\overline{CE}$ in Read Mode) (Note 2)	t_{CRY}	—	50 + tr (R/$\overline{B}$)	ns
Device Resetting Time (Read/Program/Erase)	t_{RST}	—	5/10/500	µs

Notes: 1. AC Test Conditions:

Operating range	V_{CC} = 2.7 to 3.6 V	V_{CC} = 3.0 to 3.6 V
Input level	2.4 V/0.4 V	
Input comparison level	1.5 V/1.5 V	
Output data comparison level	1.5 V/1.5 V	
Output load	1TTL	
Load capacitance (C_L)	50 pF	100 pF
Transition time (t_T)	5 ns	

2. The time to go from $\overline{CE}$ high to Ready depends on the pull-up resister of the R/$\overline{B}$ pin (see Application Notes (6)) toward the end of this document.
3. In case that toggling $\overline{CE}$ to high after access to the last address (address 527) in the resister in the read mode (1), (2), and (3), the $\overline{CE}$ high time must be held for 100 ns or more when the delay time of $\overline{CE}$ with respect to $\overline{RE}$ is 0 to 200 ns (see the figure below). When the $\overline{CE}$ delay time is within 30 ns, the device is kept in the Ready state and will output no Busy signal.



■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Average Programming Time	t_{PROG}	—	200	1000	µs	
Number of Programming Cycles on Same Page	N	—	—	10		*1
Block Erasing Time	t_{BERASE}	—	2	10	ms	
Number of Program/Erase Cycles	P/E	1×10^6	—	—		*2

*1: Refer to Application Note (10) toward the end of this document.

*2: Refer to Application Note (13) toward the end of this document.
This specification is on conditions that ECC system would be combined.

■ VALID BLOCKS

The MBM30LV0032 occasionally contains unusable blocks. Refer to Application Note (12) toward the end of this document.

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Valid Block Number	N_{VB}	502	—	512	Block

■ PIN CAPACITANCE

Parameter	Symbol	Condition	Value		Unit
			Typ.	Max.	
Input Capacitance	C_{IN}	V_{IN} = 0	—	10	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	—	10	pF

Notes: 1. Test conditions T_A = 25 °C, f = 1.0 MHz
2. Sampled, not 100% tested.

■ TIMING DIAGRAMS

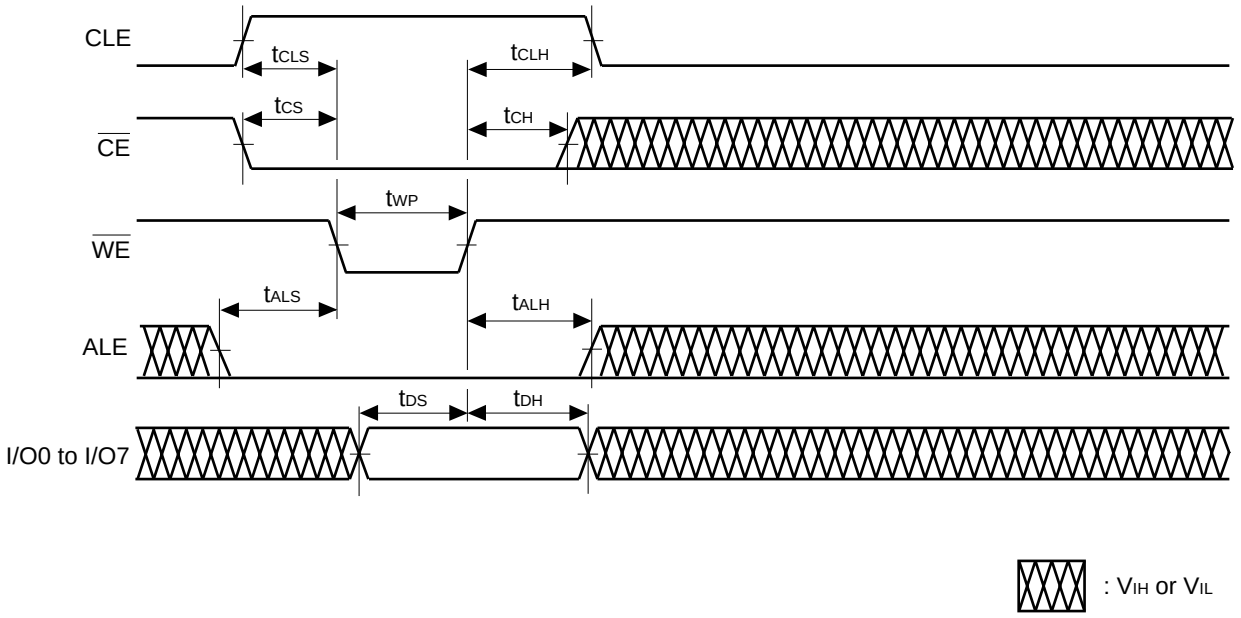


Figure 9 Command Input Cycle Timing Diagram

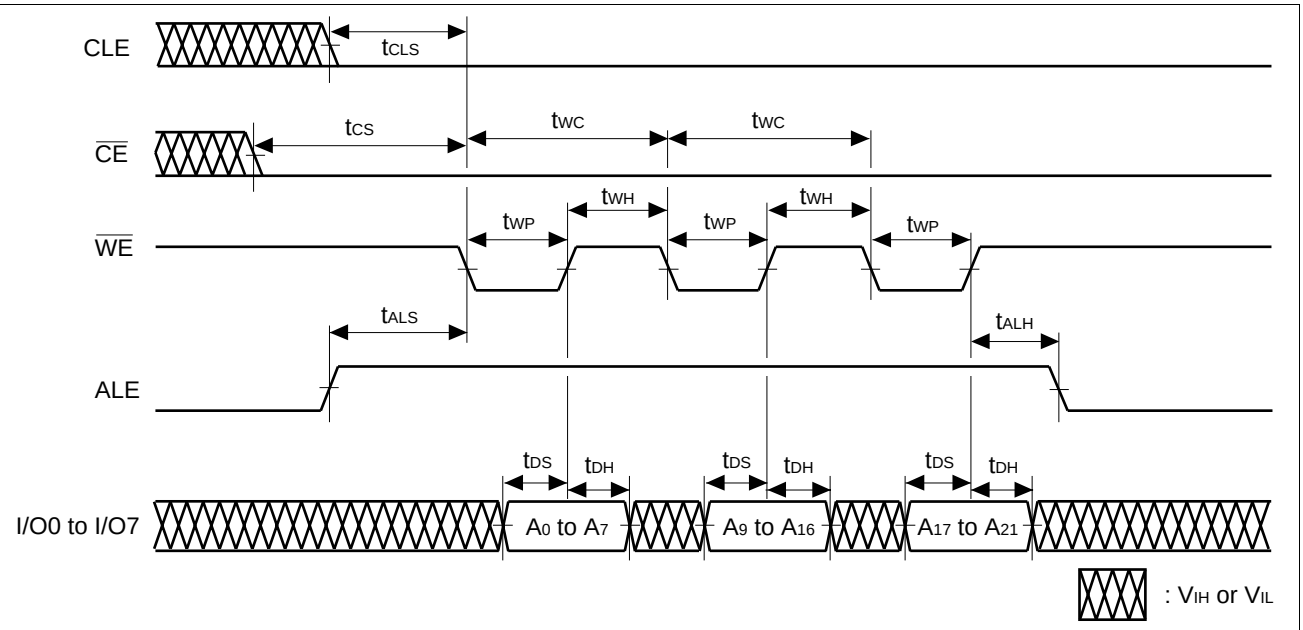


Figure 10 Address Input Cycle Timing Diagram

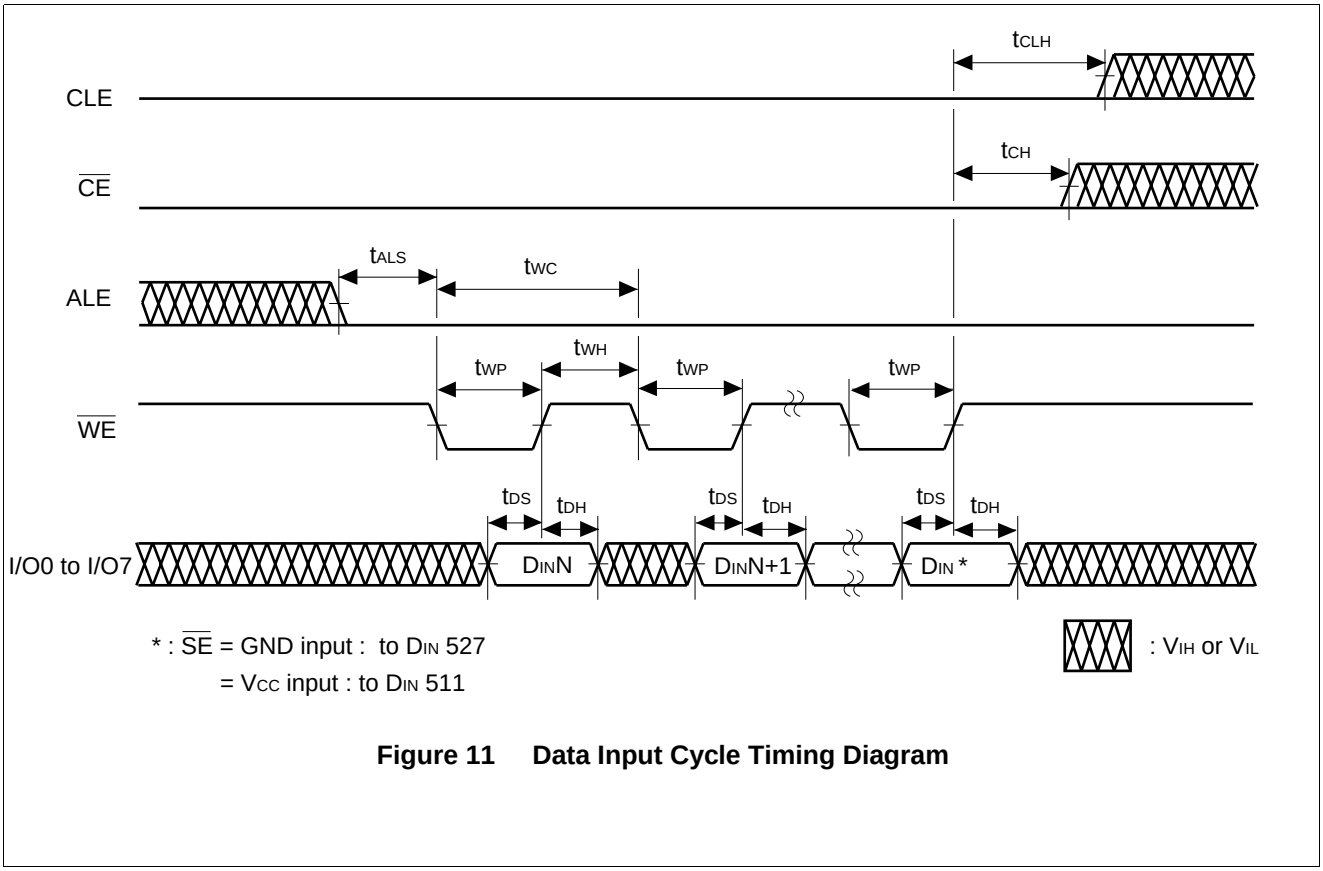


Figure 11 Data Input Cycle Timing Diagram

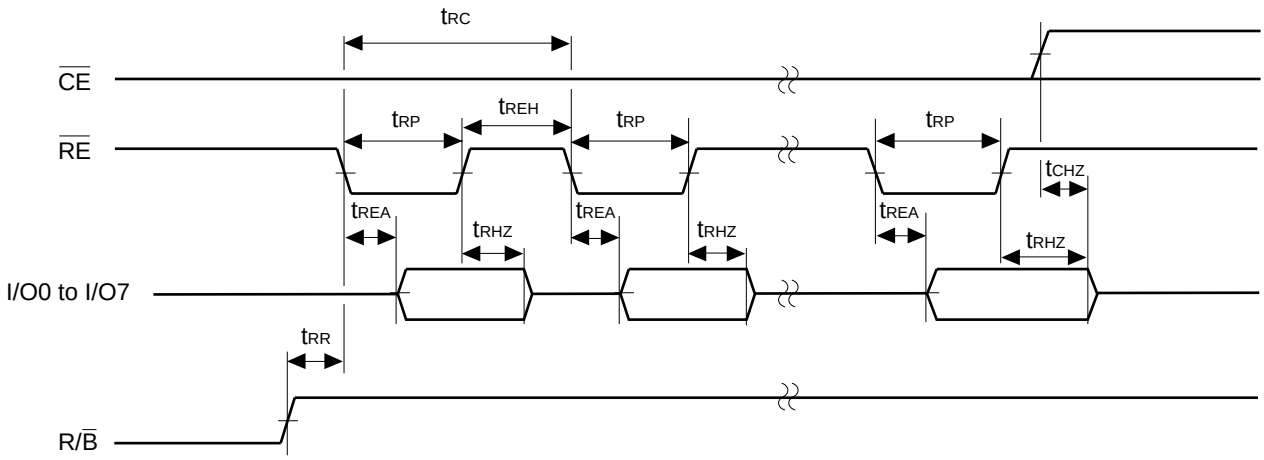


Figure 12 Serial Read Cycle Timing Diagram

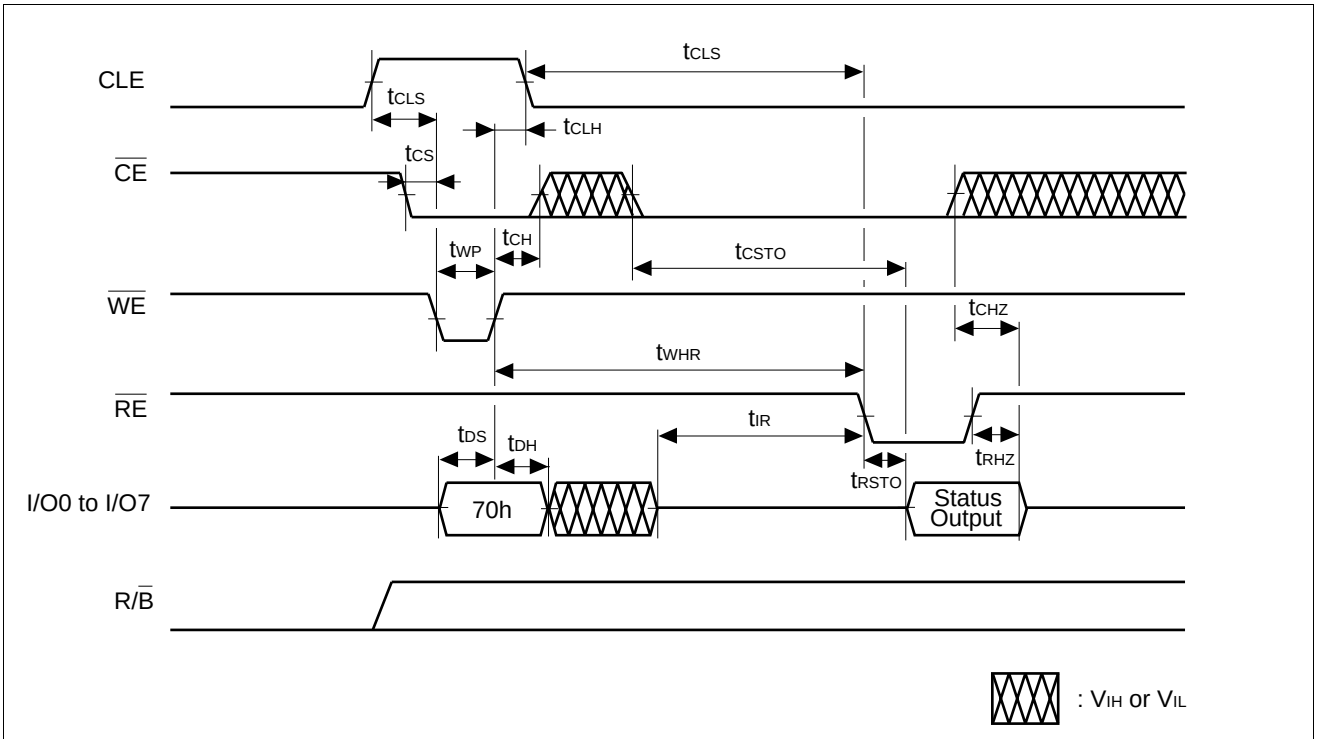
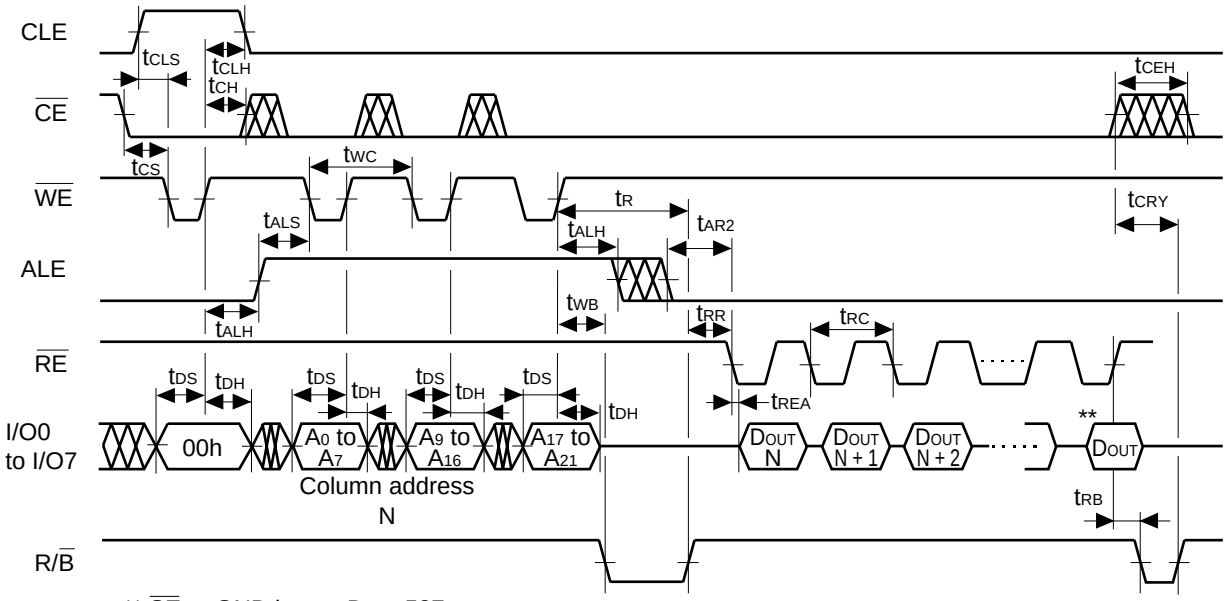


Figure 13 Status Read Cycle Timing Diagram

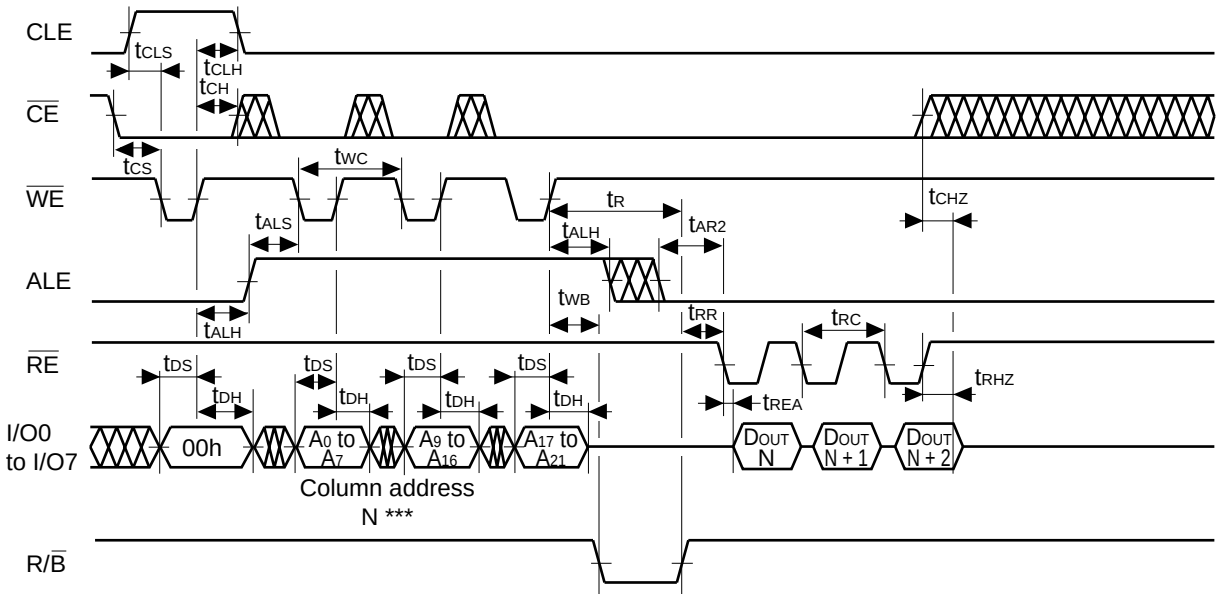


**:$\overline{SE}$ = GND input : D_{OUT} 527
= V_{CC} input : D_{OUT} 511

: V_{IH} or V_{IL}

Note: The $\overline{CE}$ signal must stay "Low" after the third address input and during Busy state.

Figure 14 Read Cycle (1) Timing Diagram

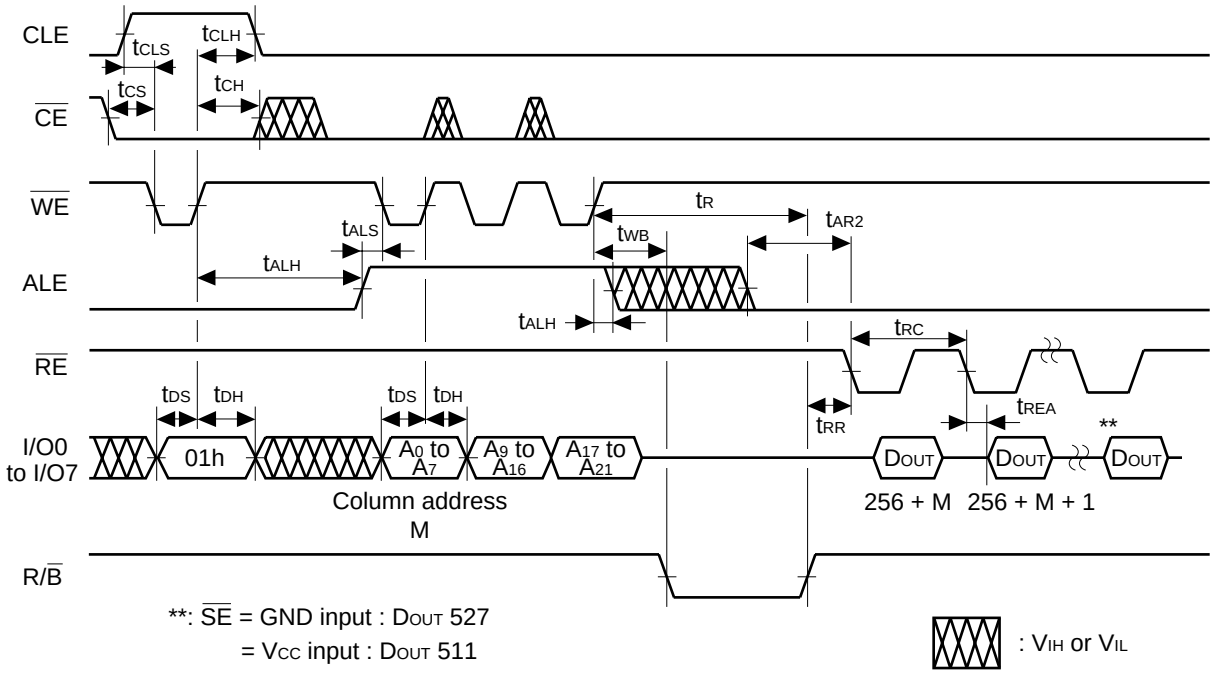


***:Read Operation using 00h Command N : 0 to 255
Read Operation using 01h Command N : 256 to 511

: V_{IH} or V_{IL}

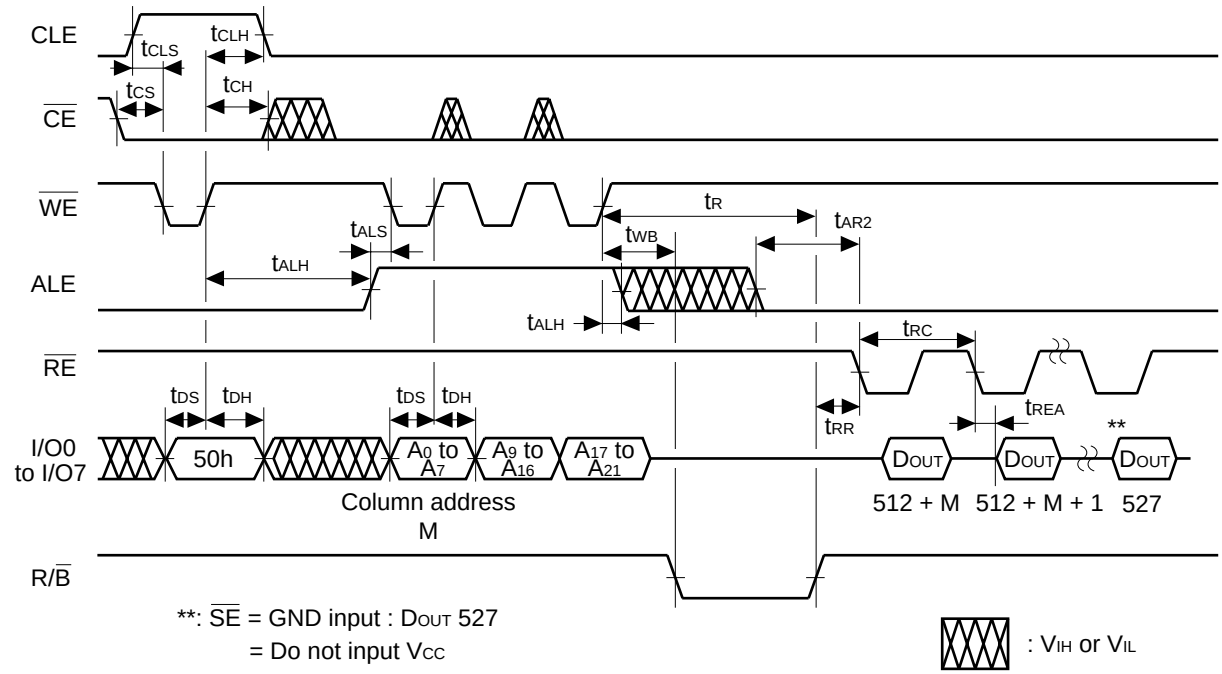
Note: The $\overline{CE}$ signal must stay "Low" after the third address input and during Busy state.

Figure 15 Read Cycle (1) Timing Diagram: Interrupted by $\overline{CE}$



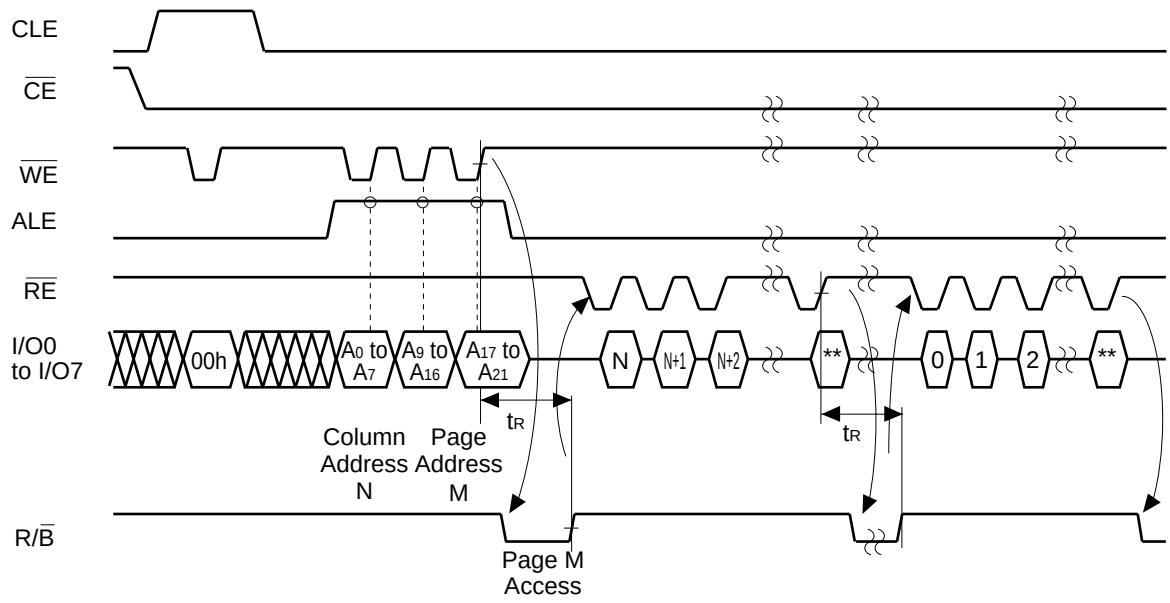
Note: The $\overline{CE}$ signal must stay "Low" after the third address input and during Busy state.

Figure 16 Read Cycle (2) Timing Diagram



Note: The $\overline{CE}$ signal must stay "Low" after the third address input and during Busy state.

Figure 17 Read Cycle (3) Timing Diagram

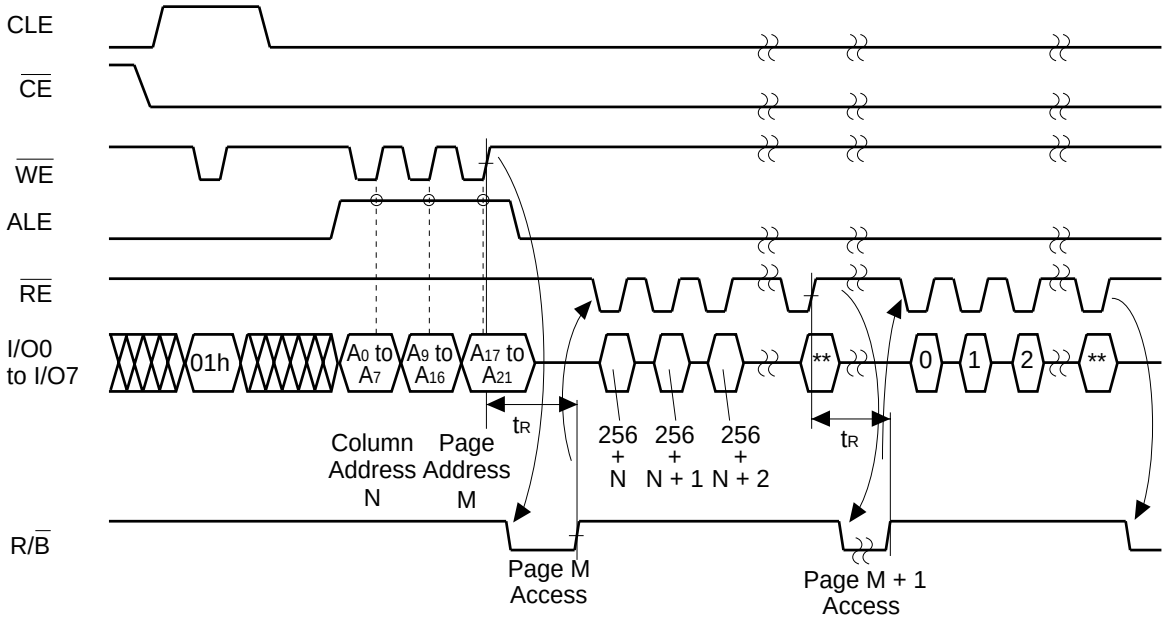


**: SE = GND input : DOUT 527
= VCC input : DOUT 511

: VIH or VIL

Note: The CE signal must stay "Low" after the third address input and during Busy state.

Figure 18 Sequential Read (1) Timing Diagram

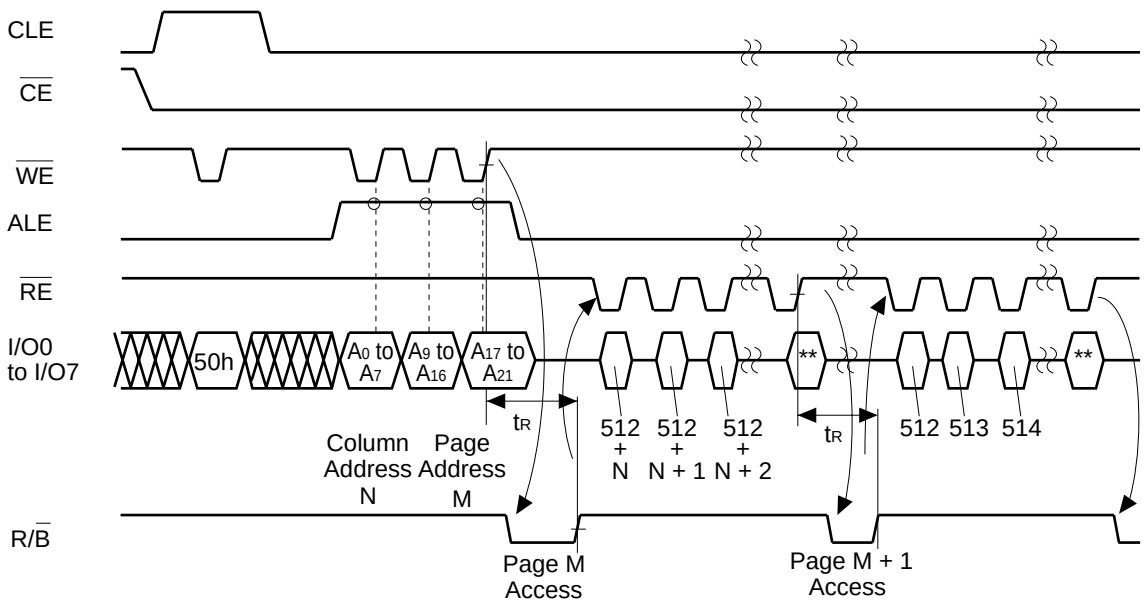


**: SE = GND input : DOUT 527
= VCC input : DOUT 511

: VIH or VIL

Note: The CE signal must stay "Low" after the third address input and during Busy state.

Figure 19 Sequential Read (2) Timing Diagram



**: $\overline{SE}$ = GND input : D_{OUT} 527
= Do not input V_{CC}

: V_{IH} or V_{IL}

Note: The $\overline{CE}$ signal must stay “Low” after the third address input and during Busy state.

Figure 20 Sequential Read Cycle (3) Timing Diagram

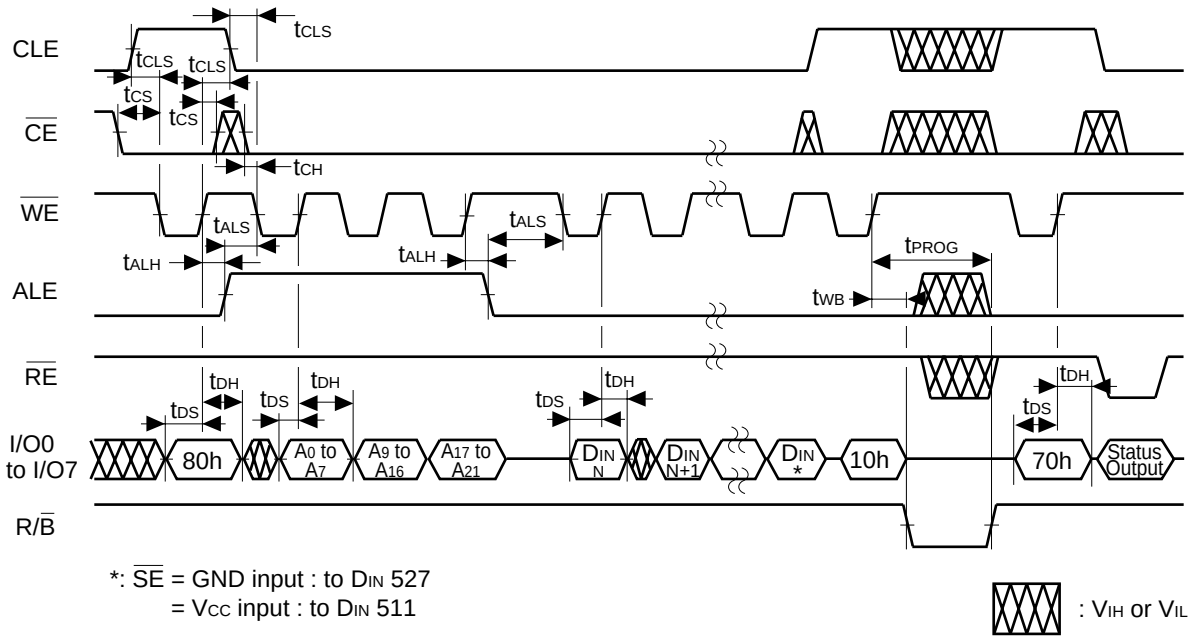


Figure 21 Auto Program Operation Timing Diagram

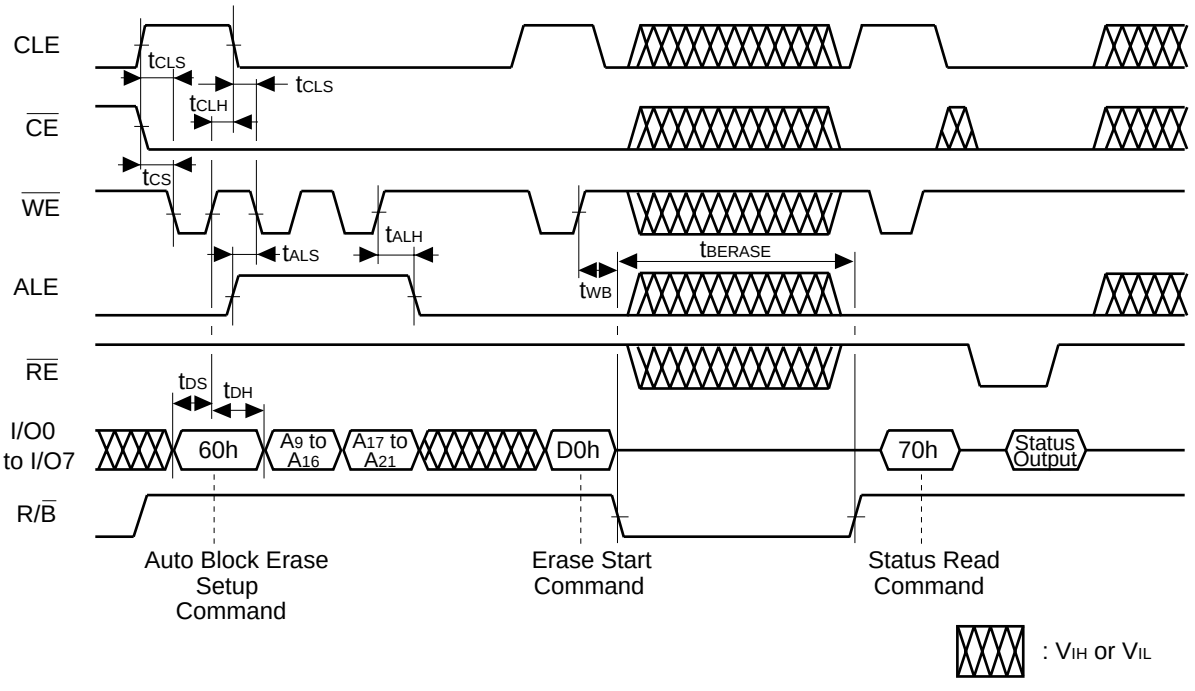


Figure 22 Auto Block Erase Timing Diagram

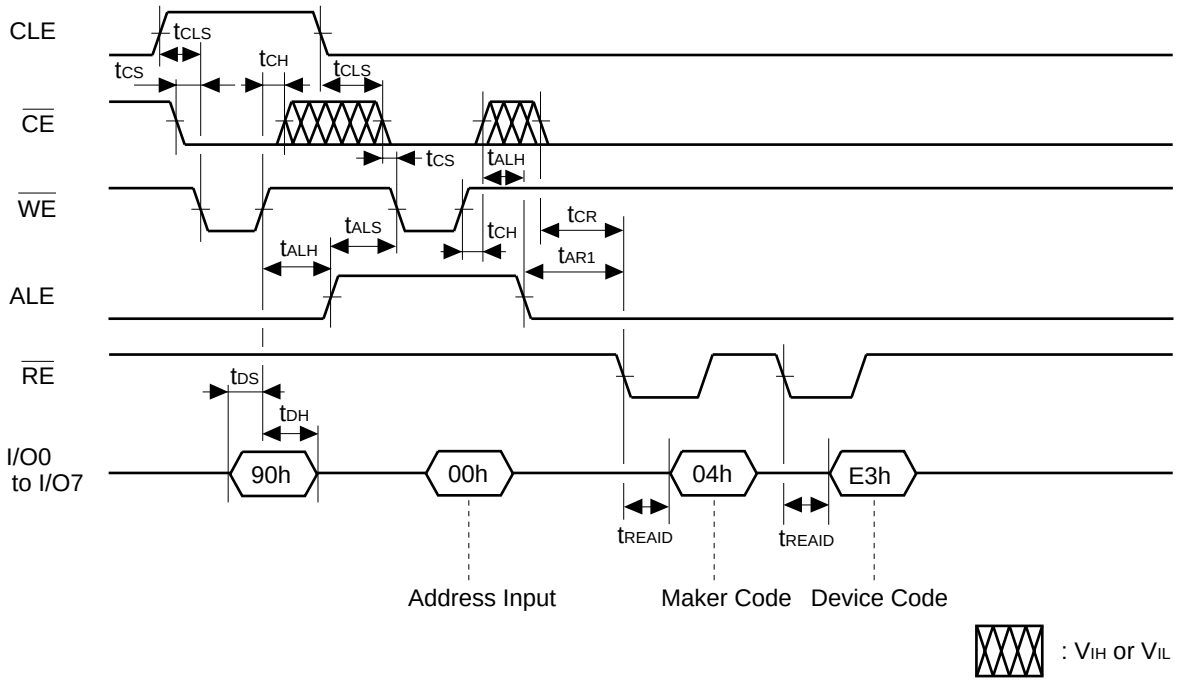


Figure 23 ID Read Operation Timing Diagram

■ APPLICATION NOTES AND COMMENTS

(1) Prohibition of unspecified commands

The operation commands are listed in Table 4. Data input as a command other than the specified commands in Table 4 is prohibited. Stored data may be corrupted if an unspecified command is entered during the command cycle.

(2) Pointer Action for Program Operation

The pointer action can be done for program operation as follows.

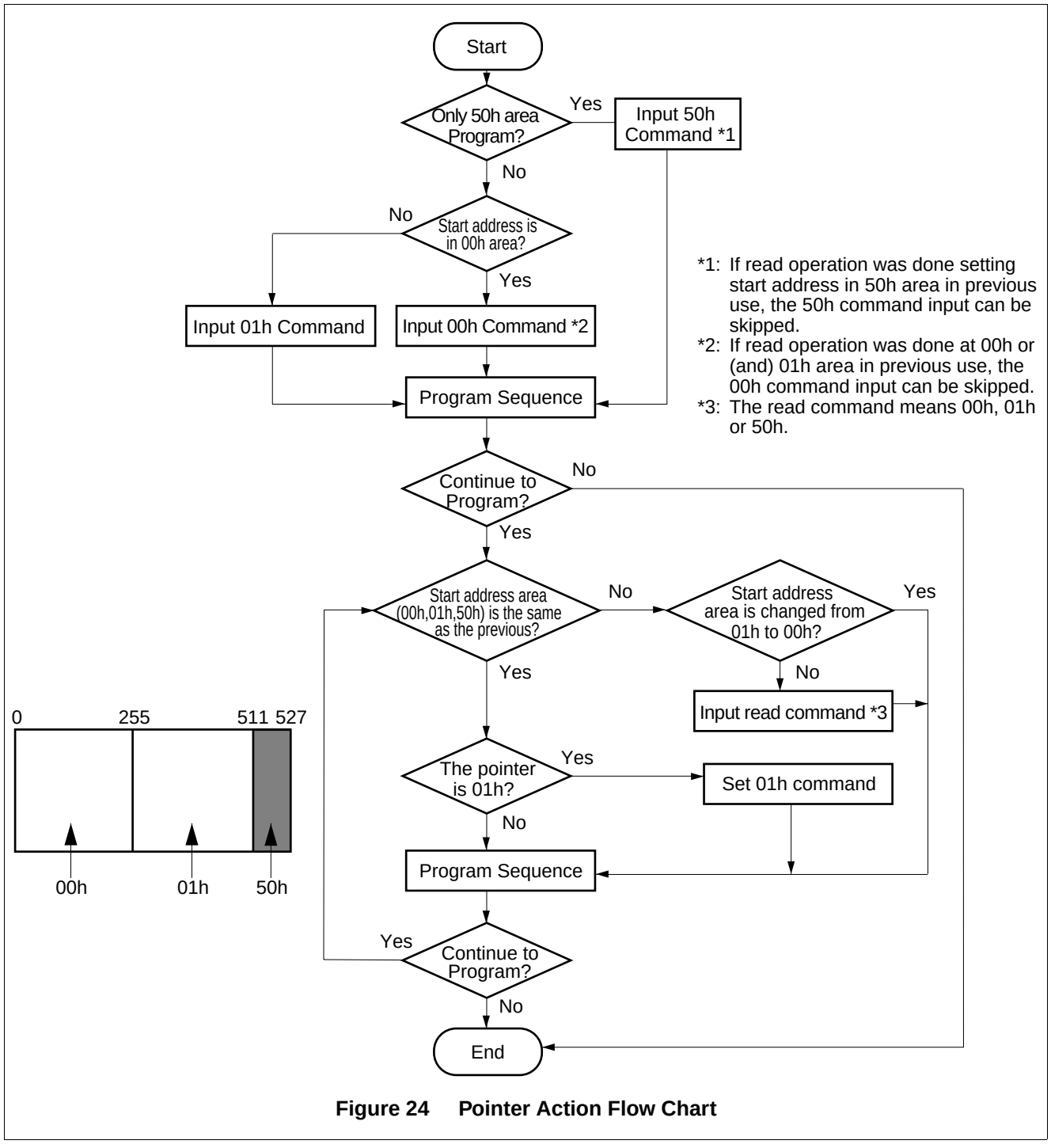


Figure 24 Pointer Action Flow Chart

(3) Acceptable commands after serial input command '80h'

When the serial input command (80h) is input for program execution, commands other than the program execution command (10h) or reset command (FFh) should not be input.

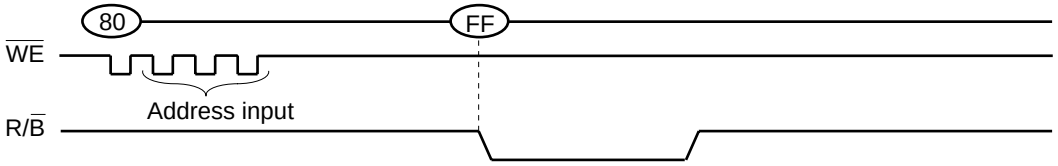
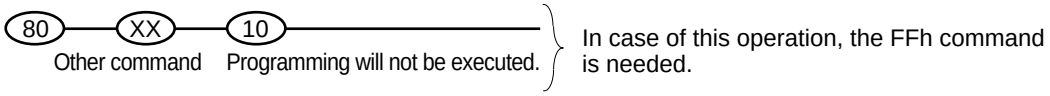


Figure 25 Reset Command After 80h Input

If a command other than '10h' or 'FFh' is input, the program operation is not performed.



(4) Status read during the read operation

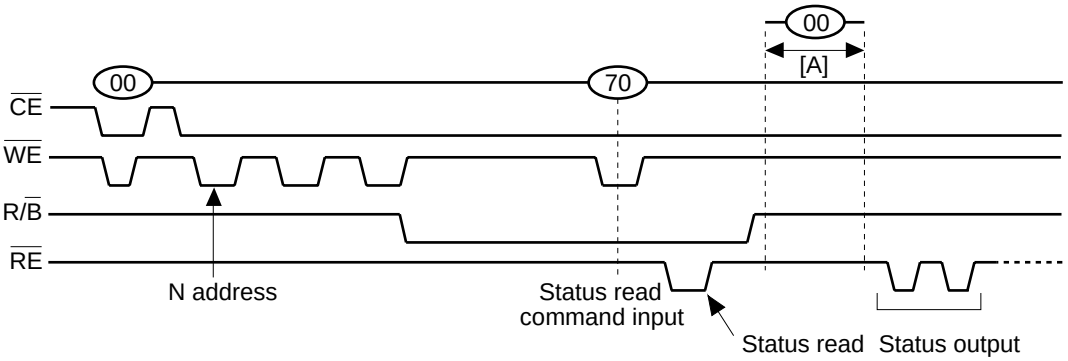


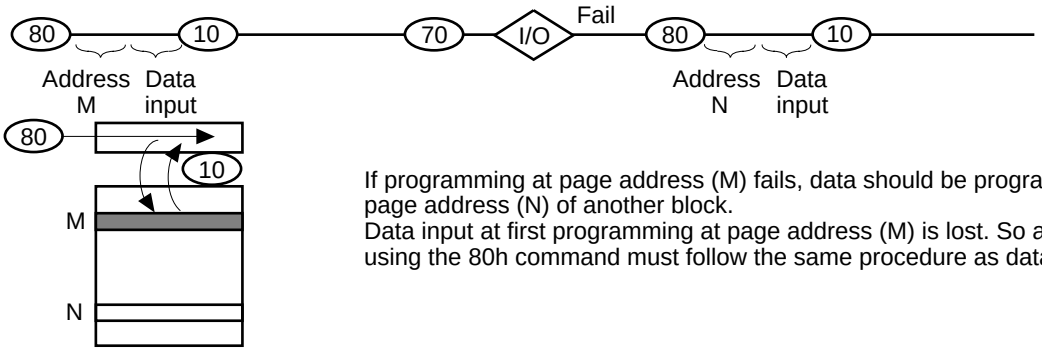
Figure 26 Status Read During Read Operation

When the status read command (70h) is input during reading, the next $\overline{RE}$ clock signal can be input to read the value of the internal status register.

Since the internal operation mode is held in Status Read, read data will not be output even if the $\overline{RE}$ clock signal is input after becoming ready. Status Read is therefore disabled at reading.

When the read command (00h) is input during the period [A], the internal operation mode of the device can be canceled, making it possible to read data at address N without inputting Add.

(5) Auto program failure

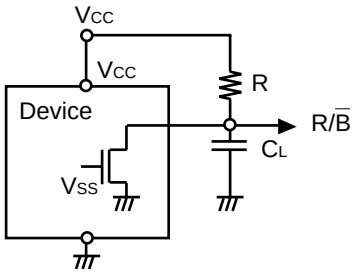


If programming at page address (M) fails, data should be programmed at the page address (N) of another block.
Data input at first programming at page address (M) is lost. So address input using the 80h command must follow the same procedure as data input.

Figure 27 Auto Program Failure

(6) R/$\overline{B}$: Termination of the Ready/Busy pin (R/$\overline{B}$)

The R/$\overline{B}$ is open-drain output. When using the R/$\overline{B}$, R/$\overline{B}$ must be pulled up V_{CC} by a resistor.



$$R = \frac{V_{CC}\ (Max.) — V_{OL}}{I_{OL} + I_L} = \frac{3.2\ V}{8\ mA + I_L}$$

Figure 28 Termination for R/$\overline{B}$

(7) Power On/Off Sequence:

After power-off, each input signal level may be undefined. Use the $\overline{WP}$ signal as shown in the figure below.

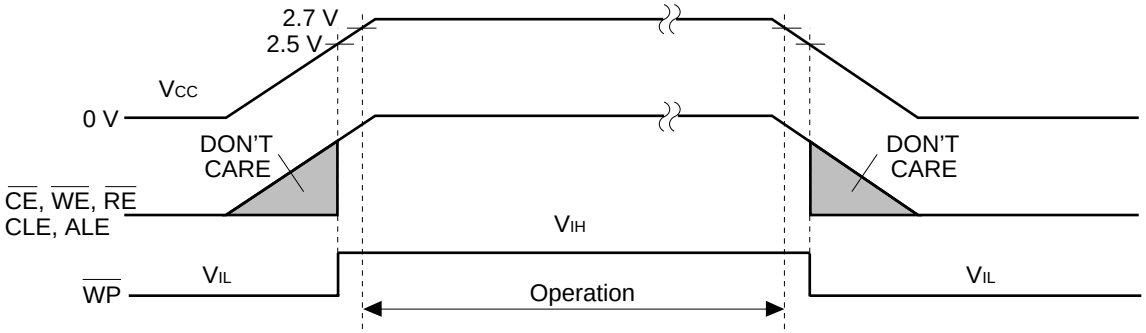
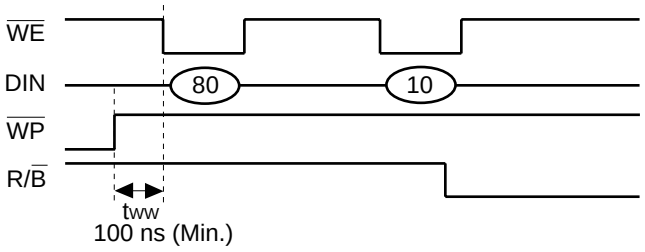


Figure 29 Power On/Off Sequence

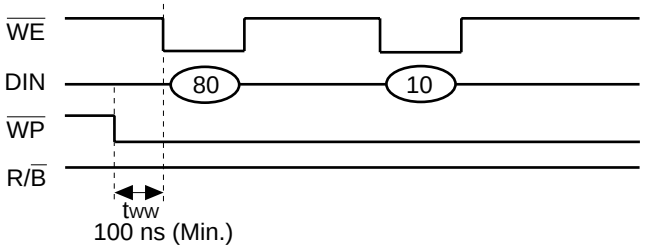
(8) Setup for $\overline{WP}$ Signal

A Low-level $\overline{WP}$ signal will force erasing and programming to be reset. To control, use the $\overline{WP}$ signal as shown below.

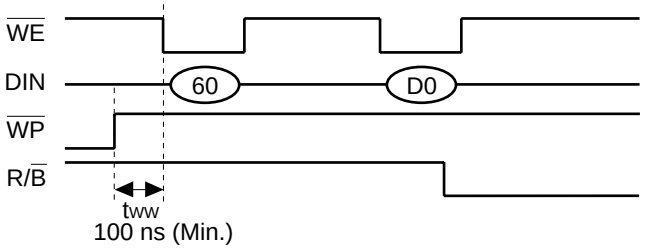
Program



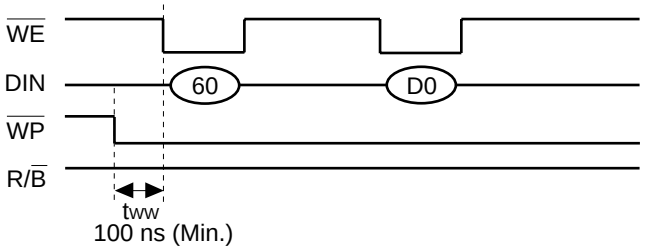
Program Prohibition



Erase

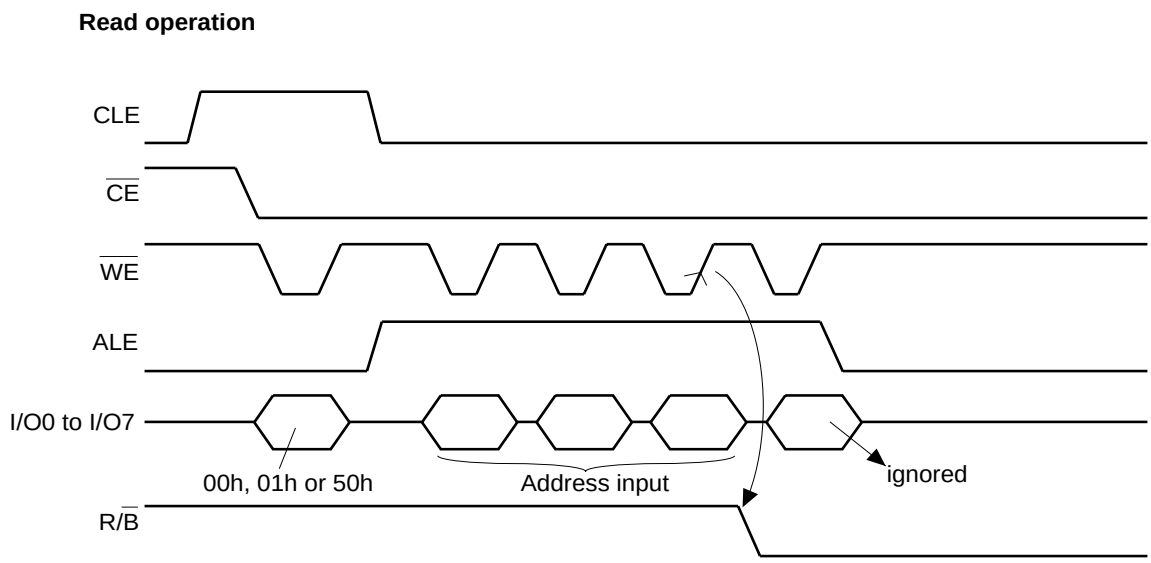


Erase Prohibition



(9) Address input in 4 cycles

The device will get addresses in three cycles. If addresses are input in four cycles, address input in the fourth cycle will be ignored in the chip.



Internal read operation starts when $\overline{WE}$ in the third cycle goes high.

Figure 30 Read Operation when 4 Address Cycles are Input

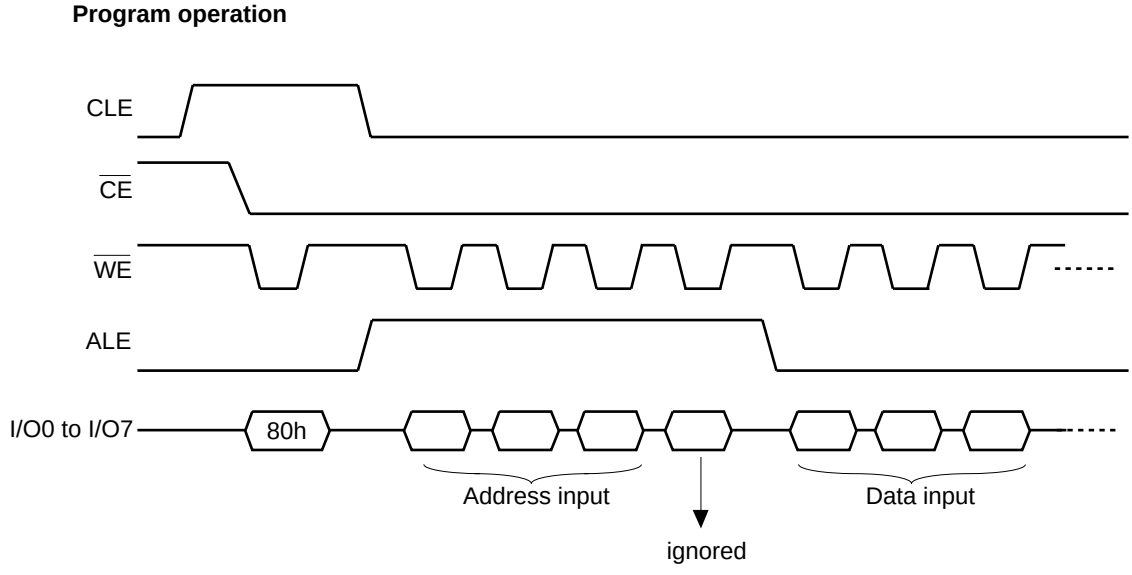


Figure 31 Program Operation when 4 Address Cycles are Input

(10) Divided programming on same page

The device uses the page programming method that allows programming up to ten times on the same page. The procedure for divided programming (programming on a part of one page) is shown below.

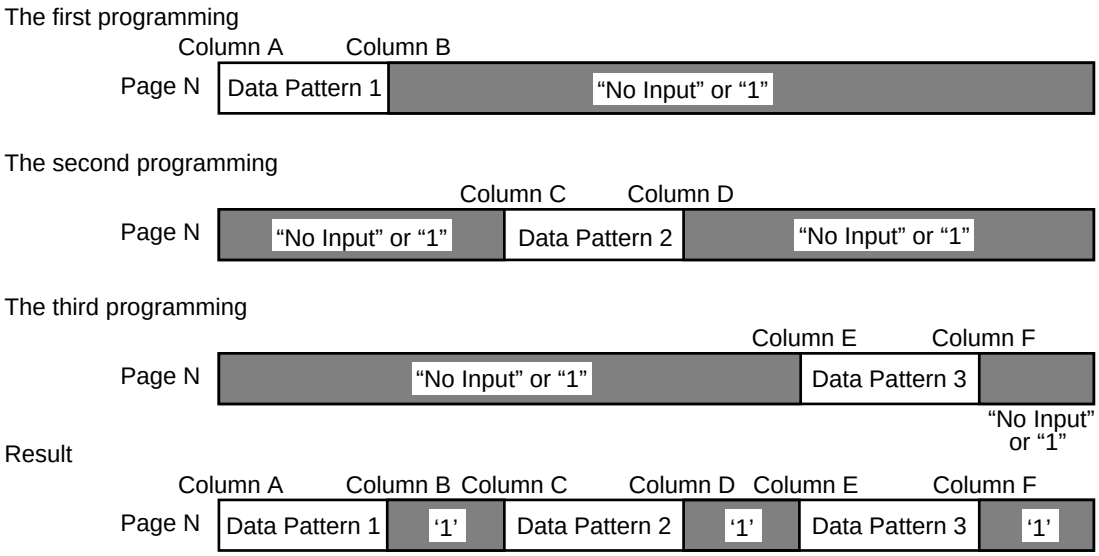


Figure 32 Divided Program in the Same Page

(11) Notification for $\overline{RE}$ Signal

When the device is in the read mode, the $\overline{RE}$ signal causes the internal column address counter to increment in synchronization with the $\overline{RE}$ clock. If the 00h, 01h, or 50h command is input to the device in the read mode, the internal column address counter will count up even after the $\overline{RE}$ signal is input prior to address input. At this mode, at input of the $\overline{RE}$ signal beyond the last column address, the device will start reading (Memory → register) even without address input and may output the Busy signal (Sequential Read is started).

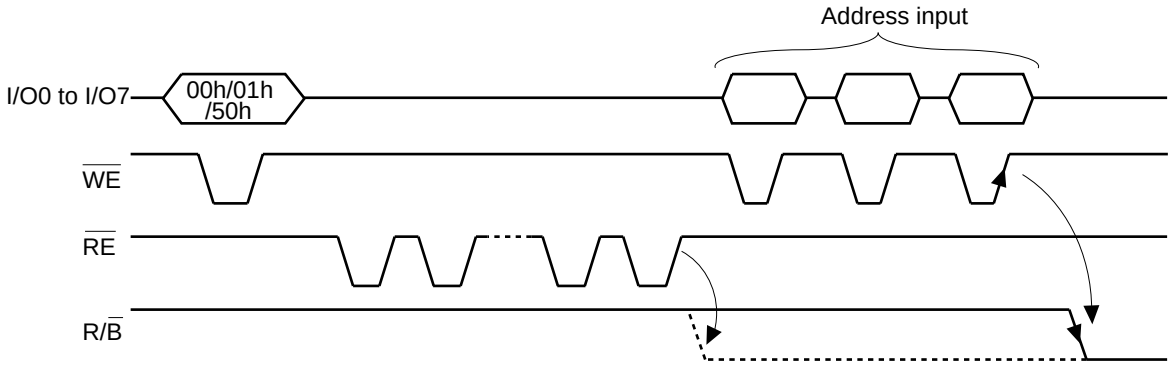
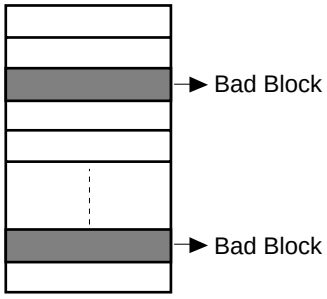


Figure 33 $\overline{RE}$ Input Before Address

In this way, once the device enters the read mode, unintentional reading may be started after the $\overline{RE}$ signal is input prior to addressing; therefore, the $\overline{RE}$ signal should be input after address input.

(12) Invalid block (bad block)

The device contains unusable blocks. Therefore, the following issues must be recognized:



Some MBM30LV0032 products have invalid blocks (bad blocks) at shipping. After mounting the device in the system, test whether there are no bad blocks. If there are any bad blocks, they should not be accessed.
The bad blocks are connected to sense-amp of the bit lines via the selector transistors. Good blocks will not be affected unless the bad blocks are accessed. The effective number of good blocks specified by Fujitsu is shown below.

	Min.	Typ.	Max.	Unit
Valid (Good) Block Number	502	—	512	Block

Figure 36. Shows the Bad Block Test Flow

Figure 34 Bad Block

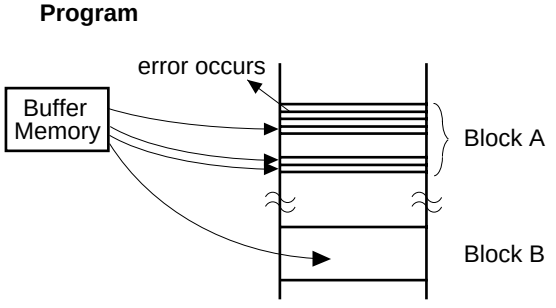
(13) Failure Phenomena for Program and Erase Operations

Repeated rewriting might cause an error at programming and erasing. Possible error modes, and detection methods and remedies are listed in the following table. System-based remedies will provide a highly reliable system.

Failure Mode		Detection and Countermeasure Sequence
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Program Failure	Status Read after Prog. → Block Replacement
Single Bit*	Program Failure '1' → '0'	(1) Block Verify after Prog. → Retry
		(2) ECC

* : (1) or (2)

- ECC : Error Correcting code → Hamming Code etc.
  Example : 1 bit correction & 2 bit detection.
- Block Replacement



If an error occurs in block A, reprogramming from the external buffer to block B. Block A should not be accessed after an error occurs.

Figure 35 Reprogramming to Good Block

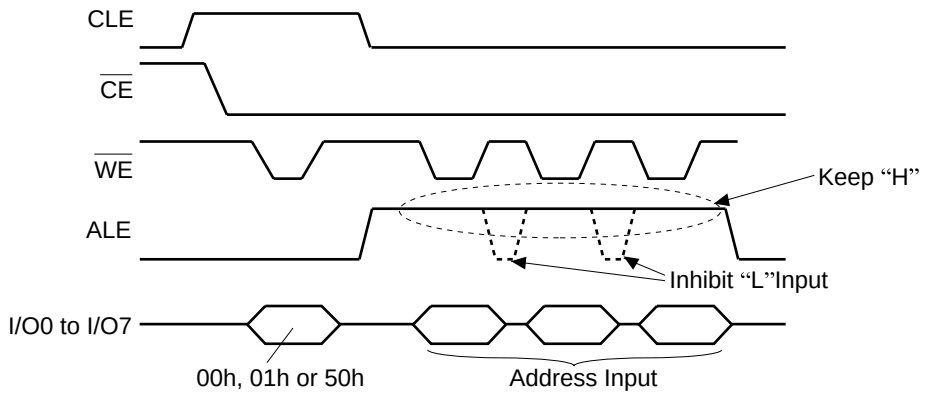
Erase

If an error occurs at erasing, like programming, remedies should be executed on a system basis to prevent access to blocks causing the error.

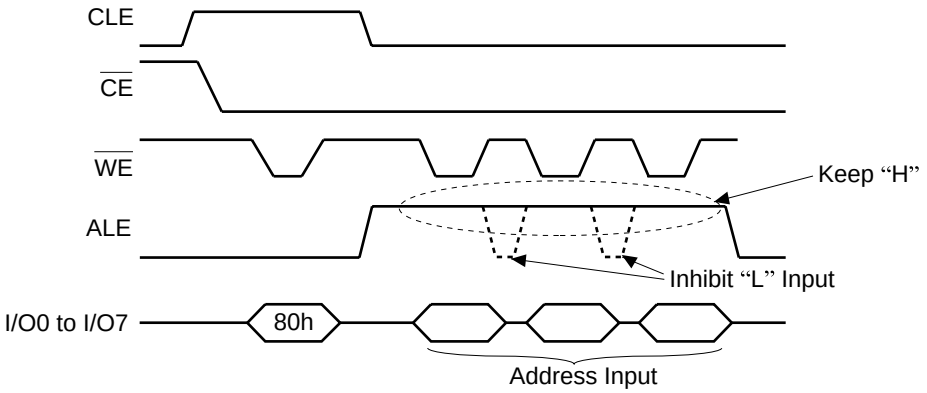
(14) ALE Input Condition during Address Input

The ALE input must remain high once asserted until the last address byte has been written to the device.

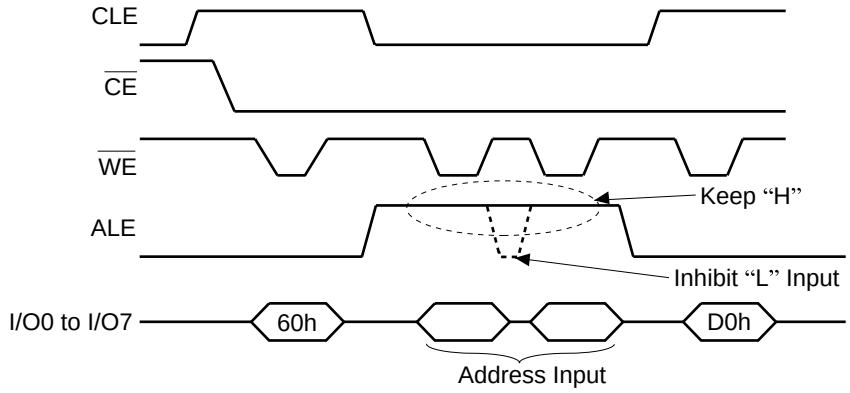
Read Operation



Program Operation

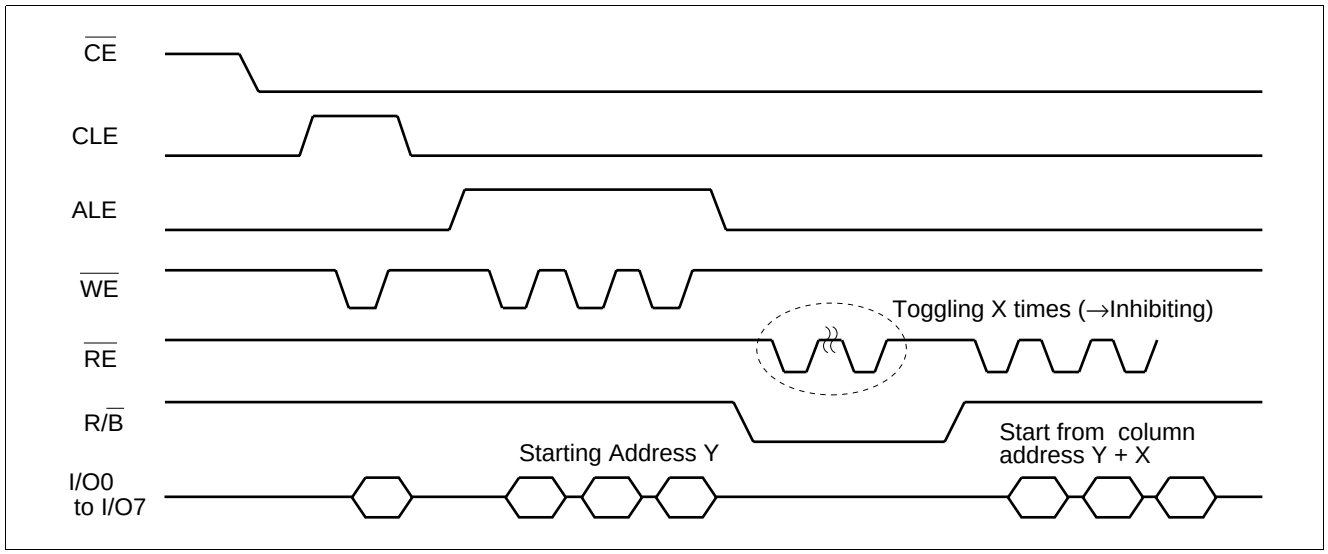


Erase Operation



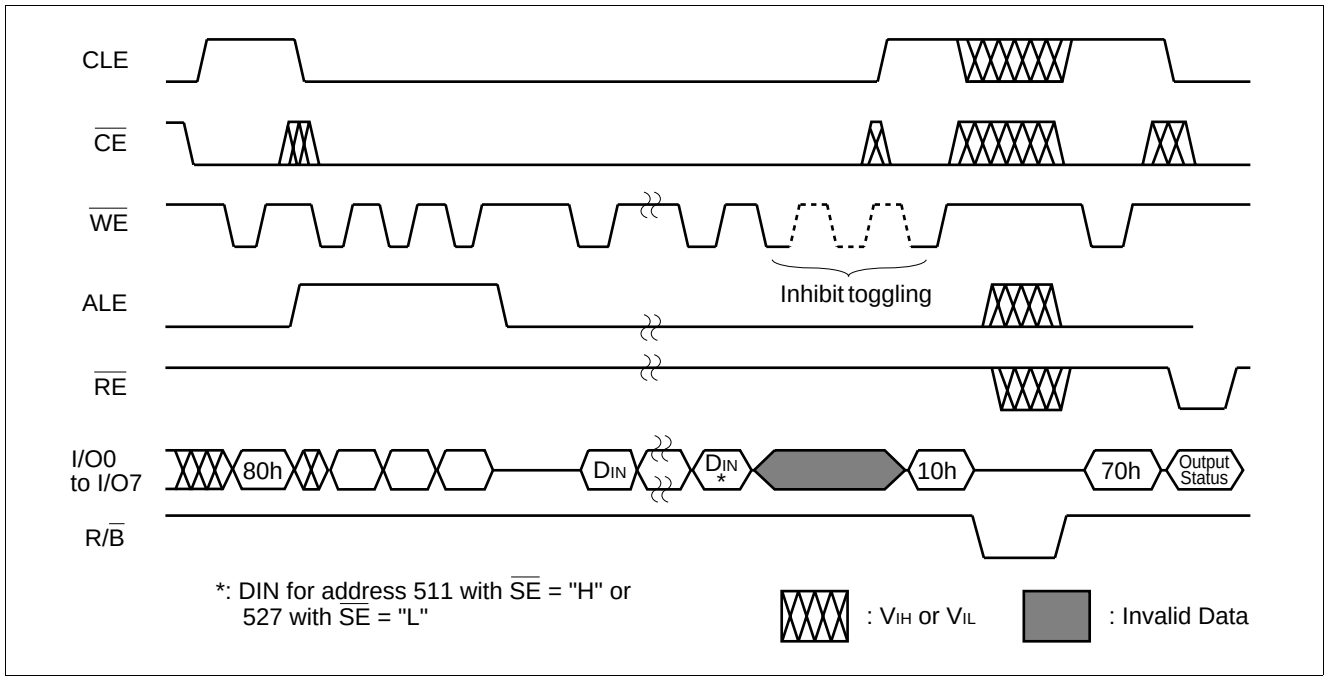
(15) Inhibit $\overline{RE}$ Toggling during Busy State

The $\overline{RE}$ input cannot be allowed to toggle during the period that a read data transfer operation is in process (busy state).
If the $\overline{RE}$ input toggles during that period, the internal column address will increment.



(16) Restriction on Toggling the $\overline{WE}$

The $\overline{WE}$ input cannot be allowed to toggle past the end of page (byte 511 with $\overline{SE}$ high or byte 527 with $\overline{SE}$ low) during an input data operation. If the $\overline{WE}$ input toggles past the end of page, the internal address counter will wrap around to the begging of the page and overwrite the information previously there.



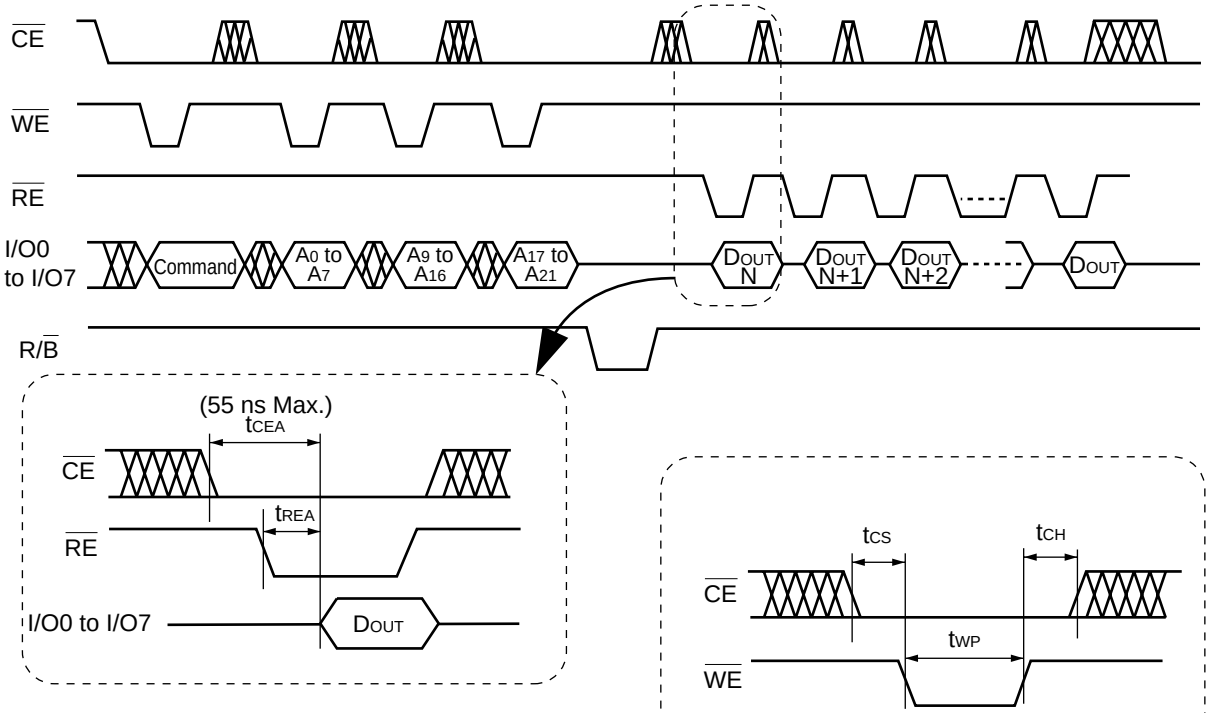
(17) Reading Past Last Device Page

When the last byte in the last page of the device is read, the internal address counter will wrap around to the fist page in the device.

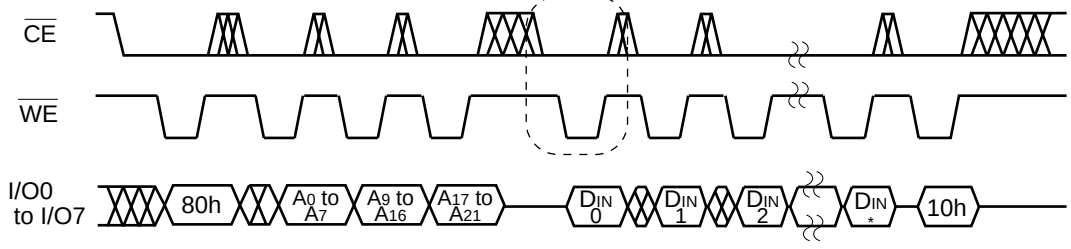
(18) $\overline{CE}$ don't care timing for read and program operation

$\overline{CE}$ can be don't-care ("H" or "L") state during read and program operation as follows.

<Read Operation>



<Program Operation>



: V_{IH} or V_{IL}

Note: In the read operation, the $\overline{CE}$ signal must stay "Low" after the third address input and during Busy state. If the $\overline{CE}$ signal goes High during this period, the read operation will be terminated and then the standby mode will be entered.

■ BAD BLOCK TEST FLOW

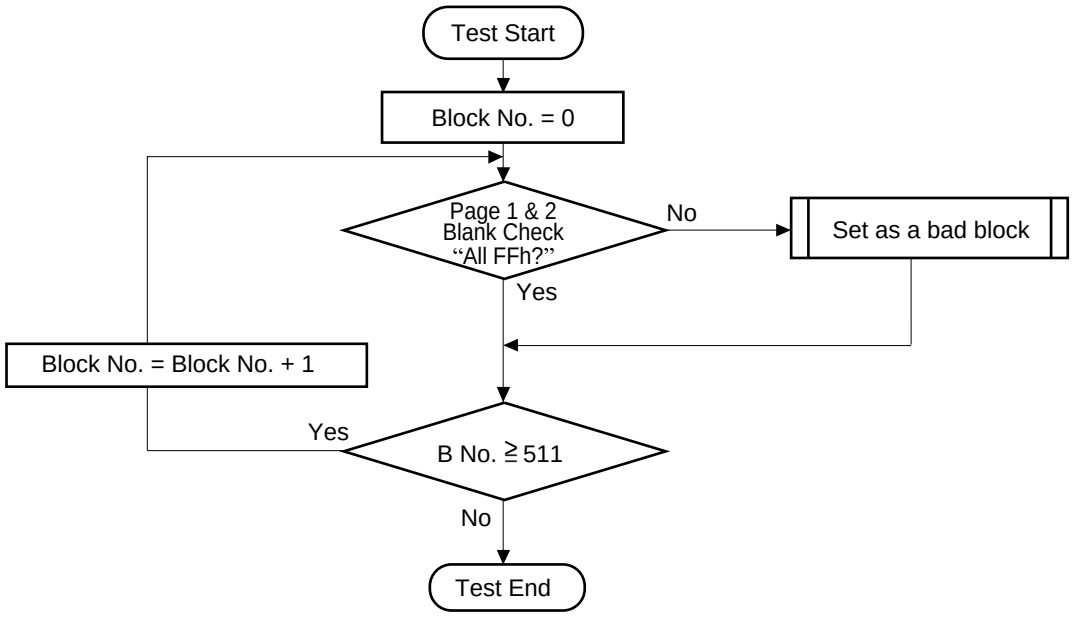
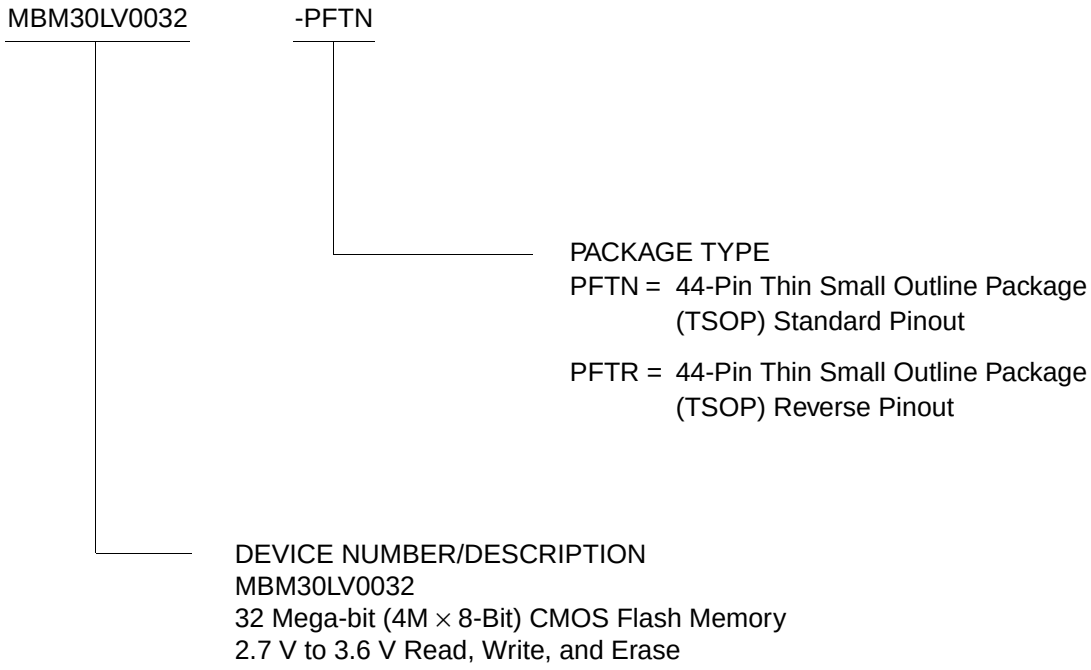


Figure 36 Bad Block Test Flow

■ ORDERING INFORMATION

Standard Products

Fujitsu standard products are available in several packages. The order number is formed by a combination of:



Valid Combinations	
MBM30LV0032	-PFTN -PFTR

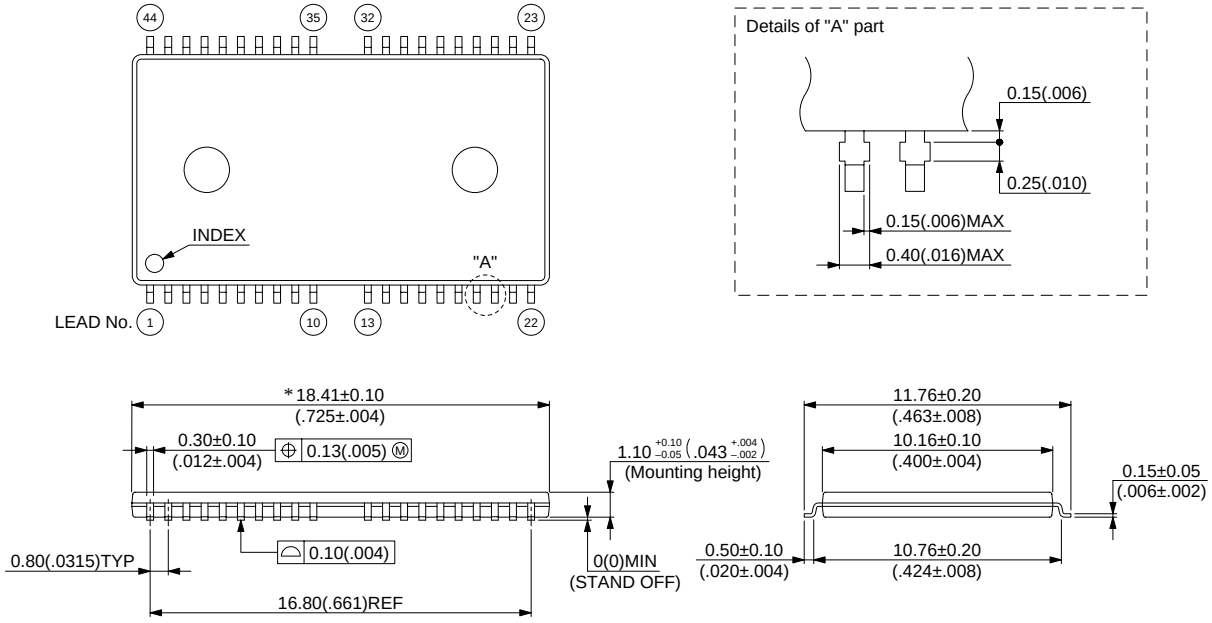
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Fujitsu sales office to confirm availability of specific valid combinations and to check on newly released combinations.

■ PACKAGE DIMENSIONS

44-pin plastic TSOP (II)
(FPT-44P-M07)

*: Resin protrusion. (Each side: 0.15(.006) Max)



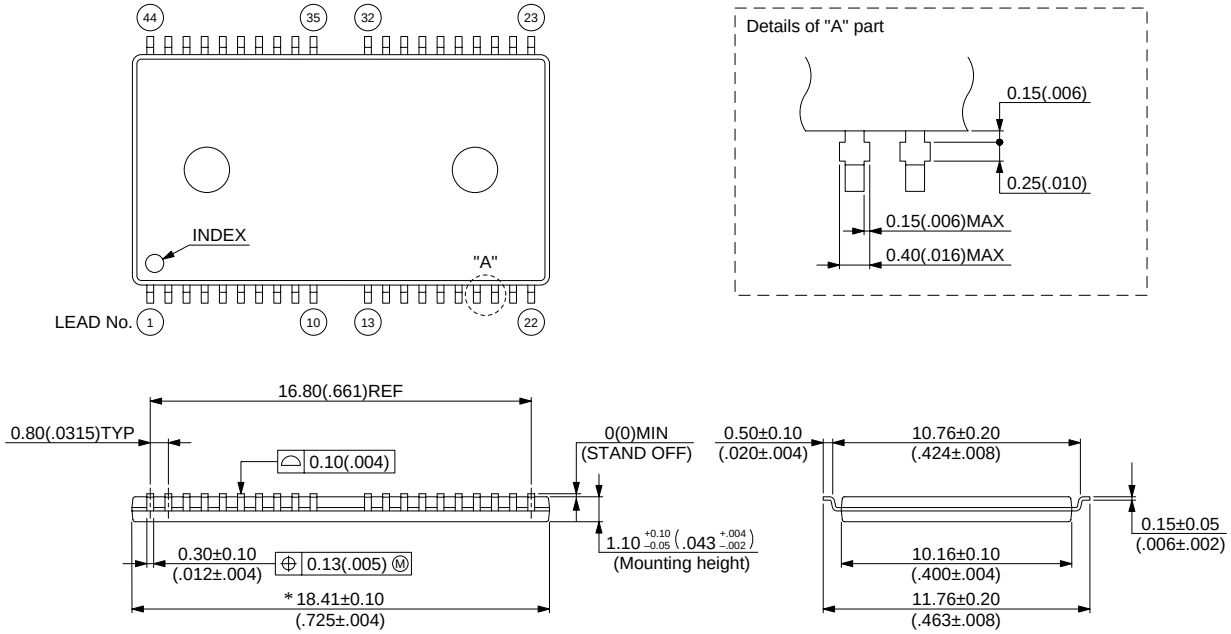
Dimensions in mm (inches)

(Continued)

(Continued)

44-pin plastic TSOP (II)
(FPT-44P-M08)

*: Resin protrusion. (Each side: 0.15(.006) Max)



Dimensions in mm (inches)

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F0012

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