QL8x12B
*Wild*Cat 1000
Very-High-Speed 1K (3K) Gate CMOS FPGA

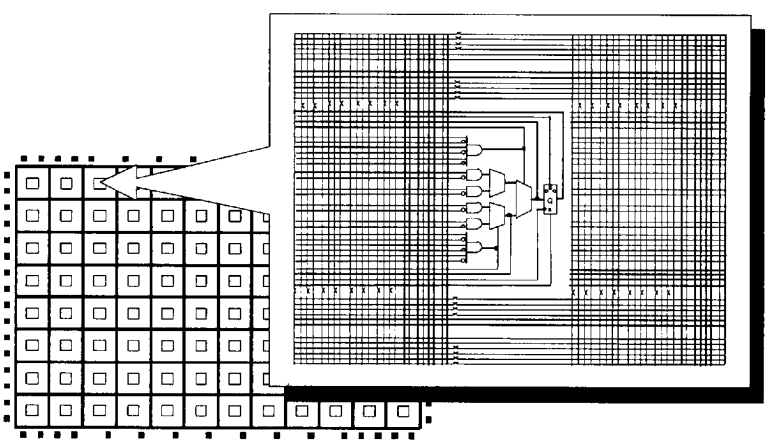
pASIC HIGHLIGHTS

...3000 total available gates

- **Very-High-Speed** – ViaLink metal-to-metal programmable-via anti-fuse technology, allows counter speeds over 150 MHz with logic cell delays of under 2 ns.
- **High Usable Density** – An 8-by-12 array of 96 logic cells provides 3000 total available gates, with 1,000 typically usable "gate array" gates in 44- and 68-pin PLCC packages, and a 100-pin Thin PQFP package.
- **Cost-Reduced, Speed-Enhanced QL8x12A** – Direct plug-in replacement. Existing QL8x12A design files can be converted using SpDE Revision 4.0 or later.
- **Low-Power, High-Output Drive** – Stand-by current typically 2 mA. A 16-bit counter operating at 100 MHz consumes less than 50 mA. Minimum IOL of 12 mA and IOH of 8 mA.
- **Low-Cost, Easy-to-Use design Tools** – Designs entered and simulated using third-party CAE Tools including Viewlogic, Synopsys, Verilog and VHDL. Fast, fully automatic place and route on PC and workstation platforms using the QuickLogic SpDE software.

QL8x12B Block Diagram

96 Logic Cells



▪ = Up to 56 I/O cells, 6 Input high-drive cells, 2 Input/CLK (high-drive) cells.

QUICKLOGIC

PRODUCT SUMMARY

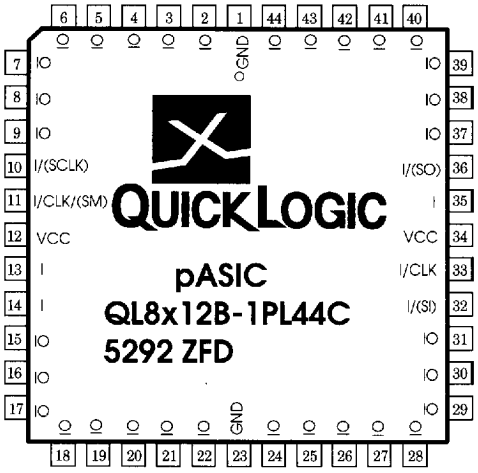
The QL8x12B is a member of the pASIC 1 Family of very-high-speed CMOS user-programmable ASIC devices. The 96-logic cell field-programmable gate array (FPGA) offers up to 3000 total available, and 1000 typically usable "gate array" gates (equivalent to 3000 gate claims of EPLD or LCA vendors) of high-performance general-purpose logic in 44- and 68-pin PLCC packages, 68-pin hermetic PGA and 100-pin Thin PQFP.

Low-impedance, metal-to-metal, ViaLink interconnect technology provides nonvolatile custom logic capable of operating in the data path above 150 MHz. Logic cell delays under 2 ns, combined with input delays of under 1.5 ns and output delays under 3 ns, permit high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

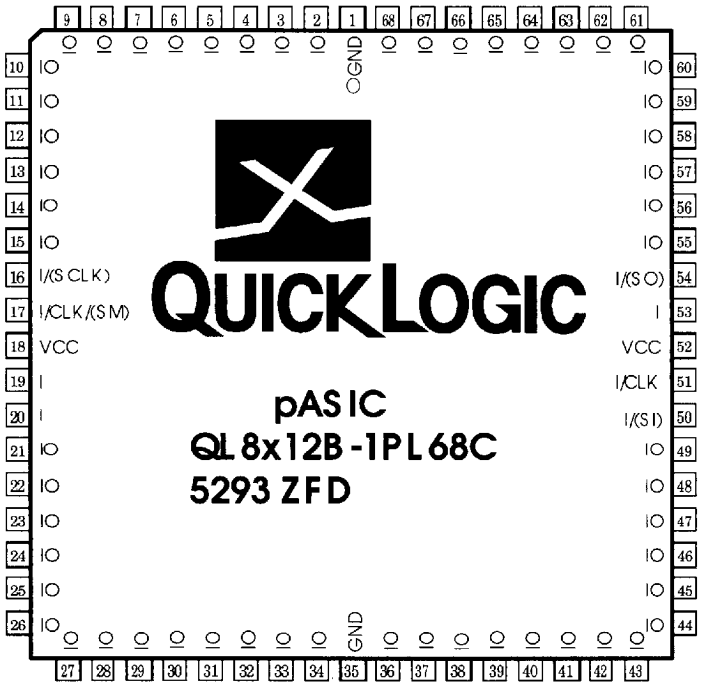
Designs are entered into the QL8x12B using a pASIC Toolkit combining third-party general-purpose design entry and simulation tools with device-specific place and route and programming software. Ample on-chip routing channels are provided to allow fast, fully automatic place and route of designs using up to 100% of the logic and I/O cells.

FEATURES

- Total of 64 input pins
  - 56 Bidirectional Input/Output pins
  - 6 Dedicated Input/High-Drive pins
  - 2 Clock/Dedicated input pins with fanout-independent, low-skew clock networks
- Input + logic cell + output delays under 6 ns
- Chip-to-chip operating frequencies up to 110 MHz
- Internal state machine frequencies up to 150 MHz
- Clock skew <.5 ns
- Input hysteresis provides high noise immunity
- Built-in scan path permits 100% factory testing of logic and I/O cells and functional testing after programming with Automatic Test Vector Generation (ATVG) software
- 44- and 68-pin PLCC, 68-pin CPGA, and 100-pin Thin PQFP
- 68-pin PLCC compatible with QL12x16B
- 100-pin Thin PQFP compatible with QL12x16B and QL16x24B
- 0.65µ CMOS gate array process with ViaLink programming technology



Pinout Diagram 44-pin PLCC



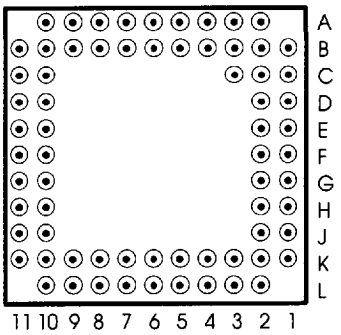
Pinout Diagram 68-pin PLCC

Pins identified I/SCLK, SM, SO and SI are used during scan path testing operation.

Pinout Diagram
68-pin CPGA

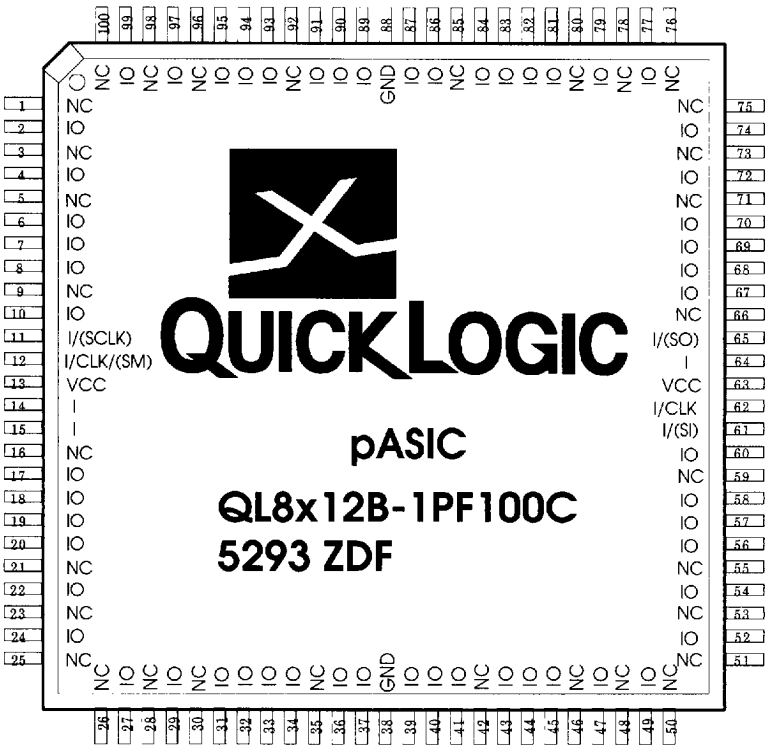
TOP VIEW

BOTTOM VIEW



CPGA 68 Function/Connector Pin Table

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
F1	IO	B7	I/(SCLK)	E11	IO	K5	I/(SI)
E10	IO	A7	I/CLK/(SM)	E1	IO	L5	I/CLK
E2	IO	A6	I	F11	IO	L6	I
K6	VCC	B5	I	G2	IO	K7	I/(SO)
D1	IO	B6	VCC	G10	IO	L4	IO
C2	IO	A8	IO	H11	IO	K4	IO
D2	IO	B8	IO	H10	IO	L3	IO
C1	IO	A9	IO	J11	IO	K3	IO
B1	IO	B9	IO	J10	IO	L2	IO
B11	IO	A10	IO	K11	IO	L10	IO
B10	IO	A2	IO	K1	IO	K10	IO
B3	IO	B2	IO	K2	IO	J2	IO
A3	IO	C10	IO	K9	IO	J1	IO
B4	IO	C11	IO	L9	IO	H2	IO
A4	IO	D10	IO	K8	IO	H1	IO
F2	GND	D11	IO	L8	IO	G1	IO
A5	IO	F10	GND	L7	IO	G11	IO



Pinout Diagram
100-pin Thin PQFP

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... –0.5 to 7.0V
Input Voltage ..... –0.5 to VCC +0.5V
ESD Pad Protection ..... ±2000V
DC Input Current ..... ±20 mA
Latch-up Immunity ..... ±200 mA

Storage Temperature
Ceramic ..... –65°C to + 150°C
Plastic ..... –40°C to + 125°C
Lead Temperature ..... 300°C

OPERATING RANGE

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
VCC	Supply Voltage		4.5	5.5	4.5	5.5	4.75	5.25	V
TA	Ambient Temperature		-55		-40	85	0	70	°C
TC	Case Temperature			125					°C
K	Delay Factor	-0 Speed Grade	0.39	1.82	0.4	1.67	0.46	1.55	
		-1 Speed Grade	0.39	1.56	0.4	1.43	0.46	1.33	
		-2 Speed Grade			0.4	1.35	0.46	1.25	

DC CHARACTERISTICS over operating range

Symbol	Parameter	Conditions	Min	Max	Unit
VIH	Input HIGH Voltage		2.0		V
VIL	Input LOW Voltage			0.8	V
VOH	Output HIGH Voltage	IOH = -4 mA	3.7		V
		IOH = -8 mA	2.4		V
		IOH = -10 µA	VCC-0.1		V
VOL	Output LOW Voltage	IOL = 12 mA*		0.4	V
		IOL = 10 µA		0.1	V
II	Input Leakage Current	VI = VCC or GND	-10	10	µA
IOZ	3-State Output Leakage Current	VI = VCC or GND	-10	10	µA
CI	Input Capacitance [1]			10	pF
IOS	Output Short Circuit Current	VO = GND	-10	-80	mA
		VO = VCC	30	140	mA
ICC	Supply Current [2]	VI, VIO = VCC or GND		10	mA

*IOL = 8 mA for industrial and military range

Notes:

[1] CI = 20 pF Max on I/(SI)

[2] For AC conditions use the formula described in Section 5 of the data book — Power vs Operating Frequency.

[3] Worst case Propagation Delay times over process variation at VCC = 5.0V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

[4] These limits are derived from a representative selection of the slowest paths through the pASIC logic cell ***including net delays***. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

AC CHARACTERISTICS at VCC = 5V, TA = 25°C (K = 1.00)

Logic Cell

Symbol	Parameter	Propagation Delays (ns) [3] Fanout				
		1	2	3	4	8
tPD	Combinatorial Delay [4]	1.7	2.1	2.6	3.0	4.8
tSU	Setup Time [4]	2.1	2.1	2.1	2.1	2.1
tH	Hold Time	0.0	0.0	0.0	0.0	0.0
tCLK	Clock to Q Delay	1.0	1.5	1.9	2.3	4.2
tCWHI	Clock High Time	2.0	2.0	2.0	2.0	2.0
tCWLO	Clock Low Time	2.0	2.0	2.0	2.0	2.0
tSET	Set Delay	1.7	2.1	2.6	3.0	4.8
tRESET	Reset Delay	1.5	1.8	2.2	2.5	3.9
tSW	Set Width	1.9	1.9	1.9	1.9	1.9
tRW	Reset Width	1.8	1.8	1.8	1.8	1.8

Input Cell

Symbol	Parameter	Propagation Delays (ns) [3]					
		1	2	3	4	6	8
tIN	High Drive Input Delay [5]	2.1	2.2	2.3	2.4	2.6	2.9
tINI	High Drive Input, Inverting Delay [5]	2.1	2.2	2.3	2.5	2.8	3.1
tIO	Input Delay (bidirectional pad)	1.4	1.8	2.2	2.6	3.4	4.2
tGCK	Clock Buffer Delay [6]	2.7	2.7	2.8	2.9	3.0	
tGCKHI	Clock Buffer Min High [6]	2.0	2.0	2.0	2.0	2.0	
tGCKLO	Clock Buffer Min Low [6]	2.0	2.0	2.0	2.0	2.0	

Output Cell

Symbol	Parameter	Propagation Delays (ns) [3] Output Load Capacitance (pF)				
		30	50	75	100	150
tOUTLH	Output Delay Low to High	2.7	3.4	4.2	5.0	6.7
tOUTHL	Output Delay High to Low	2.8	3.7	4.7	5.6	7.6
tPZH	Output Delay Tri-state to High	4.0	4.9	6.1	7.3	9.7
tPZL	Output Delay Tri-state to Low	3.6	4.2	5.0	5.8	7.3
tPHZ	Output Delay High to Tri-state [7]	2.9				
tPLZ	Output Delay Low to Tri-state [7]	3.3				

Notes:

[5] See High Drive Buffer Table for more information.

[6] Clock buffer fanout refers to the maximum number of flip flops per half column. The number of half columns used does not affect clock buffer delay.

[7] The following loads are used for tPXZ:

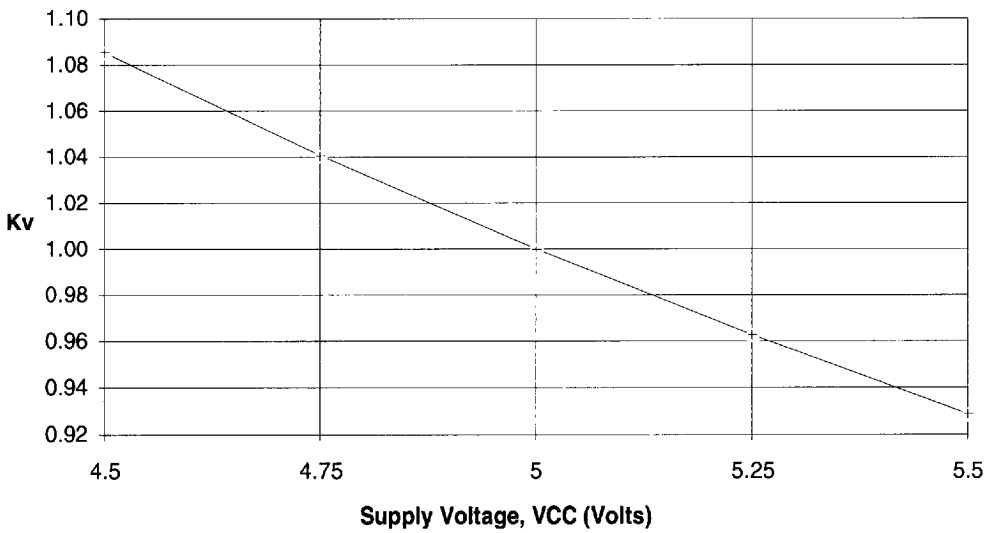
High Drive Buffer

Symbol	Parameter	Clock Drivers Wired Together	Propagation Delays (ns) [3] Fanout				
			12	24	48	72	96
tIN	High Drive Input Delay	1	4.0	4.9			
		2		3.5	5.0		
		3			4.0	4.8	5.6
		4				4.1	4.8
tINI	High Drive Input, Inverting Delay	1	4.2	5.1			
		2		3.7	5.2		
		3			4.2	5.0	5.8
		4				4.3	5.0

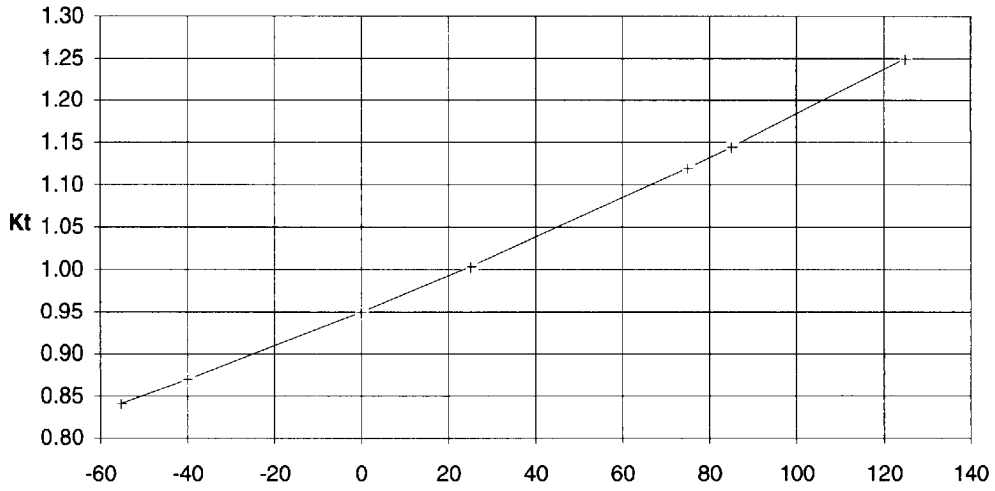
AC Performance

Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified in the Operating Range. The effects of voltage and temperature variation are illustrated in the following graphs. The SpDE Toolkit incorporates data sheet AC Characteristics into the QDIF database for pre-place-and-route timing analysis. The SpDE Delay Modeler extracts specific timing parameters for precise path analysis or simulation results following place and route.

Kv, Voltage Factor versus Vcc, Supply Voltage

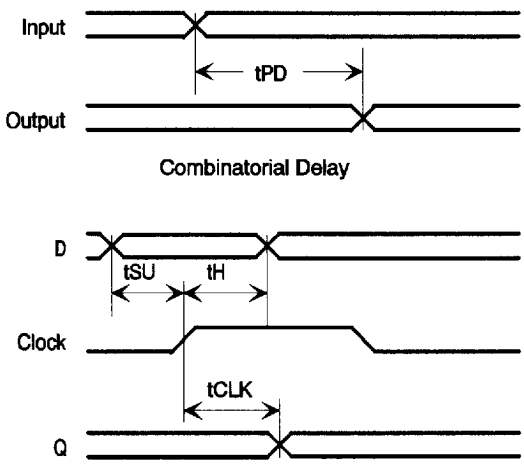


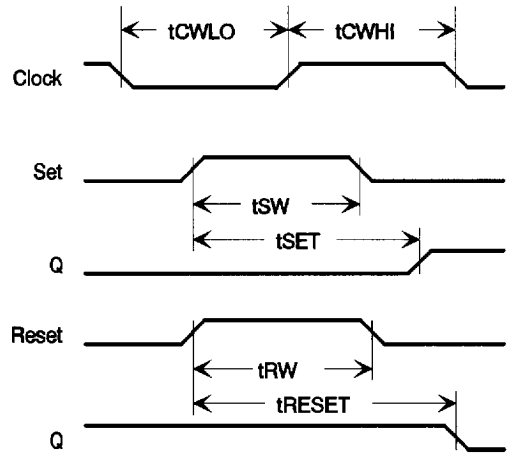
Kt, Temperature Factor versus Temperature



(Theta JA = 45 °C/Watt for PLCC)

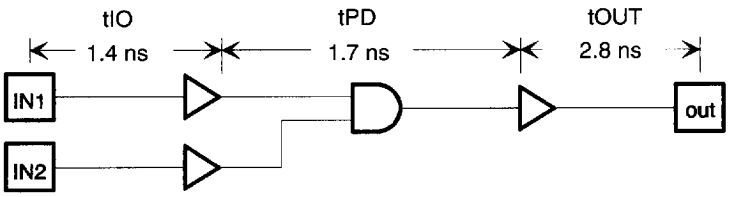
Timing Waveforms





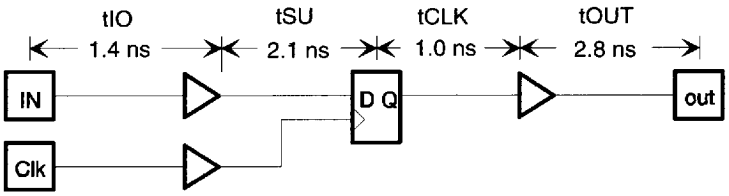
Combinatorial Delay Example

Nominal I/O Delays Load = 30 pF



Input Delay + Combinatorial Delay + Output Delay = 5.9 ns

Sequential Delay Example



Input Delay + Reg Setup + Clock to Output + Output Delay = 7.3 ns

ORDERING INFORMATION

QL 8x12B -1 PL68 C

- **QL** — QuickLogic pASIC device prefix
- **8x12B** — pASIC device part number for 8 by 12 array of 96 logic cells
- **-1** — Speed Grade (see data sheet)
- **PL68** — Package Code
  - First Letter
    - P = Plastic
    - C = Ceramic
  - Second Letter
    - L = LCC
    - F = QFP
    - G = PGA
  - Number of Leads
    - 68 = 68 Leads
- **C** — Operating Range
  - C = Commercial
  - I = Industrial
  - M = Military