

# HG62F SERIES

## (Hitachi CMOS Gate Array)

### High I/O to Gate Ratio

JANUARY, 1990



The F series consists of 6 masterslices ranging from 2,178 to 10,076 available gates with high I/O pin counts ranging from 136 pins to 208 pins.

The HG62F series is a mastersliced gate array fabricated on 1.0  $\mu\text{m}$  CMOS process with double metal interconnect technology and has a capability of Auto-diagnosis support.

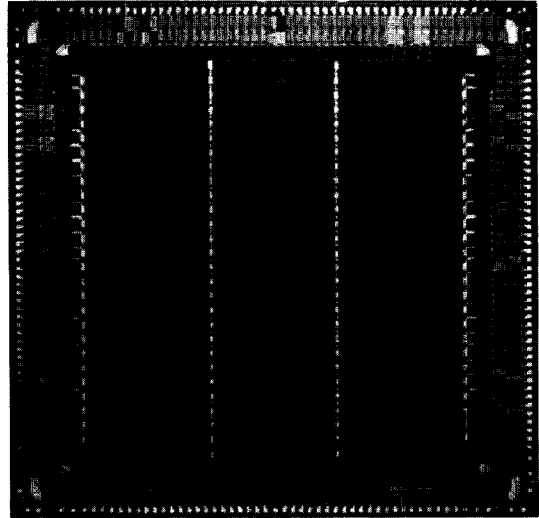
Internal gate delay time is as low as 0.7 nanosecond per gate and output buffer speed is improved as 3.5 ns with maximum drivability of 24 mA output current.

As LSI design is fully automated by DA (Design Automation) system, a desirable LSI can be designed in a short development turn around time by user description of logic diagrams and test vectors.

#### ■ FEATURES

- **High I/O pin counts**  
20 to 50% improvement in a comparison with current HG62E series.  
\* ex. maximum 152 I/O signal pads for 4,309 gates
- **Auto-diagnosis**  
Automatic test circuit and test pattern generation
- **High speed operation**  
Internal gate (2 input NAND, FO = 2, AI = 2 mm) . . . 0.7 ns typ.  
Input buffer (FO = 2, AI = 2 mm) . . . . . 1.2 ns typ.  
Output buffer ( $C_L = 50$  pF) . . . . . 3.5 ns typ.
- **High drivability output**  
Selective buffers with  $I_{OL} = 8$  mA or 24 mA
- **Low power dissipation**  
Internal gate at 10 MHz operation . . . . . 200  $\mu\text{W/gate}$  typ.
- **Flexible input and output variations**  
Input, output and I/O common buffers  
Choice of CMOS and TTL I/O interface  
Noise reduced output buffers for simultaneous switching operation  
Oscillator, Schmitt inputs, pull up/down resistors etc.
- **Design support environment**  
Hierarchical design capabilities  
Fault simulator availability for test pattern evaluation  
Automatic test pattern generation  
Local design support centers  
Variety of EWS interface designs  
DAISY, MENTOR, VALID, SYNOPSIS & VERILOG® supported.
- **Quick development turn around time**

Verilog® is a registered trademark of Gateway Design Automation Corporation.



## ■ LINE UP

		HG62F22	HG62F33	HG62F43	HG62F58	HG62F75	HG62F101
Gate count		2,178	3,297	4,309	5,821	7,488	10,076
Package type and max. available Signal pin number	QFP-100	○96	○96	○96			
	QFP5-136	○128	○128	○128	○128	○128	
	QFP5-168			○152	○152	○152	○152
	QFP5-208					○192	○192

Notes QFP : QFP1420  
QFP5: QFP2828

## ■ ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Rating	Unit
Supply Voltage		$V_{CC}$	-0.3 to +6.7	V
Terminal Voltage	Input	$V_{TI}$	-0.3 to +6.7	V
	Output	$V_{TO}$	-0.3 to $V_{CC}+0.3$	V
Output Current	per one output	$I_O$	-32 to +32	mA
	per one $V_{CC}$ -GND	$I_{OT}$	-70 to +70	mA
Operating Temperature		$T_{opr}$	-20 to +75	°C
Storage Temperature	with Bias	$T_{bias}$	-20 to +85	°C
	without Bias	$T_{stg}$	-55 to +125	°C

## ■ ELECTRICAL CHARACTERISTICS

- $V_{CC} = 5\text{ V} \pm 5\%$ ,  $T_a = 0\text{ to }+70^\circ\text{C}$

Item	Symbol	Test Conditions	min.	typ.	max.	Unit	
Input Voltage (TTL Level)	$V_{IHT}$		2.2	-	$V_{CC}+0.3$	V	
	$V_{ILT}$		-0.3	-	0.8	V	
Input Voltage (CMOS Level)	$V_{IHC}$		$0.7 \times V_{CC}$	-	$V_{CC}+0.3$	V	
	$V_{ILC}$		-0.3	-	$0.3 \times V_{CC}$	V	
Schmitt Trigger (TTL Level)	$V_{TT}^*$	$V_{CC} = 5\text{ V}$	1.5	-	2.5	V	
	$V_{TT}^-$	$V_{CC} = 5\text{ V}$	0.5	-	1.5	V	
	$\Delta V_{TT}$	$V_{CC} = 5\text{ V}$	0.3	-	-	V	
Schmitt Trigger (CMOS Level)	$V_{TC}^+$	$V_{CC} = 5\text{ V}$	2.8	-	4.0	V	
	$V_{TC}^-$	$V_{CC} = 5\text{ V}$	1.2	-	2.4	V	
	$\Delta V_{TC}$	$V_{CC} = 5\text{ V}$	0.3	-	-	V	
Output Voltage ( $I_{OL} = 2\text{ mA}$ )	$V_{OH}$	TBD	-	-	-	V	
	$V_{OL}$		-	-	-	V	
Output Voltage ( $I_{OL} = 8\text{ mA}$ )	$V_{OH}$	$I_{OH} = -2\text{ mA}$	3.5	-	-	V	
	$V_{OL}$	$I_{OL} = 8\text{ mA}$	-	-	0.4	V	
Output Voltage ( $I_{OL} = 12\text{ mA}$ )	$V_{OH}$	TBD	-	-	-	V	
	$V_{OL}$		-	-	-	V	
Output Voltage ( $I_{OL} = 24\text{ mA}$ )	$V_{OH}$	$I_{OH} = -12\text{ mA}$	3.5	-	-	V	
	$V_{OL}$	$I_{OL} = 24\text{ mA}$	-	-	0.4	V	
Input Leakage Current	$I_{LI}$		-	-	1	$\mu\text{A}$	
Output Leakage Current	$I_{LO}$	at high impedance	-	-	1	$\mu\text{A}$	
Pull-up Current	$I_{PU}$	$V_{IN} = \text{GND}$	80	220	550	$\mu\text{A}$	
Pull-down Current	$I_{PD}$	$V_{IN} = V_{CC}$	80	220	550	$\mu\text{A}$	
Gate Delay	Internal	$t_{pd}$	2 input NAND, FO = 2, A $\ell$ = 2 mm		-	0.7	ns
	Input Buffer	$t_{pd}$	FO = 2, A $\ell$ = 2 mm		-	3.5	ns
	Output Buffer	$t_{pd}$	$C_L = 50\text{ pF}$		-	1.2	ns
Power Dissipation	$I_{CC}$	Internal 2 input NAND at 10 MHz	-	40	-	$\mu\text{A}/\text{Gate}$	

- $V_{CC} = 5\text{ V} \pm 5\%$ ,  $T_a = -20\text{ to }+75^\circ\text{C}$

Item	Symbol	Test Conditions	min.	typ.	max.	Unit	
Input Voltage (TTL Level)	$V_{IHT}$		2.4	–	$V_{CC}+0.3$	V	
	$V_{ILT}$		–0.3	–	0.8	V	
Input Voltage (CMOS Level)	$V_{IHC}$		$0.7 \times V_{CC}$	–	$V_{CC}+0.3$	V	
	$V_{ILC}$		–0.3	–	$0.3 \times V_{CC}$	V	
Schmitt Trigger (TTL Level)	$V_{TT}^*$	$V_{CC} = 5\text{ V}$	1.5	–	2.5	V	
	$V_{TT}^-$	$V_{CC} = 5\text{ V}$	0.5	–	1.5	V	
	$\Delta V_{TT}$	$V_{CC} = 5\text{ V}$	0.3	–	–	V	
Schmitt Trigger (CMOS Level)	$V_{TC}^*$	$V_{CC} = 5\text{ V}$	2.8	–	4.0	V	
	$V_{TC}^-$	$V_{CC} = 5\text{ V}$	1.2	–	2.4	V	
	$\Delta V_{TC}$	$V_{CC} = 5\text{ V}$	0.3	–	–	V	
Output Voltage ( $I_{OL} = 2\text{ mA}$ )	$V_{OH}$	TBD	–	–	–	V	
	$V_{OL}$		–	–	–	V	
Output Voltage ( $I_{OL} = 8\text{ mA}$ )	$V_{OH}$	$I_{OH} = -2\text{ mA}$	3.5	–	–	V	
	$V_{OL}$	$I_{OL} = 8\text{ mA}$	–	–	0.4	V	
Output Voltage ( $I_{OL} = 12\text{ mA}$ )	$V_{OH}$	TBD	–	–	–	V	
	$V_{OL}$		–	–	–	V	
Output Voltage ( $I_{OL} = 24\text{ mA}$ )	$V_{OH}$	$I_{OH} = -12\text{ mA}$	3.5	–	–	V	
	$V_{OL}$	$I_{OL} = 24\text{ mA}$	–	–	0.4	V	
Input Leakage Current	$I_{LI}$		–	–	1	$\mu\text{A}$	
Output Leakage Current	$I_{LO}$	at high impedance	–	–	1	$\mu\text{A}$	
Pull-up Current	$I_{PU}$	$V_{IN} = \text{GND}$	80	220	550	$\mu\text{A}$	
Pull-down Current	$I_{PD}$	$V_{IN} = V_{CC}$	80	220	550	$\mu\text{A}$	
Gate Delay	Internal	$t_{pd}$	2 input NAND, FO = 2, A $\ell$ = 2 mm	–	0.7	–	ns
	Input Buffer	$t_{pd}$	FO = 2, A $\ell$ = 2 mm	–	1.2	–	ns
	Output Buffer	$t_{pd}$	$C_L = 50\text{ pF}$	–	3.5	–	ns
Power Dissipation	$I_{CC}$	Internal 2 input NAND at 10 MHz	–	40	–	$\mu\text{A}/\text{Gate}$	

#### ■ TERMINAL CAPACITANCE ( $T_a = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ )

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
Terminal Capacitance	$C_T$	$V_{in} = 0\text{ V}$	–	–	12.5	pF

\*This parameter is sampled and not 100% tested.

■ DEVELOPMENT FLOW

Development flow of gate arrays is shown below. Logic design and test patterns development are done by users. These are fed to a computer which performs logic simulation. The machine drawn logic diagram is checked by the user. After the logic simulation and timing rule check, fault simulation is performed with test patterns designed by user to verify logic design. Auto-diagnosis detects the faults which fault simulation could not find. Then automatic layout and delay check of critical path are performed. After these design check, PG tape and test tape are generated. Sample production takes very short time because it needs only metal wiring on inventory wafers.

Finished wafers are probed with following two test patterns,

of users design and auto-generation, then assembled, tested again and shipped.

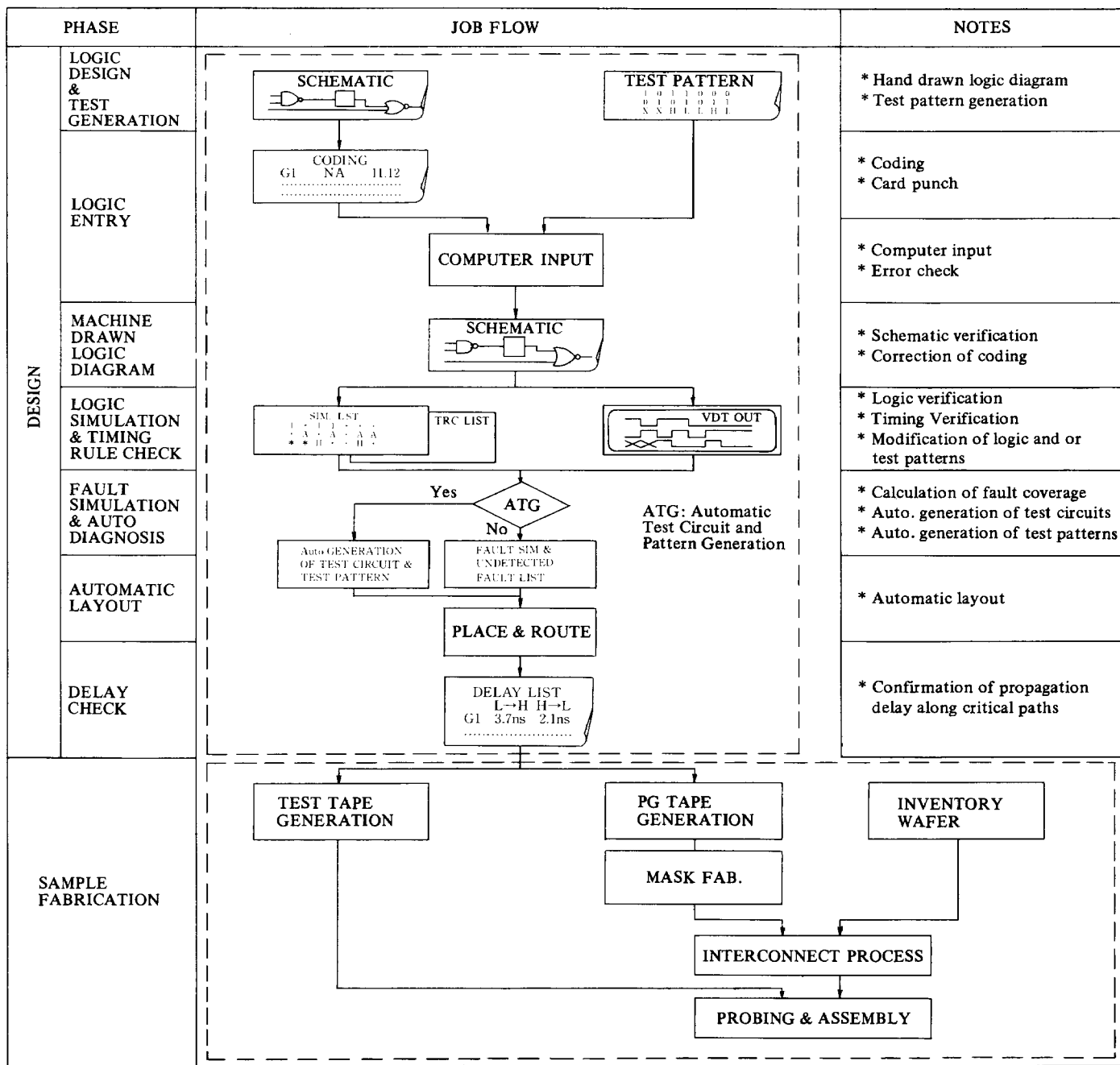
There are two standard interfaces between a user and Hitachi, Namely:

(1) Logic diagram interface

The user supplies logic diagram and test patterns to Hitachi. Further jobs are done by Hitachi except for some confirmation by the user.

(2) Logic file interface

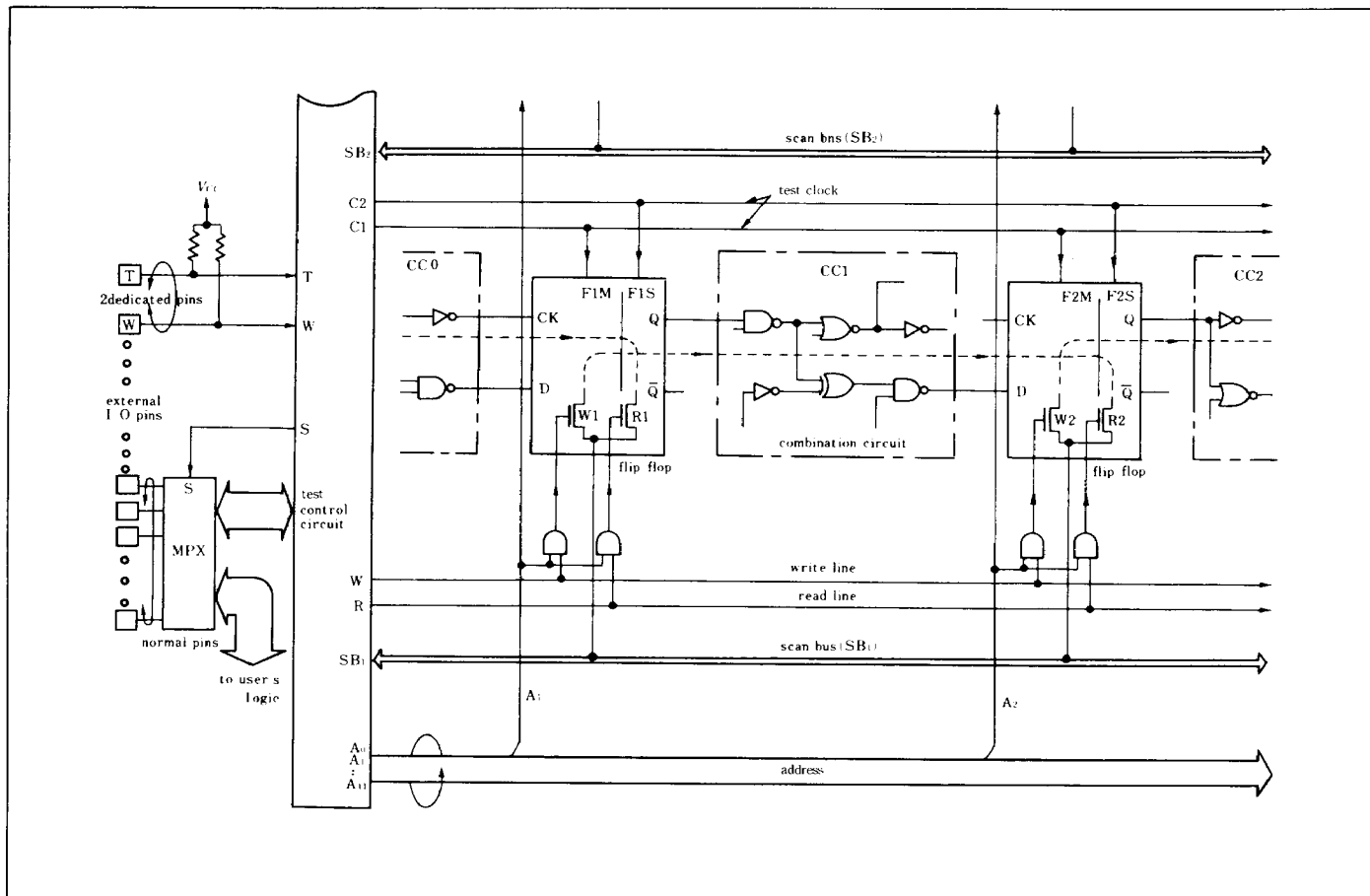
The user performs simulations by himself on his EWS, simulator or Hitachi's terminal for design. Then the user supplies Hitachi with complete logic file. Our engineers are willing to support the customer.



■ AUTO-DIAGNOSIS

Following is a schematic diagram of auto-diagnosis using scan bus. Auto-diagnosis requires such signals as address and scan bus assigned to flip-flop, read/write line, test clock etc. Diagnosis control circuit including address decoder controls these signals. Normal pin can be used as the pin of address and scan bus. Two test dedicated pins are required to control

the test control circuit. Use flip-flops with scan (read/write) function, which consist of master part (performs normal functions) and slave part (latches data for a time). When you design logic, it is not necessary to take the circuits mentioned before into consideration.



The algorithm of combination circuit is not so complex, it is possible to generate high fault coverage of test patterns. But if the circuit includes flip-flops, it is difficult to get high fault coverage. Entire circuit is partitioned into combination circuits separated by flip-flops. Flip-flops are regarded as I/O terminals using scan bus. DA will generate the test patterns of every combination circuit separated by flip-flops.

● Procedure

(1) Auto-generation of test circuit

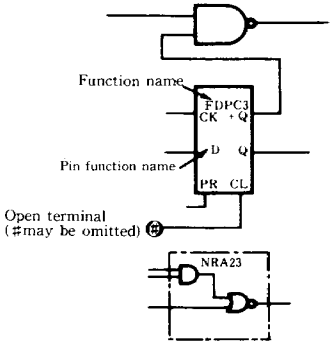
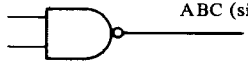
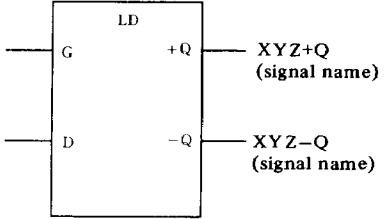
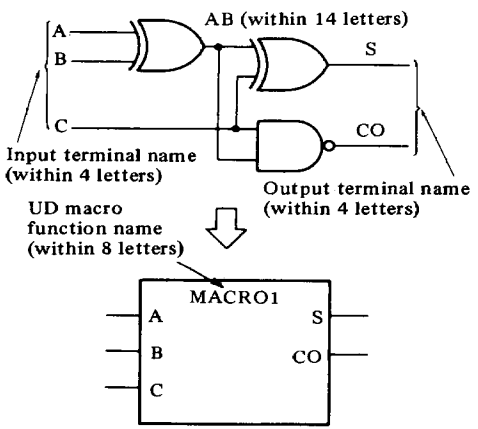
DA system will generate all test circuits; test control circuit, multiplexer, address, scan bus and clock after the logic verification by simulation.

(2) Auto-generation of test patterns

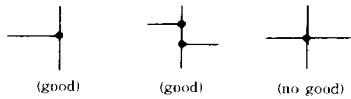
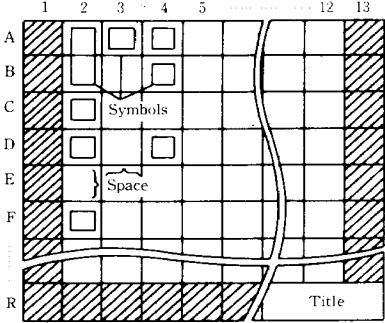
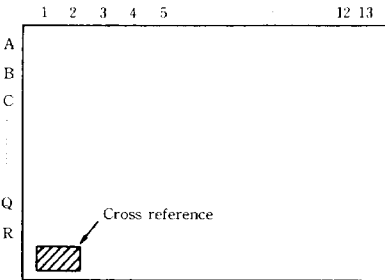
DA system will generate test patterns. The following is an example of testing combination circuit CC1 in the diagram.

- ① Scan in the data for CC1 testing at the slave side of flip-flop. Select address A<sub>1</sub>, then data is transmitted by the route of external I/O Pin → Scan bus (SB<sub>1</sub>) → W<sub>1</sub> → F<sub>1</sub>M → F<sub>1</sub>S.
- ② The data passed CC1 is transmitted to flip-flop. The circuit becomes normal operation mode and the data is transmitted by the route of F<sub>1</sub>S → CC1 → F<sub>2</sub>M.
- ③ The data in flip-flop is scanned out on external I/O Pin. Select address A<sub>2</sub>, then data is transmitted by the route of F<sub>2</sub>M → F<sub>2</sub>S → SB<sub>1</sub> → external I/O Pin.

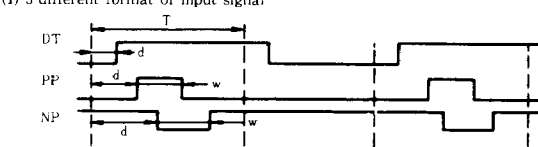
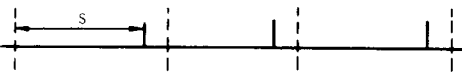
Apply these procedure to generate high fault coverage of test patterns based on the fault detection algorithm of combination circuit.

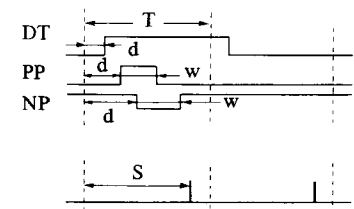
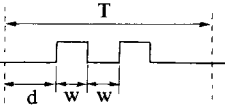
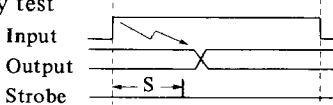
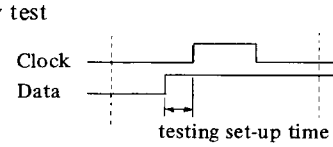
No.	Item	Rules	Examples										
1.	Forms	Size A-3 forms supplied by Hitachi											
2.	Logic symbol	(1) Draw logic diagram with exactly the same symbols as shown in Macrocell Library including function name, terminal name and the size. (2) The internal symbol surrounded by dotted line can be omitted but macro function name must be described and the position of terminal can not be changed instead. (3) The template shall be provided. (4) 3-state gate will occupy 2 blocks in the drawing form.											
3.	Characters	(1) 2 to 3mm higher or larger alphabets, +, -, 0 to 9 in total 38 characters. (2) The letters shown in the table must be written as in the bottom column.	<table border="1" data-bbox="1044 661 1439 735"> <tr> <td>Alphabet</td> <td>I</td> <td>J</td> <td>O</td> <td>U</td> </tr> <tr> <td>Script</td> <td>i</td> <td>j</td> <td>ō</td> <td>u</td> </tr> </table>	Alphabet	I	J	O	U	Script	i	j	ō	u
Alphabet	I	J	O	U									
Script	i	j	ō	u									
4.	Signal/element name	(1) Give name all LSI pins within 8 letters. (2) Give name elements and internal signals within 14 letters. You can use different names for element and its output signal. For easy reference of signal name, (a) Use same name for a element and its output when it has only one output signal. (b) For the output signal names, use the combined names of element and its output terminals, when it has two or more output terminals. (c) It is easier to name a macrocell by using its location and page number of logic diagram.	<p>ABC (element name)</p>  <p>XYZ (element name)</p> 										
5.	Hierarchical design	The user can define his own macrocell as block (UD macro) and also can define blocks within the block. (1) Give name to the macrocells which composes UD macro within 14 letters. (2) Name input and output terminals of UD macro within 4 letters. (3) Give functional name to UD macro within 8 letters. Don't use letter '-' (minus) in the UD macro name. (4) For the symbol size of a UD macro, the width is the 'A' size of the template. Hight can be determined in proportion to the number of input or output terminals.											

(to be continued)

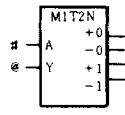
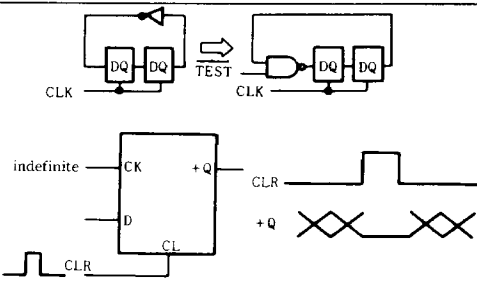
No.	Item	Rules	Examples
		<p>Now, UD-macro can be used in a same way as macrocells in cell library.</p> <p>For users' convenience it is recommended to give element or signal names 8 letters or less.</p> <p>User has to deal with the longer names proportion to the depth of hierarchical level in the simulation.</p>	
6.	Signal line	<p>(1) LSI input/output signal must be shown by and LSI pin number in [ ].</p> <p>(2) Up to three lines can be connected to one junction point</p>	
7.	Symbol layout	<p>(1) A signal should flow from left to right.</p> <p>(2) No symbol is allowed to be placed in the first, the 13th column and in the R row. (Shadow area)</p> <p>(3) Keep at least one spacing row every four adjacent occupied rows to keep area for wiring.</p> <p>(4) Keep at least one spacing column in every other column, to assure indication of signal names.</p>	
8.	Cross reference	<p>(1) When signal line extends to another sheet of machine drawing, following informations are indicated automatically.</p> <p><u>K...15</u>, <u>B-10</u></p> <p>→logic location to be connected</p> <p>→page number of logic diagram to be connected</p> <p>→terminal specification of signal destination</p> <p>K . . . . Sink  S . . . . Source  Z . . . . 3-state output  N . . . . 3-state control</p>	

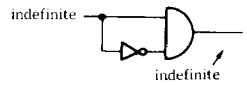
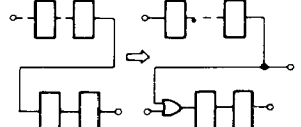
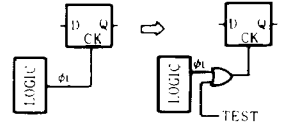
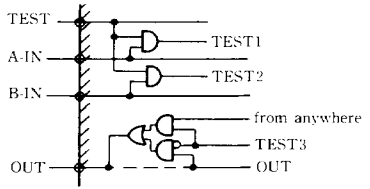
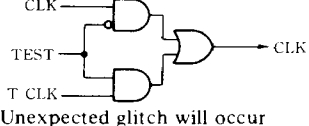
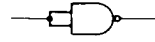
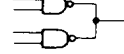
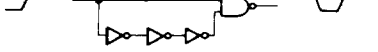
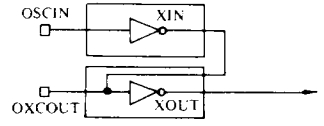
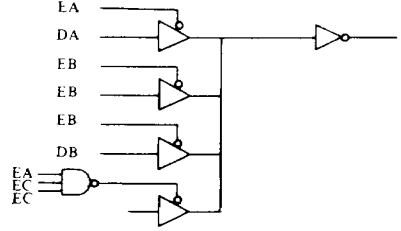
■ DESTINATION OF TEST PATTERNS

No.	Item	Rules	Examples																																																																																																											
1.	Timing format	<p>(1) 3 different format of input signal</p>  <p>(2) 1 strobe timing for output</p> 	<table border="1" data-bbox="1008 241 1478 577"> <thead> <tr> <th colspan="2">Test Rate</th> <th colspan="3">300 ns</th> </tr> <tr> <th>Timing No.</th> <th>Format</th> <th>d(ns)</th> <th>w(ns)</th> <th></th> </tr> </thead> <tbody> <tr> <td>I<sub>0</sub></td> <td>DT</td> <td>—</td> <td>—</td> <td></td> </tr> <tr> <td>I<sub>1</sub></td> <td>DT</td> <td>20</td> <td>—</td> <td></td> </tr> <tr> <td>I<sub>2</sub></td> <td>PP</td> <td>50</td> <td>150</td> <td></td> </tr> <tr> <td>I<sub>3</sub></td> <td>NP</td> <td>70</td> <td>100</td> <td></td> </tr> <tr> <td>I<sub>4</sub></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>I<sub>5</sub></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>I<sub>6</sub></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>Output</td> <td>O<sub>1</sub></td> <td colspan="3">250 ns</td> </tr> </tbody> </table> <p>[Notes] 1. Number of input timing pulses: up to 7. 2. I<sub>0</sub> must be DT format with d = 0.</p>	Test Rate		300 ns			Timing No.	Format	d(ns)	w(ns)		I <sub>0</sub>	DT	—	—		I <sub>1</sub>	DT	20	—		I <sub>2</sub>	PP	50	150		I <sub>3</sub>	NP	70	100		I <sub>4</sub>					I <sub>5</sub>					I <sub>6</sub>					Output	O <sub>1</sub>	250 ns																																																											
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2.	Test patterns	<p>(1) Specify signal order. iT = input (TTL Level) iC = input (CMOS Level) iTO = I/O (TTL Level) iCO = I/O (CMOS Level) OT = output OZ = 3-state output ODN = open drain output</p> <p>(2) Describe test pattern with following expression. Horizontal axis shows time.</p> <table border="1" data-bbox="485 997 931 1113"> <thead> <tr> <th>Input</th> <th>Format</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td></td> <td>DT format</td> <td>0,1</td> </tr> <tr> <td></td> <td>PP format</td> <td>0,P</td> </tr> <tr> <td></td> <td>NP format</td> <td>1,N</td> </tr> <tr> <td>Output</td> <td></td> <td>H, L, Z, X, M</td> </tr> </tbody> </table> <p>(Note 1) P or N shows an active pulse in PP and NP format. (Note 2) Z . . . . high impedance X . . . . indefinite or masked M . . . . masked (Note 3) Black can be applied for no signal change.</p> <p>(3) When the same patterns are repeated, describe the following at the beginning of signal block.</p> <p>HORIZONTAL sc, ec; s<sub>1</sub>, e<sub>1</sub>, n<sub>1</sub> / s<sub>2</sub>, e<sub>2</sub>, n<sub>2</sub> / ..</p> <div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 10px auto;"> <p>Signal block</p> </div> <p>sc~ec: valid column range for test patterns n<sub>i</sub> : repeat number s<sub>i</sub> : start column of repeat e<sub>i</sub> : end column of repeat</p>	Input	Format	Value		DT format	0,1		PP format	0,P		NP format	1,N	Output		H, L, Z, X, M	<table border="1" data-bbox="1008 735 1478 966"> <thead> <tr> <th>Signal name</th> <th>I/O Format</th> <th>Pin No.</th> <th>Timing</th> </tr> </thead> <tbody> <tr> <td>INP-1</td> <td>iT</td> <td>15</td> <td>I<sub>1</sub></td> </tr> <tr> <td>INP-2</td> <td>iC</td> <td>7</td> <td>I<sub>3</sub></td> </tr> <tr> <td>⋮</td> <td></td> <td></td> <td></td> </tr> <tr> <td>BUS-1</td> <td>iTO</td> <td>41</td> <td>I<sub>0</sub></td> </tr> <tr> <td>⋮</td> <td></td> <td></td> <td></td> </tr> <tr> <td>OUT-1</td> <td>OT</td> <td>22</td> <td></td> </tr> <tr> <td>⋮</td> <td></td> <td></td> <td></td> </tr> </tbody> </table> <p>[Notes] 1. Signal name order may be free 2. BUS-1 input timing is I<sub>0</sub> and output strobe timing is O.</p> <div style="border: 1px solid black; padding: 5px; margin: 10px auto; width: fit-content;"> <p>1      5      10      15      20      25      30</p> <p>HORIZONTAL 1, 30; 5, 10, 6/20, 25, 10</p> <table border="1" style="width: 100%; text-align: center;"> <tr> <td>0</td><td>1</td><td></td><td>0</td><td></td><td>1</td><td></td><td>0</td><td></td><td>1</td><td></td><td>0</td> </tr> <tr> <td>1</td><td></td><td>0</td><td></td><td>1</td><td></td><td>0</td><td></td><td>1</td><td></td><td>0</td><td></td> </tr> <tr> <td>0</td><td></td><td>X</td><td>H</td><td>L</td><td></td><td>Z</td><td>0</td><td></td><td>L</td><td></td><td>H</td> </tr> <tr> <td>X</td><td>H</td><td></td><td>L</td><td></td><td></td><td></td><td>H</td><td></td><td></td><td></td><td>L</td> </tr> <tr> <td>H</td><td></td><td>L</td><td></td><td></td><td>H</td><td></td><td></td><td></td><td></td><td>L</td><td></td> </tr> </table> </div> <p>[Note] "HORIZONTAL" line shows the start column and end column of described patterns together with the conditions for repeating.</p>	Signal name	I/O Format	Pin No.	Timing	INP-1	iT	15	I <sub>1</sub>	INP-2	iC	7	I <sub>3</sub>	⋮				BUS-1	iTO	41	I <sub>0</sub>	⋮				OUT-1	OT	22		⋮				0	1		0		1		0		1		0	1		0		1		0		1		0		0		X	H	L		Z	0		L		H	X	H		L				H				L	H		L			H					L	
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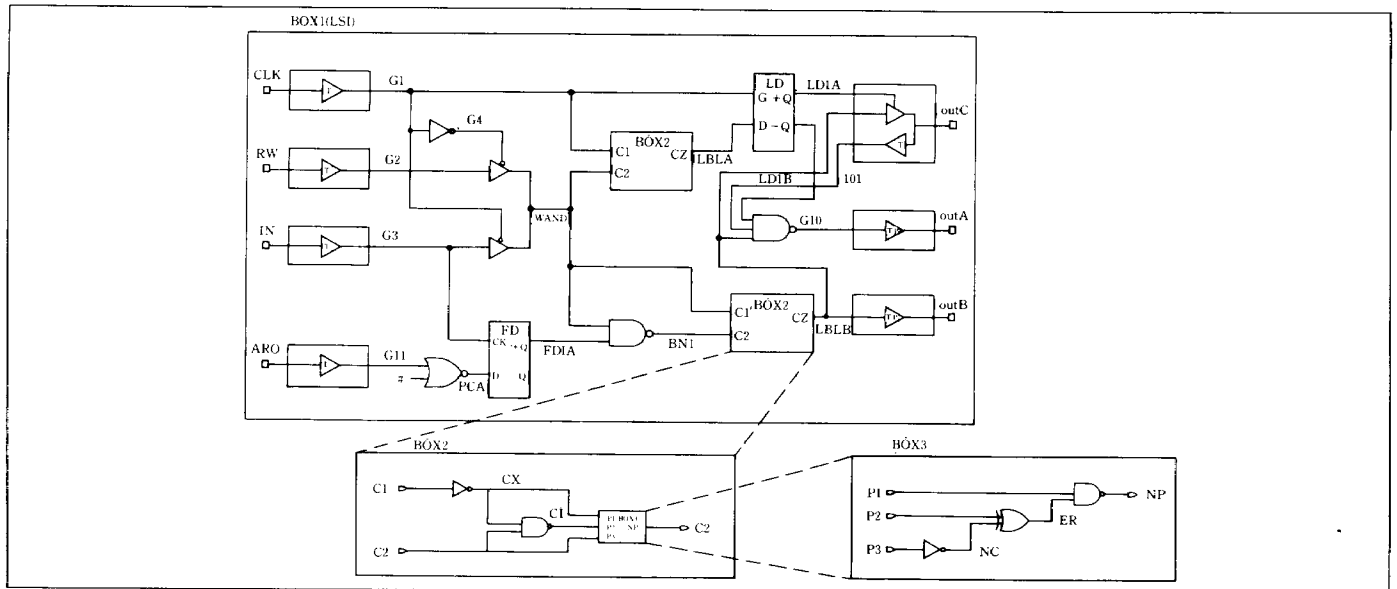
No.	Item	Rules	Examples																				
3	Fault coverage and auto-generation of test patterns	<p>(1) Auto generated test patterns detects the faults which test patterns of user's design have not detected. Two test patterns, of user's design and auto-generation, are available for final testing of products.</p> <p>(2) Auto-generated test patterns is to increase the fault coverage. It disregards the real time function of user's hardware. Therefore, user has to design test patterns taking real time function into consideration. When auto-diagnosis is not required, the final test of products is performed only with test patterns designed for logic verification. Fault coverage of test patterns shall be as high as possible (final target <math>\geq 95\%</math>). Undetected faults by the test patterns is strongly suggested to be checked in the system test at the user's assembly line.</p>																					
4	Contents of test patterns	<p>It is requested to submit following two test patterns, functional test patterns and high speed test patterns which are generated under the timing restriction shown below respectively. In low speed application, it is allowed to omit high speed test patterns.</p> <p>(1) Functional test  <math>T \geq 150, d \geq 20, w \geq 50</math>  <math>T - (d + w) \geq 20, 0 \leq S &lt; T</math></p> <p>(2) High speed test                      (a) Cycle test                      To test real dynamic function.                      (b) Delay test                      To measure delay time along specified critical path of input to output.                      (c) Skew test                      To test set up time and hold time.</p> <table border="1" data-bbox="369 1302 947 1459"> <thead> <tr> <th></th> <th>Cycle test</th> <th>Delay test</th> <th>Skew test</th> </tr> </thead> <tbody> <tr> <td>T</td> <td>500</td> <td>500</td> <td>500</td> </tr> <tr> <td>d</td> <td><math>\geq 20</math></td> <td>0</td> <td><math>\geq 20</math></td> </tr> <tr> <td>w</td> <td><math>\geq 12.5</math></td> <td>-</td> <td></td> </tr> <tr> <td>s</td> <td>450</td> <td><math>\geq 0</math></td> <td>450</td> </tr> </tbody> </table>		Cycle test	Delay test	Skew test	T	500	500	500	d	$\geq 20$	0	$\geq 20$	w	$\geq 12.5$	-		s	450	$\geq 0$	450	<p>(1) Functional test</p>  <p>(2) High speed test</p> <p>(a) Cycle test                      Corresponding 40 MHz                      When assuming <math>w = 12.5</math></p>  <p>(b) Delay test</p>  <p>(c) Skew test</p> 
	Cycle test	Delay test	Skew test																				
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d	$\geq 20$	0	$\geq 20$																				
w	$\geq 12.5$	-																					
s	450	$\geq 0$	450																				
5	Limitation of test patterns	<p>(1) Up to 10 sets of test patterns.                      (2) Up to 30000 test cycles after expanding the repeat in a set of test patterns.                      (3) Total steps for all sets of test patterns. (Repeat is counted as 1 time) is limited as shown in table on right.</p>	<table border="1" data-bbox="977 1533 1463 1690"> <thead> <tr> <th></th> <th>Functional test</th> <th>High speed test</th> </tr> </thead> <tbody> <tr> <td>F22~F43</td> <td>4000</td> <td rowspan="3">4000</td> </tr> <tr> <td>F58</td> <td>6000</td> </tr> <tr> <td>F75</td> <td>8000</td> </tr> <tr> <td>F101</td> <td>11000</td> <td>8000</td> </tr> </tbody> </table>		Functional test	High speed test	F22~F43	4000	4000	F58	6000	F75	8000	F101	11000	8000							
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■ NOTES FOR LOGIC DESIGN

No.	Item	Notes													
1.	Utilization	<p>Must be 90% or less in order to place and route successfully. When auto-diagnosis is used, must be 85% or less.</p> <p>Auto-diagnosis causes overhead. You have to take overhead into consideration when auto-diagnosis is required.</p> <p>The estimation of overhead depends on the numbers of latches, flip-flops and shift resistors (<math>N_F</math>). The right equation shows the calculation.</p>	<p>Maximum gate counts to be used actually.</p> <table border="1"> <thead> <tr> <th>F22</th> <th>F33</th> <th>F43</th> <th>F58</th> <th>F75</th> <th>F101</th> </tr> </thead> <tbody> <tr> <td>1960 (1850)</td> <td>2970 (2800)</td> <td>3880 (3660)</td> <td>5240 (4950)</td> <td>6740 (6360)</td> <td>9070 (8560)</td> </tr> </tbody> </table> <p>( ) : When auto-diagnosis is used.</p> <p>[Maximum gate counts] <math>\geq</math> (gate counts in user's logic) + 1.7 × <math>N_F</math></p>	F22	F33	F43	F58	F75	F101	1960 (1850)	2970 (2800)	3880 (3660)	5240 (4950)	6740 (6360)	9070 (8560)
F22	F33	F43	F58	F75	F101										
1960 (1850)	2970 (2800)	3880 (3660)	5240 (4950)	6740 (6360)	9070 (8560)										
2.	Auto-diagnosis	<p>(1) Need two test dedicated pins.</p> <p>(2) Use latch, flip-flop and shift resistor with scan function.</p>													
3.	Gate delay	<p>Gate delay is obtained more accurately after place and route. However rough estimate should also be done using the equations shown right to prevent timing design errors in the earlier design phase.</p> <p>Effective Fan Out is calculated as sum of Normalized Loading Factor of the output node. These equation may contain the design margin a little bit.</p>	<div style="border: 1px solid black; padding: 5px; width: fit-content;"> <math display="block">t_{PLH} = t_{OLH} + K_{LH} \cdot C_L</math> <math display="block">t_{PHL} = t_{OHL} + K_{HL} \cdot C_L</math> </div> <p>Where, for internal gates</p> <p><math>C_L = 0.4 \times EFO</math></p> <p><math>EFO = \sum NLF</math></p> <p>Variational range:</p> <p>Min = 0.35 × typ</p> <p>Max = 1.8 × typ</p> <p>(<math>T_a = -20</math> to <math>+75^\circ C</math>, <math>V_{CC} = 5V \pm 5\%</math>)</p>												
4.	Maximum fanout	<p>A clock driver, which drives CK inputs of FF's, has a restriction on the number of applicable fanouts, though the other signals have no limitation if lower speed is acceptable.</p>	<p>○ Max. Fanout of CK driver</p> <p>Power Inverter . . . 20/30/40</p> <p>The others . . . . . 10</p> <p>○ The other signals . . . . . 24</p>												
5.	Automatic Modification of unconnected inputs of macro	<p>When an input of a macro is left unconnected, the automatic router connects it to either VCC ("1" level) or GND ("0" level). The macrocell list shows which input of each macro will be connected to which level.</p> <p>An input of AND or NAND gates will be connected to VCC, and that of OR or NOR gates to GND, even though these are not indicated in the list. "@" beside an input shows that the input will be connected to VCC, and "#" to GND. It is not allowed to leave an input unconnected dropping "@" nor "#" except the cases of AND, NAND, OR or NOR.</p>	 <p>When inputs are left open, input A will be fixed to "0" and input Y will be fixed to "1".</p>												
6.	Simultaneous Turn on/off of Output Buffers	<p>The number of output buffers which simultaneously change their output levels must be equal to or less than the figures in the table respectively depending on the buffers.</p>	<table border="1"> <thead> <tr> <th>Buffer</th> <th>max. number</th> </tr> </thead> <tbody> <tr> <td>OT3, OZ3, ODN3</td> <td>8</td> </tr> <tr> <td>OT3R, OZ3R, ODN3R</td> <td>12</td> </tr> </tbody> </table>	Buffer	max. number	OT3, OZ3, ODN3	8	OT3R, OZ3R, ODN3R	12						
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OT3R, OZ3R, ODN3R	12														
7.	Testing	<p>(1) All the logic must be able to be initialized by external inputs.</p> <p>(2) Restriction due to the Simulator.</p> <p>(a) When one or more inputs associated with FF such as CK, CL and PR is indefinite the output is also indefinite. For example, output of FF will not be fixed when CK input is indefinite even if it is quite evident logically that CK input is stable either in high or low level.</p>													

No.	Item	Notes	
		<p>(b) For the given logical variables X, Y, suppose that there is the following relation between them  <math>X = \bar{Y}</math>                      When X or Y is indefinite, both <math>X + Y</math> and <math>X \cdot Y</math> are also indefinite contrary to the theoretical result.</p>	
		<p>(3) It is preferable to split a multistage shift registers and/or counters to provide test signals in the proper positions in order to improve the efficiency of testing.</p>	
		<p>(4) It is preferable to provide test clock in addition to the original clock whose frequency is much lower than other clocks such as a system clock.</p>	
		<p>(5) The figure shows an example of additional test logic to generate several test signals from a single TEST pin, which is helpful when we suffer from the shortage of pins. Another example shown here is to share the output pin to monitor another internal signal.</p>	
		<p>(6) It is very important to do timing design of test logic as well. Is test logic speed OK? Won't unexpected events occur at the transition time from test to normal mode or contrary?</p>	 <p>Unexpected glitch will occur when TEST turns on/off.</p>
8.	Others	<p>(1) As far as a macro is concerned, one signal is prohibited to be employed to multi-input terminals.</p>	
		<p>(2) Output-to-output connection is not allowed except among 3-state buffers.</p>	
		<p>(3) A chopper circuit using gate delay is prohibited.</p>	
		<p>(4) Oscillator circuit should be built as shown. OSC IN and OSC OUT pins should be assigned next to the pins which never change their levels, such as <math>V_{CC}</math> and GND.</p>	
		<p>(5) Internal bus lines should be prevented from floating. Dummy 3-state buffer is recommended to be added.</p>	

■ LOGIC DIAGRAM



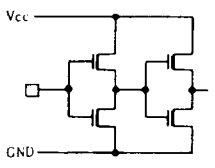
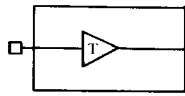
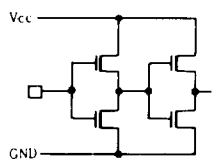
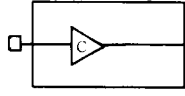
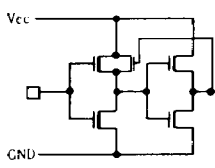
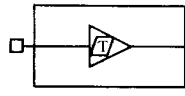
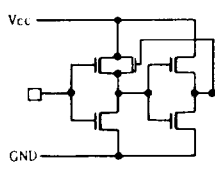
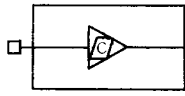
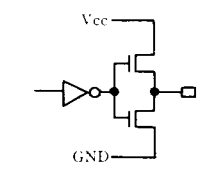
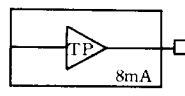
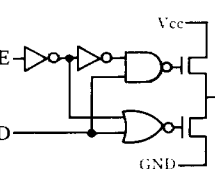
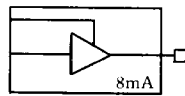
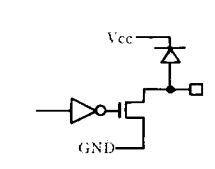
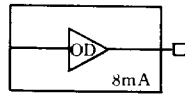
■ EXAMPLE OF LOGIC DESCRIPTION

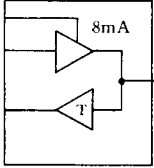
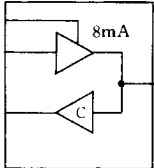
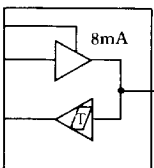
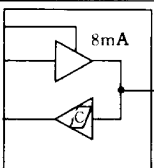
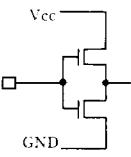
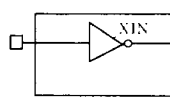
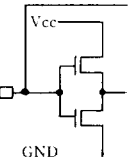
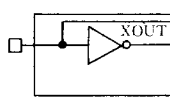
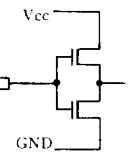
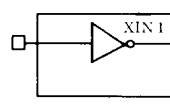
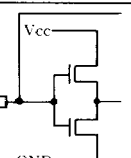
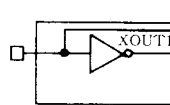
<p>LSI profile</p>	<pre> BEGIN PROFILE BEGIN PRODUCT BOX1 IMPLEMENT GATEARRAY SERIES (HG62F43) ARRAY (HG62F) ROOTBLOCK BOX1 ARRANGE DP40B0 PACKAGE DP40 END PRODUCT END PROFILE         </pre>	<p>Device Type, master type, package type</p>
<p>Schematic description</p>	<pre> BEGIN LOGIC BEGIN BLOCK BOX1 INTERFACE RW, IN, CLK, ARO; OUTB, OUTA; OUTC BEGIN NETLIST G11 (L3, ,1) IT ARO; G11 G1 (B3, ,1) IT CLK; G1 G2 (D3, ,1) IT RW; G2 G3 (F3, ,1) IT IN; G3 AR (L4, ,1) NR2 G11; PCA G4 (C4, ,1) NA1 G1; G4 FD1 (J5, ,1) FD G3, PCA; FD1A G5 (D5, ,1) ANZ G4, G2; WAND G6 (F5, ,1) ANZ G1, G3; WAND BN1 (J6, ,1) NA2 WAND, FD1A,; BN1 LBL2 (G7, ,1) BOX2 BN1, WAND; LBLB LBL1 (C7, ,1) BOX2 WAND, G1; LBLA LD1 (B8, ,1) LD G1, LBLA; LD1A, LD1B G8 (E11, ,1) OT C10; OUTA G7 (G9, ,1) OT LBLB; OUTB G10 (E9, ,1) NA3 IO1, LD1B, LBLB; G10 G9 (C11, ,1) ITO LD1A, LBLB; IO1; OUTC END NETLIST END BLOCK         </pre>	<p>Diagram illustrating the syntax for defining a macro function in a netlist:</p> <p><b>G4 (C4, ,1) NA1 G1; G4</b></p> <ul style="list-style-type: none"> <li><b>G4</b>: Element name</li> <li><b>(C4, ,1)</b>: Location of symbol</li> <li><b>NA1</b>: Macro function name</li> <li><b>G1; G4</b>: Input signal name and Output signal name</li> </ul>

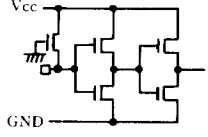
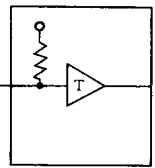
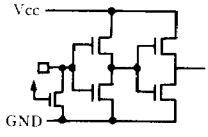
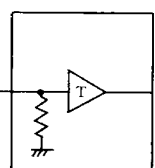
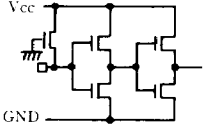
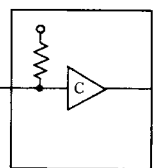
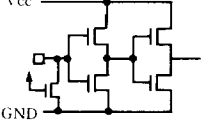
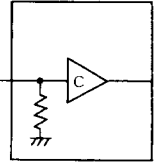
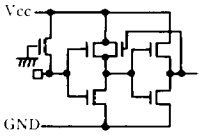
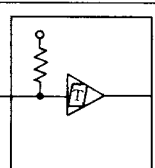
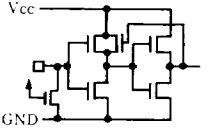
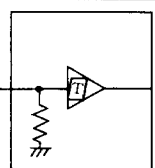
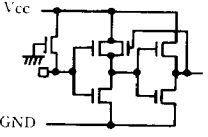
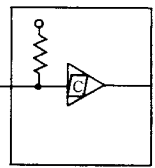
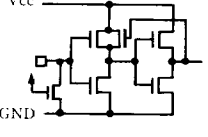
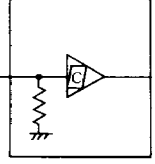
	<pre> BEGIN BLOCK BOX2 INTERFACE C2, C1; CZ SHAPE; J4, 2, A3 BEGIN NETLIST   CX      (D3, ,2)   NA1      C1; CX   CY      (F5, ,2)   NA2      CX, C2; CY   PBK1    (F7, ,2)   BOX3     C2, CY, CX; CZ END NETLIST END BLOCK         </pre>	<p>Description of BOX2 (User defined macro)</p>
	<pre> BEGIN BLOCK BOX3 INTERFACE P3, P2, P1; NP SHAPE; J6, 1, A3 BEGIN NETLIST   NG      (E3, ,3)   NA1      P3; NG   ER      (D4, ,3)   EOR      P2, NG; ER   NP      (B5, ,3)   NAP2     P1, ER; NP END NETLIST END BLOCK END LOGIC         </pre>	<p>Description of BOX3 (User defined macro)</p>
<p>Test patterns</p>	<pre> BEGIN TEST BEGIN PATTERN CASE1 BLOCKNAME BOX1 TIMING TRATE (150. 0N) STRB (120. 0N) BEGIN SIGNAL   ARO      DT (20. 0N)   CLK      DT (0. 0N)   IN       PP (50. 0N, 100. 0N)   OUTA   OUTB   OUTC     DT (0. 0N)   RW       NP (50. 0N, 100. 0N) END SIGNAL         </pre>	<p>Definition of timing</p>
	<pre> BEGIN VECTOR HORIZONTAL 1, 1010101  ARO 1100101  CLK POPOPOP  IN LLLLLLL  OUTA LLLLLLL  OUTB 111H1H1  OUTC N1N1111  RW END VECTOR END PATTERN END TEST         </pre>	<p>Description of test patterns</p> <p>In this case, the horizontal axis shows time, but there is another way of description that the vertical axis shows time.</p>
<p>Verification</p>	<pre> BEGIN VERIFY BEGIN LOGSIM CASE1 TESTNAME CASE1 DELAY TYPICAL LOADC FANOUT DEFAULT STRB (120. 0N) BEGIN MONITOR MON1   BOX1. LBL1. CX STRB (140. 0N)   BOX1. LBL2. CX STRB (140. 0N) END MONITOR COMPARE SRL SIGNAL (EXTERNAL' MONITOR (MON1)) SRF SIGNAL (EXTERNAL, MONITOR (MON1)) ERROR CONFLICT' TIME (10, 0N, 10. 0N) FAULT SEPARATE (1,999), ASSUME (1), DETECT (2), MODIFY STOP 7 END LOGSIM         </pre>	<p>Condition of logic simulation</p>
	<pre> BEGIN TIMING TIM1 TESTNAME CASE1 DELAY TYPICAL LOADC ROUTING END TIMING END VERIFY         </pre>	<p>Specification of timing verification</p>

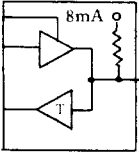
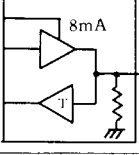
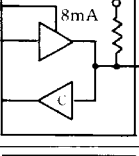
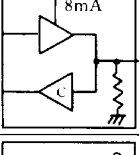
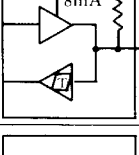
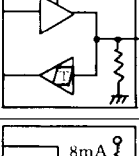
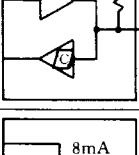
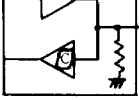
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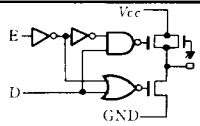
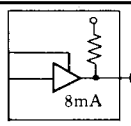
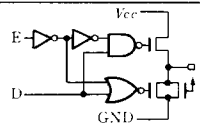
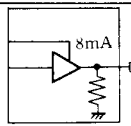
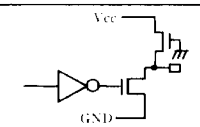
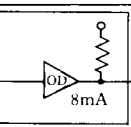
1. Input/Output Buffers

Macrocell		Equiva- lent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						tPLH (ns)		tPHL (ns)	
Macro Function Name							tOLH	kLH	tOHL	kHL
Input Buffer TTL Level		—	—			D1	0.6	0.3	0.8	0.3
IT										
Input Buffer CMOS Level		—	—			D1	0.5	0.3	0.9	0.3
IC										
SCHMITT TTL Level		—	—			D1	2.5	1.3	9.2	2.0
ITS										
SCHMITT CMOS Level		—	—			D1	2.0	0.6	3.6	1.1
ICS										
OUTPUT		—	1.1			D1	1.8	0.06	3.7	0.06
OT3										
3-State OUTPUT		—	1.0 1.4			(E) D1 (D)	2.2	0.06	3.9	0.06
OZ3										
Open Drain Output		—	1.1			D1	(tOLZ) 1.8	(tOZL)	(kZL) 3.7	0.06
ODN3										

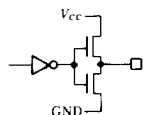
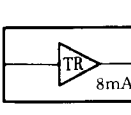
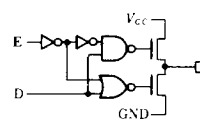
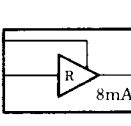
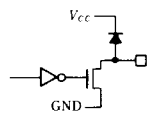
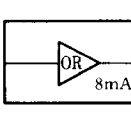
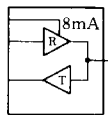
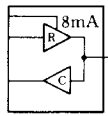
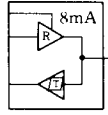
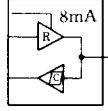
Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Macro Function Name							t <sub>OLH</sub>	k <sub>LH</sub>	t <sub>OHL</sub>	k <sub>HL</sub>
I/O Buffer TTL Level	Output See "3-state"	-	1.0 1.4			D2	Output See "3-state" (OZ3)			
ITO3	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer CMOS Level	Output See "3-state"	-	1.0 1.4			D2	Output See "3-state" (OZ3)			
ICO3	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer TTL SCHMITT Level	Output See "3-state"	-	1.0 1.4			D2	Output See "3-state" (OZ3)			
ITSO3	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer CMOS SCHMITT Level	Output See "3-state"	-	1.0 1.4			D2	Output See "3-state" (OZ3)			
ICSO3	Input See "Input Buffer"						Input See "Input Buffer"			
OSC In 2MHz to 20MHz		-	-			D1	3.1	0.8	3.2	0.8
OSC Out 2MHz to 20MHz		-	-			D1	4.0	1.2	2.5	0.9
OSC In 32kHz to 400kHz		-	-			D1	3.1	40	3.2	40
OSC Out 32kHz to 400kHz		-	-			D1	4.0	1.2	2.5	0.9

Macrocell		Equiva- lent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Macro Function Name							t <sub>OLH</sub>	k <sub>LH</sub>	t <sub>OHL</sub>	k <sub>HL</sub>
Input Buffer TTL Level with Pull-Up  ITU		—	—			D2	0.6	0.3	0.8	0.3
Input Buffer TTL Level with Pull- Down  ITD		—	—			D2	0.6	0.3	0.8	0.3
Input Buffer CMOS Level with Pull-Up  ICU		—	—			D2	0.5	0.3	0.9	0.3
Input Buffer CMOS Level with Pull- Down  ICD		—	—			D2	0.5	0.3	0.9	0.3
Schmitt TTL Level with Pull-Up  ITSU		—	—			D2	2.5	1.3	9.2	2.0
Schmitt TTL Level with Pull- Down  ITSD		—	—			D2	2.5	1.3	9.2	2.0
Schmitt CMOS Level with Pull-Up  ICSU		—	—			D2	2.0	0.6	3.6	1.1
Schmitt CMOS Level with Pull- Down  ICSD		—	—			D2	2.0	0.6	3.6	1.1

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Macro Function Name							t <sub>OLH</sub>	k <sub>LH</sub>	t <sub>OHL</sub>	k <sub>HL</sub>
I/O Buffer TTL Level with Pull-Up ITO3U	Output See "3-state"	—	1.0 1.4			D2	Output See "3-state" (OZ3)			
	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer TTL Level with Pull- Down ITO3D	Output See "3-state"	—	1.0 1.4			D2	Output See "3-state" (OZ3)			
	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer CMOS Level with Pull-Up ICO3U	Output See "3-state"	—	1.0 1.4			D2	Output See "3-state" (OZ3)			
	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer CMOS Level with Pull- Down ICO3D	Output See "3-state"	—	1.0 1.4			D2	Output See "3-state" (OZ3)			
	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer TTL Schmitt Level with Pull-Up ITSO3U	Output See "3-state"	—	1.0 1.4			D2	Output See "3-state" (OZ3)			
	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer TTL Schmitt Level with Pull-Down ITSO3D	Output See "3-state"	—	1.0 1.4			D2	Output See "3-state" (OZ3)			
	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer CMOS Schmitt Level with Pull-Up ICSO3U	Output See "3-state"	—	1.0 1.4			D2	Output See "3-state" (OZ3)			
	Input See "Input Buffer"						Input See "Input Buffer"			
I/O Buffer CMOS Schmitt Level with Pull-Down ICSO3D	Output See "3-state"	—	1.0 1.4			D2	Output See "3-state" (OZ3)			
	Input See "Input Buffer"						Input See "Input Buffer"			

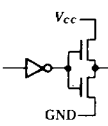
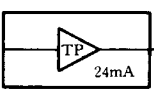
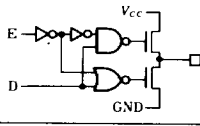
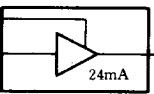
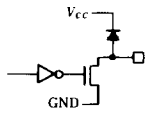
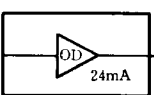
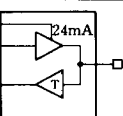
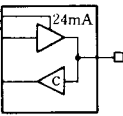
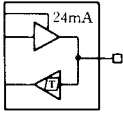
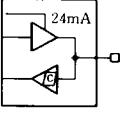
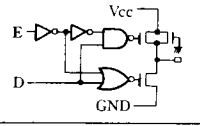
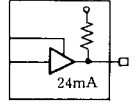
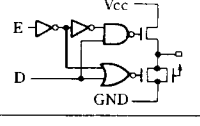
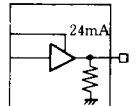
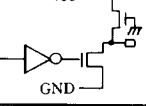
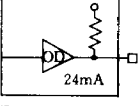
Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Macro Function Name							t <sub>OLH</sub>	k <sub>LH</sub>	t <sub>OHL</sub>	k <sub>HL</sub>
3-State Output with Pull-Up OZ3U		—	1.0 1.4			(E) D2 (D)	2.2 1.8	0.06	3.9 3.7	0.06
3-State Output with Pull-Down OZ3D		—	1.0 1.4			(E) D2 (D)	2.2 1.8	0.06	3.9 3.7	0.06
Open Drain Output with Pull-Up ODN3U		—	1.1			D2	(t <sub>OLZ</sub> ) 1.8	—	(t <sub>OZL</sub> ) 3.7	(k <sub>ZL</sub> ) 0.06

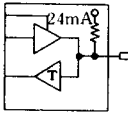
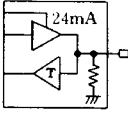
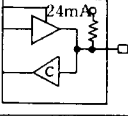
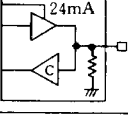
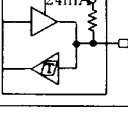
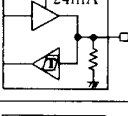
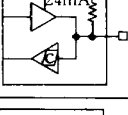
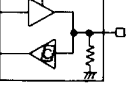
**GND Noise Reduction Buffers**

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Macro Function Name							t <sub>OLH</sub>	k <sub>LH</sub>	t <sub>OHL</sub>	k <sub>HL</sub>
Totem-pole output OT3R		—	1.1			D1	2.8	0.06	11.7	0.06
3-state output OZ3R		—	1.0 1.8			(E) D1 (D)	3.2 2.8	0.06	11.9 11.7	0.06
Open-drain output ODN3R		—	1.1			D1	(t <sub>OLZ</sub> ) 2.8	—	(t <sub>OZL</sub> ) 11.7	(k <sub>ZL</sub> ) 0.06
I/O buffer TTL level ITO3R	Output See "3-state" Input See "Input buffers"	—	1.0 1.8			D2	Output See "3-state" (OZ3R) Input See "Input buffers"			
I/O buffer CMOS level ICO3R	Output See "3-state" Input See "Input buffers"	—	1.0 1.8			D2	Output See "3-state" (OZ3R) Input See "Input buffers"			
I/O buffer TTL Schmitt-trigger ITSO3R	Output See "3-state" Input See "Input buffers"	—	1.0 1.8			D2	Output See "3-state" (OZ3R) Input See "Input buffers"			
I/O buffer CMOS Schmitt-trigger ICSO3R	Output See "3-state" Input See "Input buffers"	—	1.0 1.8			D2	Output See "3-state" (OZ3R) Input See "Input buffers"			


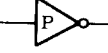

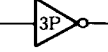

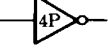

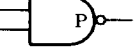

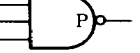

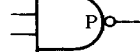
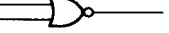

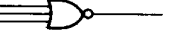




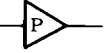

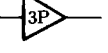

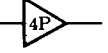
Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Macro Function Name							t <sub>OLH</sub>	k <sub>LH</sub>	t <sub>OHL</sub>	k <sub>HL</sub>
3-state output with Pull-Up OZ3RU		—	1.0 1.8			(E) D2 (D)	3.2 — 2.8	0.06 — 0.06	11.9 — 11.7	0.06 — 0.06
3-state output with Pull-Down OZ3RD		—	1.0 1.8			(E) D2 (D)	3.2 — 2.8	0.06 — 0.06	11.9 — 11.7	0.06 — 0.06
Open-drain output with Pull-Up ODN3RU		—	1.1			D2	(t <sub>OLZ</sub> ) 2.8	—	(t <sub>OZL</sub> ) 11.7	(k <sub>ZL</sub> ) 0.06
I/O buffer TTL level with Pull-Up ITO3RU	Output See "3-state" Input See "Input buffers"	—	1.0 1.8			D2	Output See "3-state" (OZ3R) Input See "Input buffers"			
I/O buffer TTL level with Pull-Down ITO3RD	Output See "3-state" Input See "Input buffers"	—	1.0 1.8			D2	Output See "3-state" (OZ3R) Input See "Input buffers"			
I/O buffer CMOS level with Pull-Up ICO3RU	Output See "3-state" Input See "Input buffers"	—	1.0 1.8			D2	Output See "3-state" (OZ3R) Input See "Input buffers"			
I/O buffer CMOS level with Pull-Down ICO3RD	Output See "3-state" Input See "Input buffers"	—	1.0 1.8			D2	Output See "3-state" (OZ3R) Input See "Input buffers"			
I/O buffer TTL Schmitt-trigger with Pull-Up ITSO3RU	Output See "3-state" Input See "Input buffers"	—	1.0 1.8			D2	Output See "3-state" (OZ3R) Input See "Input buffers"			
I/O buffer TTL Schmitt-trigger with Pull-Down ITSO3RD	Output See "3-state" Input See "Input buffers"	—	1.0 1.8			D2	Output See "3-state" (OZ3R) Input See "Input buffers"			
I/O buffer CMOS Schmitt-trigger with Pull-Up ICSO3RU	Output See "3-state" Input See "Input buffers"	—	1.0 1.8			D2	Output See "3-state" (OZ3R) Input See "Input buffers"			
I/O buffer CMOS Schmitt-trigger with Pull-Down ICSO3RD	Output See "3-state" Input See "Input buffers"	—	1.0 1.8			D2	Output See "3-state" (OZ3R) Input See "Input buffers"			

High Drivability Buffers

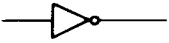

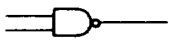





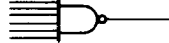
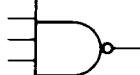
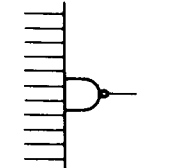
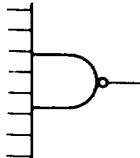
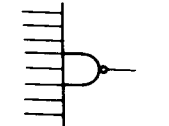
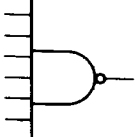
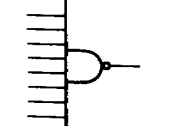
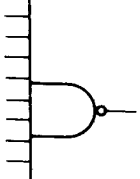
Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Macro Function Name							t <sub>OLH</sub>	k <sub>LH</sub>	t <sub>OHL</sub>	k <sub>HL</sub>
Totem-pole output		—	1.8			D1	1.4	0.04	2.0	0.033
OT5										
3-state output		—	1.0 2.8			(E) D1 (D)	1.8 1.4	0.04	2.2 2.0	0.033
OZ5										
Open-drain output		—	1.8			D1	(t <sub>OLZ</sub> ) 1.4	—	(t <sub>OZL</sub> ) 2.0	(k <sub>ZL</sub> ) 0.033
ODN5										
I/O buffer TTL level	Output See "3-state"	—	1.0 2.8			D2	Output See "3-state" (OZ5)			
ITO5	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer CMOS level	Output See "3-state"	—	1.0 2.8			D2	Output See "3-state" (OZ5)			
ICO5	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer TTL Schmitt-trigger	Output See "3-state"	—	1.0 2.8			D2	Output See "3-state" (OZ5)			
ITSO5	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer CMOS Schmitt-trigger	Output See "3-state"	—	1.0 2.8			D2	Output See "3-state" (OZ5)			
ICSO5	Input See "Input buffers"						Input See "Input buffers"			
3-state output with Pull-Up		—	1.0 2.8			(E) D2 (D)	1.8 1.4	0.04	2.2 2.0	0.033
OZ5U										
3-state output with Pull-Down		—	1.0 2.8			(E) D2 (D)	1.8 1.4	0.04	2.2 2.0	0.033
OZ5D										
Open-drain output with Pull-Up		—	1.8			D2	(t <sub>OLZ</sub> ) 1.4	—	(t <sub>OZL</sub> ) 2.0	(k <sub>ZL</sub> ) 0.033
ODN5U										

Macrocell		Equiva- lent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function Macro Function Name	Equivalent Circuit						t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
							t <sub>OLH</sub>	k <sub>LH</sub>	t <sub>OHL</sub>	k <sub>HL</sub>
I/O buffer TTL level with Pull-Up ITO5U	Output See "3-state"	-	1.0 2.8			D2	Output See "3-state" (OZ5)			
	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer TTL level with Pull-Down ITO5D	Output See "3-state"	-	1.0 2.8			D2	Output See "3-state" (OZ5)			
	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer CMOS level with Pull-Up ICO5U	Output See "3-state"	-	1.0 2.8			D2	Output See "3-state" (OZ5)			
	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer CMOS level with Pull-Down ICO5D	Output See "3-state"	-	1.0 2.8			D2	Output See "3-state" (OZ5)			
	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer TTL Schmitt- trigger with Pull- Up ITS05U	Output See "3-state"	-	1.0 2.8			D2	Output See "3-state" (OZ5)			
	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer TTL Schmitt- trigger with Pull- Down ITS05D	Output See "3-state"	-	1.0 2.8			D2	Output See "3-state" (OZ5)			
	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer CMOS Schmitt- trigger with Pull- Up ICSO5U	Output See "3-state"	-	1.0 2.8			D2	Output See "3-state" (OZ5)			
	Input See "Input buffers"						Input See "Input buffers"			
I/O buffer CMOS Schmitt- trigger with Pull- Down ICSO5D	Output See "3-state"	-	1.0 2.8			D2	Output See "3-state" (OZ5)			
	Input See "Input buffers"						Input See "Input buffers"			

## 2. Power Gates

Macrocell		Equiva- lent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Macro Function Name							t <sub>OLH</sub>	k <sub>LH</sub>	t <sub>OHL</sub>	k <sub>HL</sub>
Power inverter		1	1.2	@		—	0.3	0.6	0.3	0.5
NAP										
Power inverter		2	1.4	@		—	0.3	0.4	0.6	0.4
NA3P										
Power inverter		2	1.6	@		—	0.3	0.3	0.6	0.3
NA4P										
2-input power NAND NAP		2	1.2	@		—	0.3	0.6	0.4	0.6
3-input power NAND NAP		3	1.2	@		—	0.3	0.6	0.4	0.7
4-input power NOR NAP		4	1.2	@		—	0.3	0.6	0.4	0.8
2-input power NOR NRP		2	1.2	#		—	0.4	1.0	0.6	0.5
3-input power NOR NRP		3	1.2	#		—	0.4	1.4	0.6	0.5
4-input power NOR NRP		4	1.2	#		—	0.5	1.9	0.6	0.5
Power buffer ANP		2	1.0	@		—	0.8	0.6	0.6	0.5
Power buffer AN3P		3	1.2	@		—	0.7	0.4	0.5	0.4
Power buffer AN4P		3	1.2	@		—	0.8	0.3	0.6	0.3

## 3. GATES

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						tPLH (ns)		tPHL (ns)	
Macro Function Name							tOLH	kLH	tOHL	kHL
Inverter NA		1	1	@		-	0.2	1.2	0.3	0.9
2-Input NAND NA		1	1	@		-	0.2	1.2	0.3	1.2
3-Input NAND NA		2	1	@		-	0.2	1.2	0.3	1.3
4-Input NAND NA		2	1	@		-	0.3	1.2	0.3	1.5
6-Input NAND NA		5	1	@		-	0.8	1.2	1.5	0.9
8-Input NAND NA		6	1	@		-	0.9	1.2	1.6	0.9
9-Input NAND NA		7	1	@		-	0.9	1.2	1.6	0.9
12-Input NAND NA		8	1	@		-	0.9	1.2	1.9	0.9

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						tPLH (ns)		tPHL (ns)	
Macro Function Name							tOLH	kLH	tOHL	kHL
16-Input NAND		11	1	@		-	0.9	1.2	1.6	1.2
NA										
2-Input NOR		1	1	#		-	0.3	2.0	0.7	0.9
NR										
3-Input NOR		2	1	#		-	0.4	2.8	0.7	0.9
NR										
4-Input NOR		2	1	#		-	0.4	3.7	0.7	0.9
NR										
6-Input NOR		5	1	#		-	1.2	1.2	1.0	0.9
NR										
8-Input NOR		6	1	#		-	1.3	1.2	1.0	0.9
NR										
9-Input NOR		7	1	#		-	1.3	1.2	1.0	0.9
NR										

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Macro Function Name							t <sub>OLH</sub>	k <sub>LH</sub>	t <sub>OHL</sub>	k <sub>HL</sub>
12-Input NOR		8	1	#		-	1.4	1.2	1.0	0.9
NR										
16-Input NOR		11	1	#		-	1.3	2.0	1.0	0.9
NR										
Buffer		1	1	@		-	0.6	1.2	0.5	0.9
AN1										
2-input AND		2	1	@		-	0.7	1.2	0.5	0.9
AN2										
3-input AND		2	1	@		-	0.9	1.2	0.7	0.9
AN3										
4-input AND		3	1	@		-	1.0	1.2	0.8	0.9
AN4										
2-input OR		2	1	#		-	0.7	1.2	0.7	0.9
OR2										

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Macro Function Name							t <sub>OLH</sub>	k <sub>LH</sub>	t <sub>OHL</sub>	k <sub>HL</sub>
3-input OR		2	1	#		-	0.7	1.2	0.9	0.9
OR3										
4-input OR		3	1	#		-	0.7	1.2	1.2	0.9
OR4										
2-input EOR		3	1.2	#		-	1.0	2.0	1.1	0.9
EOR										
2-input ENOR		3	1.2	#		-	0.9	1.2	1.0	1.2
ENR										

4. 3-STATE GATES

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent Circuit						Input Name	Output Name	$t_{PLH}(ns)$		$t_{PHL}(ns)$	
Function Name									$t_{OLH}$	$K_{LH}$	$t_{OHL}$	$K_{HL}$
3-State Inverter (Internal)		1	1	@		-	D	0.4	2.0	0.8	1.2	
							E/ $\bar{E}$	0.2	0.3			
NAZ												
3-State Buffer (Internal)		3	1.2	# @		-	D	0.8	1.2	0.7	0.9	
							E	1.0	1.0			
ANZ												

5. AND-NOR, OR-AND GATES

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent circuit						Input Name	Output Name	$t_{PLH}(ns)$		$t_{PHL}(ns)$	
Function Name									$t_{OLH}$	$K_{LH}$	$t_{OHL}$	$K_{HL}$
2-OR-NAND		2	1	# # @		A1	OR input	0.4	2.0	0.8	1.2	
							NAND input	0.3	0.8			
NAR23												
3-OR-NAND		2	1	# # # @		A2	OR input	0.5	2.8	0.8	1.2	
							NAND input	0.4	0.8			
NAR34												
2-OR-3NAND		2	1	# # @ @		A2	OR input	0.4	2.0	0.9	1.3	
							NAND input	0.4	0.8			
NAR24												
2-Wide 2-Input OR-NAND		2	1	# # # #		A1		0.4	2.0	0.8	1.2	
NA2R2												

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Input Name	Output Name	Delay				
Function	Equivalent Circuit								t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)		
Function Name									t <sub>OLH</sub>	K <sub>LH</sub>	t <sub>OHL</sub>	K <sub>HL</sub>	
3-Wide 3-Input OR-NAND		3	1	# # # # #		A3			0.4	2.0	0.9	1.3	
NA3R2													
2-Wide 3-Input OR-NAND		4	1	# # # # #		A2	NAND		0.8	2.8	1.0	1.2	
NA2R3N							In-verter		1.2	1.2	1.1	0.9	
2-Wide 4-Input OR-NAND		5	1	# # # # #		A4	NAND		1.1	3.7	1.0	1.2	
NA2R4N							In-verter		1.2	1.2	1.4	0.9	
3-Wide 3-Input OR-NAND		5	1	# # # # #			NAND		1.0	2.8	1.2	1.3	
NA3R3N							In-verter		1.4	1.2	1.3	0.9	
3-Wide 4-Input OR-NAND		7	1	# # # # # # #			NAND		1.4	3.7	1.2	1.3	
NA3R4N							In-verter		1.4	1.2	1.7	0.9	

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent Circuit						Input Name	Output Name	t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Function Name									t <sub>OLH</sub>	K <sub>LH</sub>	t <sub>OHL</sub>	K <sub>HL</sub>
4-Wide 2-Input OR-NAND		5	1	@@@ @@@ @@@ @@@ @@@		A4	NAND	0.7	2.0	1.3	1.5	
NA4R2N	Inverter						1.5	1.2	1.0	0.9		
4-Wide 3-Input OR-NAND		7	1	# # # # # # # #			NAND	1.2	2.8	1.6	1.5	
NA4R3N	Inverter						1.8	1.2	1.5	0.9		
4-Wide 4-Input OR-NAND		9	1	# # # # # # # # # #		A5	NAND	1.7	3.7	1.6	1.5	
NA4R4N	Inverter						1.8	1.2	2.0	0.9		
6-Wide 2-Input OR-NAND		8	1	@@@@ @@@@ @@@@ @@@@ @@@@ @@@@ @@@@ @			NAND	1.4	1.2	1.6	0.9	
NA6R2N	Inverter						1.3	2.0	1.2	0.9		

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent Circuit						Input Name	Output Name	t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Function Name									t <sub>OLH</sub>	K <sub>LH</sub>	t <sub>OHL</sub>	K <sub>HL</sub>
8-Wide 2-Input OR-NAND		10	1	@@@ @@@ @@@ @@@ @@@ @@@ @@@ @@@		A5	NAND	1.5	1.2	1.6	0.9	
NA8R2N	In-verter							1.4	2.8	1.2	0.9	
2 AND OR-NAND		2	1	@ @ # @		A1		0.4		0.8	1.3	
NARA24	OR input							0.4	2.0	0.8		
	NAND input							0.4		0.7		
2 AND-NOR		2	1	@ @ #		A1		0.4		0.8	1.2	
NRA23	NOR input							0.3	2.0	0.7		
3 AND-NOR		2	1	@ @ @ #		A2		0.4		0.8	1.3	
NRA34	NOR input							0.3	2.0	0.7		
2 AND-3 NOR		2	1	@ @ # #		A2		0.5		0.8	1.2	
NRA24	NOR input							0.4	2.8	0.7		
2-Wide 2-Input AND-NOR		2	1	@ @ @ @		A1		0.4	2.0	0.8	1.2	
NR2A2												

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent Circuit						Input Name	Output Name	t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Function Name									t <sub>OLH</sub>	K <sub>LH</sub>	t <sub>OHL</sub>	K <sub>HL</sub>
3-Wide 2-Input AND-NOR		3	1	@ @ @ @ @ @		A3			0.6	2.8	0.8	1.2
NR3A2												
2-Wide 3-Input AND-NOR		4	1	@ @ @ @ @ @		A2	NOR		0.6	2.0	1.0	1.3
NR2A3N											In-verter	
2-Wide 4-Input AND-NOR		5	1	@ @ @ @ @ @ @		A4	NOR		0.6	2.0	1.1	1.5
NR2A4N											In-verter	
3-Wide 3-Input AND-NOR		5	1	@ @ @ @ @ @ @			NOR		0.8	2.8	1.0	1.3
NR3A3N											In-verter	
3-Wide 4-Input AND-NOR		7	1	@ @ @ @ @ @ @ @			NOR		1.3	2.8	1.3	1.5
NR4A4N											In-verter	

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent Circuit						Input Name	Output Name	t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Function Name									t <sub>OLH</sub>	K <sub>LH</sub>	t <sub>OHL</sub>	K <sub>HL</sub>
4-Wide 2-Input AND-NOR		5	1	# # # # # #		A4		NOR	1.0	3.7	1.1	1.2
NR4A2N	In-verter								1.3	1.2	1.3	0.9
4-Wide 3-Input AND-NOR		7	1	@ @ @ @ @ @ @ @ @ @				NOR	1.5	3.7	1.1	1.3
NR4A3N	In-verter								1.3	1.2	1.8	0.9
4-Wide 4-Input AND-NOR		9	1	@ @ @ @ @ @ @ @ @ @ @ @		A5		NOR	2.3	3.7	1.5	1.5
NR4A4N	In-verter								1.7	1.2	2.6	0.9

Macrocell		Equiv- alent Gate Count	Normal- ized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent Circuit						Input Name	Output Name	t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Function Name									t <sub>OLH</sub>	K <sub>LH</sub>	t <sub>OHL</sub>	K <sub>HL</sub>
6-Wide 2-Input AND-NOR		8	1	# # # # # # # #			NOR	1.6	1.2	1.3	0.9	
NR6A2N	In- verter							1.0	1.2	1.4	1.2	
8-Wide 2-Input AND-NOR		10	1	# # # # # # # # # #		A5	NOR	1.3	1.2	1.4	0.9	
NR8A2N	In- verter							1.6	1.2	1.6	0.9	
2 AND- OR-NAND		2	1	# # @ #		A1	OR input	0.5	2.8	1.2	1.2	
NRAR24	AND input						0.4	0.8				
	NOR input						0.3	0.7				

6. MULTIPLEXERS

Macrocell		Equiva- lent Gate Count	Normal- ized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent Circuit						Input Name	Output Name	$t_{PLH}(ns)$		$t_{PHL}(ns)$	
Function Name									$t_{OLH}$	$K_{LH}$	$t_{OHL}$	$K_{HL}$
2 to 1 Multi- plexer  M2T1N		3	1.2 1 1	# # #		B2	Y0	+Y	1.1	1.2	0.8	0.9
							Y1		1.1		0.8	
							S		1.3		1.2	
							Y0	-Y	0.5	2.0	0.9	1.2
							Y1		0.5		0.9	
							S		0.9		1.1	
4 to 1 Multi- plexer  M4T1N		9	1	# # # # # #		B4	Y0	+Y	1.2	1.2	1.7	0.9
							Y1		1.2		1.7	
							Y2		1.2		1.7	
							Y3		1.2		1.7	
							A	-Y	2.5	3.7	2.7	1.3
							B		2.5		2.7	
							Y0		1.4		1.0	
							Y1		1.4		1.0	
							Y2	1.4	1.0			
							Y3	1.4	1.0			
							A	2.4	2.3			
							B	2.4	2.3			
8 to 1 Multi- plexer  M8T1N		21	1	# # # # # # # #		B6	Y0	+Y	1.7	1.2	2.0	1.3
							Y7		1.7		2.0	
							A, B, C		2.5		2.4	
							Y0	-Y	2.2	1.2	2.0	0.9
							Y7		2.2		2.0	
							A, B, C		2.6		2.8	
1 to 2 Demulti- plexer  M1T2N		4	1.2	# @		B3	Y	+0	1.2	1.2	0.8	0.9
							A		1.3		1.1	
							Y	+1	1.2	1.2	0.8	0.9
							A		1.2		0.8	
							Y	-0	0.5	1.2	1.0	1.2
							A		0.8		1.1	
Y	-1	0.5	1.2	1.0	1.2							
A		0.5		1.0								

7. DECODERS

Macrocell		Equiva- lent Gate Count	Normal- ized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent Circuit						Input Name	Output Name	t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)	
Function Name									t <sub>OLH</sub>	K <sub>LH</sub>	t <sub>OHL</sub>	K <sub>HL</sub>
2-bit Decoder		8	1	# #		B5	A	-0	1.5	1.2	1.7	1.2
							B	-0	1.5	1.2	1.7	
							A	-1	1.7	1.2	2.0	1.2
							B	-1	1.5	1.2	1.7	
							A	-2	1.5	1.2	1.7	1.2
							B	-2	1.7	1.2	2.0	
							A	-3	1.7	1.2	2.0	1.2
							B	-3	1.7	1.2	2.0	
							A	+0	2.0	1.2	1.7	0.9
							B	+0	2.0	1.2	1.7	
							A	+1	2.3	1.2	1.9	0.9
							B	+1	2.0	1.2	1.7	
							A	+2	2.0	1.2	1.7	0.9
							B	+2	2.3	1.2	1.9	
A	+3	2.3	1.2	1.9	0.9							
B	+3	2.3	1.2	1.9								
3-bit Decoder		1.4	1.8	# # #		B5	A	-0	1.4	1.2	1.2	1.3
							B	-0				
							C	-0				
							A	-1				
							B	-1				
							C	-1				
							A	-2				
							B	-2				
							C	-2				
							A	-3				
							B	-3				
							C	-3				
							A	-4				
							B	-4				
C	-4											
A	-5											
B	-5											
C	-5											
A	-6											
B	-6											
C	-6											
A	-7											
B	-7											
C	-7											

8. LATCHES (with Scan Function)

Macrocell		Equiva- lent Gate Count	Normal- ized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay																																			
Function	Truth table						Input Name	Output Name	$t_{PLH}(ns)$		$t_{PHL}(ns)$																															
Function Name								$t_{OLH}$	$K_{LH}$	$t_{OHL}$	$K_{HL}$																															
RS- Latch LRS0	<table border="1"> <tr><th>SN</th><th>RN</th><th>+Q</th><th>-Q</th></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td colspan="2">Latch</td></tr> </table>	SN	RN	+Q	-Q	0	0	0	0	0	1	1	0	1	0	0	1	1	1	Latch		8	1	@		A3	$\bar{S}$	+Q	2.7	1.0	—	0.6										
		SN	RN	+Q	-Q																																					
		0	0	0	0																																					
		0	1	1	0																																					
1	0	0	1																																							
1	1	Latch																																								
$\bar{R}$	2.5	2.6																																								
$\bar{S}$	-Q	2.5	1.0	2.6	—	0.6																																				
$\bar{R}$		2.7		—																																						
RS- Latch LRS3	<table border="1"> <tr><th>S</th><th>R</th><th>+Q</th><th>-Q</th></tr> <tr><td>0</td><td>0</td><td colspan="2">Latch</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td></tr> </table>	S	R	+Q	-Q	0	0	Latch		0	1	0	1	1	0	1	0	1	1	1	1	8	1	#		A3	S	+Q	2.4	1.0	2.7	0.6										
		S	R	+Q	-Q																																					
		0	0	Latch																																						
		0	1	0	1																																					
1	0	1	0																																							
1	1	1	1																																							
R	—	3.3																																								
S	-Q	—	1.0	3.3	—	0.6																																				
R		2.4		2.7																																						
2-Input RS Latch LR2S20	<table border="1"> <tr><th>SN</th><th>RN</th><th>+Q</th><th>-Q</th></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td colspan="2">Latch</td></tr> </table>	SN	RN	+Q	-Q	0	0	0	0	0	1	1	0	1	0	0	1	1	1	Latch		9	1	@		A4	$\bar{S}$	+Q	2.7	1.0	—	0.6										
		SN	RN	+Q	-Q																																					
		0	0	0	0																																					
		0	1	1	0																																					
1	0	0	1																																							
1	1	Latch																																								
$\bar{R}$	2.6	2.6																																								
$\bar{S}$	-Q	2.6	1.0	2.6	—	0.6																																				
$\bar{R}$		2.7		—																																						
2-Input RS Latch LR2S23	<table border="1"> <tr><th>S</th><th>R</th><th>+Q</th><th>-Q</th></tr> <tr><td>0</td><td>0</td><td colspan="2">Latch</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td></tr> </table>	S	R	+Q	-Q	0	0	Latch		0	1	0	1	1	0	1	0	1	1	1	1	9	1	#		A4	S	+Q	2.4	1.0	3.1	0.6										
		S	R	+Q	-Q																																					
		0	0	Latch																																						
		0	1	0	1																																					
1	0	1	0																																							
1	1	1	1																																							
R	—	3.7																																								
S	-Q	—	1.0	3.7	—	0.6																																				
R		2.4		3.1																																						
D-Latch LD	<table border="1"> <tr><th>G</th><th>+Q</th><th>-Q</th></tr> <tr><td>1</td><td>D</td><td><math>\bar{D}</math></td></tr> <tr><td><math>\downarrow</math></td><td colspan="2">Latch</td></tr> </table>	G	+Q	-Q	1	D	$\bar{D}$	$\downarrow$	Latch		5	1	@		C	G	+Q	3.2	1.2	2.9	0.9																					
		G	+Q	-Q																																						
		1	D	$\bar{D}$																																						
		$\downarrow$	Latch																																							
D	3.2	2.9																																								
G	-Q	2.6	1.2	2.9	—	0.9																																				
D		2.6		2.9																																						
D-Latch with CLR LDC1	<table border="1"> <tr><th>G</th><th>CL</th><th>+Q</th><th>-Q</th></tr> <tr><td>1</td><td>0</td><td>D</td><td><math>\bar{D}</math></td></tr> <tr><td><math>\downarrow</math></td><td>0</td><td colspan="2">Latch</td></tr> <tr><td>X</td><td>1</td><td>0</td><td>1</td></tr> </table> <p>X: Don't care</p>	G	CL	+Q	-Q	1	0	D	$\bar{D}$	$\downarrow$	0	Latch		X	1	0	1	6	1	@		C	G	+Q	3.5	1.2	3.4	0.9														
		G	CL	+Q	-Q																																					
		1	0	D	$\bar{D}$																																					
		$\downarrow$	0	Latch																																						
		X	1	0	1																																					
		CL	2.3	2.4																																						
D	-Q	3.5	1.2	3.4	—	0.9																																				
CL		2.1		2.0																																						
D	3.1	3.2																																								
D-Latch with PRE LDP1	<table border="1"> <tr><th>G</th><th>PR</th><th>+Q</th><th>-Q</th></tr> <tr><td>1</td><td>0</td><td>D</td><td><math>\bar{D}</math></td></tr> <tr><td><math>\downarrow</math></td><td>0</td><td colspan="2">Latch</td></tr> <tr><td>X</td><td>1</td><td>1</td><td>0</td></tr> </table> <p>X: Don't care</p>	G	PR	+Q	-Q	1	0	D	$\bar{D}$	$\downarrow$	0	Latch		X	1	1	0	6	1	@		C	G	+Q	3.3	1.2	3.2	0.9														
		G	PR	+Q	-Q																																					
		1	0	D	$\bar{D}$																																					
		$\downarrow$	0	Latch																																						
		X	1	1	0																																					
		PR	2.4	2.5																																						
D	-Q	3.3	1.2	3.2	—	0.9																																				
G		2.9		3.0																																						
PR	2.2	2.1																																								
D	2.9	3.0																																								
D-Latch with PRE/ CLR LDPC3	<table border="1"> <tr><th>G</th><th>PR</th><th>CL</th><th>+Q</th><th>-Q</th></tr> <tr><td>1</td><td>0</td><td>0</td><td>D</td><td><math>\bar{D}</math></td></tr> <tr><td><math>\downarrow</math></td><td>0</td><td>0</td><td colspan="2">Latch</td></tr> <tr><td>X</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>X</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>X</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> </table> <p>X: Don't care</p>	G	PR	CL	+Q	-Q	1	0	0	D	$\bar{D}$	$\downarrow$	0	0	Latch		X	1	0	1	0	X	0	1	0	1	X	1	1	0	1	7	1	@		C	G	+Q	3.8	1.2	3.5	0.9
		G	PR	CL	+Q	-Q																																				
		1	0	0	D	$\bar{D}$																																				
		$\downarrow$	0	0	Latch																																					
		X	1	0	1	0																																				
		X	0	1	0	1																																				
		X	1	1	0	1																																				
		PR	2.9	2.8																																						
CL	-Q	2.3	1.2	2.4	—	0.9																																				
D		3.8		3.5																																						
G	3.2	3.5																																								
PR	2.5	2.6																																								
CL	2.1	2.0																																								
D	3.2	3.5																																								

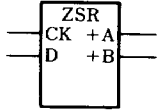
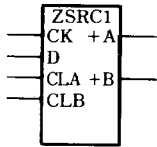
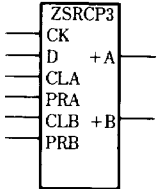
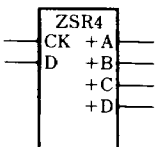
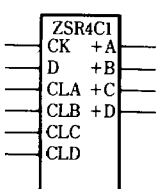
Macrocell		Equiva- lent Gate Count	Normal- ized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay																													
Function	Truth table						Input Name	Output Name	$t_{PLH}(ns)$		$t_{PHL}(ns)$																									
Function Name									$t_{OLH}$	$k_{LH}$	$t_{OHL}$	$k_{HL}$																								
4-Bit latch	<table border="1"> <tr> <td>G</td> <td>+Q<sub>0</sub></td> <td>+Q<sub>1</sub></td> <td>+Q<sub>2</sub></td> <td>+Q<sub>3</sub></td> </tr> <tr> <td>1</td> <td>D<sub>0</sub></td> <td>D<sub>1</sub></td> <td>D<sub>2</sub></td> <td>D<sub>3</sub></td> </tr> <tr> <td><math>\bar{L}</math></td> <td colspan="4">Latch</td> </tr> </table>	G	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>	1	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	$\bar{L}$	Latch				20	1	@		B4	G	+Q <sub>0</sub>	3.5	1.2	3.2	0.9									
G	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>																																
1	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>																																
$\bar{L}$	Latch																																			
LD4	$\bar{L}$	D <sub>0</sub>	+Q <sub>3</sub>	3.2	2.9																															
4-Bit latch with CLR				<table border="1"> <tr> <td>G</td> <td>CL</td> <td>+Q<sub>0</sub></td> <td>+Q<sub>1</sub></td> <td>+Q<sub>2</sub></td> <td>+Q<sub>3</sub></td> </tr> <tr> <td>1</td> <td>0</td> <td>D<sub>0</sub></td> <td>D<sub>1</sub></td> <td>D<sub>2</sub></td> <td>D<sub>3</sub></td> </tr> <tr> <td><math>\bar{L}</math></td> <td>0</td> <td colspan="4">Latch</td> </tr> <tr> <td>X</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	G	CL	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>	1	0	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	$\bar{L}$	0	Latch				X	1	0	0	0	0	26	1	@		B4	G	+Q <sub>0</sub>	3.6
G	CL	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>																															
1	0	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>																															
$\bar{L}$	0	Latch																																		
X	1	0	0	0	0																															
LD4C1	$\bar{L}$	D <sub>0</sub>	+Q <sub>3</sub>	3.3	2.9																															
				CL	3.0	2.7																														

9. FLIP-FLOPS (with Scan Function)

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay																																															
Function	Truth table						Input Name	Output Name	$t_{PLH}(ns)$		$t_{PHL}(ns)$																																											
Function Name									$t_{OLH}$	$K_{LH}$	$t_{OHL}$	$K_{HL}$																																										
DFF	<table border="1"> <tr><td>CK</td><td>+Q</td><td>-Q</td></tr> <tr><td>f</td><td>D</td><td><math>\bar{D}</math></td></tr> <tr><td><math>\bar{L}</math></td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> </table>	CK	+Q	-Q	f	D	$\bar{D}$	$\bar{L}$	+Q <sub>0</sub>	-Q <sub>0</sub>	7	1	@ @		C	CK	+Q	3.9	1.2	3.8	0.9																																	
CK	+Q	-Q																																																				
f	D	$\bar{D}$																																																				
$\bar{L}$	+Q <sub>0</sub>	-Q <sub>0</sub>																																																				
FD								-Q	3.5	1.2	3.6	0.9																																										
DFF with Load FDL1	<table border="1"> <tr><td>CK</td><td>L</td><td>+Q</td><td>-Q</td></tr> <tr><td>f</td><td>0</td><td>D<sub>C</sub></td><td><math>\bar{D}_C</math></td></tr> <tr><td>f</td><td>1</td><td>D<sub>L</sub></td><td><math>\bar{D}_L</math></td></tr> <tr><td><math>\bar{L}</math></td><td>X</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> </table>	CK	L	+Q	-Q	f	0	D <sub>C</sub>	$\bar{D}_C$	f	1	D <sub>L</sub>	$\bar{D}_L$	$\bar{L}$	X	+Q <sub>0</sub>	-Q <sub>0</sub>	9	1 1 1 1.2	@ @ @ #		C	CK	+Q	3.9	1.2	3.8	0.9																										
CK	L	+Q	-Q																																																			
f	0	D <sub>C</sub>	$\bar{D}_C$																																																			
f	1	D <sub>L</sub>	$\bar{D}_L$																																																			
$\bar{L}$	X	+Q <sub>0</sub>	-Q <sub>0</sub>																																																			
								-Q	3.5	1.2	3.6	0.9																																										
DFF with CLR FDC1	<table border="1"> <tr><td>CK</td><td>CL</td><td>+Q</td><td>-Q</td></tr> <tr><td>f</td><td>0</td><td>D</td><td><math>\bar{D}</math></td></tr> <tr><td><math>\bar{L}</math></td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>X</td><td>1</td><td>0</td><td>1</td></tr> </table>	CK	CL	+Q	-Q	f	0	D	$\bar{D}$	$\bar{L}$	0	+Q <sub>0</sub>	-Q <sub>0</sub>	X	1	0	1	8	1 1 1.2	@ @ #		C	CK	+Q	4.0	1.2	4.1	0.9																										
CK	CL	+Q	-Q																																																			
f	0	D	$\bar{D}$																																																			
$\bar{L}$	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																			
X	1	0	1																																																			
								CL	-	-	2.1	-																																										
								CK	-Q	3.8	1.2	3.7	0.9																																									
								CL	-Q	1.8	-	-	0.9																																									
DFF with PRE FDP1	<table border="1"> <tr><td>CK</td><td>PR</td><td>+Q</td><td>-Q</td></tr> <tr><td>f</td><td>0</td><td>D</td><td><math>\bar{D}</math></td></tr> <tr><td><math>\bar{L}</math></td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>X</td><td>1</td><td>1</td><td>0</td></tr> </table>	CK	PR	+Q	-Q	f	0	D	$\bar{D}$	$\bar{L}$	0	+Q <sub>0</sub>	-Q <sub>0</sub>	X	1	1	0	8	1 1 1.2	@ @ #		C	CK	+Q	4.4	1.2	4.1	0.9																										
CK	PR	+Q	-Q																																																			
f	0	D	$\bar{D}$																																																			
$\bar{L}$	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																			
X	1	1	0																																																			
								RR	-	-	-	-																																										
								CK	-Q	3.8	1.2	4.1	0.9																																									
								PR	-	-	2.5	-																																										
DFF with PRE/CLR FDPC3	<table border="1"> <tr><td>CK</td><td>PR</td><td>CL</td><td>+Q</td><td>-Q</td></tr> <tr><td>f</td><td>0</td><td>0</td><td>D</td><td><math>\bar{D}</math></td></tr> <tr><td><math>\bar{L}</math></td><td>0</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>X</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>X</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>X</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> </table>	CK	PR	CL	+Q	-Q	f	0	0	D	$\bar{D}$	$\bar{L}$	0	0	+Q <sub>0</sub>	-Q <sub>0</sub>	X	1	0	1	0	X	0	1	0	1	X	1	1	0	1	9	1 1 1.2 1.2	@ @ # #		C	CK	+Q	4.5	-	4.4	-												
CK	PR	CL	+Q	-Q																																																		
f	0	0	D	$\bar{D}$																																																		
$\bar{L}$	0	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																		
X	1	0	1	0																																																		
X	0	1	0	1																																																		
X	1	1	0	1																																																		
								CL	+Q	2.0	1.2	2.1	0.9																																									
								PR	-	2.9	-	-	-																																									
								CK	-Q	4.1	-	4.2	-																																									
								CL	-Q	1.8	1.2	1.7	0.9																																									
								PR	-	-	-	2.6	-																																									
JKFF	<table border="1"> <tr><td>CK</td><td>J</td><td>K</td><td>+Q</td><td>-Q</td></tr> <tr><td>f</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>f</td><td>1</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>f</td><td>0</td><td>1</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>f</td><td>1</td><td>0</td><td>-Q<sub>0</sub></td><td>+Q<sub>0</sub></td></tr> <tr><td><math>\bar{L}</math></td><td>X</td><td>X</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> </table>	CK	J	K	+Q	-Q	f	0	0	0	1	f	1	1	1	0	f	0	1	+Q <sub>0</sub>	-Q <sub>0</sub>	f	1	0	-Q <sub>0</sub>	+Q <sub>0</sub>	$\bar{L}$	X	X	+Q <sub>0</sub>	-Q <sub>0</sub>	10	1.2 1 1	@ @ #		C	CK	+Q	3.7	1.2	4.4	0.9												
CK	J	K	+Q	-Q																																																		
f	0	0	0	1																																																		
f	1	1	1	0																																																		
f	0	1	+Q <sub>0</sub>	-Q <sub>0</sub>																																																		
f	1	0	-Q <sub>0</sub>	+Q <sub>0</sub>																																																		
$\bar{L}$	X	X	+Q <sub>0</sub>	-Q <sub>0</sub>																																																		
FJ								-Q	3.6	1.2	4.4	0.9																																										
JKFF with CLR FJC1	<table border="1"> <tr><td>CK</td><td>J</td><td>K</td><td>CL</td><td>+Q</td><td>-Q</td></tr> <tr><td>f</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>f</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>f</td><td>0</td><td>1</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>f</td><td>1</td><td>0</td><td>0</td><td>-Q<sub>0</sub></td><td>+Q<sub>0</sub></td></tr> <tr><td><math>\bar{L}</math></td><td>X</td><td>X</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>X</td><td>X</td><td>X</td><td>1</td><td>0</td><td>1</td></tr> </table>	CK	J	K	CL	+Q	-Q	f	0	0	0	0	1	f	1	1	0	1	0	f	0	1	0	+Q <sub>0</sub>	-Q <sub>0</sub>	f	1	0	0	-Q <sub>0</sub>	+Q <sub>0</sub>	$\bar{L}$	X	X	0	+Q <sub>0</sub>	-Q <sub>0</sub>	X	X	X	1	0	1	13	1.2 1 1 1	@ @ # #		C	CK	+Q	4.3	1.2	4.6	0.9
CK	J	K	CL	+Q	-Q																																																	
f	0	0	0	0	1																																																	
f	1	1	0	1	0																																																	
f	0	1	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																	
f	1	0	0	-Q <sub>0</sub>	+Q <sub>0</sub>																																																	
$\bar{L}$	X	X	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																	
X	X	X	1	0	1																																																	
								CL	-	-	4.8	-																																										
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JKFF with PRE/CLR	<table border="1"> <tr><th>CK</th><th>J</th><th>K</th><th>PR</th><th>CL</th><th>+Q</th><th>-Q</th></tr> <tr><td>f</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>f</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>f</td><td>0</td><td>1</td><td>1</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>f</td><td>1</td><td>0</td><td>1</td><td>0</td><td>-Q<sub>0</sub></td><td>+Q<sub>0</sub></td></tr> <tr><td>l</td><td>x</td><td>x</td><td>1</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>x</td><td>x</td><td>x</td><td>0</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> </table>	CK	J	K	PR	CL	+Q	-Q	f	0	0	1	0	0	1	f	1	1	1	0	1	0	f	0	1	1	0	+Q <sub>0</sub>	-Q <sub>0</sub>	f	1	0	1	0	-Q <sub>0</sub>	+Q <sub>0</sub>	l	x	x	1	0	+Q <sub>0</sub>	-Q <sub>0</sub>	x	x	x	0	0	1	0	x	x	x	1	1	0	1	x	x	x	0	1	1	1	14	1.2 1 1	@ @ #		C	CK	+Q	4.3	1.2	4.6	0.9
CK	J	K	PR	CL	+Q	-Q																																																																					
f	0	0	1	0	0	1																																																																					
f	1	1	1	0	1	0																																																																					
f	0	1	1	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																																					
f	1	0	1	0	-Q <sub>0</sub>	+Q <sub>0</sub>																																																																					
l	x	x	1	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																																					
x	x	x	0	0	1	0																																																																					
x	x	x	1	1	0	1																																																																					
x	x	x	0	1	1	1																																																																					
FJPC1						PR	-Q	2.6	2.6	4.8																																																																	
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						CK	-Q	4.1	1.2	4.6	0.9																																																																
						PR		-		2.6																																																																	
						CL		3.6		2.6																																																																	
TFF with CLR	<table border="1"> <tr><th>CK</th><th>CL</th><th>+Q</th><th>-Q</th></tr> <tr><td>f</td><td>0</td><td>-Q<sub>0</sub></td><td>+Q<sub>0</sub></td></tr> <tr><td>l</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>x</td><td>1</td><td>0</td><td>1</td></tr> </table>	CK	CL	+Q	-Q	f	0	-Q <sub>0</sub>	+Q <sub>0</sub>	l	0	+Q <sub>0</sub>	-Q <sub>0</sub>	x	1	0	1	9	1 1.2	@ #		C	CK	+Q	4.0	1.2	4.1	0.9																																															
CK	CL	+Q	-Q																																																																								
f	0	-Q <sub>0</sub>	+Q <sub>0</sub>																																																																								
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x	1	0	1																																																																								
FTC1						CL		-	2.1																																																																		
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TFF with PRE	<table border="1"> <tr><th>CK</th><th>PR</th><th>+Q</th><th>-Q</th></tr> <tr><td>f</td><td>0</td><td>-Q<sub>0</sub></td><td>+Q<sub>0</sub></td></tr> <tr><td>l</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>x</td><td>1</td><td>1</td><td>0</td></tr> </table>	CK	PR	+Q	-Q	f	0	-Q <sub>0</sub>	+Q <sub>0</sub>	l	0	+Q <sub>0</sub>	-Q <sub>0</sub>	x	1	1	0	9	1 1.2	@ #		C	CK	+Q	4.4	1.2	4.1	0.9																																															
CK	PR	+Q	-Q																																																																								
f	0	-Q <sub>0</sub>	+Q <sub>0</sub>																																																																								
l	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																																								
x	1	1	0																																																																								
FTP1						PR		2.8	-																																																																		
						CK	-Q	3.8	1.2	4.1	0.9																																																																
						PR		-		2.5																																																																	
TFF with PRE/CLR	<table border="1"> <tr><th>CK</th><th>PR</th><th>CL</th><th>+Q</th><th>-Q</th></tr> <tr><td>f</td><td>0</td><td>0</td><td>-Q<sub>0</sub></td><td>+Q<sub>0</sub></td></tr> <tr><td>l</td><td>0</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>x</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>x</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>x</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> </table>	CK	PR	CL	+Q	-Q	f	0	0	-Q <sub>0</sub>	+Q <sub>0</sub>	l	0	0	+Q <sub>0</sub>	-Q <sub>0</sub>	x	1	0	1	0	x	0	1	0	1	x	1	1	0	1	10	1 1.2 1.2	@ # #		C	CK	+Q	4.5	1.2	4.4	0.9																																	
CK	PR	CL	+Q	-Q																																																																							
f	0	0	-Q <sub>0</sub>	+Q <sub>0</sub>																																																																							
l	0	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																																							
x	1	0	1	0																																																																							
x	0	1	0	1																																																																							
x	1	1	0	1																																																																							
FTPC3						PR		2.9	-																																																																		
						CL		2.0		2.1																																																																	
						CK	-Q	4.1	1.2	4.2	0.9																																																																
						PR		-		2.6																																																																	
						CL		1.8		1.7																																																																	
4-Bit DFF	<table border="1"> <tr><th>CK</th><th>+Q<sub>0</sub></th><th>+Q<sub>1</sub></th><th>+Q<sub>2</sub></th><th>+Q<sub>3</sub></th></tr> <tr><td>f</td><td>D<sub>0</sub></td><td>D<sub>1</sub></td><td>D<sub>2</sub></td><td>D<sub>3</sub></td></tr> <tr><td>l</td><td>+Q<sub>00</sub></td><td>+Q<sub>10</sub></td><td>+Q<sub>20</sub></td><td>+Q<sub>30</sub></td></tr> </table>	CK	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>	f	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	l	+Q <sub>00</sub>	+Q <sub>10</sub>	+Q <sub>20</sub>	+Q <sub>30</sub>	28	1 1 1 1	@ @ @ @		B4	CK	+Q <sub>0</sub>	4.1	1.2	4.0	0.9																																																
CK	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>																																																																							
f	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>																																																																							
l	+Q <sub>00</sub>	+Q <sub>10</sub>	+Q <sub>20</sub>	+Q <sub>30</sub>																																																																							
FD4							+Q <sub>3</sub>																																																																				
4-Bit DFF with CLR	<table border="1"> <tr><th>CK</th><th>CL</th><th>+Q<sub>0</sub></th><th>+Q<sub>1</sub></th><th>+Q<sub>2</sub></th><th>+Q<sub>3</sub></th></tr> <tr><td>f</td><td>0</td><td>D<sub>0</sub></td><td>D<sub>1</sub></td><td>D<sub>2</sub></td><td>D<sub>3</sub></td></tr> <tr><td>l</td><td>0</td><td>+Q<sub>00</sub></td><td>+Q<sub>10</sub></td><td>+Q<sub>20</sub></td><td>+Q<sub>30</sub></td></tr> <tr><td>x</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> </table>	CK	CL	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>	f	0	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	l	0	+Q <sub>00</sub>	+Q <sub>10</sub>	+Q <sub>20</sub>	+Q <sub>30</sub>	x	1	0	0	0	0	33	1 1 1 1 1	@ @ @ @ #		B4	CK	+Q <sub>0</sub>	4.4	1.2	4.3	0.9																																							
CK	CL	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>																																																																						
f	0	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>																																																																						
l	0	+Q <sub>00</sub>	+Q <sub>10</sub>	+Q <sub>20</sub>	+Q <sub>30</sub>																																																																						
x	1	0	0	0	0																																																																						
FD4C1							+Q <sub>3</sub>	-	3.3																																																																		

10. SHIFT REGISTERS (with Scan Function)

Macrocell		Equival-ent Gate Count	Normal-ized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay																																																																				
Function	Truth table						Input Name	Output Name	t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)																																																																
Function Name									t <sub>OLH</sub>	k <sub>LH</sub>	t <sub>OHL</sub>	k <sub>HL</sub>																																																															
2-Bit SR	<table border="1"> <tr><td>CK</td><td>+A</td><td>+B</td></tr> <tr><td>f</td><td>D</td><td>+A<sub>0</sub></td></tr> <tr><td>1</td><td>+A<sub>0</sub></td><td>+B<sub>0</sub></td></tr> </table>	CK	+A	+B	f	D	+A <sub>0</sub>	1	+A <sub>0</sub>	+B <sub>0</sub>	12	1 1	@ @		B1	CK	+A	4.1	1.2	4.0	0.9																																																						
CK	+A	+B																																																																									
f	D	+A <sub>0</sub>																																																																									
1	+A <sub>0</sub>	+B <sub>0</sub>																																																																									
ZSR								+B	4.1	1.2	4.0	0.9																																																															
2-Bit SR with CLR	<table border="1"> <tr><td>CK</td><td>CLA</td><td>CLB</td><td>+A</td><td>+B</td></tr> <tr><td>f</td><td>0</td><td>0</td><td>D</td><td>+A<sub>0</sub></td></tr> <tr><td>1</td><td>0</td><td>0</td><td>+A<sub>0</sub></td><td>+B<sub>0</sub></td></tr> <tr><td>x</td><td>1</td><td>x</td><td>0</td><td>x</td></tr> <tr><td>x</td><td>x</td><td>1</td><td>x</td><td>0</td></tr> </table>	CK	CLA	CLB	+A	+B	f	0	0	D	+A <sub>0</sub>	1	0	0	+A <sub>0</sub>	+B <sub>0</sub>	x	1	x	0	x	x	x	1	x	0	15	1 1 1.2 1.2	@ @ # #		C	CK	+A	2.4	1.2	2.6	0.9																																						
CK	CLA	CLB	+A	+B																																																																							
f	0	0	D	+A <sub>0</sub>																																																																							
1	0	0	+A <sub>0</sub>	+B <sub>0</sub>																																																																							
x	1	x	0	x																																																																							
x	x	1	x	0																																																																							
ZSRC1							CLA		—		2.5																																																																
							CK	+B	2.4	1.2	2.6	0.9																																																															
							CLB		—		2.5																																																																
2-Bit SR with CLR/PRE	<table border="1"> <tr><td>CK</td><td>CLA</td><td>CLB</td><td>PRA</td><td>PRB</td><td>+A</td><td>+B</td></tr> <tr><td>f</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D</td><td>+A<sub>0</sub></td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>+A<sub>0</sub></td><td>+B<sub>0</sub></td></tr> <tr><td>x</td><td>1</td><td>x</td><td>x</td><td>x</td><td>0</td><td>x</td></tr> <tr><td>x</td><td>x</td><td>1</td><td>x</td><td>x</td><td>x</td><td>0</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>1</td><td>x</td><td>1</td><td>x</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>1</td><td>x</td><td>1</td></tr> <tr><td>x</td><td>1</td><td>x</td><td>1</td><td>x</td><td>0</td><td>x</td></tr> <tr><td>x</td><td>x</td><td>1</td><td>x</td><td>1</td><td>x</td><td>0</td></tr> </table>	CK	CLA	CLB	PRA	PRB	+A	+B	f	0	0	0	0	D	+A <sub>0</sub>	1	0	0	0	0	+A <sub>0</sub>	+B <sub>0</sub>	x	1	x	x	x	0	x	x	x	1	x	x	x	0	x	x	x	1	x	1	x	x	x	x	x	1	x	1	x	1	x	1	x	0	x	x	x	1	x	1	x	0	17	1 1 1.2 1.2 1.2 1.2	@ @ # # # #		B4	CK	+A	4.7	1.2	4.6	0.9
CK	CLA	CLB	PRA	PRB	+A	+B																																																																					
f	0	0	0	0	D	+A <sub>0</sub>																																																																					
1	0	0	0	0	+A <sub>0</sub>	+B <sub>0</sub>																																																																					
x	1	x	x	x	0	x																																																																					
x	x	1	x	x	x	0																																																																					
x	x	x	1	x	1	x																																																																					
x	x	x	x	1	x	1																																																																					
x	1	x	1	x	0	x																																																																					
x	x	1	x	1	x	0																																																																					
ZSRCP3							CLA		2.0	1.2	2.1	0.9																																																															
							PRA		2.9		—																																																																
							CK	+B	4.7	1.2	4.6	0.9																																																															
							CLB		2.0	1.2	2.1	0.9																																																															
							PRB		2.9		—																																																																
4-Bit SR	<table border="1"> <tr><td>CK</td><td>+A</td><td>+B</td><td>+C</td><td>+D</td></tr> <tr><td>f</td><td>D</td><td>+A<sub>0</sub></td><td>+B<sub>0</sub></td><td>+C<sub>0</sub></td></tr> <tr><td>1</td><td>+A<sub>0</sub></td><td>+B<sub>0</sub></td><td>+C<sub>0</sub></td><td>+D<sub>0</sub></td></tr> </table>	CK	+A	+B	+C	+D	f	D	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>	1	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>	+D <sub>0</sub>	28	1 1	@ @		C	CK	+A	4.2	1.2	4.1	0.9																																																
CK	+A	+B	+C	+D																																																																							
f	D	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>																																																																							
1	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>	+D <sub>0</sub>																																																																							
ZSR4							CK	+B	4.2	1.2	4.1	0.9																																																															
							CK	+C	4.2	1.2	4.1	0.9																																																															
							CK	+D	4.2	1.2	4.1	0.9																																																															
4-Bit SR with CLR	<table border="1"> <tr><td>CK</td><td>CLA</td><td>CLB</td><td>CLC</td><td>CLD</td><td>+A</td><td>+B</td><td>+C</td><td>+D</td></tr> <tr><td>f</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D</td><td>+A<sub>0</sub></td><td>+B<sub>0</sub></td><td>+C<sub>0</sub></td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>+A<sub>0</sub></td><td>+B<sub>0</sub></td><td>+C<sub>0</sub></td><td>+D<sub>0</sub></td></tr> <tr><td>x</td><td>1</td><td>x</td><td>x</td><td>x</td><td>0</td><td>x</td><td>x</td><td>x</td></tr> <tr><td>x</td><td>x</td><td>1</td><td>x</td><td>x</td><td>x</td><td>0</td><td>x</td><td>x</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>1</td><td>x</td><td>x</td><td>x</td><td>0</td><td>x</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>1</td><td>x</td><td>x</td><td>x</td><td>0</td></tr> </table>	CK	CLA	CLB	CLC	CLD	+A	+B	+C	+D	f	0	0	0	0	D	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>	1	0	0	0	0	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>	+D <sub>0</sub>	x	1	x	x	x	0	x	x	x	x	x	1	x	x	x	0	x	x	x	x	x	1	x	x	x	0	x	x	x	x	x	1	x	x	x	0	36	1 1 1.2 1.2 1.2 1.2	@ @ # # # #		B4	CK	+A	4.5	1.2	4.4	0.9
CK	CLA	CLB	CLC	CLD	+A	+B	+C	+D																																																																			
f	0	0	0	0	D	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>																																																																			
1	0	0	0	0	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>	+D <sub>0</sub>																																																																			
x	1	x	x	x	0	x	x	x																																																																			
x	x	1	x	x	x	0	x	x																																																																			
x	x	x	1	x	x	x	0	x																																																																			
x	x	x	x	1	x	x	x	0																																																																			
ZSR4C1							CLA		—		2.1																																																																
							CK	+B	4.5	1.2	4.4	0.9																																																															
							CLB		—		2.1																																																																
							CK	+C	4.5	1.2	4.4	0.9																																																															
							CLC		—		2.1																																																																
							CK	+D	4.5	1.2	4.4	0.9																																																															
							CLD		—		2.1																																																																

11. Latches (Normal Type)

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay																																				
Function	Truth table						Input Name	Output Name	$t_{PLH}(ns)$		$t_{PHL}(ns)$																																
Function Name									$t_{OLH}$	$k_{LH}$	$t_{OHL}$	$k_{HL}$																															
RS latch	<table border="1"> <tr><th>SN</th><th>RN</th><th>+Q</th><th>-Q</th></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td colspan="2">Latch</td></tr> </table>	SN	RN	+Q	-Q	0	0	0	0	0	1	1	0	1	0	0	1	1	1	Latch		3	1	@		A3	$\bar{S}$	+Q	1.2	1.2	-	0.9											
SN	RN	+Q	-Q																																								
0	0	0	0																																								
0	1	1	0																																								
1	0	0	1																																								
1	1	Latch																																									
LRS0	$\bar{R}$	+Q	1.0	0.9																																							
				@			$\bar{S}$	-Q	1.0	1.2	-	0.9																															
				@			$\bar{R}$	-Q	1.2		-																																
RS latch	<table border="1"> <tr><th>S</th><th>R</th><th>+Q</th><th>-Q</th></tr> <tr><td>0</td><td>0</td><td colspan="2">Latch</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td></tr> </table>	S	R	+Q	-Q	0	0	Latch		0	1	0	1	1	0	1	0	1	1	1	1	3	1	#		A3	S	+Q	0.9	1.2	1.0	0.9											
S	R	+Q	-Q																																								
0	0	Latch																																									
0	1	0	1																																								
1	0	1	0																																								
1	1	1	1																																								
LRS3	R	+Q	-	1.6																																							
				#			S	-Q	-	1.2	1.6	0.9																															
				#			R	-Q	0.9		1.0																																
2-Input RS latch	<table border="1"> <tr><th>SN</th><th>RN</th><th>+Q</th><th>-Q</th></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td colspan="2">Latch</td></tr> </table>	SN	RN	+Q	-Q	0	0	0	0	0	1	1	0	1	0	0	1	1	1	Latch		4	1	@		A4	$\bar{S}$	+Q	1.2	1.2	-	0.9											
SN	RN	+Q	-Q																																								
0	0	0	0																																								
0	1	1	0																																								
1	0	0	1																																								
1	1	Latch																																									
LRS20	$\bar{R}$	+Q	1.1	0.9																																							
				@			$\bar{S}$	-Q	1.1	1.2	0.9	0.9																															
				@			$\bar{R}$	-Q	1.2		-																																
2-Input RS latch	<table border="1"> <tr><th>S</th><th>R</th><th>+Q</th><th>-Q</th></tr> <tr><td>0</td><td>0</td><td colspan="2">Latch</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td></tr> </table>	S	R	+Q	-Q	0	0	Latch		0	1	0	1	1	0	1	0	1	1	1	1	4	1	#		A4	S	+Q	0.9	1.2	1.4	0.9											
S	R	+Q	-Q																																								
0	0	Latch																																									
0	1	0	1																																								
1	0	1	0																																								
1	1	1	1																																								
LRS23	R	+Q	-	2.0																																							
				#			S	-Q	-	1.2	2.0	0.9																															
				#			R	-Q	0.9		1.4																																
D latch	<table border="1"> <tr><th>G</th><th>+Q</th><th>-Q</th></tr> <tr><td>1</td><td>D</td><td><math>\bar{D}</math></td></tr> <tr><td><math>\downarrow</math></td><td colspan="2">Latch</td></tr> </table>	G	+Q	-Q	1	D	$\bar{D}$	$\downarrow$	Latch		4	1.2	1	@		C	G	+Q	1.5	1.2	1.5	0.9																					
G	+Q	-Q																																									
1	D	$\bar{D}$																																									
$\downarrow$	Latch																																										
LD	D	+Q	1.5	1.5																																							
				@			G	-Q	1.6	1.2	1.8	0.9																															
				@			D	-Q	1.6		1.8																																
D latch with CLR	<table border="1"> <tr><th>G</th><th>CL</th><th>+Q</th><th>-Q</th></tr> <tr><td>1</td><td>0</td><td>D</td><td><math>\bar{D}</math></td></tr> <tr><td><math>\downarrow</math></td><td>0</td><td colspan="2">Latch</td></tr> <tr><td>X</td><td>1</td><td>0</td><td>1</td></tr> </table> <p>X: Don't care</p>	G	CL	+Q	-Q	1	0	D	$\bar{D}$	$\downarrow$	0	Latch		X	1	0	1	5	1.2	1	@		C	G	+Q	2.8	1.2	2.4	0.9														
G	CL	+Q	-Q																																								
1	0	D	$\bar{D}$																																								
$\downarrow$	0	Latch																																									
X	1	0	1																																								
LDC1	D	+Q	1.6	1.4																																							
				@			D	+Q	2.8	1.2	2.4	0.9																															
				#			G	-Q	2.1		1.2		2.8	0.9																													
				#			CL	-Q	1.1	1.2		1.6	0.9																														
				#			D	-Q	2.1		2.8																																
D latch with PRE	<table border="1"> <tr><th>G</th><th>PR</th><th>+Q</th><th>-Q</th></tr> <tr><td>1</td><td>0</td><td>D</td><td><math>\bar{D}</math></td></tr> <tr><td><math>\downarrow</math></td><td>0</td><td colspan="2">Latch</td></tr> <tr><td>X</td><td>1</td><td>1</td><td>0</td></tr> </table> <p>X: Don't care</p>	G	PR	+Q	-Q	1	0	D	$\bar{D}$	$\downarrow$	0	Latch		X	1	1	0	5	1.2	1	@		C	G	+Q	1.6	1.2	1.8	0.9														
G	PR	+Q	-Q																																								
1	0	D	$\bar{D}$																																								
$\downarrow$	0	Latch																																									
X	1	1	0																																								
LDP1	D	+Q	0.7	1.1																																							
				@			D	+Q	1.6	1.2	1.8	0.9																															
				#			G	-Q	1.9		1.2		1.9	0.9																													
				#			PR	-Q	1.2	1.2		1.0	0.9																														
				#			D	-Q	1.9		1.9																																
D latch with PRE/CLR	<table border="1"> <tr><th>G</th><th>PR</th><th>CL</th><th>+Q</th><th>-Q</th></tr> <tr><td>1</td><td>0</td><td>0</td><td>D</td><td><math>\bar{D}</math></td></tr> <tr><td><math>\downarrow</math></td><td>0</td><td>0</td><td colspan="2">Latch</td></tr> <tr><td>X</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>X</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>X</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> </table> <p>X: Don't care</p>	G	PR	CL	+Q	-Q	1	0	0	D	$\bar{D}$	$\downarrow$	0	0	Latch		X	1	0	1	0	X	0	1	0	1	X	1	1	0	1	6	1.2	1	@		C	G	+Q	3.1	1.2	2.5	0.9
G	PR	CL	+Q	-Q																																							
1	0	0	D	$\bar{D}$																																							
$\downarrow$	0	0	Latch																																								
X	1	0	1	0																																							
X	0	1	0	1																																							
X	1	1	0	1																																							
LDPC3	D	+Q	2.2	1.8																																							
				@			CL	+Q	1.6	1.2	1.4	0.9																															
				#			D	+Q	3.1		1.2		2.5	0.9																													
				#			G	-Q	2.2	1.2		2.9	0.9																														
				#			PR	-Q	1.5		1.2	2.0		0.9																													
				#			CL	-Q	1.1	1.2		1.4	0.9																														
				#			D	-Q	2.2		2.9																																

Macrocell		Equiva- lent Gate Count	Normal- ized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay																													
Function	Truth table						Input Name	Output Name	$t_{PLH}(ns)$		$t_{PHL}(ns)$																									
Function Name									$t_{OLH}$	$k_{LH}$	$t_{OHL}$	$k_{HL}$																								
4-Bit D latch  LD4	<table border="1"> <tr> <td>G</td> <td>+Q<sub>0</sub></td> <td>+Q<sub>1</sub></td> <td>+Q<sub>2</sub></td> <td>+Q<sub>3</sub></td> </tr> <tr> <td>1</td> <td>D<sub>0</sub></td> <td>D<sub>1</sub></td> <td>D<sub>2</sub></td> <td>D<sub>3</sub></td> </tr> <tr> <td><math>\bar{1}</math></td> <td colspan="4">Latch</td> </tr> </table>	G	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>	1	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	$\bar{1}$	Latch				13	1 1 1 1 1	@ @ @ @ @		B4	G	+Q <sub>0</sub>	1.8	1.2	1.8	0.9									
G	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>																																
1	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>																																
$\bar{1}$	Latch																																			
						D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub>	+Q <sub>3</sub>	1.5		1.5																										
4-Bit D latch with CLR  LD4C1	<table border="1"> <tr> <td>G</td> <td>CL</td> <td>+Q<sub>0</sub></td> <td>+Q<sub>1</sub></td> <td>+Q<sub>2</sub></td> <td>+Q<sub>3</sub></td> </tr> <tr> <td>1</td> <td>0</td> <td>D<sub>0</sub></td> <td>D<sub>1</sub></td> <td>D<sub>2</sub></td> <td>D<sub>3</sub></td> </tr> <tr> <td><math>\bar{1}</math></td> <td>0</td> <td colspan="4">Latch</td> </tr> <tr> <td>X</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	G	CL	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>	1	0	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	$\bar{1}$	0	Latch				X	1	0	0	0	0	14	1 1 1 1 1	@ @ @ @ #		B4	G	+Q <sub>0</sub>	1.9	1.2	1.8	0.9
G	CL	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>																															
1	0	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>																															
$\bar{1}$	0	Latch																																		
X	1	0	0	0	0																															
						D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub>	+Q <sub>3</sub>	1.6		1.5																										
						CL		1.3		1.3																										

12. FLIP-FLOPS (Normal Type)

Macrocell		Equiva- lent Gate Count	Normal- ized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay																					
Function	Truth table						Input Name	Output Name	$t_{PLH}(ns)$		$t_{PHL}(ns)$																	
Function Name									$t_{OLH}$	$k_{LH}$	$t_{OHL}$	$k_{HL}$																
DFF  FD	<table border="1"> <tr> <td>CK</td> <td>+Q</td> <td>-Q</td> </tr> <tr> <td><math>\bar{1}</math></td> <td>D</td> <td><math>\bar{D}</math></td> </tr> <tr> <td><math>\bar{1}</math></td> <td>+Q<sub>0</sub></td> <td>-Q<sub>0</sub></td> </tr> </table>	CK	+Q	-Q	$\bar{1}$	D	$\bar{D}$	$\bar{1}$	+Q <sub>0</sub>	-Q <sub>0</sub>	6	1	@ @		C	CK	+Q	2.2	1.2	2.4	0.9							
CK	+Q	-Q																										
$\bar{1}$	D	$\bar{D}$																										
$\bar{1}$	+Q <sub>0</sub>	-Q <sub>0</sub>																										
							-Q	2.5	1.2	2.5	0.9																	
DFF with Load FDL1	<table border="1"> <tr> <td>CK</td> <td>L</td> <td>+Q</td> <td>-Q</td> </tr> <tr> <td><math>\bar{1}</math></td> <td>0</td> <td>D<sub>C</sub></td> <td><math>\bar{D}_C</math></td> </tr> <tr> <td><math>\bar{1}</math></td> <td>1</td> <td>D<sub>L</sub></td> <td><math>\bar{D}_L</math></td> </tr> <tr> <td><math>\bar{1}</math></td> <td>X</td> <td>+Q<sub>0</sub></td> <td>-Q<sub>0</sub></td> </tr> </table>	CK	L	+Q	-Q	$\bar{1}$	0	D <sub>C</sub>	$\bar{D}_C$	$\bar{1}$	1	D <sub>L</sub>	$\bar{D}_L$	$\bar{1}$	X	+Q <sub>0</sub>	-Q <sub>0</sub>	8	1 1 1 1.2	@ @ @ #		C	CK	+Q	2.2	1.2	2.4	0.9
CK	L	+Q	-Q																									
$\bar{1}$	0	D <sub>C</sub>	$\bar{D}_C$																									
$\bar{1}$	1	D <sub>L</sub>	$\bar{D}_L$																									
$\bar{1}$	X	+Q <sub>0</sub>	-Q <sub>0</sub>																									
							-Q	2.5	1.2	2.5	0.9																	
DFF with CLR FDC1	<table border="1"> <tr> <td>CK</td> <td>CL</td> <td>+Q</td> <td>-Q</td> </tr> <tr> <td><math>\bar{1}</math></td> <td>0</td> <td>D</td> <td><math>\bar{D}</math></td> </tr> <tr> <td><math>\bar{1}</math></td> <td>0</td> <td>+Q<sub>0</sub></td> <td>-Q<sub>0</sub></td> </tr> <tr> <td>X</td> <td>1</td> <td>0</td> <td>1</td> </tr> </table>	CK	CL	+Q	-Q	$\bar{1}$	0	D	$\bar{D}$	$\bar{1}$	0	+Q <sub>0</sub>	-Q <sub>0</sub>	X	1	0	1	7	1 1 1.2	@ @ #		C	CK	+Q	2.2	1.2	2.4	0.9
CK	CL	+Q	-Q																									
$\bar{1}$	0	D	$\bar{D}$																									
$\bar{1}$	0	+Q <sub>0</sub>	-Q <sub>0</sub>																									
X	1	0	1																									
						CL		—		2.5																		
						CK	-Q	2.9	1.2	2.6	0.9																	
						CL		0.9		—																		

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay																																																																				
Function	Truth table						Input Name	Output Name	t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)																																																																
Function Name									t <sub>OLH</sub>	K <sub>LH</sub>	t <sub>OHL</sub>	K <sub>HL</sub>																																																															
DFF with PRE FDP1	<table border="1"> <tr><th>CK</th><th>PR</th><th>+Q</th><th>-Q</th></tr> <tr><td>f</td><td>0</td><td>D</td><td><math>\bar{D}</math></td></tr> <tr><td><math>\bar{1}</math></td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>X</td><td>1</td><td>1</td><td>0</td></tr> </table>	CK	PR	+Q	-Q	f	0	D	$\bar{D}$	$\bar{1}$	0	+Q <sub>0</sub>	-Q <sub>0</sub>	X	1	1	0	7	1.2	@ @ #		C	CK	+Q	2.6	1.2	2.8	0.9																																															
	CK	PR	+Q	-Q																																																																							
	f	0	D	$\bar{D}$																																																																							
	$\bar{1}$	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																																							
X	1	1	0																																																																								
PR	+Q	1.0	1.2	—																																																																							
CK	-Q	2.8	1.2	3.0																																																																							
PR	-Q	—	1.2	1.4																																																																							
DFF with PRE/CLR FDPC3	<table border="1"> <tr><th>CK</th><th>PR</th><th>CL</th><th>+Q</th><th>-Q</th></tr> <tr><td>f</td><td>0</td><td>0</td><td>D</td><td><math>\bar{D}</math></td></tr> <tr><td><math>\bar{1}</math></td><td>0</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>X</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>X</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>X</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> </table>	CK	PR	CL	+Q	-Q	f	0	0	D	$\bar{D}$	$\bar{1}$	0	0	+Q <sub>0</sub>	-Q <sub>0</sub>	X	1	0	1	0	X	0	1	0	1	X	1	1	1	1	8	1.2	@ @ # #		C	CK	+Q	2.6	1.2	2.8	0.9																																	
	CK	PR	CL	+Q	-Q																																																																						
	f	0	0	D	$\bar{D}$																																																																						
	$\bar{1}$	0	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																																						
	X	1	0	1	0																																																																						
	X	0	1	0	1																																																																						
X	1	1	1	1																																																																							
CL	+Q	—	1.2	2.9																																																																							
PR	+Q	1.0	1.2	1.2																																																																							
CK	-Q	3.2	1.2	3.1																																																																							
CL	-Q	0.9	1.2	0.6																																																																							
PR	-Q	—	1.2	1.5																																																																							
JKFF FJ	<table border="1"> <tr><th>CK</th><th>J</th><th>K</th><th>+Q</th><th>-Q</th></tr> <tr><td>f</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>f</td><td>1</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>f</td><td>0</td><td>1</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>f</td><td>1</td><td>0</td><td>-Q<sub>0</sub></td><td>+Q<sub>0</sub></td></tr> <tr><td><math>\bar{1}</math></td><td>X</td><td>X</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> </table>	CK	J	K	+Q	-Q	f	0	0	0	1	f	1	1	1	0	f	0	1	+Q <sub>0</sub>	-Q <sub>0</sub>	f	1	0	-Q <sub>0</sub>	+Q <sub>0</sub>	$\bar{1}$	X	X	+Q <sub>0</sub>	-Q <sub>0</sub>	9	1.2	@ @ #		C	CK	+Q	2.7	1.2	2.1	0.9																																	
	CK	J	K	+Q	-Q																																																																						
	f	0	0	0	1																																																																						
	f	1	1	1	0																																																																						
f	0	1	+Q <sub>0</sub>	-Q <sub>0</sub>																																																																							
f	1	0	-Q <sub>0</sub>	+Q <sub>0</sub>																																																																							
$\bar{1}$	X	X	+Q <sub>0</sub>	-Q <sub>0</sub>																																																																							
CK	-Q	2.7	1.2	2.2																																																																							
CK	+Q	2.7	1.2	2.1																																																																							
CK	-Q	2.7	1.2	2.2																																																																							
JKFF with CLR FJC1	<table border="1"> <tr><th>CK</th><th>J</th><th>K</th><th>CL</th><th>+Q</th><th>-Q</th></tr> <tr><td>f</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>f</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>f</td><td>0</td><td>1</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>f</td><td>1</td><td>0</td><td>0</td><td>-Q<sub>0</sub></td><td>+Q<sub>0</sub></td></tr> <tr><td><math>\bar{1}</math></td><td>X</td><td>X</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>X</td><td>X</td><td>X</td><td>1</td><td>0</td><td>1</td></tr> </table>	CK	J	K	CL	+Q	-Q	f	0	0	0	0	1	f	1	1	0	1	0	f	0	1	0	+Q <sub>0</sub>	-Q <sub>0</sub>	f	1	0	0	-Q <sub>0</sub>	+Q <sub>0</sub>	$\bar{1}$	X	X	0	+Q <sub>0</sub>	-Q <sub>0</sub>	X	X	X	1	0	1	12	1.2	@ @ # #		C	CK	+Q	3.2	1.2	2.6	0.9																					
	CK	J	K	CL	+Q	-Q																																																																					
	f	0	0	0	0	1																																																																					
	f	1	1	0	1	0																																																																					
f	0	1	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																																						
f	1	0	0	-Q <sub>0</sub>	+Q <sub>0</sub>																																																																						
$\bar{1}$	X	X	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																																						
X	X	X	1	0	1																																																																						
CL	+Q	—	1.2	2.1																																																																							
CK	-Q	2.8	1.2	2.8																																																																							
CL	-Q	3.0	1.2	—																																																																							
JKFF with PRE/CLR FJPC1	<table border="1"> <tr><th>CK</th><th>J</th><th>K</th><th>PR</th><th>CL</th><th>+Q</th><th>-Q</th></tr> <tr><td>f</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>f</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>f</td><td>0</td><td>1</td><td>1</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>f</td><td>1</td><td>0</td><td>1</td><td>0</td><td>-Q<sub>0</sub></td><td>+Q<sub>0</sub></td></tr> <tr><td><math>\bar{1}</math></td><td>X</td><td>X</td><td>1</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>X</td><td>X</td><td>X</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>0</td><td>0</td></tr> </table>	CK	J	K	PR	CL	+Q	-Q	f	0	0	1	0	0	1	f	1	1	1	0	1	0	f	0	1	1	0	+Q <sub>0</sub>	-Q <sub>0</sub>	f	1	0	1	0	-Q <sub>0</sub>	+Q <sub>0</sub>	$\bar{1}$	X	X	1	0	+Q <sub>0</sub>	-Q <sub>0</sub>	X	X	X	0	0	1	0	X	X	X	1	1	0	1	X	X	X	0	1	0	0	13	1.2	@ @ # @ #		C	CK	+Q	3.2	1.2	2.6	0.9
	CK	J	K	PR	CL	+Q	-Q																																																																				
	f	0	0	1	0	0	1																																																																				
	f	1	1	1	0	1	0																																																																				
	f	0	1	1	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																																				
	f	1	0	1	0	-Q <sub>0</sub>	+Q <sub>0</sub>																																																																				
$\bar{1}$	X	X	1	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																																																					
X	X	X	0	0	1	0																																																																					
X	X	X	1	1	0	1																																																																					
X	X	X	0	1	0	0																																																																					
PR	+Q	2.9	1.2	—																																																																							
CL	+Q	0.9	1.2	2.1																																																																							
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PR	-Q	0.9	1.2	1.1																																																																							
CL	-Q	3.1	1.2	—																																																																							
TFF with CLR FTC1	<table border="1"> <tr><th>CK</th><th>CL</th><th>+Q</th><th>-Q</th></tr> <tr><td>f</td><td>0</td><td>-Q<sub>0</sub></td><td>+Q<sub>0</sub></td></tr> <tr><td><math>\bar{1}</math></td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>X</td><td>1</td><td>0</td><td>1</td></tr> </table>	CK	CL	+Q	-Q	f	0	-Q <sub>0</sub>	+Q <sub>0</sub>	$\bar{1}$	0	+Q <sub>0</sub>	-Q <sub>0</sub>	X	1	0	1	8	1.2	@ #		C	CK	+Q	2.2	1.2	2.4	0.9																																															
	CK	CL	+Q	-Q																																																																							
	f	0	-Q <sub>0</sub>	+Q <sub>0</sub>																																																																							
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CL	-Q	0.9	1.2	—																																																																							

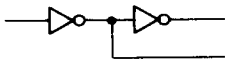
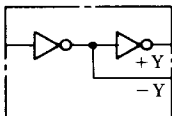
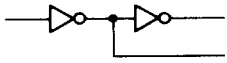
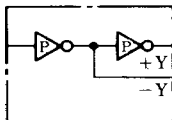
Macrocell		Equiva- lent Gate Count	Normal- ized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay																																			
Function	Truth table						Input Name	Output Name	$t_{PLH}(ns)$		$t_{PHL}(ns)$																															
Function Name									$t_{OLH}$	$K_{LH}$	$t_{OHL}$	$K_{HL}$																														
TFF with PRE	<table border="1"> <tr><td>CK</td><td>PR</td><td>+Q</td><td>-Q</td></tr> <tr><td>f</td><td>0</td><td>-Q<sub>0</sub></td><td>+Q<sub>0</sub></td></tr> <tr><td>1</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>x</td><td>1</td><td>1</td><td>0</td></tr> </table>	CK	PR	+Q	-Q	f	0	-Q <sub>0</sub>	+Q <sub>0</sub>	1	0	+Q <sub>0</sub>	-Q <sub>0</sub>	x	1	1	0	8	1	@		C	CK	+Q	2.6	1.2	2.8	0.9														
CK	PR	+Q	-Q																																							
f	0	-Q <sub>0</sub>	+Q <sub>0</sub>																																							
1	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																							
x	1	1	0																																							
PR		1.0																																								
CK	-Q	2.8	1.2	3.0	0.9																																					
PR		-		1.4																																						
FTP1			1.2	#																																						
TFF with PRE/CLR	<table border="1"> <tr><td>CK</td><td>PR</td><td>CL</td><td>+Q</td><td>-Q</td></tr> <tr><td>f</td><td>0</td><td>0</td><td>-Q<sub>0</sub></td><td>+Q<sub>0</sub></td></tr> <tr><td>1</td><td>0</td><td>0</td><td>+Q<sub>0</sub></td><td>-Q<sub>0</sub></td></tr> <tr><td>x</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>x</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>x</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> </table>	CK	PR	CL	+Q	-Q	f	0	0	-Q <sub>0</sub>	+Q <sub>0</sub>	1	0	0	+Q <sub>0</sub>	-Q <sub>0</sub>	x	1	0	1	0	x	0	1	0	1	x	1	1	1	1	9	1	@		C	CK		2.6		2.8	0.9
CK	PR	CL	+Q	-Q																																						
f	0	0	-Q <sub>0</sub>	+Q <sub>0</sub>																																						
1	0	0	+Q <sub>0</sub>	-Q <sub>0</sub>																																						
x	1	0	1	0																																						
x	0	1	0	1																																						
x	1	1	1	1																																						
PR	+Q	1.0	1.2	1.2																																						
CL		-		2.9																																						
CK	-Q	3.2		3.1	0.9																																					
PR		-	1.2	1.5																																						
CL		0.9		0.6																																						
FTPC3			1.2	#																																						
4-Bit DFF	<table border="1"> <tr><td>CK</td><td>+Q<sub>0</sub></td><td>+Q<sub>1</sub></td><td>+Q<sub>2</sub></td><td>+Q<sub>3</sub></td></tr> <tr><td>f</td><td>D<sub>0</sub></td><td>D<sub>1</sub></td><td>D<sub>2</sub></td><td>D<sub>3</sub></td></tr> <tr><td>1</td><td>+Q<sub>00</sub></td><td>+Q<sub>10</sub></td><td>+Q<sub>20</sub></td><td>+Q<sub>30</sub></td></tr> </table>	CK	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>	f	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	1	+Q <sub>00</sub>	+Q <sub>10</sub>	+Q <sub>20</sub>	+Q <sub>30</sub>	21	1	@		B4	CK	+Q <sub>0</sub>	2.4	1.2	2.6	0.9															
CK	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>																																						
f	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>																																						
1	+Q <sub>00</sub>	+Q <sub>10</sub>	+Q <sub>20</sub>	+Q <sub>30</sub>																																						
+Q <sub>3</sub>																																										
FD4			1	@																																						
4-Bit DFF with CLR	<table border="1"> <tr><td>CK</td><td>CL</td><td>+Q<sub>0</sub></td><td>+Q<sub>1</sub></td><td>+Q<sub>2</sub></td><td>+Q<sub>3</sub></td></tr> <tr><td>f</td><td>0</td><td>D<sub>0</sub></td><td>D<sub>1</sub></td><td>D<sub>2</sub></td><td>D<sub>3</sub></td></tr> <tr><td>1</td><td>0</td><td>+Q<sub>00</sub></td><td>+Q<sub>10</sub></td><td>+Q<sub>20</sub></td><td>+Q<sub>30</sub></td></tr> <tr><td>x</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> </table>	CK	CL	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>	f	0	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	1	0	+Q <sub>00</sub>	+Q <sub>10</sub>	+Q <sub>20</sub>	+Q <sub>30</sub>	x	1	0	0	0	0	25	1	@		B4	CK	+Q <sub>0</sub>	2.6	1.2	2.6	0.9						
CK	CL	+Q <sub>0</sub>	+Q <sub>1</sub>	+Q <sub>2</sub>	+Q <sub>3</sub>																																					
f	0	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>																																					
1	0	+Q <sub>00</sub>	+Q <sub>10</sub>	+Q <sub>20</sub>	+Q <sub>30</sub>																																					
x	1	0	0	0	0																																					
+Q <sub>3</sub>																																										
CL	+Q <sub>3</sub>	-		1.6																																						
FD4C1			1	#																																						

13. SHIFT REGISTERS (Normal Type)

Macrocell		Equiva- lent Gate Count	Normal- ized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay																																																																				
Function	Truth table						Input Name	Output Name	t <sub>PLH</sub> (ns)		t <sub>PHL</sub> (ns)																																																																
Function Name									t <sub>OLH</sub>	K <sub>LH</sub>	t <sub>OHL</sub>	K <sub>HL</sub>																																																															
2-Bit SR	<table border="1"> <tr><td>CK</td><td>+A</td><td>+B</td></tr> <tr><td>f</td><td>D</td><td>+A<sub>0</sub></td></tr> <tr><td>l</td><td>+A<sub>0</sub></td><td>+B<sub>0</sub></td></tr> </table>	CK	+A	+B	f	D	+A <sub>0</sub>	l	+A <sub>0</sub>	+B <sub>0</sub>	10	1	@		B1	CK	+A	2.3	1.2	2.5	0.9																																																						
CK	+A	+B																																																																									
f	D	+A <sub>0</sub>																																																																									
l	+A <sub>0</sub>	+B <sub>0</sub>																																																																									
ZSR							CK	+B	2.3	1.2	2.5	0.9																																																															
2-Bit SR with CLR	<table border="1"> <tr><td>CK</td><td>CLA</td><td>CLB</td><td>+A</td><td>+B</td></tr> <tr><td>f</td><td>0</td><td>0</td><td>D</td><td>+A<sub>0</sub></td></tr> <tr><td>l</td><td>0</td><td>0</td><td>+A<sub>0</sub></td><td>+B<sub>0</sub></td></tr> <tr><td>x</td><td>1</td><td>x</td><td>0</td><td>x</td></tr> <tr><td>x</td><td>x</td><td>1</td><td>x</td><td>0</td></tr> </table>	CK	CLA	CLB	+A	+B	f	0	0	D	+A <sub>0</sub>	l	0	0	+A <sub>0</sub>	+B <sub>0</sub>	x	1	x	0	x	x	x	1	x	0	12	1	@		C	CK	+A	2.4	1.2	2.6	0.9																																						
CK	CLA	CLB	+A	+B																																																																							
f	0	0	D	+A <sub>0</sub>																																																																							
l	0	0	+A <sub>0</sub>	+B <sub>0</sub>																																																																							
x	1	x	0	x																																																																							
x	x	1	x	0																																																																							
ZSRC1							CLA		-		2.5																																																																
							CK	+B	2.4	1.2	2.6	0.9																																																															
							CLB		-		2.5																																																																
2-Bit SR with CLR/PRE	<table border="1"> <tr><td>CK</td><td>CLA</td><td>CLB</td><td>PRA</td><td>PRB</td><td>+A</td><td>+B</td></tr> <tr><td>f</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D</td><td>+A<sub>0</sub></td></tr> <tr><td>l</td><td>0</td><td>0</td><td>0</td><td>0</td><td>+A<sub>0</sub></td><td>+B<sub>0</sub></td></tr> <tr><td>x</td><td>1</td><td>x</td><td>x</td><td>x</td><td>0</td><td>x</td></tr> <tr><td>x</td><td>x</td><td>1</td><td>x</td><td>x</td><td>x</td><td>0</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>1</td><td>x</td><td>1</td><td>x</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>1</td><td>x</td><td>1</td></tr> <tr><td>x</td><td>1</td><td>x</td><td>1</td><td>x</td><td>1</td><td>x</td></tr> <tr><td>x</td><td>x</td><td>1</td><td>x</td><td>1</td><td>x</td><td>1</td></tr> </table>	CK	CLA	CLB	PRA	PRB	+A	+B	f	0	0	0	0	D	+A <sub>0</sub>	l	0	0	0	0	+A <sub>0</sub>	+B <sub>0</sub>	x	1	x	x	x	0	x	x	x	1	x	x	x	0	x	x	x	1	x	1	x	x	x	x	x	1	x	1	x	1	x	1	x	1	x	x	x	1	x	1	x	1	14	1	@		B4	CK	+A	2.8	1.2	3.0	0.9
CK	CLA	CLB	PRA	PRB	+A	+B																																																																					
f	0	0	0	0	D	+A <sub>0</sub>																																																																					
l	0	0	0	0	+A <sub>0</sub>	+B <sub>0</sub>																																																																					
x	1	x	x	x	0	x																																																																					
x	x	1	x	x	x	0																																																																					
x	x	x	1	x	1	x																																																																					
x	x	x	x	1	x	1																																																																					
x	1	x	1	x	1	x																																																																					
x	x	1	x	1	x	1																																																																					
ZSRCP3							CLA		-		2.9																																																																
							PRA		1.0		1.2																																																																
							CK	+B	2.8	1.2	3.0	0.9																																																															
							CLB		-		2.9																																																																
							PRB		1.0		1.2																																																																
4-Bit SR	<table border="1"> <tr><td>CK</td><td>+A</td><td>+B</td><td>+C</td><td>+D</td></tr> <tr><td>f</td><td>D</td><td>+A<sub>0</sub></td><td>+B<sub>0</sub></td><td>+C<sub>0</sub></td></tr> <tr><td>l</td><td>+A<sub>0</sub></td><td>+B<sub>0</sub></td><td>+C<sub>0</sub></td><td>+D<sub>0</sub></td></tr> </table>	CK	+A	+B	+C	+D	f	D	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>	l	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>	+D <sub>0</sub>	19	1	@		C	CK	+A	2.4	1.2	2.6	0.9																																																
CK	+A	+B	+C	+D																																																																							
f	D	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>																																																																							
l	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>	+D <sub>0</sub>																																																																							
ZSR4							CK	+B	2.4	1.2	2.6	0.9																																																															
							CK	+C	2.4	1.2	2.6	0.9																																																															
							CK	+D	2.4	1.2	2.6	0.9																																																															
4-Bit SR with CLR	<table border="1"> <tr><td>CK</td><td>CLA</td><td>CLB</td><td>CLC</td><td>CLD</td><td>+A</td><td>+B</td><td>+C</td><td>+D</td></tr> <tr><td>f</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D</td><td>+A<sub>0</sub></td><td>+B<sub>0</sub></td><td>+C<sub>0</sub></td></tr> <tr><td>l</td><td>0</td><td>0</td><td>0</td><td>0</td><td>+A<sub>0</sub></td><td>+B<sub>0</sub></td><td>+C<sub>0</sub></td><td>+D<sub>0</sub></td></tr> <tr><td>x</td><td>1</td><td>x</td><td>x</td><td>x</td><td>0</td><td>x</td><td>x</td><td>x</td></tr> <tr><td>x</td><td>x</td><td>1</td><td>x</td><td>x</td><td>x</td><td>0</td><td>x</td><td>x</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>1</td><td>x</td><td>x</td><td>x</td><td>0</td><td>x</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>1</td><td>x</td><td>x</td><td>x</td><td>0</td></tr> </table>	CK	CLA	CLB	CLC	CLD	+A	+B	+C	+D	f	0	0	0	0	D	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>	l	0	0	0	0	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>	+D <sub>0</sub>	x	1	x	x	x	0	x	x	x	x	x	1	x	x	x	0	x	x	x	x	x	1	x	x	x	0	x	x	x	x	x	1	x	x	x	0	23	1	@		B4	CK	+A	2.6	1.2	2.8	0.9
CK	CLA	CLB	CLC	CLD	+A	+B	+C	+D																																																																			
f	0	0	0	0	D	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>																																																																			
l	0	0	0	0	+A <sub>0</sub>	+B <sub>0</sub>	+C <sub>0</sub>	+D <sub>0</sub>																																																																			
x	1	x	x	x	0	x	x	x																																																																			
x	x	1	x	x	x	0	x	x																																																																			
x	x	x	1	x	x	x	0	x																																																																			
x	x	x	x	1	x	x	x	0																																																																			
ZSR4C1							CLA		-		2.5																																																																
							CK	+B	2.6	1.2	2.8	0.9																																																															
							CLB		-		2.5																																																																
							CK	+C	2.6	1.2	2.8	0.9																																																															
							CLC		-		2.5																																																																
							CK	+D	2.6	1.2	2.8	0.9																																																															
							CLD		-		2.5																																																																

14. OTHERS

Macrocell		Equiva- lent Gate Count	Normal- ized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay										
Function	Equivalent circuit						Input Name	Output Name	$t_{PLH}(ns)$		$t_{PHL}(ns)$						
Function Name									$t_{OLH}$	$K_{LH}$	$t_{OHL}$	$K_{HL}$					
4-Bit comparator		12	1.2	#		B5	A0		1.4	3.7	1.6	0.9					
ZEQC4	A1						A2						A3				
1-Bit full- adder		7	1.2	#		B2	A, B	+Co	1.8	1.2	1.5	1.2					
FA1	Ci						0.9	0.8									
	A, B						+S	1.6	1.2	2.2	0.9						
	Ci						0.9	1.3									
2-Bit full- adder		14	1.2	#		C	An, Bn	+Co	2.7	1.2	2.6	1.2					
FA2	Ci						1.8	1.6									
	An, Bn						+Sn	2.7	1.2	3.0	0.9						
	Ci						1.8	2.1									
	4-Bit full- adder		43	1.2	#		B5	An, Bn	+Co	2.2	1.2	1.9	0.9				
FA4	Ci	2.0						1.7									
	An, Bn	+Sn						4.3	2.0	4.4	0.9						
	Ci	3.6						3.7									
	9-Bit parity generator/ checker							37	1	#		B5	A	Ev	4.2	3.7	3.0
PTGEN	?	OD															
			I	OD	3.2	1.2	4.5										

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent circuit						Input Name	Output Name	$t_{PLH}(ns)$		$t_{PHL}(ns)$	
Function Name									$t_{OLH}$	$K_{LH}$	$t_{OHL}$	$K_{HL}$
Buffer		1	1	@		A1	+Y	0.6	1.2	0.6	0.9	
BUF							-Y	0.3	1.2	0.4	0.9	
Power buffer		2	1.2	@		A1	+Y	0.7	0.6	0.7	0.5	
BUFP							-Y	0.4	0.6	0.4	0.5	

## 15. TTL 74 SERIES

Macro Function Name	Function	Gate count	
			with scan-function
HS00	QUADRUPLE 2-INPUT POSITIVE NAND GATES	4	
HS02	QUADRUPLE 2-INPUT POSITIVE NOR GATES	4	
HS04	HEX INVERTERS	6	
HS08	QUADRUPLE 2-INPUT POSITIVE AND GATES	8	
HS10	TRIPLE 3-INPUT POSITIVE NAND GATES	6	
HS11	TRIPLE 3-INPUT POSITIVE AND GATES	9	
HS20	DUAL 4-INPUT POSITIVE NAND GATES	4	
HS21	DUAL 4-INPUT POSITIVE AND GATES	6	
HS27	TRIPLE 3-INPUT POSITIVE NOR GATES	6	
HS30	8-INPUT POSITIVE NAND GATES	6	
HS32	QUADRUPLE 2-INPUT POSITIVE OR GATES	8	
HS42	BCD-TO-DECIMAL DECODER	28	
HS43	EXCESS 3-TO-DECIMAL DECODER	28	
HS44	EXCESS 3-GRAY-TO-DECIMAL DECODER	28	
HS51	2-WIDE 2-INPUT, 2-WIDE 3-INPUT AND-OR-INVERT GATES	6	
HS54	4-WIDE 2-INPUT, 3-INPUT AND-OR-INVERT GATE	9	
HS55	2-WIDE 4-INPUT AND-OR-INVERT GATE	5	
HS73	DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS (WITH CLEAR)	32	34
HS74	D-TYPE POSITIVE EDGE-TRIGGERED FLIP FLOPS	20	22
HS75	QUADRUPLE LATCHES	16	20
HS76	DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS (WITH PRESET AND CLEAR)	32	34
HS77	4-BIT BISTABLE LATCHES	16	20
HS78	DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS (WITH PRESET, COMMON CLEAR, AND COMMON CLOCK)	30	32
HS82	2-BIT BINARY FULL ADDER	29	
HS83	4-BIT BINARY FULL ADDER	63	
HS85	4-BIT MAGNITUDE COMPARATOR	78	
HS86	QUADRUPLE EXCLUSIVE-OR GATES	12	
HS90	DECADE COUNTER	41	45
HS91	8-BIT SHIFT REGISTER	50	58
HS92	DIVIDE-BY-TWELVE COUNTER	34	38
HS93	4-BIT BINARY COUNTER	32	36
HS94	4-BIT SHIFT REGISTER	44	48
HS95	4-BIT SHIFT REGISTER	40	44

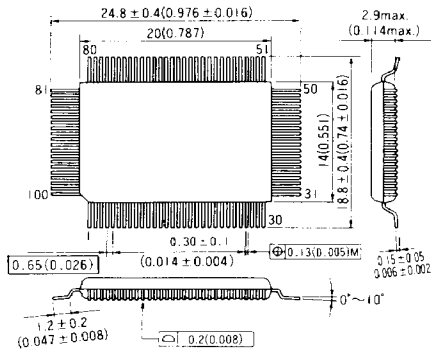
Macro Function Name	Function	Gate count	
			with scan-function
HS96	5-BIT SHIFT REGISTER (DUAL PARALLEL-IN, PARALLEL-OUT)	51	56
HS97	SYNCHRONOUS 6-BIT BINARY RATE MULTIPLEXER	144	150
HS98	4-BIT DATA SELECTOR/STORAGE REGISTER	35	39
HS99	4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTER	46	49
HS109	DUAL J-K POSITIVE EDGE-TRIGGERED FLIP FLOPS (WITH PRESET AND CLEAR)	28	30
HS113	DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS (WITH PRESET)	30	32
HS135	QUADRUPLE EXCLUSIVE-OR/NOR GATES	24	
HS137	3-LINE-TO-8-LINE DECODER/DEMUTIPLEXER WITH ADDRESS LATCHES	36	51
HS138	3-TO-8-LINE DECODER/DEMUTIPLEXER	25	
HS139	DUAL 2-TO-4-LINE DECODERS/DEMUTIPLEXERS	26	
HS147	10-LINE-TO-4-LINE PRIORITY ENCODER	46	
HS148	8-LINE-TO-3-LINE PRIORITY ENCODER	49	
HS150	16-BIT DATA SELECTOR/MULTIPLEXER	101	
HS151	1-OF-8-LINE DATA SELECTOR/MULTIPLEXER (WITH STROBE)	54	
HS152	1-OF-8-LINE DATA SELECTOR/MULTIPLEXER	29	
HS153	DUAL 4-OF-1-LINE DATA SELECTORS/MULTIPLEXERS	26	
HS154	4-OF-16-LINE DECODER/DEMUTIPLEXER	89	
HS155	DUAL 2-OF-4-LINE DECODERS/DEMUTIPLEXERS	23	
HS157	QUADRUPLE 2-OF-1-LINE DATA SELECTORS/MULTIPLEXERS (WITH NONINVERTED DATA OUTPUTS)	15	
HS158	QUADRUPLE 2-OF-1-LINE DATA SELECTORS/MULTIPLEXERS (WITH INVERTED DATA OUTPUTS)	11	
HS160	SYNCHRONOUS DECADE COUNTER	76	80
HS161	SYNCHRONOUS 4-BIT BINARY COUNTER	80	84
HS162	FULLY SYNCHRONOUS DECADE COUNTER	72	76
HS163	FULLY SYNCHRONOUS 4-BIT BINARY COUNTER	76	80
HS164	8-BIT PARALLEL-OUT SHIFT REGISTER	59	67
HS165	PARALLEL-LOAD 8-BIT SHIFT REGISTER	93	101
HS166	PARALLEL-LOAD 8-BIT SHIFT REGISTER	85	93
HS168	SYNCHRONOUS DECADE UP/DOWN COUNTER	94	98
HS169	SYNCHRONOUS BINARY UP/DOWN COUNTER	85	89
HS173	4-BIT D-TYPE REGISTER (WITH 3-STATE OUTPUTS)	51	55
HS174	HEX D-TYPE FLIP FLOPS (WITH CLEAR)	43	49
HS175	QUADRUPLE D-TYPE FLIP FLOPS (WITH CLEAR)	29	33
HS176	PRESETTABLE DECADE COUNTER	74	78

Macro Function Name	Function	Gate count	
			with scan-function
HS177	PRESETTABLE 4-BIT BINARY COUNTER	60	64
HS180	8-BIT ODD/EVEN PARITY GENERATOR/CHECKER	30	
HS181	ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR	119	
HS182	LOOK-AHEAD CARRY GENERATOR	41	
HS183	DUAL CARRY SAVE FULL ADDERS	40	
HS190	SYNCHRONOUS UP/DOWN DECADE COUNTER (SINGLE CLOCK LINE)	105	109
HS191	SYNCHRONOUS UP/DOWN 4-BIT BINARY COUNTER (SINGLE CLOCK LINE)	101	105
HS192	SYNCHRONOUS UP/DOWN DECADE COUNTER (DUAL CLOCK LINE)	91	95
HS193	SYNCHRONOUS UP/DOWN 4-BIT BINARY COUNTER (DUAL CLOCK LINE)	87	91
HS194	4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER	73	77
HS195	4-BIT PARALLEL ACCESS SHIFT REGISTER	47	51
HS198	8-BIT PARALLEL-IN, PARALLEL-OUT BIDIRECTIONAL SHIFT REGISTER	103	111
HS199	8-BIT PARALLEL-IN, PARALLEL-OUT SHIFT REGISTER (J-K INPUT FIRST STAGE)	89	97
HS251	1-OF-8-LINE DATA SELECTOR/MULTIPLEXER (WITH 3-STATE OUTPUTS)	34	
HS253	DUAL DATA SELECTORS/MULTIPLEXERS (WITH 3-STATE OUTPUTS)	32	
HS257	QUADRUPLE 2-TO-1-LINE DATA SELECTORS/MULTIPLEXERS (WITH NONINVERTED 3-STATE OUTPUTS)	19	
HS258	QUADRUPLE 2-TO-1-LINE DATA SELECTORS/MULTIPLEXERS (WITH 3-STATE OUTPUTS)	23	
HS259	8-BIT ADDRESSABLE LATCH	95	103
HS273	OCTAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP FLOPS (WITH CLEAR)	57	65
HS279	QUADRUPLE S-R LATCHES	18	38
HS280	9-BIT ODD/EVEN PARITY GENERATOR/CHECKER	62	
HS283	4-BIT BINARY FULL ADDER (WITH FAST CARRY)	66	
HS290	DECADE COUNTER	40	44
HS293	4-BIT BINARY COUNTER	32	36
HS298	QUADRUPLE 2-INPUT MULTIPLEXERS (WITH STORAGE)	35	39
HS299	8-BIT UNIVERSAL SHIFT/STORAGE REGISTER (WITH 3-STATE OUTPUTS)	160	168
HS373	OCTAL D-TYPE TRANSPARENT LATCHES (WITH 3-STATE OUTPUTS)	49	57
HS374	OCTAL D-TYPE EDGE-TRIGGERED FLOP FLOPS (WITH 3-STATE OUTPUTS)	65	73
HS390	DUAL DECADE COUNTERS	66	74
HS393	DUAL 4-BIT BINARY COUNTERS	58	66
HS490	DUAL 4-BIT DECADE COUNTERS	78	86
HS668	SYNCHRONOUS DECADE UP/DOWN COUNTER	95	99
HS669	SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER	80	84

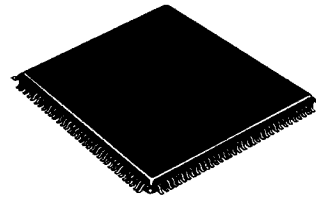
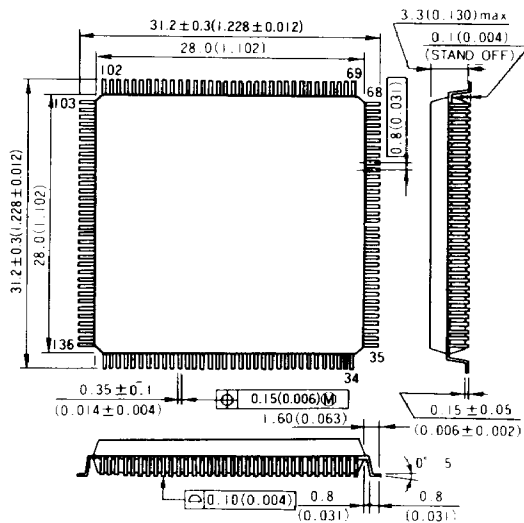
PACKAGE OUTLINE

Unit: mm (inch)

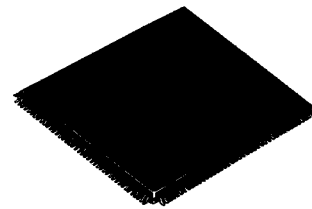
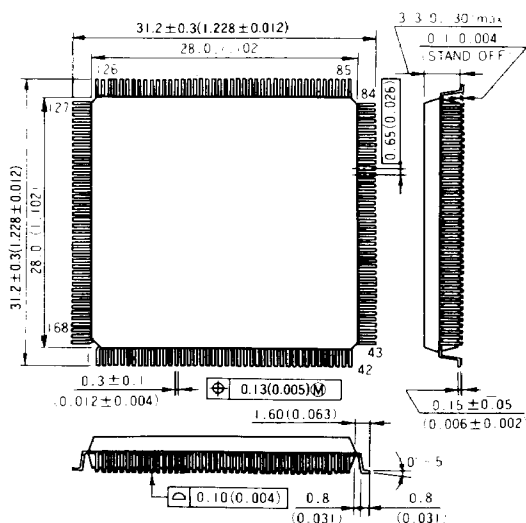
QFP-100



QFP5-136



QFP5-168



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