ProASIC3 Flash Family FPGAs

FlashLock

Features and Benefits

High Capacity

- 30 k to 1 Million System Gates
- Up to 144 kbits of True Dual-Port SRAM
- Up to 288 User I/Os

Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Live-At-Power-Up Level 0 Support
- Single-Chip Solution
- Retains Programmed Design When Powered Off

On-Chip User Nonvolatile Memory

- 1 kbit of FlashROM (FROM)

Performance

- 150+ MHz Internal System Performance with 3.3 V, 66 MHz 64-bit PCI (except A3P030)
- Up to 350 MHz External System Performance

In-System Programming (ISP) and Security

- Secure ISP Using On-Chip 128-Bit AES Decryption via JTAG (IEEE1532-compliant) (except A3P030)
- FlashLock™ to Secure FPGA Contents

Low Power

- 1.5 V Core Voltage for Low Power
- Support for 1.5-V-Only Systems
- Low-Impedance Flash Switches

High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure
- Ultra-Fast Local and Long-Line Network
- Enhanced High-Speed, Very Long-Line Network
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Advanced I/O

- 700 Mbps DDR, LVDS-Capable I/Os (A3P250 and above)
- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages – Up to 4 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X (except A3P030), and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL and LVDS (A3P250 and above)
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable I/Os (A3P030 only)
- Programmable Output Slew Rate and Drive Strength
- Weak Pull-Up/Down
- IEEE1149.1 (JTAG) Boundary-Scan Test
- Pin-Compatible Packages Across the ProASIC3 Family

Clock Conditioning Circuit (CCC) and PLL (except A3P030)

- Six CCC Blocks Total, One with an Integrated PLL
- Flexible Phase Shift, Multiply/Divide, and Delay Capabilities
- Wide Input Frequency Range (1.5 MHz to 350 MHz)

SRAMs and FIFOs (except A3P030)

- Variable-Aspect Ratio 4,608-bit RAM Blocks (x1, x2, x4, x9, x18 Organizations Available)
- True Dual-Port SRAM (except x18)
- 24 SRAM and FIFO Configurations with Synchronous Operation up to 350 MHz
- Programmable Embedded FIFO Control Logic

Table 1 • **ProASIC3 Product Family**

	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
System Gates	30 k	60 k	125 k	250 k	400 k	600 k	1 M
VersaTiles (D-Flip-Flops)	768	1,536	3,072	6,144	9,216	13,824	24,576
RAM kbits (1,024 bits)	–	18	36	36	54	108	144
4,608 Bit Blocks	–	4	8	8	12	24	32
FlashROM (FROM) Bits	1 k	1 k	1 k	1 k	1 k	1 k	1 k
Secure (AES) ISP	–	Yes	Yes	Yes	Yes	Yes	Yes
Integrated PLL in CCCs	–	1	1	1	1	1	1
VersaNet Globals[1]	6	18	18	18	18	18	18
I/O Banks	2	2	2	4	4	4	4
Maximum User I/Os	81	96	133	157	194	227	288
Package Pins QFN VQFP TQFP PQFP FBGA	 QN132 VQ100	 VQ100 TQ144 FG144	 VQ100 TQ144 PQ208 FG144	 VQ100 PQ208 FG144, FG256	 PQ208 FG144, FG256, FG484	 PQ208 FG144, FG256, FG484	 PQ208 FG144, FG256, FG484

Notes:

1. *Six chip (main) and three quadrant global networks are available for A3P060 and above.*
2. *For higher densities and support of additional features, refer to the ProASIC3E Flash FPGAs datasheet.*

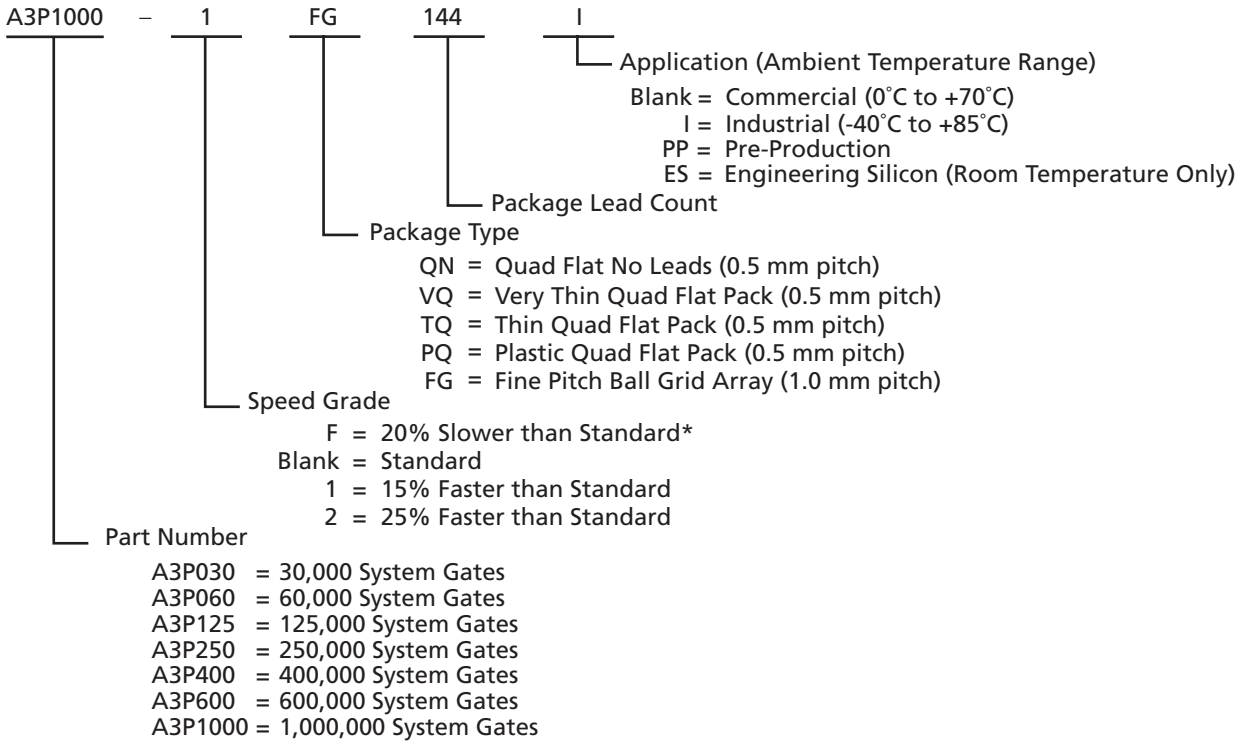
I/Os Per Package

Package	A3P030	A3P060	A3P125	A3P250		A3P400		A3P600		A3P1000	
	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs	Single-Ended I/O	Differential I/O Pairs
QN132	81	–	–	–	–	–	–		–	–	–
VQ100	79	71	71	68	13	–	–		–	–	–
TQ144	–	91	100	–	–	–	–	–	–	–	–
PQ208	–	–	133	151	34	151	33	154	35	154	35
FG144	–	96	97	97	24	97	24	97	24	97	24
FG256	–	–	–	157	38	178	38	179	45	179	45
FG484	–	–	–	–	–	194	38	227	56	288	68

Notes:

1. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
2. *FG256 and FG484 are footprint-compatible packages.*
3. *Advanced information subject to change.*

Ordering Information



Note: **DC and switching characteristics for –F speed grade targets based only on simulation. The characteristics provided for –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in commercial temperature range.*

Figure 1 • **Ordering Information**

Temperature Grade Offerings

Package	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
QN132	C, I	–	–	–	–	–	–
VQ100	C, I	C, I	C, I	C, I	–	–	–
TQ144	–	C, I	C, I	–	–	–	–
PQ208	–	–	C, I	C, I	C, I	C, I	C, I
FG144	–	C, I	C, I	C, I	C, I	C, I	C, I
FG256	–	–	–	C, I	C, I	C, I	C, I
FG484	–	–	–	–	C, I	C, I	C, I

Note: *C = Commercial Temperature Range: 0°C to 70°C Ambient*
I = Industrial Temperature Range: –40°C to 85°C Ambient

Speed Grade and Temperature Grade Matrix

	–F [3]	Std.	–1	–2
C	✓	✓	✓	✓
I	–	✓	✓	✓

Notes:

1. *C = Commercial Temperature Range: 0°C to 70°C Ambient*
2. *I = Industrial Temperature Range: –40°C to 85°C Ambient*
3. *DC and switching characteristics for –F speed grade targets based only on simulation. The characteristics provided for –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in commercial temperature range.*

Contact your local Actel representative for device availability (http://www.actel.com/contact/offices/index.html).

Table of Contents

Introduction and Overview

General Description

ProASIC3, the third-generation family of Actel Flash FPGAs, offers performance, density, and features beyond those of the ProASIC[PLUS®] family. The nonvolatile Flash technology gives ProASIC3 devices the advantage of being a secure, low-power, single-chip solution that is live at power-up. ProASIC3 is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3 devices offer 1 kbit of on-chip, user nonvolatile FlashROM (FROM) memory storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The A3P030 device has no PLL or RAM support. ProASIC3 devices have up to 1 million system gates, supported with up to 144 kbits of true dual-port SRAM and up to 288 user I/Os.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low-unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, the Flash-based ProASIC3 devices allow for all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3 family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3 family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Security

The nonvolatile, Flash-based ProASIC3 devices require no boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3 devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile, Flash programming can offer.

ProASIC3 devices utilize a 128-bit Flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FROM data in the ProASIC3 devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000, and replaces the 1977 DES standard. ProASIC3 devices have a built-in AES decryption engine and a Flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3 devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed ProASIC3 device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3 family. The Flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. ProASIC3, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. A ProASIC3 device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store the configuration information in on-chip Flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, Flash-based ProASIC3 FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load the device configuration data. This reduces bill-of-materials costs and printed circuit board (PCB) area, and increases security and system reliability.

Live at Power-Up

Actel's Flash-based ProASIC3 devices support Level 0 of the live-at-power-up classification standard, hence helping in system components initialization, executing critical tasks before the processor wakes up, setup and configure memory blocks, clock generation, and bus activity management. The live-at-power-up feature of Flash-based ProASIC3 devices greatly simplifies total system design and reduces total system cost, often eliminating the need for Complex Programmable Logic Device (CPLD) and clock generation PLL that are used for this purpose in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC3 device's Flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC3 devices simplify total system design, and reduce cost and design risk, while increasing system reliability and improving system initialization time.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC3 Flash-based FPGAs. Once it is programmed, the Flash cell configuration element of ProASIC3 FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based ProASIC3 devices exhibit power characteristics similar to an ASIC, making them an ideal choice for power-sensitive applications. ProASIC3 devices have only a very limited power-on current surge, and no high-current transition period, both of which occur on many FPGAs.

ProASIC3 devices also have low dynamic power consumption to further maximize power savings.

Advanced Flash Technology

The ProASIC3 family offers many benefits, including nonvolatility and reprogrammability through an advanced Flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant Flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

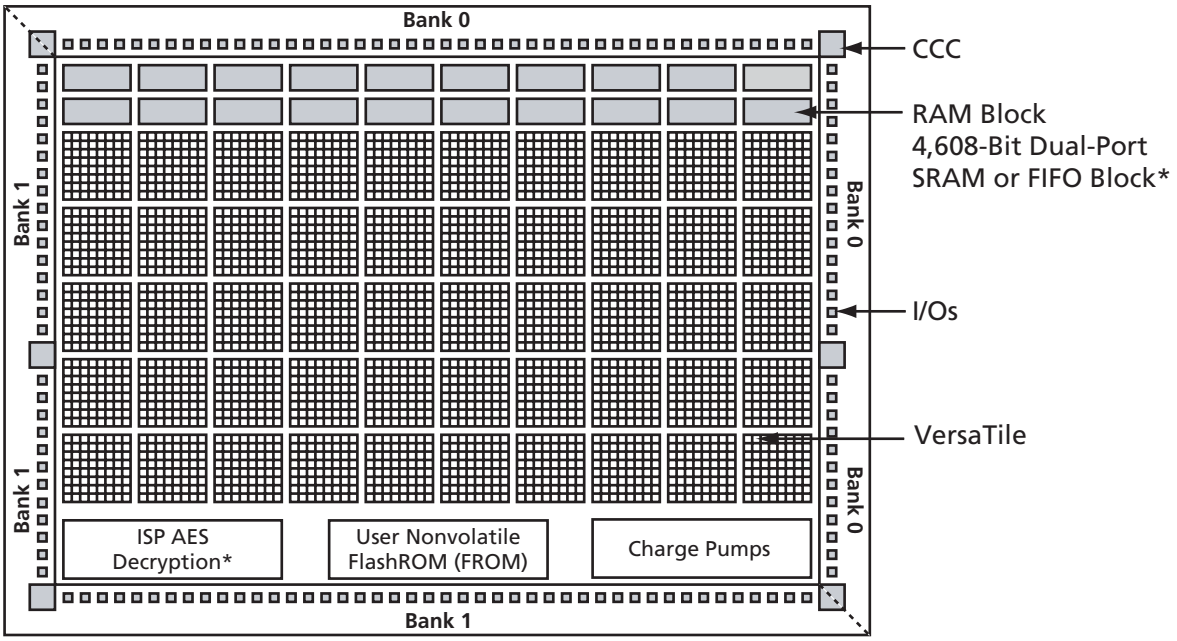
The proprietary ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-3 and Figure 1-2 on page 1-3):

- Dedicated FlashROM (FROM) memory
- Dedicated SRAM/FIFO memory[1]
- Extensive clock conditioning circuitry (CCC) and PLLs[1]
- Advanced I/O structure
- FPGA VersaTiles

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function or a D-flip-flop (with or without enable) or latch by programming the appropriate Flash switch interconnections. The versatility of the ProASIC3 core tile as either a three-input look-up-table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC families of Flash-based FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of the ProASIC3 devices via an IEEE1532 JTAG interface.

1. The A3P030 device does not support PLL and SRAM.



Note: **Not supported by A3P030.*

Figure 1-1 • **ProASIC3 Device Architecture Overview with Two I/O Banks (A3P030, A3P060, A3P125)**

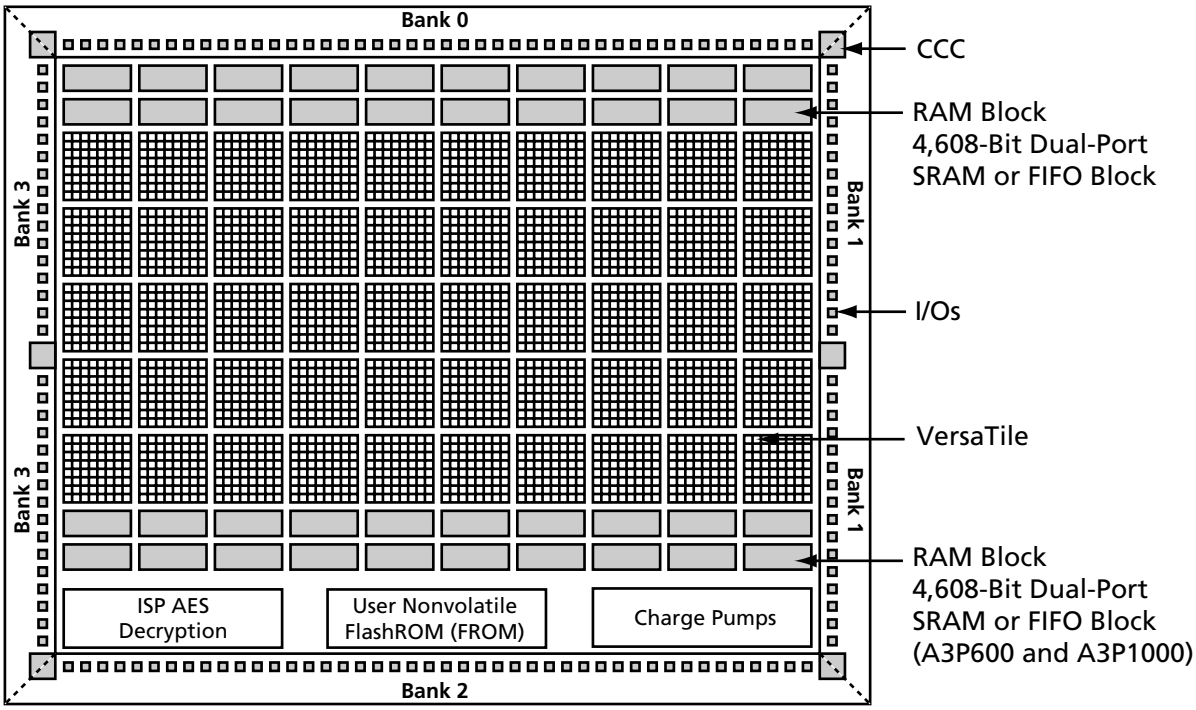


Figure 1-2 • **ProASIC3 Device Architecture Overview with Four I/O Banks (A3P250, A3P400, A3P600, and A3P1000)**

User Nonvolatile FlashROM (FROM)

Actel ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM (FROM). The FROM can be used in diverse system applications such as:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FROM is written using the standard ProASIC3 IEEE1532 JTAG programming interface. The core can be individually programmed (erased and written) and on-chip AES decryption can be used selectively to securely load data over public networks (except in the A3P030 device), such as security keys stored in the FROM for a user design.

The FROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FROM can ONLY be programmed from the JTAG interface, and cannot be programmed from the internal logic array.

The FROM is programmed as 8 banks of 128 bits; however, reading is performed on a random byte-by-byte basis. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three MSBs of the FROM address determine the bank and the four LSBs of the FROM address define the byte.

The Actel ProASIC3 development software solutions, Libero® Integrated Design Environment (IDE) and Designer version 6.1 or later, have extensive support for the FROM memory. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. The second part allows the inclusion of static data for system version control. Data for the FROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FROM contents.

SRAM and FIFO

ProASIC3 devices (except in the A3P030 device) have embedded SRAM blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256x18, 512x9, 1kx4, 2kx2, or 4kx1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a four-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode), using the UJTAG macro (except for the A3P030 device). Refer to the application note, *UJTAG in ProASIC3/E Devices*, for more details.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost-Empty (AEMPTY) and Almost-Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for the generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and Clock Conditioning Circuitry (CCC)

ProASIC3 devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3 family contains six CCCs. One CCC (center west side) has a phase-locked loop (PLL) (Figure 2-10 on page 2-10). The A3P030 does not have a PLL.

The six CCC blocks are located in the four corners and the centers of the east and west sides.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access (refer to the "Clock Conditioning Circuits" section on page 2-13 for more information).

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several I/O inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has the following key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- Two programmable delay types; refer to Figure 2-17 on page 2-17, Table 2-4 on page 2-18, and the "Features Supported on Every I/O" section on page 2-29 for more information.
- Clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% * clock period peak-to-peak period jitter (for PLL only)
  - 70 ps at 350 MHz
  - 90 ps at 100 MHz
  - 180 ps at 24 MHz
- Maximum acquisition time = 150 µs (for PLL only)
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter – allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps * (350 MHz / f_{OUT_CCC}) (for PLL only)

Global Clocking

ProASIC3 devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks (Figure 2-10 on page 2-10). The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

The ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). In all, ProASIC3 FPGAs support many different I/O standards, both single-ended and differential. For more information, see Table 2-19 on page 2-42.

The I/Os are organized into banks, with two or four banks per device. Refer to Table 2-18 on page 2-42 for details on I/O bank configuration. The configuration of these banks determines the I/O standards supported (see Table 2-18 on page 2-42 for more information).

Each I/O module contains several input, output, and enable registers (Figure 2-23 on page 2-30). These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications – DDR LVDS I/O for point-to-point communications

VersaTiles

The ProASIC3 core consists of VersaTiles, which have been enhanced over the ProASIC^{PLUS} core tiles. The ProASIC3 VersaTile supports the following:

- All three-input logic functions – LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-3 for VersaTile configurations.

For more information about VersaTiles, refer to the "VersaTile" section on page 2-2.

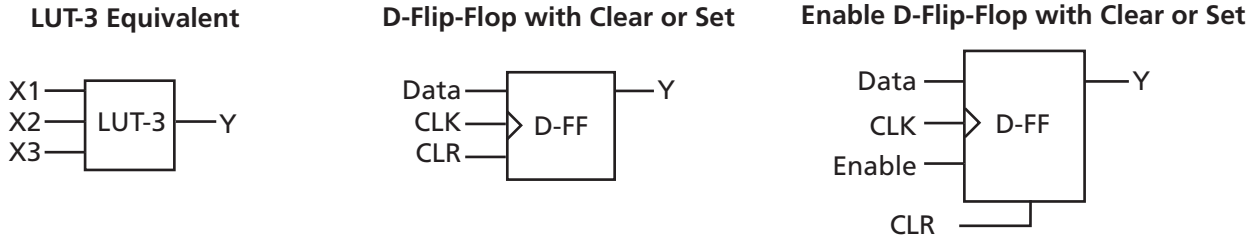


Figure 1-3 • **VersaTile Configurations**

Related Documents

Application Notes

In-System Programming (ISP) in ProASIC3/E Using FlashPro3
http://www.actel.com/documents/PA3_E_ISP_AN.pdf
Optimal Usage of Global Network Spines in ProASIC^{PLUS} Devices
http://www.actel.com/documents/PAPLUS_Spines_AN.pdf
ProASIC3/E FlashROM (FROM)
http://www.actel.com/documents/PA3_E_FROM_AN.pdf
ProASIC3/E Security
http://www.actel.com/documents/PA3_E_Security_AN.pdf
ProASIC3/E SRAM/FIFO Blocks
http://www.actel.com/documents/PA3_E_SRAMFIFO_AN.pdf
Programming a ProASIC3/E Using a Microprocessor
http://www.actel.com/documents/PA3_E_Microprocessor_AN.pdf
UJTAG Applications in ProASIC3/E Devices
http://www.actel.com/documents/PA3_E_UJTAG_AN.pdf
Using DDR for ProASIC3/E Devices
http://www.actel.com/documents/PA3_E_DDR_AN.pdf
Using Global Resources in Actel ProASIC3/E Devices
http://www.actel.com/documents/PA3_E_Global_AN.pdf

For additional ProASIC3 application notes, go to http://www.actel.com/techdocs/appnotes/products.aspx.

User's Guides

ACTgen Core Reference Guide
http://www.actel.com/documents/gen_refguide.pdf
Designer's User's Guide
http://www.actel.com/documents/designerUG.pdf
ProASIC3/E Macro Library Guide
http://www.actel.com/documents/pa3_libguide.pdf

Device Architecture

Introduction

Flash Technology

Advanced Flash Switch

Unlike SRAM FPGAs, the ProASIC3 family uses a live-on-power-up ISP Flash switch as its programming element. Flash cells are distributed throughout the device to provide nonvolatile, reconfigurable programming to connect signal lines to the appropriate VersaTile inputs and outputs. In the Flash switch, two transistors share the floating gate, which stores the programming information (Figure 2-1). One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. The latter is used to connect or separate routing nets, or to configure VersaTile logic. It is also used to erase the floating gate. Dedicated high-performance lines are connected as required using the Flash switch for fast, low-skew, global signal distribution throughout the device core. Maximum core utilization is possible for virtually any design. The use of the Flash switch technology also removes the possibility of firm errors, which are increasingly common in SRAM-based FPGAs.

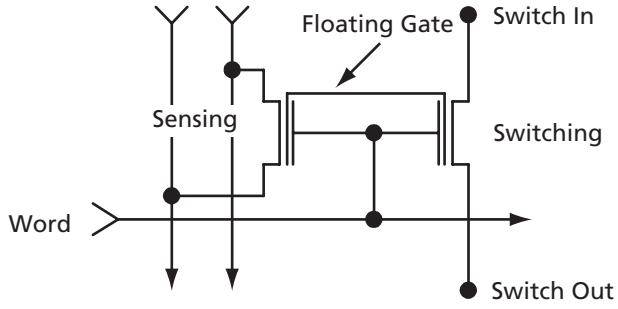


Figure 2-1 • **ProASIC3 Flash-Based Switch**

Device Overview

The ProASIC3 device family consists of five distinct programmable architectural features (Figure 2-2 and Figure 2-3 on page 2-3):

- FPGA fabric/core (VersaTiles)
- Routing and clock resources (VersaNets)
- FlashROM (FROM) memory
- Dedicated SRAM/FIFO memory (except A3P030)
- Advanced I/O structure

Core Architecture

VersaTile

The proprietary ProASIC3 family architecture provides granularity comparable to gate arrays. The ProASIC3 device core consists of a sea-of-VersaTiles architecture.

As illustrated in Figure 2-4 on page 2-4, there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate Flash switch connections:

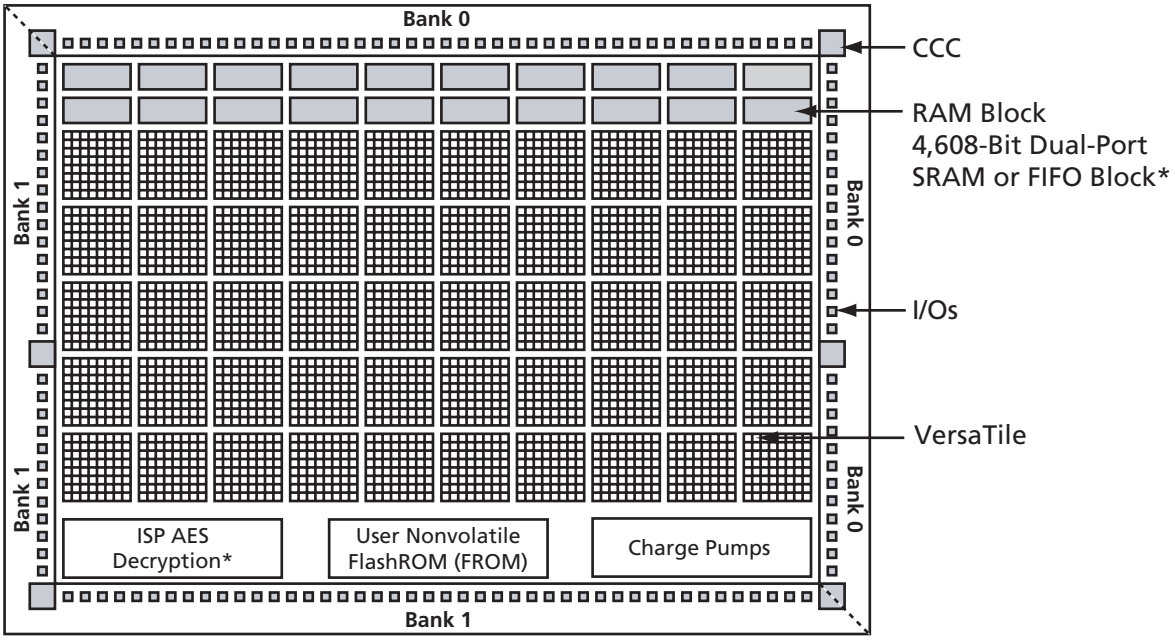
- Any three-input logic function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a fourth input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, the SET/CLR is supported by a fourth input. The fourth input is routed to the core cell over the VersaNet (global) network.

The SET/CLR signal can only be routed to this fourth input over the VersaNet (global) network. However, if in the user design, the SET/CLR signal is not routed over the VersaNet network, a compile warning message will be given and the intended logic function will be implemented by two VersaTiles instead of one.

The output of the VersaTile is F2 when the connection is to the ultra-fast local lines, or YL when connection is to the efficient long-lines or very-long-lines resources.



Note: **Not supported by A3P030.*

Figure 2-2 • **ProASIC3 Device Architecture Overview with Two I/O Banks (A3P030, A3P060, A3P125)**

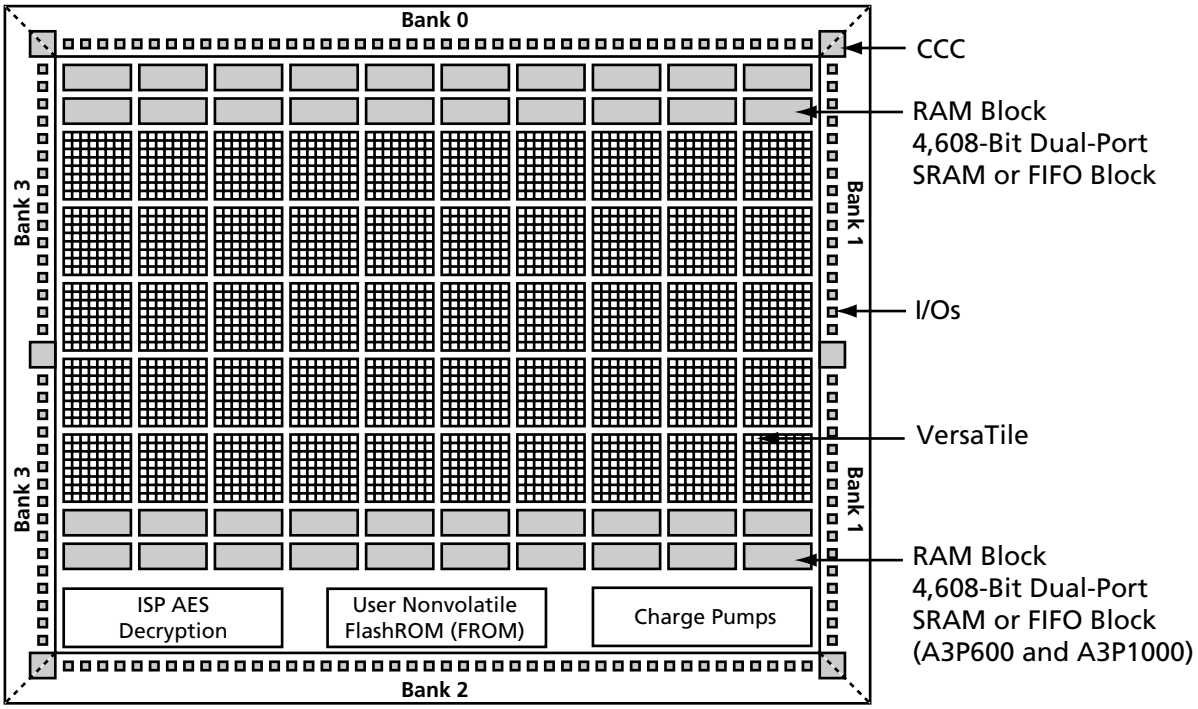
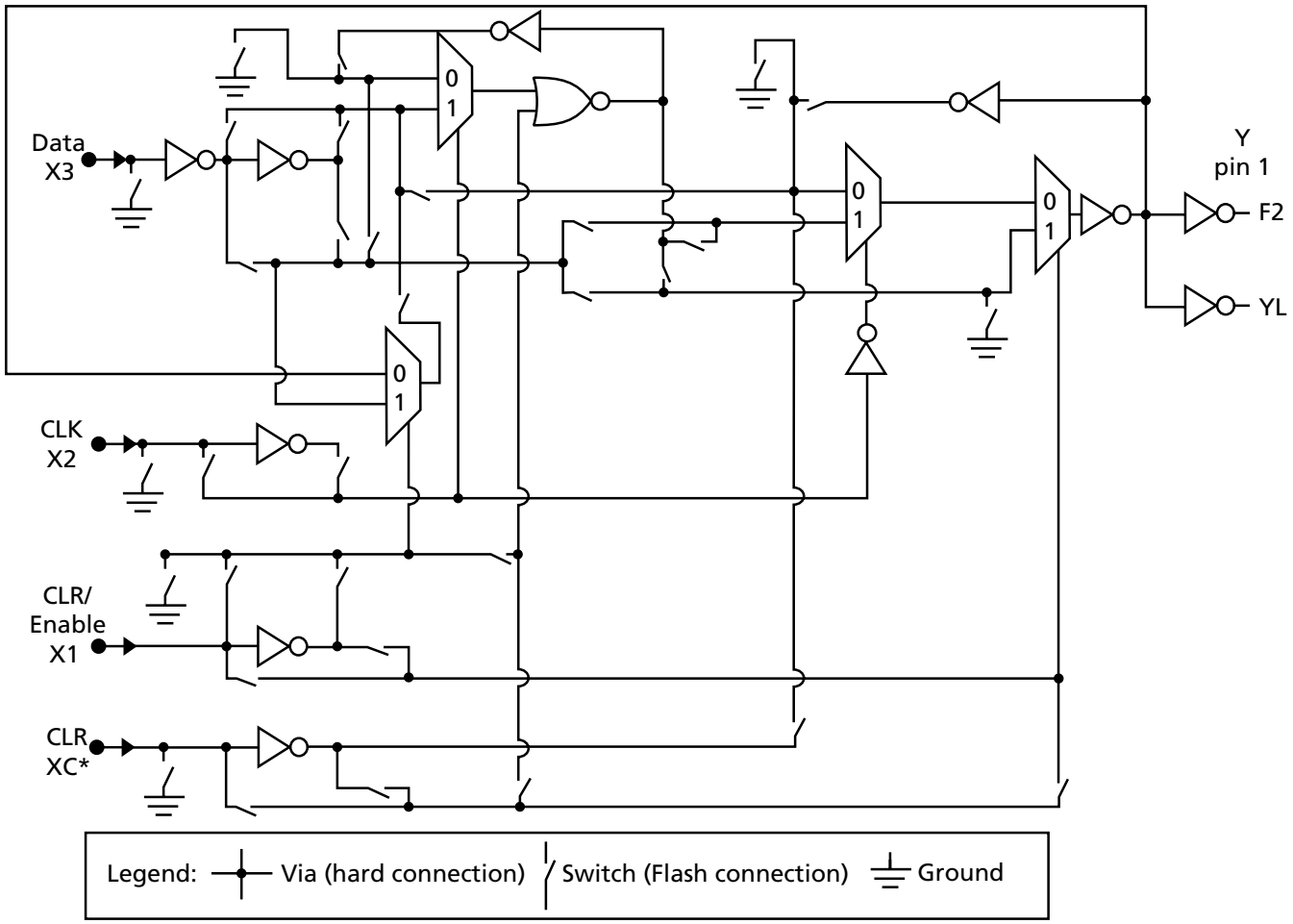


Figure 2-3 • **ProASIC3 Device Architecture Overview with Four I/O Banks (A3P250, A3P400, A3P600, A3P1000)**



Note: **This input can only be connected to the global clock distribution network.*

Figure 2-4 • **ProASIC3 Core VersaTile**

Array Coordinates

During many place-and-route operations in the Actel Designer software tool, it is possible to set constraints that require array coordinates. Table 2-1 is provided as a reference. The array coordinates are measured from the lower left (0, 0). They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

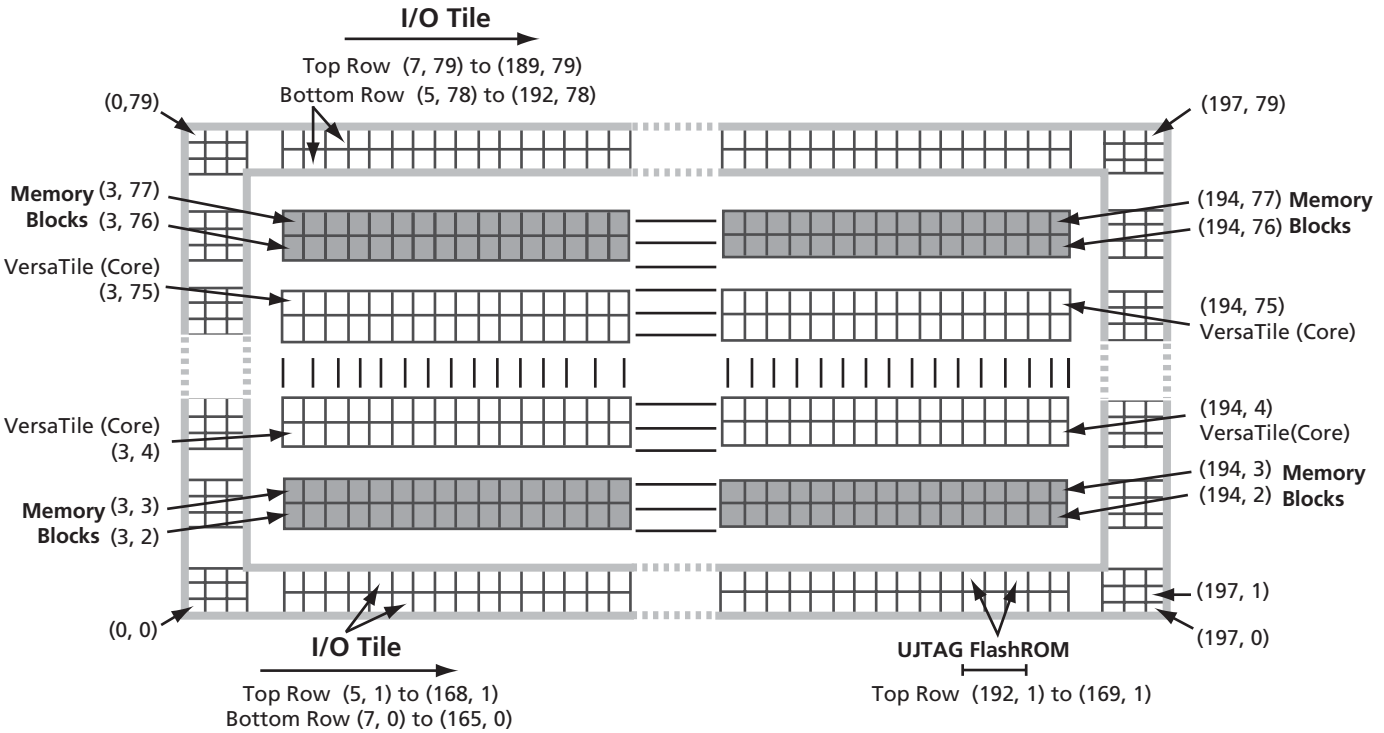
Table 2-1 provides array coordinates of core cells and memory blocks.

Since the I/O coordinate system changes depending on the die/package combination, it is not listed in Table 2-1. The Designer ChipPlanner tool provides array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 2-5 illustrates the array coordinates of an A3P600 device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for ProASIC3 software tools.

Table 2-1 • **ProASIC3 Array Coordinates**

	VersaTiles				Memory Rows		All	
	Min.		Max.		Bottom	Top	Min.	Max.
Device	**x**	**y**	**x**	**y**	**(x, y)**	**(x, y)**	**(x, y)**	**(x, y)**
A3P030	–	–	–	–	–	–	–	–
A3P060	3	2	66	25	None	(3, 26)	(0, 0)	(69, 29)
A3P125	3	2	130	25	None	(3, 26)	(0, 0)	(133, 29)
A3P250	3	2	130	49	None	(3, 50)	(0, 0)	(133, 53)
A3P400	3	2	194	49	None	(3, 50)	(0, 0)	(197, 53)
A3P600	3	4	194	75	(3,2)	(3, 76)	(0, 0)	(197, 79)
A3P1000	3	4	258	99	(3,2)	(3, 100)	(0, 0)	(261, 103)



Note: *The vertical I/O tile coordinates are not shown. West side coordinates are {(0, 2) to (2, 2)} to {(0, 77) to (2, 77)}; east side coordinates are {(195, 2) to (197, 2)} to {(195, 77) to (197, 77)}.*

Figure 2-5 • **Array Coordinates for A3P600**

Routing Architecture

Routing Resources

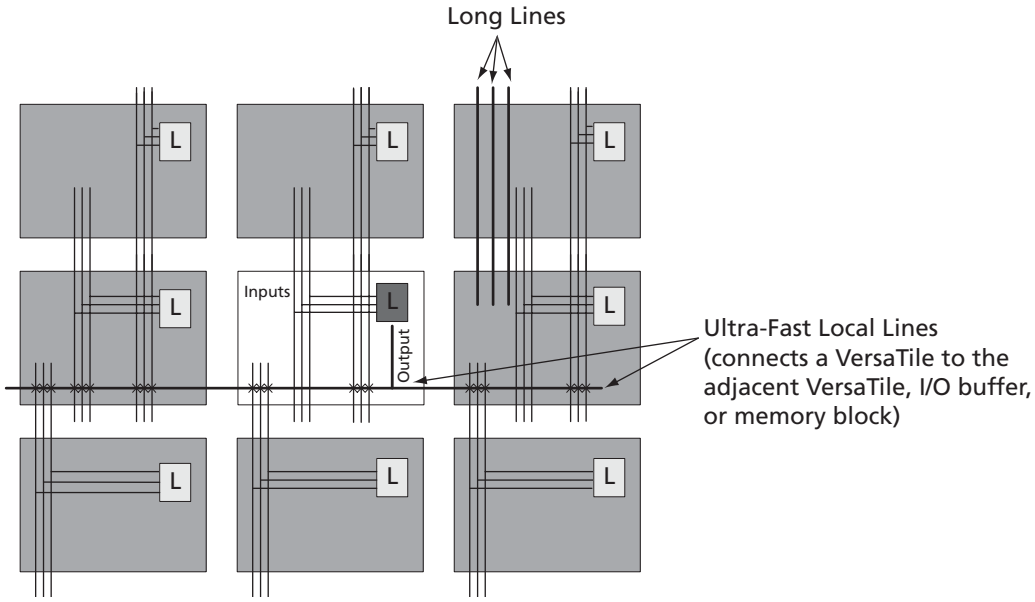
The routing structure of ProASIC3 devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources, efficient long-line resources, high-speed, very-long-line resources, and the high-performance VersaNet networks.

The ultra-fast local resources are dedicated lines that allow the output of each VersaTile to connect directly to every input of the eight surrounding VersaTiles (Figure 2-6). The exception to this is that the SET/CLR input of a VersaTile configured as a D-type flip-flop is driven only by the VersaTile global network.

The efficient, long-line resources provide routing for longer distances and higher fanout connections. These resources vary in length (spanning 1, 2, or 4 VersaTiles), run both vertically and horizontally, and cover the entire ProASIC3 device (Figure 2-7 on page 2-7). Each VersaTile can drive signals onto the efficient long-line resources, which can access every input of every VersaTile. Active buffers are inserted automatically by routing software to limit the loading effects.

The high-speed, very-long-line resources, which span the entire device with minimal delay, are used to route very long or high-fanout nets: length +/–12 VersaTiles in the vertical direction and length +/–16 in the horizontal direction from a given core VersaTile (Figure 2-8 on page 2-8). Very long lines in ProASIC3 devices have been enhanced over those in previous ProASIC families. This provides a significant performance boost for long-reach signals.

The high-performance VersaNet global networks are low-skew, high-fanout nets that are accessible from external pins or from internal logic (Figure 2-9 on page 2-9). These nets are typically used to distribute clocks, resets, and other high-fanout nets requiring minimum skew. The VersaNet networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically with signals accessing every input on all VersaTiles.



Note: *Input to the core cell for the D-flip-flop set and reset is only available via the VersaNet global network connection.*

Figure 2-6 • **Ultra-Fast Local Lines Connected to the Eight Nearest Neighbors**

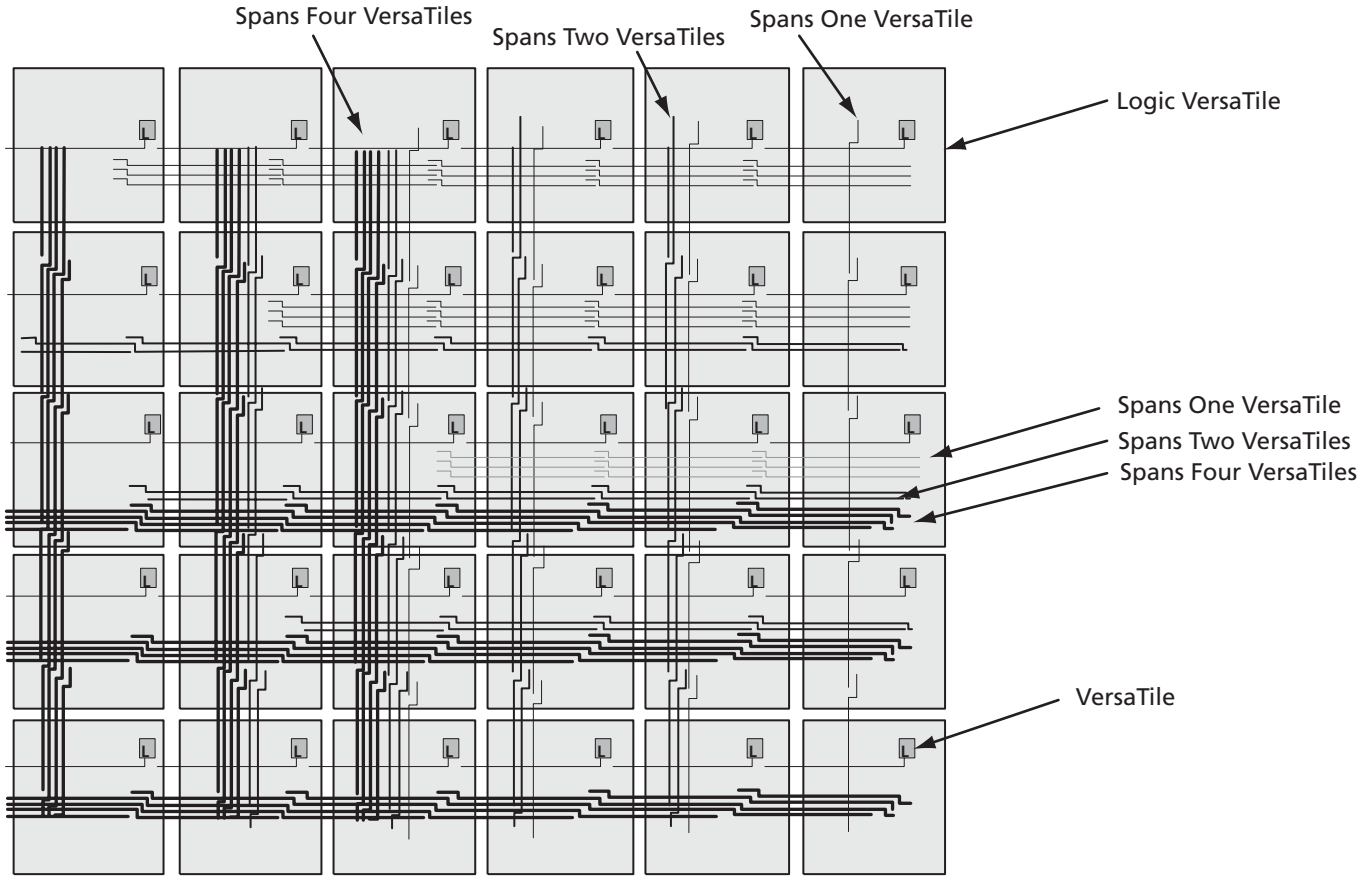


Figure 2-7 • **Efficient Long-Line Resources**

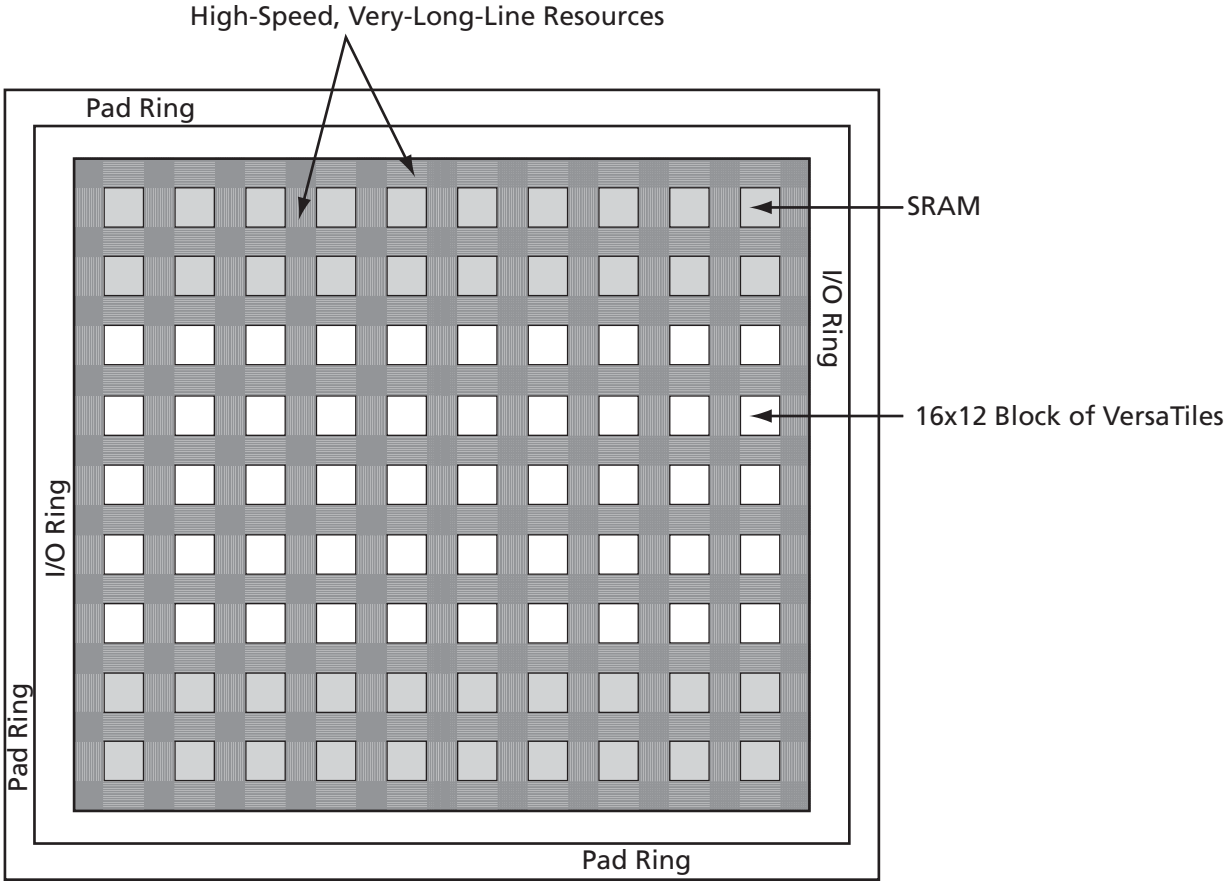


Figure 2-8 • **Very-Long-Line Resources**

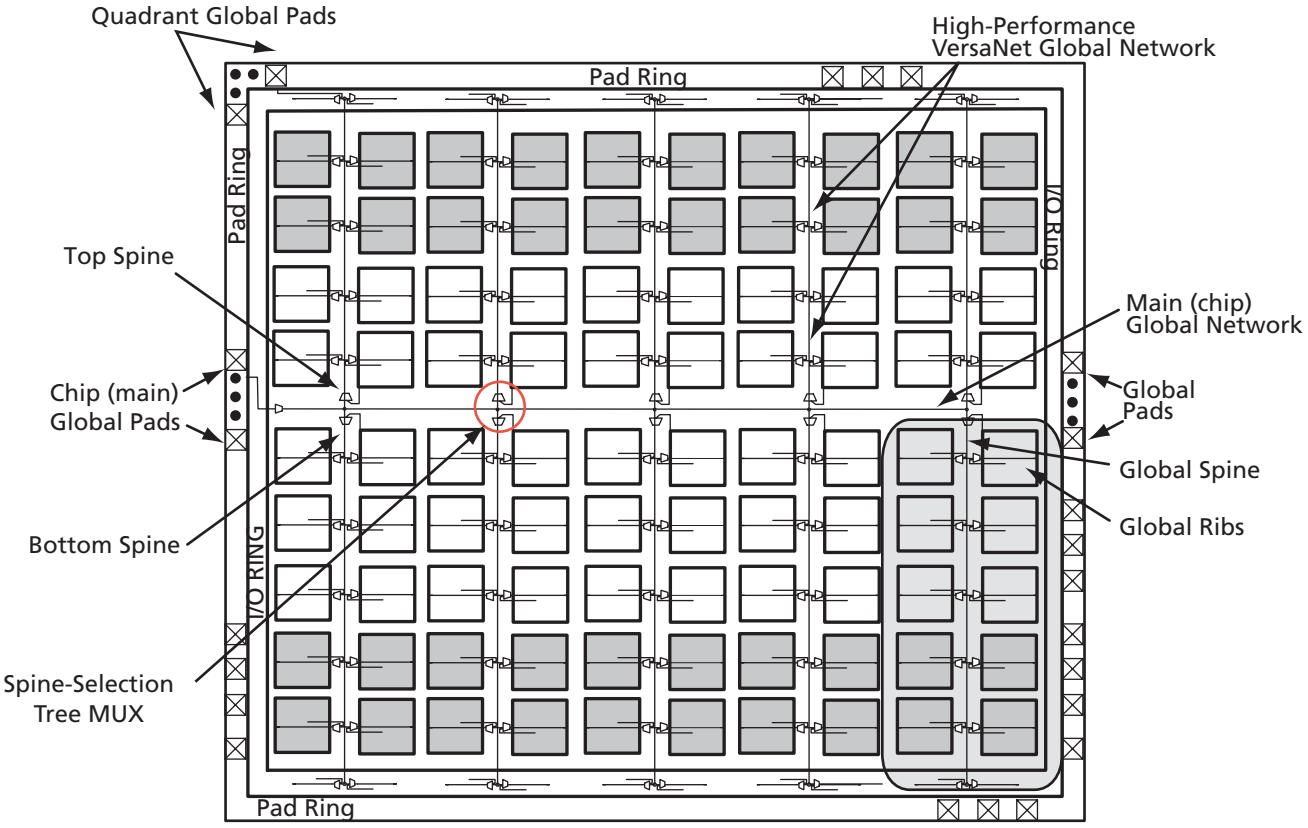
Clock Resources (VersaNets)

ProASIC3 devices offer powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has up to six CCCs. The west CCC also contains a phase-locked loop (PLL) core, delay lines, phase shifter (0°, 90°, 180°, 270°), and clock multiplier/dividers. Each CCC has all the circuitry needed for the selection and interconnection of inputs to the VersaNet global network. The east and west CCCs each have access to three VersaNet global lines on each side of the chip (six total lines).

Advantages of the VersaNet Approach

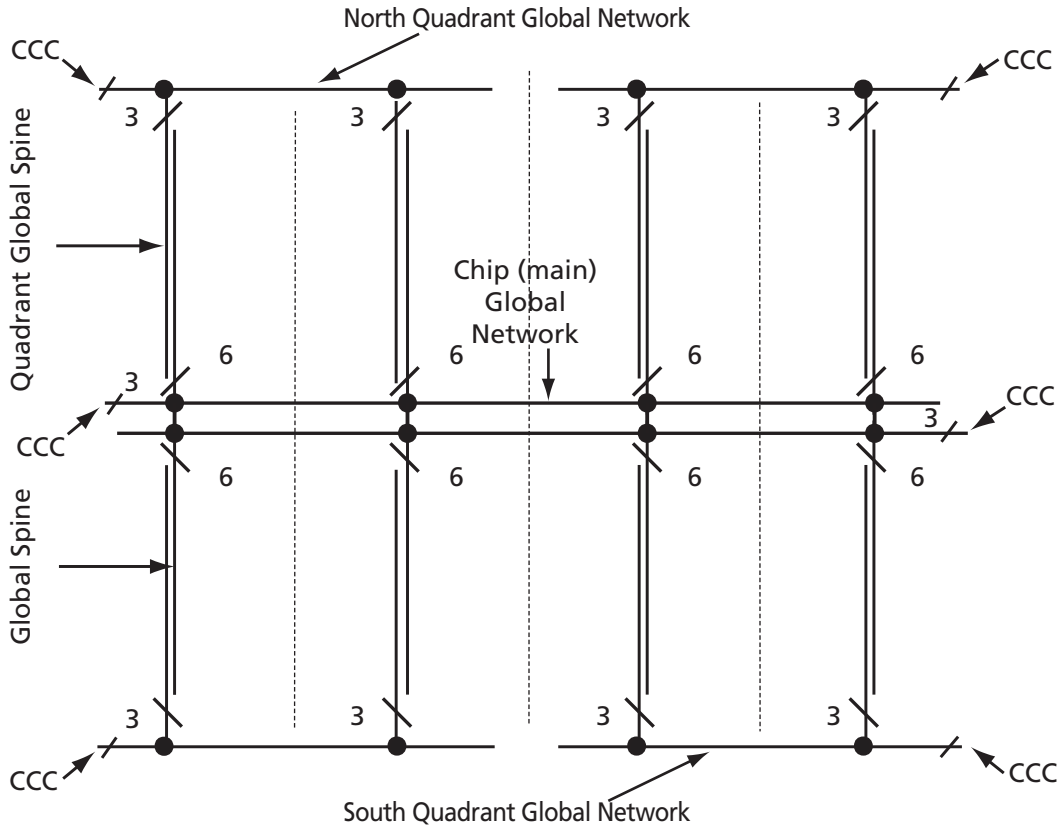
One of the architectural benefits of ProASIC3 is the set of powerful and low-delay VersaNet global networks. ProASIC3 offers six chip (main) global networks that are distributed from the center of the FPGA array (Figure 2-9). In addition, ProASIC3 devices have three regional globals in each of the four chip quadrants. Each core VersaTile has access to nine global network resources: three quadrant and six chip (main) global networks, and a total of 18 globals on the device. Each of these networks contain spines and rows that reach all the VersaTiles in the quadrants (Figure 2-10 on page 2-10). This flexible VersaNet global network architecture allows users to map up to 144 different internal/external clocks in a ProASIC3 device. Details on the VersaNet networks are given in Table 2-2 on page 2-10. The flexible use of the ProASIC3 VersaNet global network allows the designer to address several design requirements. User applications that are clock-resource-intensive can easily route external or gated internal clocks using VersaNet global routing networks. Designers can also drastically reduce delay penalties and minimize resource usage by mapping critical, high-fanout nets to the VersaNet global network.

In A3P030 devices, all six VersaNets come from the North edge of the FPGA fabric. The A3P030 does not support the VersaNet global network concept of top and bottom spines due to the limited gate density of this part.



Note: *Not applicable to the A3P030 device.*

Figure 2-9 • **Overview of ProASIC3 VersaNet Global Network**



Note: *This does not apply to the A3P030, since the VersaNet global network is sourced only for the north edge of the FPGA fabric.*

Figure 2-10 • **Global Network Architecture**

Table 2-2 • **ProASIC3 Globals/Spines/Rows by Device**

	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
Global VersaNets (Trees)*	6	9	9	9	9	9	9
VersaNet Spines/Tree	4	4	4	8	8	12	16
Total Spines	24	36	36	72	72	108	144
VersaTiles in Each Top or Bottom Spine	384	384	384	768	768	1,152	1,536
Total VersaTiles	768	1,536	3,072	6,144	9,216	13,824	24,576

Note: **There are six chip (main) globals and three globals per quadrant (except in the A3P030 device).*

VersaNet Global Networks and Spine Access

The ProASIC3 architecture contains nine segmented global networks that can access all the VersaTiles, SRAM memory, and I/O tiles on the ProASIC3 device. These VersaNet global networks offer fast, low-skew routing resources for high-fanout nets, including clock signals. In addition, these highly-segmented global networks offer users the flexibility to create low-skew local networks using spines for up to 144 internal/external clocks (in an A3P1000 device) or other high-fanout nets in ProASIC3 devices. Optimal usage of these low-skew networks can result in significant improvement in design performance on ProASIC3 devices.

The nine spines available in a vertical column reside in global networks with two separate regions of scope: the quadrant global network, which has three spines, and the chip (main) global network, which has six spines. There are four quadrant global network regions per device (Figure 2-10).

The spines are the vertical branches of the global network tree, shown in Figure 2-11 on page 2-11. Each spine in a vertical column of a chip (main) global network is further divided into two spine segments: one in the top and one in the bottom half of the die. Top and

bottom spine segments, radiating from the center of a device, are the same height.

Each spine covers a certain area of the ProASIC3 device (the "scope" of the spine). Each spine is accessed by the dedicated global network MUX tree architecture, which defines how a particular spine is driven—either by the signal on the global network from a CCC, for example, or another net defined by the user (Figure 2-12 on page 2-12). Quadrant spines can be driven from user I/Os on the north and south sides of the die. The ability to drive spines in the quadrant global networks can have a significant effect on system performance for high-fanout inputs to a design.

Details of the chip (main) global network spine-selection MUX are presented in Figure 2-12 on page 2-12. The spine drivers for each spine are located in the middle of the die.

Quadrant spines are driven from a north or south rib. Access to the top and bottom ribs is from the corner CCC or from the I/O on the north and south sides of the device.

For details on using spines in ProASIC3 devices, see the Actel application note *Optimal Usage of Global Network Spines in ProASIC^{PLUS} Devices*.

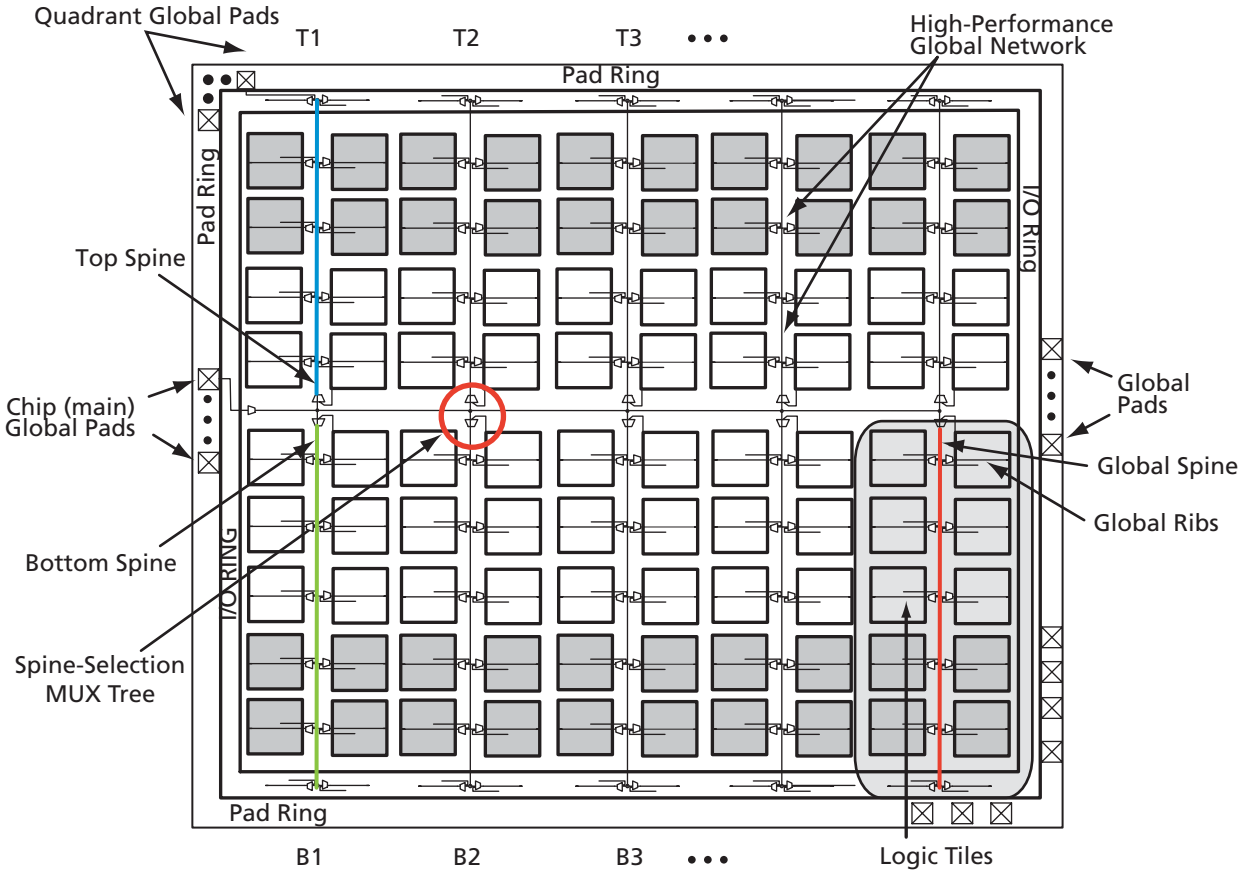


Figure 2-11 • **Spines in a Global Clock Tree Network**

Clock Aggregation

Clock aggregation allows for multi-spine clock domains. A MUX tree provides the necessary flexibility to allow long lines or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib, and also through local resources in the north and south ribs, allowing I/Os to directly feed into the clock system. As Figure 2-13 indicates, this access system is contiguous.

There is no break in the middle of the chip for the north and south I/O VersaNet access. This is different from the quadrant clocks, located in these ribs, which only reach the middle of the rib. Refer to the *Using Global Resources in Actel ProASIC3/E Devices* application note.

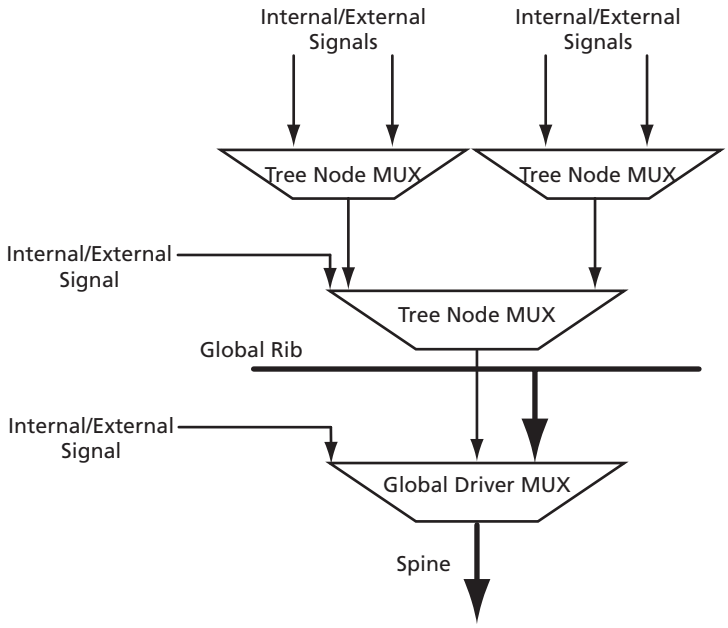


Figure 2-12 • **Spine Selection MUX of Global Tree**

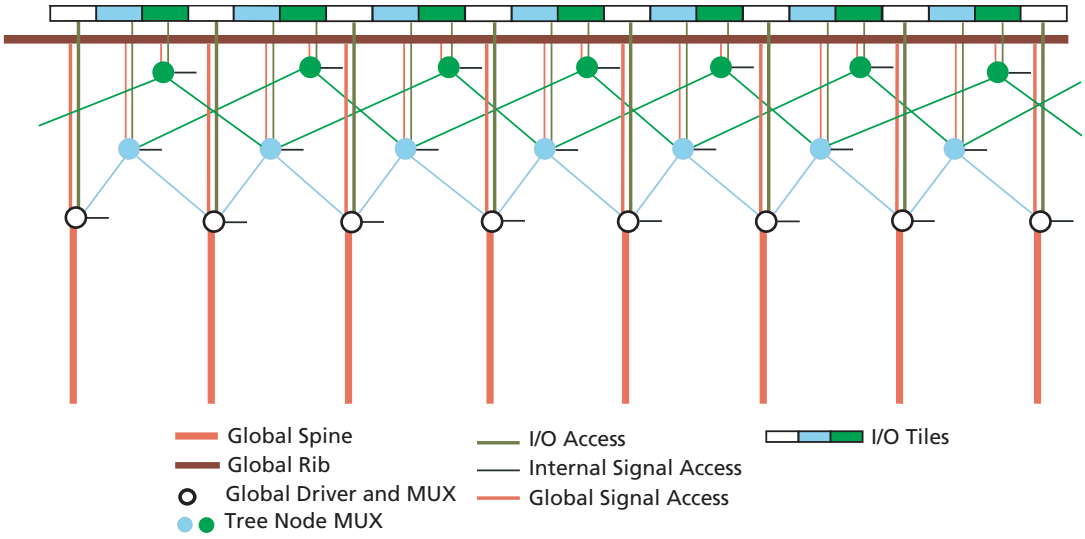


Figure 2-13 • **Clock Aggregation Tree Architecture**

Clock Conditioning Circuits

Overview of Clock Conditioning Circuitry

In ProASIC3 devices, the clock conditioning circuits (CCCs) are used to implement frequency division, frequency multiplication, phase shifting, and delay operations.

The CCCs are available in six chip locations – each of the four chip corners and in the middle of the east and west chip sides.

Each CCC can implement up to three independent global buffers (with or without programmable delay), or a PLL function (programmable frequency division/ multiplication, phase shift, and delays) with up to three global outputs. Unused global outputs of a PLL can be used to implement independent global buffers, up to a maximum of three global outputs for a given CCC.

A global buffer can be placed in any of the three global locations (CLKA-GLA, CLKB-GLB, and CLKC-GLC) of a given CCC.

A PLL macro uses the CLKA CCC input to drive its reference clock. It uses the GLA and optionally the GLB and GLC global outputs to drive the global networks. A PLL macro can also drive the YB and YC regular core outputs. The GLB (or GLC) global outputs cannot be reused if the YB (or YC) outputs are used (Figure 2-14 on page 2-14).

Each global buffer, as well as the PLL reference clock, can be driven from one of the following:

- Three dedicated single-ended I/Os using a hardwired connection
- Two dedicated differential I/Os using a hardwired connection
- The FPGA core

The CCC block is fully configurable, either via Flash configuration bits set in the programming bitstream or through an asynchronous interface. This asynchronous interface is dynamically accessible from inside the ProASIC3 device to permit parameter changes (such as divide ratios) during device operation. To increase the versatility and flexibility of the clock conditioning system, the CCC configuration is determined either by the user during the design process, with configuration data being stored in Flash memory as part of the device programming procedure, or by writing data into a dedicated shift register during normal device operation. This latter mode allows the user to dynamically reconfigure the CCC without the need for core programming. The shift register is accessed through a simple serial interface. Refer to the *UJTAG Applications in ProASIC3/E Devices* application note and the "CCC Electrical Specifications" section on page 2-18 for more information.

Global Buffers with No Programmable Delays

The CLKBUF and CLKBUF_LVPECL/LVDS macros are composite macros that include an I/O macro driving a global buffer, which uses a hardwired connection.

The CLKBUF, CLKBUF_LVPECL/LVDS, and CLKINT macros are pass-through clock sources and do not use the PLL or provide any programmable delay functionality.

The CLKINT macro provides a global buffer function driven by the FPGA core.

Many specific CLKBUF macros support the wide variety of single-ended and differential I/O standards supported by ProASIC3 devices. The available CLKBUF macros are described in the *ProASIC3/E Macro Library Guide*.

Global Buffer with Programmable Delay

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay. The CLKDLY macro takes the selected clock input and adds a user-defined delay element. This has the effect of a frequency-dependent output clock phase shift from the input clock.

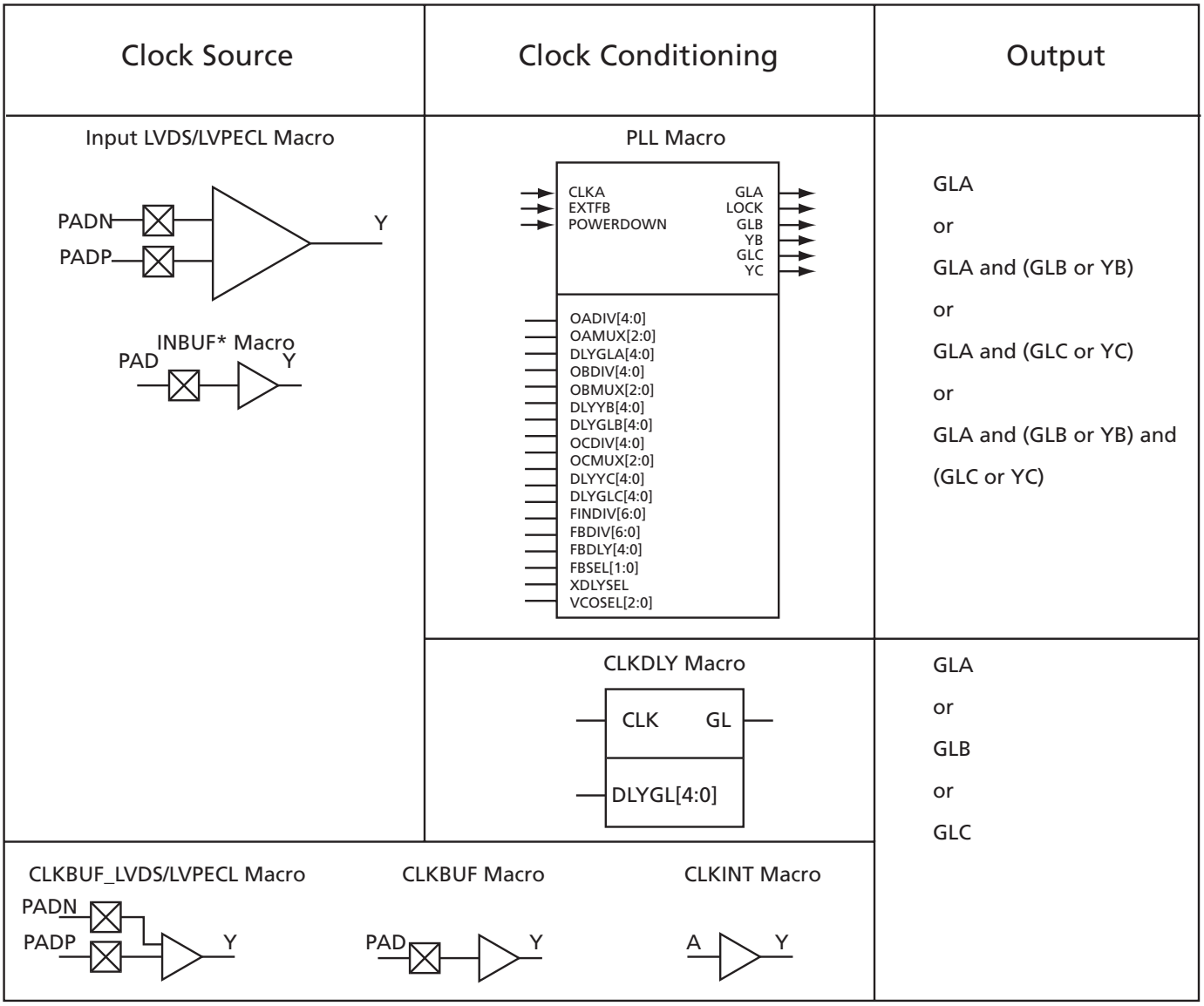
The CLKDLY macro can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

The CLKDLY macro can be driven directly from the FPGA core.

The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual CLKDLY configuration in the ACTgen part of the Libero IDE and Designer tools allows the user to select the desired amount of delay, and configures the delay elements appropriately. ACTgen also allows the user to select where the input clock is coming from. ACTgen will automatically instantiate the special macro, PLLINT, when needed.

Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the ProASIC3 family. The available INBUF macros are described in the *ProASIC3/E Macro Library Guide*.



Notes:

1. *See the Actel website for future application notes concerning the dynamic PLL.The PLL is only supported on the west center CCC. The A3P030 has no PLL support. Refer to "PLL Function" section on page 2-15 for signal descriptions.*
2. *Refer to the ProASIC3/E Macro Library Guide for more information.*

Figure 2-14 • **ProASIC3 CCC Options**

PLL Function[1]

The PLL functionality of the clock conditioning block is supported by the PLL macro. Note that the PLL macro reference clock uses the CLKA input of the CCC block, which is only accessible from the global A[0:2] package pins. Refer to Figure 2-15 on page 2-16 for more information.

The PLL macro supports three inputs and up to six outputs (Figure 2-17 on page 2-17).

Inputs:

- CLKA: selected clock input
- EXTFB: allows an external signal to be compared to a reference clock in the PLL core's phase detector
- Powerdown (active Low): disables PLLs. The default state is Powerdown On (active Low).

Outputs:

- Lock: indicates that PLL output has locked on the input reference signal
- GLA, GLB, GLC: outputs to respective global networks
- YB, YC: allows output from the CCC to be routed back to the FPGA core

As previously described, the PLL allows up to five flexible and independently configurable clock outputs. Figure 2-14 on page 2-14 illustrates the various clock output options and delay elements.

As illustrated, the PLL will support three distinct output frequencies from a given input clock. Two of these (GLB and GLC) can be routed to the B and C global network access, respectively, and/or routed to the device core (YB and YC).

Also in the feedback loop, there is a delay element that can be used to advance the clock relative to the reference clock.

There are five delay elements to support phase control on all five outputs (GLA, GLB, GLC, YB, and YC).

Note: Care must be taken if the output delay element is used in conjunction with an output divide. As there are a finite number of dividers and delay elements, exact output frequency and output phase may not always be derived from the input clock frequency.

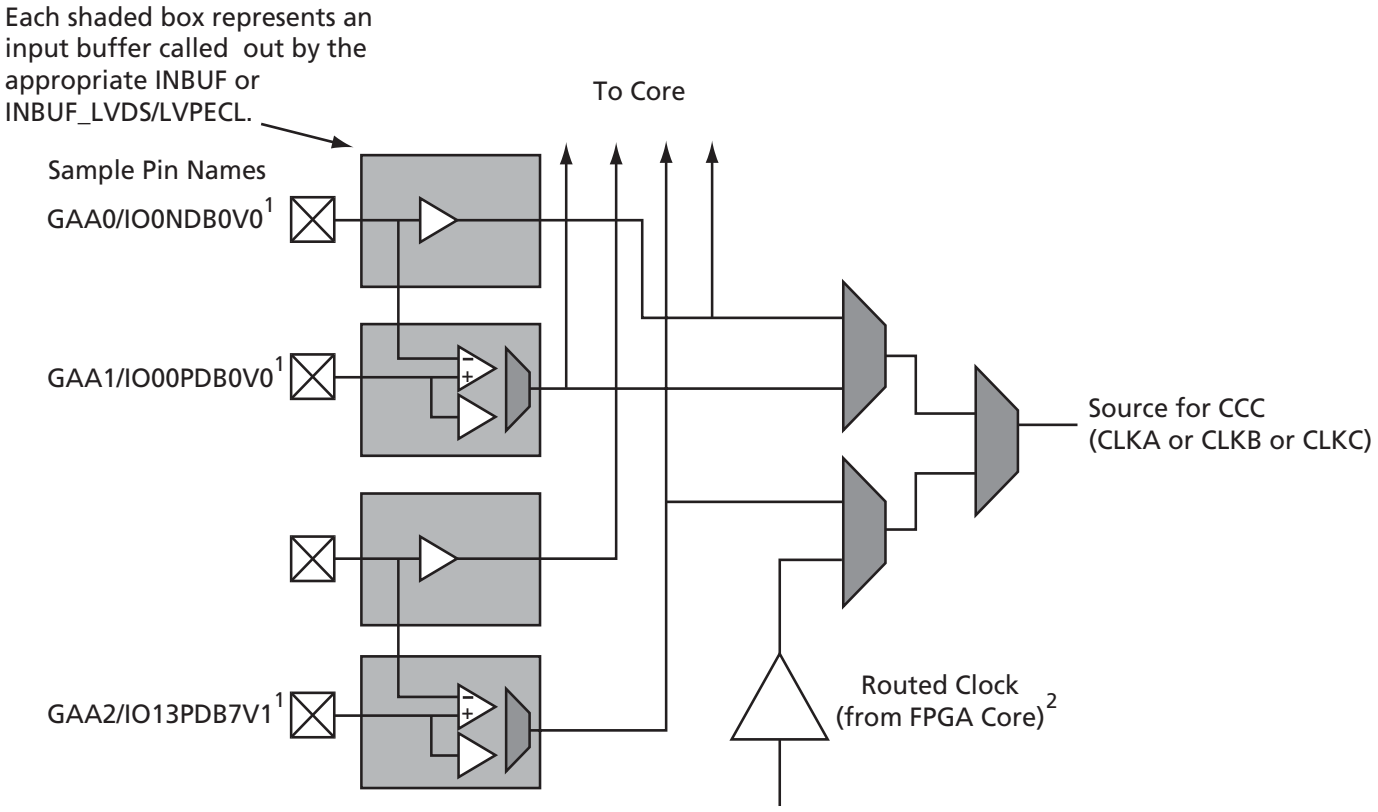
The PLL macro reference clock can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

The PLL macro reference clock can be driven directly from the FPGA core.

The PLL macro reference clock can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual PLL configuration in ACTgen, associated with the Libero IDE and Designer tools, will derive the necessary internal divider ratios based on the input frequency and desired output frequencies selected by the user. ACTgen also allows the user to select the various delays and phase shift values necessary to adjust the phases between the reference clock (CLKA) and the derived clocks (GLA, GLB, GLC, YB and YC). ACTgen also allows the user to select where the input clock is coming from. ACTgen automatically instantiates the special macro, PLLINT, when needed.

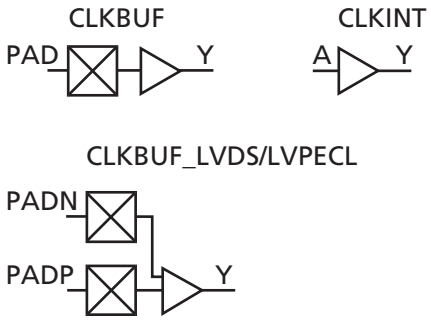
1. *The A3P030 device does not support PLL.*



Notes:

1. *Represents the global input pins. Globals have direct access to the clock conditioning block and are not routed via the FPGA fabric. Refer to the "User I/O Naming Convention" on page 2-44 for more information.*
2. *Instantiate the routed clock source input as follows:*
   a) Connect the output of a logic element to the clock input of PLL, CLKDLY, or CLKINT macro.
   b) Do not place a clock source I/O (INBUF or INBUF_LVPECL/LVDS) in a relevant global pin location.
3. *LVDS-based clock sources are only available on A3P250 through A3P1000 family members. A3P060 and A3P125 support single-ended clock sources only. The A3P030 device does not support this feature.*

Figure 2-15 • **Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT**



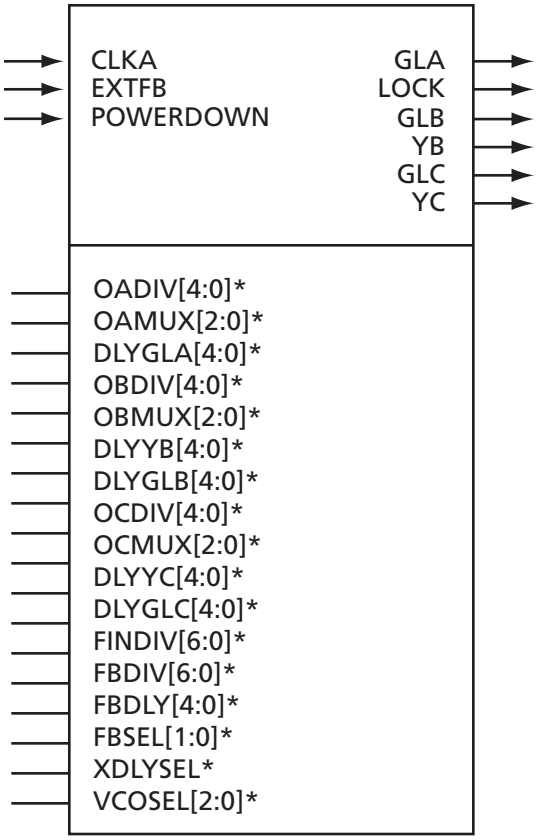
Note: *The A3P030 device does not support this feature.*

Figure 2-16 • **CLKBUF and CLKINT**

Table 2-3 • **Available Selections of I/O Standards within CLKBUF and CLKBUF_LVDS/LVPECL Macros**

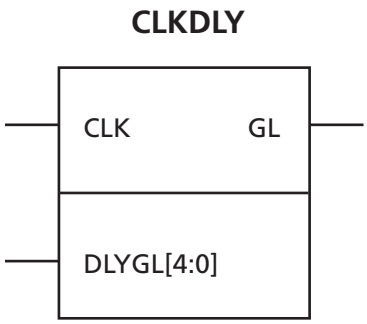
CLKBUF Macros
CLKBUF_LVCMOS5
CLKBUF_LVCMOS33*
CLKBUF_LVCMOS18
CLKBUF_LVCMOS15
CLKBUF_PCI
CLKBUF_LVDS
CLKBUF_LVPECL

Note: **By default, the CLKBUF macro uses the 3.3 V LVTTL I/O technology. For more details refer to the ProASIC3/E Macro Library Guide.*



Note: **See the Actel website for future application notes concerning the dynamic PLL.*
The A3P030 device does not support PLL.

Figure 2-17 • **CCC/PLL Macro**



Note: *The CLKDLY macro uses programmable delay element type 2.*

Figure 2-18 • **CLKDLY**

CCC Electrical Specifications

Timing Characteristics

Table 2-4 • **ProASIC3 CCC/PLL Specification**

Parameter	Min.	Typ.	Max.	Unit
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350	MHz
Delay Increments in Programmable Delay Blocks[1, 2]		160		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
Long Term Output Pk-Pk Period Jitter				
at f_{PLL_OUT} = 24 MHz	–		180	ps
at f_{PLL_OUT} = 100 MHz	–		90	ps
at f_{PLL_OUT} = 350 MHz	–		70	ps
Acquisition Time			150	µs
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.025		5.56	ns
Delay Range in Block: Fixed Delay [1, 2]		2.2		ns

Notes:

1. *This delay is a function of voltage and temperature. See Table 3-6 on page 3-4 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.5 V*
3. *The A3P030 device does not support PLL.*

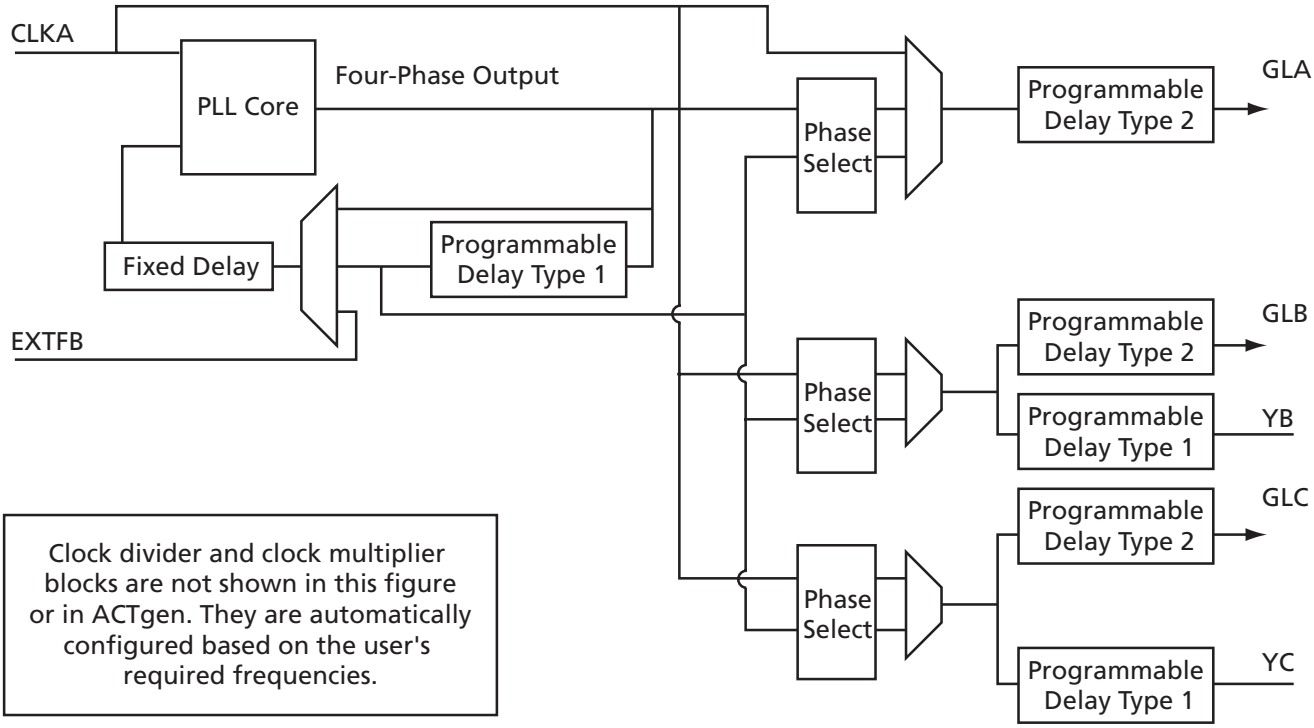
Physical Implementation of CCC[2]

The CCC circuit is composed of the following (Figure 2-19):

- PLL core
- Three phase selectors
- Six programmable delays and one fixed delay that advance/delay phase
- Five programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-19, because they are automatically configured based on the user's required frequencies)
- One dynamic shift register that provides CCC dynamic reconfiguration capability

CCC Programming

The clock conditioning circuit block is fully configurable, either via static Flash configuration bits in the array, set by the user in the programming bitstream, or through an asynchronous dedicated shift register dynamically accessible from inside the ProASIC3 device. The dedicated shift register permits parameter changes such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface. Refer to the *UJTAG Applications in ProASIC3/E Devices* application note for more information.



Note: *Refer to the "Clock Conditioning Circuits" section on page 2-13 and Table 2-4 on page 2-18 for signal descriptions.*

Figure 2-19 • **PLL Block**

2. *The A3P030 device does not support PLL.*

Nonvolatile Memory (NVM)

Overview of User Nonvolatile FlashROM (FROM)

ProASIC3 devices have 1 kbit of on-chip nonvolatile Flash memory that can be read from the FPGA core fabric. The FROM is arranged in 8 banks of 128 bits during programming. The 128 bits in each bank are addressable as 16 bytes during the read back of the FROM from the FPGA core (Figure 2-20).

The FROM can only be programmed via the IEEE1532 JTAG port. It cannot be programmed directly from the FPGA core. When programming, each of the 8 128-bit banks can be selectively reprogrammed. The FROM can only be reprogrammed on a bank boundary. Programming involves an automatic, on-chip bank erase prior to reprogramming the bank. The FROM supports asynchronous read with a nominal 10 ns access time. The FROM can be read on byte boundaries. The top 3 bits of the FROM address from the FPGA core define the bank that is being accessed. The bottom 4 bits of the FROM address from the FPGA core define which of the 16 bytes in the bank is being accessed.

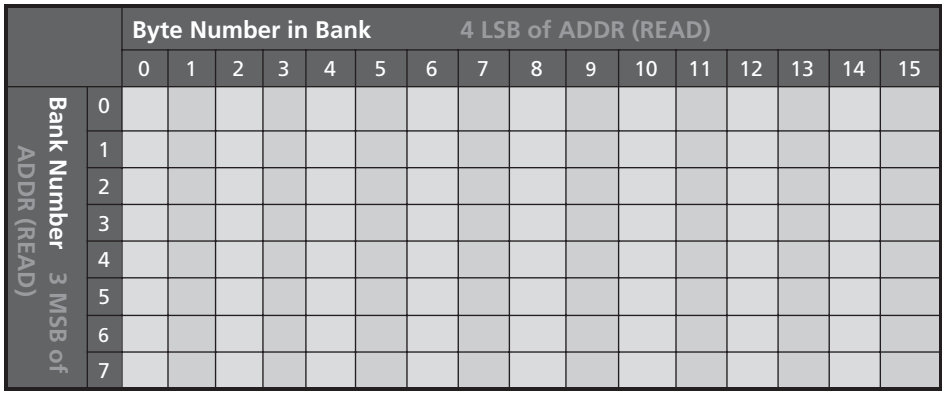


Figure 2-20 • **FROM Architecture**

SRAM and FIFO[3]

ProASIC3 devices have embedded SRAM blocks along the north side of the device. In addition, A3P600 and A3P100 have an embedded SRAM block on the south side of the device. To meet the needs of high performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 350 MHz.

- 4kx1, 2kx2, 1kx4, 512x9 (dual-port RAM – two read, two write or one read, one write)
- 512x9, 256x18 (two-port RAM – one read and one write)
- Sync write, sync pipelined, and nonpipelined read

The ProASIC3 memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (Full, Empty, AFULL, AEMPTY). Block diagrams of the memory modules are illustrated in Figure 2-21 on page 2-22.

During RAM operation, addresses are sourced by the user logic and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to Figure 2-22 on page 2-23 for more information about the implementation of the embedded FIFO controller.

The ProASIC3 architecture enables the read side and write side of RAMs to be organized independently, allowing for bus conversion. For example, the write side can be set to 256x18 and the read side to 512x9.

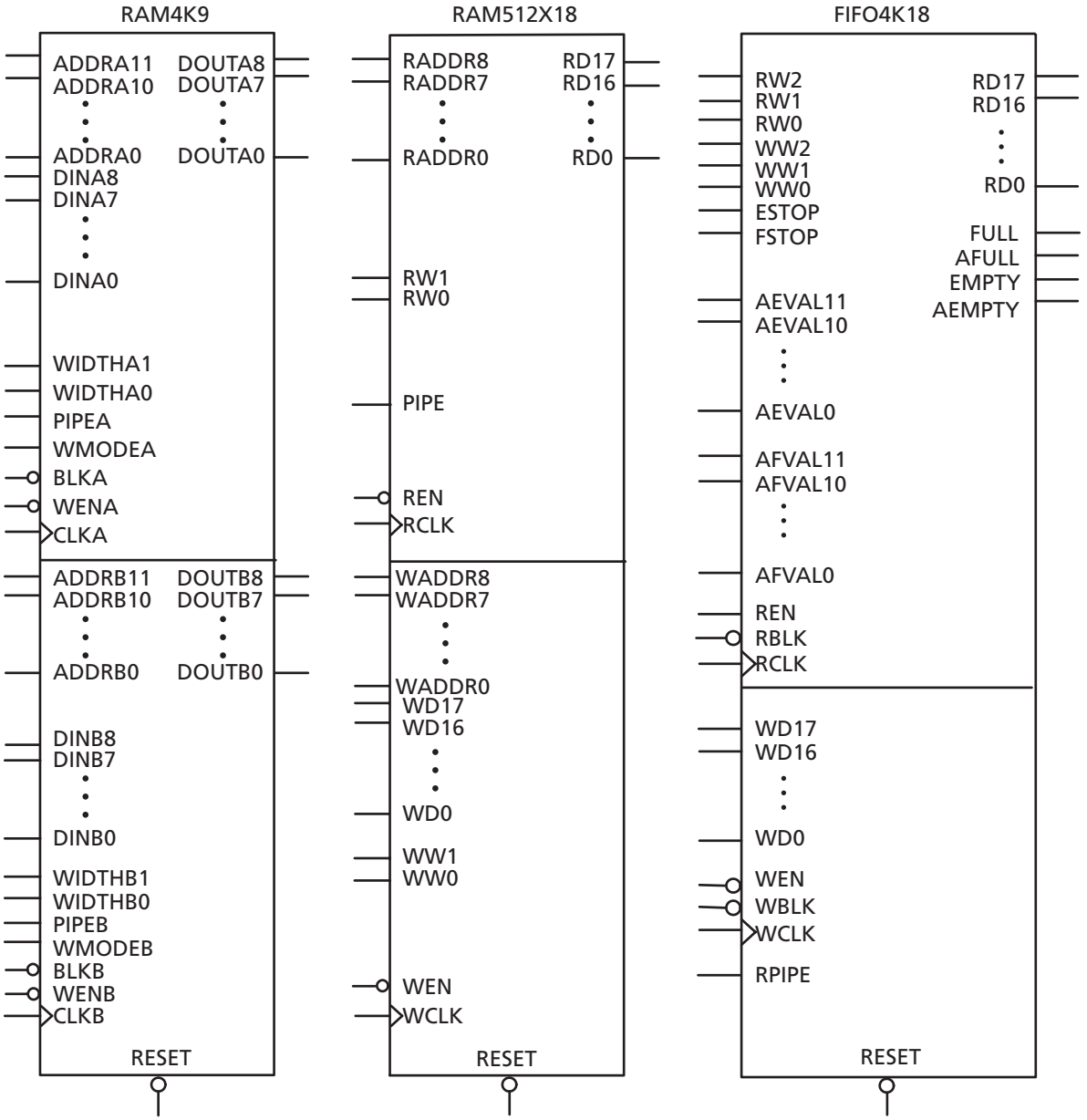
Both the write width and read width for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different DxW configurations are: 256x18, 512x9, 1kx4, 2kx2, and 4kx1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in Table 2-5 on page 2-24.

When widths of one, two, and four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible.

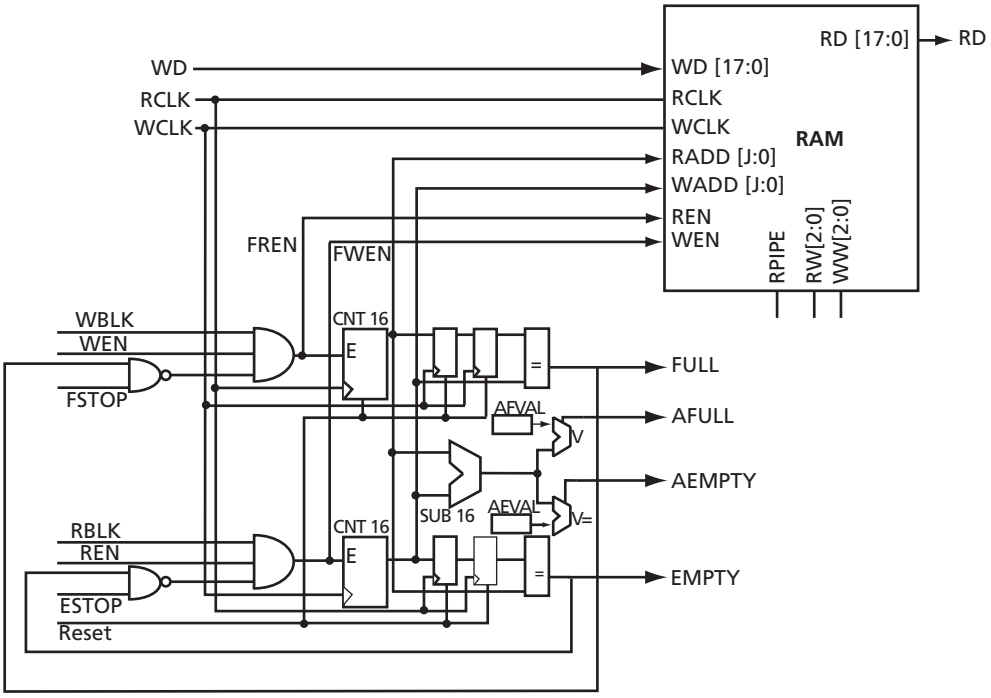
Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.

3. *The A3P030 device does not support SRAM and FIFO.*



Note: *The A3P030 device does not support SRAM and FIFO.*

Figure 2-21 • **Supported Basic RAM Macros**



Note: *The A3P030 device does not support SRAM and FIFO.*

Figure 2-22 • **ProASIC3 RAM Block with Embedded FIFO Controller**

Signal Descriptions for RAM4K9[4]

The following signals are used to configure the RAM4K9 memory element:

WIDTHA and WIDTHB

These signals enable the RAM to be configured in one of four allowable aspect ratios (Table 2-5).

Table 2-5 • **Allowable Aspect Ratio Settings for WIDTHA[1:0]**

WIDTHA1, WIDTHA0	WIDTHB1, WIDTHB0	DxW
00	00	4kx1
01	01	2kx2
10	10	1kx4
11	11	512x9

BLKA and BLKB

These signals are active low and will enable the respective ports when asserted. When a BLKx signal is deasserted, that port's outputs hold the previous value.

WENA and WENB

These signals switch the RAM between read and write modes for the respective ports. A Low on these signals indicates a write operation, and a High indicates a read.

CLKA and CLKB

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

PIPEA and PIPEB

These signals are used to specify pipelined read on the output. A Low on PIPEA and/or PIPEB indicates a nonpipelined read and the data appears on the corresponding output in the same clock cycle. A High indicates a pipelined read and data appears on the corresponding output in the next clock cycle.

WMODEA and WMODEB

These signals are used to configure the behavior of the output when RAM is in the write mode. A Low on these signals makes the output retain data from the previous read. A High indicates pass-through behavior where the data being written will appear immediately on the output. This signal gets overridden when RAM is being read.

RESET

This active low signal resets the output to zero when asserted. It does not reset the content of the memory.

ADDRA and ADDRB

These are used as read or write addresses and are 12 bits wide. When a depth of less than 4 k is specified, the unused high-order bits must be grounded (Table 2-6).

Table 2-6 • **Address Pins Used for Various Supported Bus Widths**

DxW	ADDRA/ADDRB UNUSED
4kx1	–
2kx2	ADDRA[11], ADDRB[11]
1kx4	ADDRA[11:10], ADDRB[11:10]
512x9	ADDRA[11:9], ADDRB[11:9]

DINA and DINB

These are the input data signals, and these are nine bits wide. Not all nine bits are valid in all configurations. When a data width less than nine is specified, unused high-order signals must be grounded (Table 2-7).

Table 2-7 • **Data Pins Used for Various Supported Bus Widths**

DxW	DINA/DINB UNUSED
4kx1	DINA[8:1], DINB[8:1]
2kx2	DINA[8:2], DINB[8:2]
1kx4	DINA[8:4], DINB[8:4]
512x9	–

DOUTA and DOUTB

These are the output data signals, and these are nine bits wide. Not all nine bits are valid in all configurations. As with DINA and DINB, high-order bits become unusable. The output data on unused pins is undefined.

Signal Descriptions for RAM512X18[4]

RAM512X18 has slightly different behavior than the RAM4K9, as it has dedicated read and write ports.

WW and RW

These signals enable the RAM to be configured in one of the two allowable aspect ratios (Table 2-8).

Table 2-8 • **Aspect Ratio Settings for WW[1:0]**

WW1, WW0	RW1, RW0	DxW
01	01	512x9
10	10	256x18
00, 11	00, 11	Reserved

4. The A3P030 device does not support SRAM and FIFO.

WD and RD

These are the input data and output signals, and they are 18 bits wide. When a 512x9 aspect ratio is used for write, WD[17:9] are unused and must be grounded. If this aspect ratio is used for read, then RD[17:9] are undefined.

WADDR and RADDR

These are read and write addresses, and they are nine bits wide. When the 256x18 aspect ratio is used for write or read, WADDR[8] or RADDR[8] is unused and must be grounded.

WCLK and RCLK

These signals are the write and read clocks, respectively. They are both active high.

WEN and REN

These signals are the write and read enables, respectively. They are both active low by default. These signals can be configured as active high.

RESET

This active low signal resets the output to zero when asserted. It does not reset the contents of the memory.

PIPE

This signal is used to specify pipelined read on the output. A Low on PIPE indicates a nonpipelined read and the data appears on the output in the same clock cycle. A High indicates a pipelined read and data appears on the output in the next clock cycle.

Clocking

The dual-port SRAM blocks are only clocked on the rising edge. ACTgen allows falling-edge triggered clocks by adding inverters to the netlist, hence achieving dual-port SRAM blocks that are clocked on either edge (rising or falling). For dual-port SRAM, each port can be clocked on either edge and/or by separate clocks by port.

ProASIC3 devices support inversion (bubble pushing) throughout the FPGA architecture, including the clock input to the SRAM modules. Inversions added to the SRAM clock pin on the design schematic or in the HDL code will be automatically accounted for during design compile without incurring additional delay in the clock path.

The two-port SRAM can be clocked on the rising edge or falling edge of the WCLK and RCLK.

If negative-edge RAM and FIFO clocking is selected for memory macros, clock edge inversion management (bubble pushing) is automatically used within the ProASIC3 development tools, without performance penalty.

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous – one clock edge): In the standard read mode, new data is driven onto the RD bus in the clock cycle immediately following RA and REN valid. The read address is registered on the read port clock active edge and data appears at RD after the RAM access time. Setting PIPE to Off enables this mode.
- Read Pipelined (synchronous – two clock edges): The pipelined mode incurs an additional clock delay from the address to the data but enables operation at a much higher frequency. The read address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting the PIPE to ON enables this mode.
- Write (synchronous – one clock edge): On the write clock active edge, the write data is written into the SRAM at the write address when WEN is high. The setup times of the write address, write enables, and write data are minimal with respect to the write clock. Write and read transfers are described with timing requirements in the "DDR Module Specifications" section on page 3-37.

RAM Initialization

Each SRAM block can be individually initialized on power-up by means of the JTAG port using the UJTAG mechanism (refer to the "JTAG 1532" section on page 2-48 and the *ProASIC3/E SRAM/FIFO Blocks* application note). The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation.

Signal Descriptions for FIFO4K18[5]

The following signals are used to configure the FIFO4K18 memory element:

WW and RW

These signals enable the FIFO to be configured in one of the five allowable aspect ratios (Table 2-9).

Table 2-9 • **Aspect Ratio Settings for WW[2:0]**

WW2, WW1, WW0	RW2, RW1, RW0	DxW
000	000	4kx1
001	001	2kx2
010	010	1kx4
011	011	512x9
100	100	256x18
101, 110, 111	101, 110, 111	Reserved

5. *The A3P030 device does not support SRAM and FIFO.*

WBLK and RBLK

These signals are active low and will enable the respective ports when low. When the RBLK signal is high, that port's outputs hold the previous value.

WEN and REN

Read and write enables. WEN is active low and REN is active high by default. These signals can be configured as active high or low.

WCLK and RCLK

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

RPIPE

This signal is used to specify pipelined read on the output. A Low on RPIPE indicates a nonpipelined read and the data appears on the output in the same clock cycle. A High indicates a pipelined read and data appears on the output in the next clock cycle.

RESET

This active low signal resets the output to zero when asserted. It resets the FIFO counters. It also sets all the RD pins low, the Full and AFULL pins low, and the Empty and AEMPTY pins high (Table 2-10).

WD

This is the input data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. When a data width less than 18 is specified, unused higher-order signals must be grounded (Table 2-10).

RD

This is the output data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. Like the WD bus, high-order bits become unusable if the data width is less than 18. The output data on unused pins is undefined (Table 2-10).

Table 2-10 • **Input Data Signal Usage for Different Aspect Ratios**

DxW	WD/RD Unused
4kx1	WD[17:1], RD[17:1]
2kx2	WD[17:2], RD[17:2]
1kx4	WD[17:4], RD[17:4]
512x9	WD[17:9], RD[17:9]
256x18	–

ESTOP, FSTOP

ESTOP is used to stop the FIFO read counter from further counting once the FIFO is empty (i.e., the Empty flag goes high). A High on this signal inhibits the counting.

FSTOP is used to stop the FIFO write counter from further counting once the FIFO is full (i.e., the Full flag goes high). A High on this signal inhibits the counting.

For more information on these signals, refer to the "ESTOP and FSTOP Usage" section.

FULL, EMPTY

When the FIFO is full and no more data can be written, the Full flag asserts high. The Full flag is synchronous to WCLK to inhibit writing immediately upon detection of a full condition and to prevent overflows. Since the write address is compared to a resynchronized (and thus time-delayed) version of the read address, the Full flag will remain asserted until two WCLK active edges after a read operation eliminates the full condition.

When the FIFO is empty and no more data can be read, the Empty flag asserts high. The Empty flag is synchronous to RCLK to inhibit reading immediately upon detection of an empty condition and to prevent underflows. Since the read address is compared to a resynchronized (and thus time delayed) version of the write address, the Empty flag will remain asserted until two RCLK active edges, after a write operation, removes the empty condition.

For more information on these signals, refer to the "FIFO Flags Usage Considerations" section on page 2-27.

AFULL, AEMPTY

These are programmable flags and will be asserted on the threshold specified by AFVAL and AEVAL, respectively.

When the number of words stored in the FIFO reaches the amount specified by AEVAL while reading, the AEMPTY output will go high. Likewise, when the number of words stored in the FIFO reaches the amount specified by AFVAL while writing, the AFULL output will go high.

AFVAL, AEVAL

The AEVAL and AFVAL pins are used to specify the almost-empty and almost-full threshold values, respectively. They are 12-bit signals. For more information on these signals, refer to the "FIFO Flags Usage Considerations" section on page 2-27.

ESTOP and FSTOP Usage

The ESTOP pin is used to stop the read counter from counting any further once the FIFO is empty (i.e., the EMPTY flag goes high). Likewise, the FSTOP pin is used to stop the write counter from counting any further once the FIFO is full (i.e., the Full flag goes high).

The FIFO counters in the ProASIC3 device start the count from 0, reach the maximum depth for the configuration (e.g., 511 for a 512x9 configuration), and then restart from 0. An example application for the ESTOP, where the read counter keeps counting, would be writing to the FIFO once and reading the same content over and over, without doing a write again.

FIFO Flags Usage Considerations

The AEVAL and AFVAL pins are used to specify the almost-empty and almost-full threshold values, respectively. They are 12-bit signals. In order to handle different read and write aspect ratios, the values specified by the AEVAL and AFVAL pins are to be interpreted as the address of the last word stored in the FIFO. The FIFO actually contains separate write address (WADDR) and read address (RADDR) counters. These counters calculate the 12-bit memory address that is a function of WW and RW, respectively. WADDR is incremented every time a write operation is performed, and RADDR is incremented every time a read operation is performed. Whenever the difference between WADDR and RADDR is greater than or equal to AFVAL, the AFULL output is asserted. Likewise, whenever the difference between WADDR and RADDR is less than or equal to AEVAL, the AEMPTY output is asserted.

To handle different read and write aspect ratios, the AFVAL and AEVAL are expressed in terms of total data bits instead of total data words. When users specify the AFVAL and AEVAL in terms of read or write words, the ACTgen tool translates them into bit addresses and configures these signals.

ACTgen configures the Almost-Full flag, AFULL, to assert when the write address exceeds the read address by a predefined value. Assume the user has a 2kx8 FIFO, a value of 1,500 for AFVAL means that the AFULL flag will be asserted when a write causes the difference between the write address and the read address to be 1,500. The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. Note that the FIFO can be configured with different read and write widths; in this case the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of read data entries.

In the case of 512x9 and 256x18 aspect ratios, since only 4,096 bits can be addressed by 12 bits of the AFVAL/AEVAL, the number of words must be multiplied by 8 and 16, instead of 9 and 18. The ACTgen tool automatically uses the proper values.

To avoid half words being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert Full or Empty as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because at this time a single word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

Refer to the *ProASIC3/E SRAM/FIFO Blocks* application note for more information.

Advanced I/Os

Introduction

ProASIC3 devices feature a flexible I/O structure, supporting a range of mixed-voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) through a bank-selectable voltage. Table 2-11, Table 2-12, and Table 2-18 on page 2-42 show the voltages and the compatible I/O standards. I/Os provide programmable slew rates, drive strengths, weak pull-up, and weak pull-down circuits. 3.3 V PCI and 3.3 V PCI-X are 5 V tolerant. See the "5 V Input Tolerance" section on page 2-35 for possible implementations of 5 V tolerance.

All I/Os are in a known state during power-up, and any power-up sequence is allowed without current impact. Refer to the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section on page 3-3 for more information.

I/O Tile

The ProASIC3 I/O tile provides a flexible, programmable structure for implementing a large number of I/O standards. In addition, the registers available in selected I/O banks can be used to support high-performance register inputs and outputs, with register enable if desired (Figure 2-23 on page 2-30). The registers can also be used to support the JESD-79C Double Data Rate (DDR) standard within the I/O structure (see the "Double Data Rate (DDR) Support" section on page 2-31 for more information).

As depicted from Figure 2-23 on page 2-30, all I/O registers share one CLR port. The output register and output enable register share one CLK port. Refer to the "I/O Registers" section on page 2-30 for more information.

I/O Banks and I/O Standards Compatibility

I/Os are grouped into I/O voltage banks. There are four I/O banks on the A3P250 through A3P1000. The A3P030, A3P060, and A3P125 have two I/O banks. Each I/O voltage bank has dedicated input/output supply and ground voltages (VMV/GNDQ for input buffers and V_{CCI}/GND for output buffers). Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank. Table 2-12 shows the required voltage compatibility values for each of these voltages.

For more information about I/O and global assignments to I/O banks, refer to the specific pin table of the device in the "Package Pin Assignments" section on page 4-1 and the "User I/O Naming Convention" section on page 2-44.

I/O standards are compatible if their V_{CCI} and VMV values are identical. VMV and GNDQ are "quiet" input power supply pins and are not used on A3P030.

Table 2-11 • **ProASIC3 Supported I/O Standards**

	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
Single-Ended							
LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5V, LVCMOS 2.5 /5.0 V	✓	✓	✓	✓	✓	✓	✓
3.3 V PCI / 3.3 V PCI-X	–	✓	✓	✓	✓	✓	✓
Differential							
LVPECL and LVDS	–	–	–	✓	✓	✓	✓

Table 2-12 • **V_{CCI} Voltages and Compatible Standards**

V_{CCI} and VMV (typ.)	Compatible Standards
3.3 V	LVTTL/LVCMOS 3.3, PCI 3.3, LVPECL
2.5 V	LVCMOS 2.5, LVCMOS 2.5/5.0, LVDS
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5

Features Supported on Every I/O

Table 2-13 lists all features supported by Transmitter/Receiver for single-ended and differential I/Os.

Table 2-13 • **I/O Features**

Feature	Description
Single-Ended Transmitter Features	• Hot insertion in every mode except PCI or 5-V-input-tolerant (these modes use clamp diodes and do not allow hot insertion) (A3P030 only) • Activation of hot insertion (disabling the clamp diode) is selectable by I/Os (A3P030 only) • Weak pull-up and pull-down • Two slew rates • Skew between output buffer enable/disable time: 2 ns delay (delay on rising edge) and 0 ns delay on falling edge (see "Selectable Skew between Output Buffer Enable/Disable Time" on page 2-39 for more information) • Three drive strengths • 5 V tolerant receiver ("5 V Input Tolerance" section on page 2-35) • LVTTL/LVCMOS 3.3 V outputs compatible with 5 V TTL inputs ("5 V Output Tolerance" section on page 2-38) • High performance (Table 2-14)
Single-Ended Receiver Features	• Electro-Statics Discharge (ESD) protection • High performance (Table 2-14) • Separate ground and power planes, GNDQ/VMV, for input buffers only to avoid output-induced noise in the input circuitry
Differential Receiver Features (A3P250 through A3P1000)	• ESD protection • High performance (Table 2-14) • Separate ground and power plane, GNDQ, and VMV pins for input buffers only to avoid output-induced noise in the input circuitry
CMOS-Style LVDS or LVPECL Transmitter	• Two I/Os and external resistors are used to provide a CMOS-style LVDS or LVPECL transmitter solution. • Weak pull-up and pull-down • Fast slew rate
LVDS/LVPECL Differential Receiver Features	• ESD protection • High performance (Table 2-14) • Separate input buffer ground and power planes to avoid output-induced noise in the input circuitry

Table 2-14 • **Maximum I/O Frequency for Single-Ended and Differential I/Os (maximum drive strength and high slew selected)**

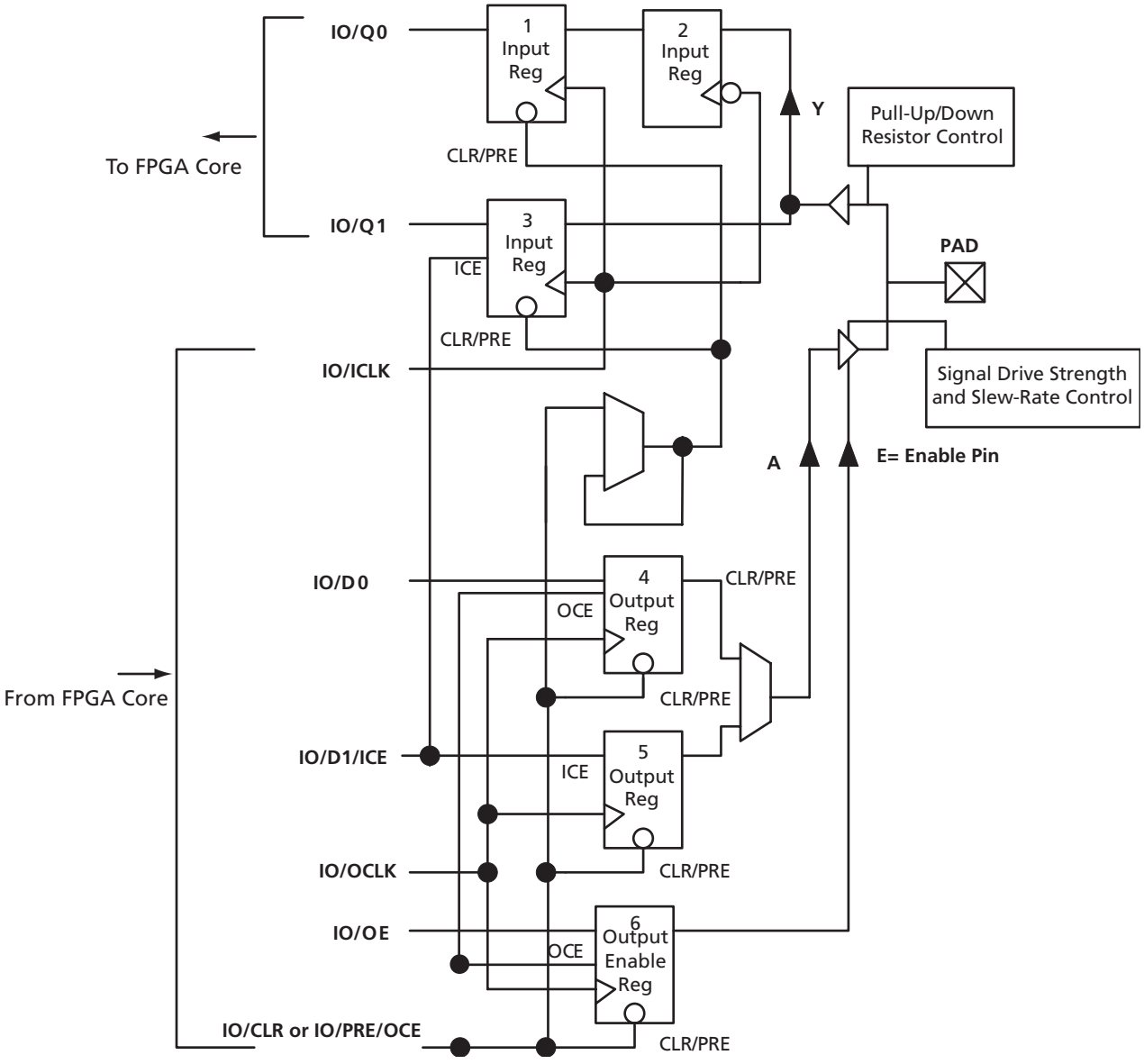
Specification	Performance Up To
LVTTL/LVCMOS 3.3 V	200 MHz
LVCMOS 2.5 V	250 MHz
LVCMOS 1.8 V	200 MHz
LVCMOS 1.5 V	130 MHz
PCI	200 MHz
PCI-X	200 MHz
LVDS	350 MHz
LVPECL	350 MHz

I/O Registers

Each I/O module contains several input, output, and enable registers. Refer to Figure 2-23 for a simplified representation of the I/O block.

The number of input registers is selected by a set of switches (not shown in Figure 2-23) in between registers to implement single or differential data transmission to and from the FPGA core. The Designer software sets these switches for the user.

A common CLR/PRE signal is employed by all I/O registers when I/O register combining is used. Input Register 2 does not have a CLR/PRE pin, as this register is used for DDR implementation.



Note: *ProASIC3 IOs have registers to support DDR functionality (see the "Double Data Rate (DDR) Support" section on page 2-31).*

Figure 2-23 • **I/O Block Logical Representation**

Double Data Rate (DDR) Support

ProASIC3 devices support 350 MHz DDR inputs and outputs. In DDR mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidth and signal integrity requirements, making it very efficient for implementing very high-speed systems.

In addition, high-speed DDR interfaces can be implemented using LVDS.

Input Support for DDR

The basic structure to support a DDR input is shown in Figure 2-24. Three input registers are used to capture incoming data, which is presented to the core on each rising edge of the I/O register clock.

Each I/O tile on ProASIC3 devices supports DDR inputs.

Output Support for DDR

The basic DDR output structure is shown in Figure 2-25 on page 2-32. New data is presented to the output every half clock cycle. Note: DDR macros and I/O registers do not require additional routing. The combiner automatically recognizes the DDR macro and pushes its registers to the I/O register area at the edge of the chip. The routing delay from the I/O registers to the I/O buffers is already taken into account in the DDR macro.

Refer to the Actel application note, *Using DDR for ProASIC3/E Devices* for more information.

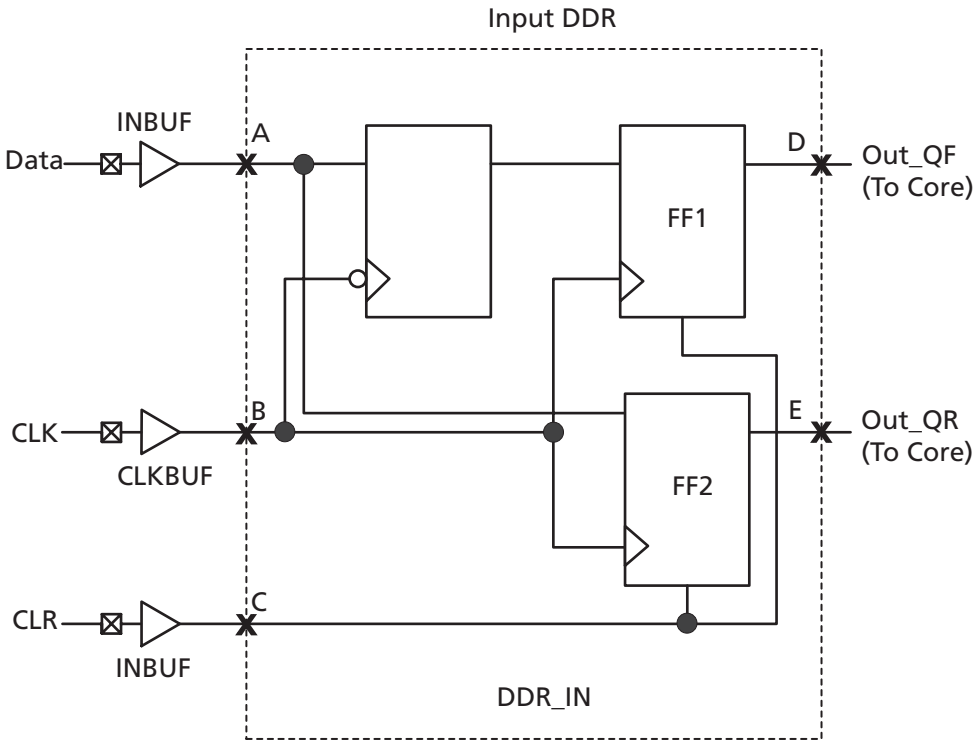


Figure 2-24 • **DDR Input Register Support in ProASIC3 Devices**

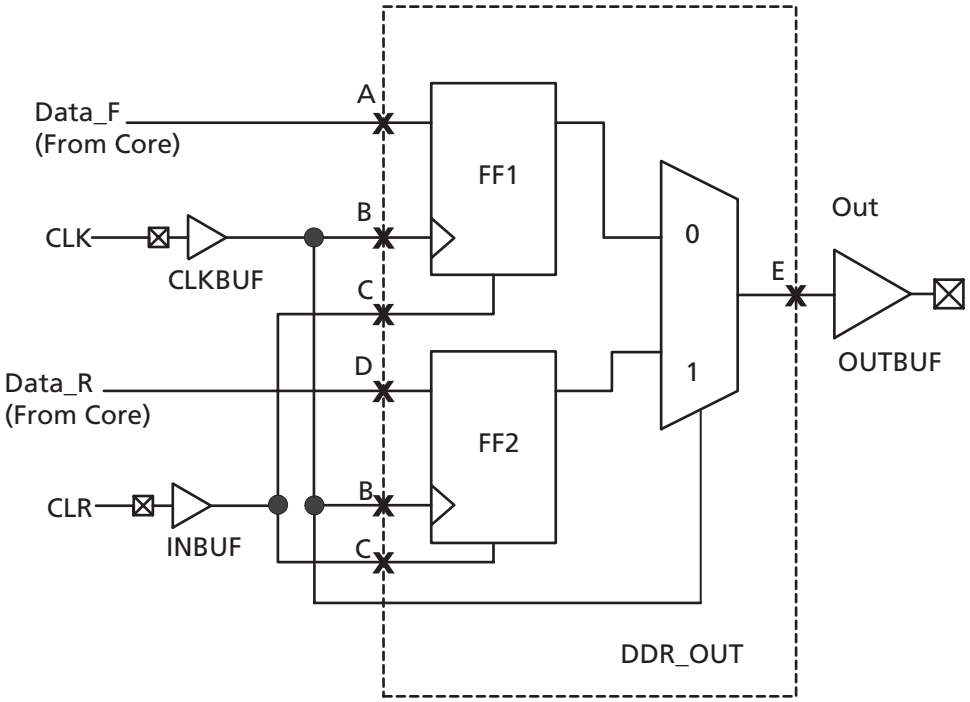


Figure 2-25 • **DDR Output Support for ProASIC3 Devices**

Hot-Swap Support

Hot swapping (also called hot plugging) is the operation of hot insertion or hot removal of a card in (or from) a powered-up system. The levels of hot-swap support and examples of related applications are described in Table 2-15. The I/Os also need to be configured in hot insertion mode if hot plugging compliance is required. The only ProASIC3 device supporting hot-swap is the A3P030, which supports hot-swapping when the clamp diode is disabled.

For boards and cards with three levels of staging, it is assumed that card power supplies have time to reach their final value before the I/Os are connected. Pay attention to the sizing of power supply decoupling capacitors on the card to ensure that the power supplies are not overloaded with capacitance.

Cards with three levels of staging should have the following sequence:

- Grounds
- Powers

I/Os and other pins

Table 2-15 • **Levels of Hot-Swap Support**

Hot Swapping Level	Description	Power Applied to Device	Bus State	Card Ground Connection	Device Circuitry Connected to Bus Pins	Example of Application with Cards that Contain ProASIC3 Devices	Compliance of ProASIC3 Devices
1	Cold swap	No	–	–	–	System and card is powered down, and then the card gets plugged into the system. Then, the power supplies are turned on.	Compliant
2	Hot swap while reset	Yes	Held in reset state	Must be made and maintained for 1 ms before, during, and after insertion/ removal	–	In PCI hot-plug specification, reset control circuitry isolates the card busses until the card supplies are at their nominal operating levels and stable.	Compliant
3	Hot swap while bus idle	Yes	Held idle (no ongoing I/O processes during insertion/removal	Same as Level 2	Must remain glitch-free during power up or power down	Board bus shared with card bus is "frozen", and there is no toggling activity on the bus, and it is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with three levels of staging
4	Hot swap on an active bus	Yes	Bus may have active I/O processes ongoing, but device being inserted or removed must be idle	Same as Level 2	Same as Level 3	There is activity on the system bus, and it is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with three levels of staging

Electro-Static Discharge (ESD) Protection

ProASIC3 devices are tested per JEDEC Standard JESD22-A114-B.

ProASIC3 devices contain clamp diodes at every I/O, global, and power pad. Clamp diodes protect all device pads against damage from ESD as well as from excessive voltage transients.

Each I/O has two clamp diodes. One diode has its positive (P) side connected to pad, and its negative (N) side connected to V_{CCI}. The second diode has its P side connected to GND, and its N side connected to pad. During operation, these diodes are normally biased in the off state, except when transient voltage is significantly above V_{CCI} or below GND levels.

In A3P030, the first diode is always off while on other ProASIC3 devices, the clamp diode is always on and cannot be switched off.

By selecting the appropriate I/O configuration, the diode is turned on or off. Refer to Table 2-16 for more information about the I/O standards and the clamp diode.

The second diode is always connected to the pad, regardless of the I/O configuration selected.

Table 2-16 • **ProASIC3I/O Hot-Swap and 5 V Input Tolerance Capabilities**

	Clamp Diode[1]		Hot Insertion		5 V Input Tolerance[2]			
I/O Assignment	A3P030	Other ProASIC3 Devices	A3P030	Other ProASIC3 Devices	A3P030	Other ProASIC3 Devices	Input Buffer	Output Buffer
3.3 V LVTTL/LVCMOS	No	Yes	Yes	No	Yes[2]	Yes[2]	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	N/A	Yes	N/A	No	N/A	Yes[2]	Enabled/Disabled	
LVCMOS 2.5 V [3]	No	Yes	Yes	No	Yes[2]	Yes[3]	Enabled/Disabled	
LVCMOS 2.5 V / 5.0 V [3]	No	Yes	Yes	No	Yes[2]	Yes[3]	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	Yes	No	No	No	Enabled/Disabled	
LVCMOS 1.5 V	No	Yes	Yes	No	No	No	Enabled/Disabled	
Differential, LVDS/ LVPECL[4]	N/A	Yes	N/A	No	N/A	No	Enabled/Disabled	

Notes:

1. *The clamp diode is always off for the A3P030 device and always active for other ProASIC3 devices.*
2. *Can be implemented with an external IDT bus switch, resistor divider, or zener with resistor.*
3. *Can be implemented with an external resistor and an internal clamp diode.*
4. *LVCMOS 2.5 V and LVCMOS 2.5 V / 5.0 V I/O standards are identical in the ProASIC3 family. For the A3P030 device, these standards have no clamp diode; therefore, they both behave like a LVCMOS 2.5 V standard. For other ProASIC3 devices, these standards have a clamp diode; therefore, they both behave like LVCMOS 2.5 V / 5.0 V input standard.*
5. *Bidirectional LVDS or LVPECL buffers are not supported. I/Os can either be configured as input buffers or output buffers.*

5 V Input Tolerance

I/Os can support 5 V input tolerance when LVTTL 3.3 V, LVCMOS 3.3 V, LVCMOS 2.5 V and LVCMOS 2.5 V configurations are used (see Table 2-17 on page 2-38 for more details). There are four recommended solutions (see Figure 2-26 to Figure 2-29 on page 2-38 for details of board and macro setups) to achieve 5 V receiver tolerance. All the solutions meet a common requirement of limiting the voltage at the I/O input to 3.6 V or less. In fact, the I/O absolute maximum voltage rating is 3.6 V, and any voltage above 3.6 V may cause long term gate oxide failures.

Solution 1

The board-level needs to ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-3 on page 3-2. This is a long term reliability requirement.

This scheme will also work for a 3.3 V PCI / PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the two external resistors as explained below. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

Examples of possible resistor values (based on a simplified simulation model with no line effects, and 10 Ω transmitter output resistance, where Rtx_out_high = (V_{CCI} - V_{OH})/ I_{OH}, Rtx_out_low = V_{OL} / I_{OL}).

Example 1: (high speed, high current)

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 36 Ω (+/-5%), P(r1)min = 0.069 Ω

R2 = 82 Ω (+/-5%), P(r2)min = 0.158 Ω

Imax_tx = 5.5 V / (82 * 0.95 + 36 * 0.95 +10) = 45.04 mA

t_{RISE} = t_{FALL} = 0.85 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

t_{RISE} = t_{FALL} = 4 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Example 2: (low-medium speed, medium current)

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 220 Ω (+/-5%), P(r1)min = 0.018 Ω

R2 = 390 Ω (+/-5%), P(r2)min = 0.032 Ω

Imax_tx = 5.5 V / (220 * 0.95 + 390 * 0.95 +10) = 9.17 mA

t_{RISE} = t_{FALL} = 4 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

t_{RISE} = t_{FALL} = 20 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Other values of resistors are also allowed as long as the resistors are sized appropriately to limit the voltage at the receiving end to 2.5 V < Vin(rx) < 3.6 V* when the transmitter sends a logic '1'. This range of Vin_dc(rx) has to be ensured for any combination of transmitter supply (5 V +/- 0.5 V), transmitter output resistance, and board resistor tolerances.

Temporary overshoots are allowed according to Table 3-3 on page 3-2.

Solution 1

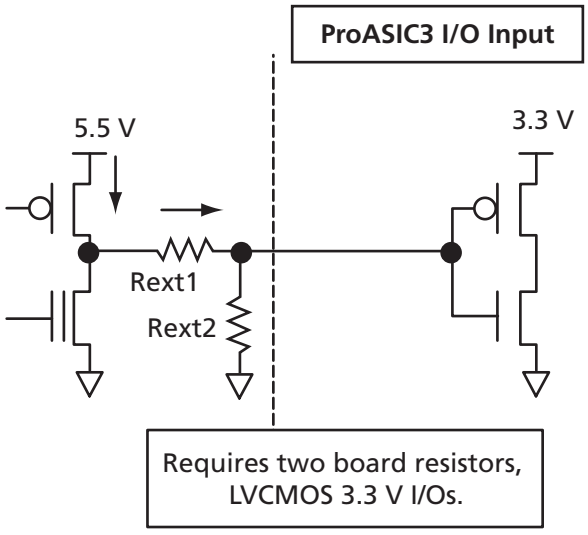


Figure 2-26 • **Solution 1**

Solution 2

The board-level design needs to ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-3 on page 3-2. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCIX configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the external resistors and zener, as shown in Figure 2-27. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

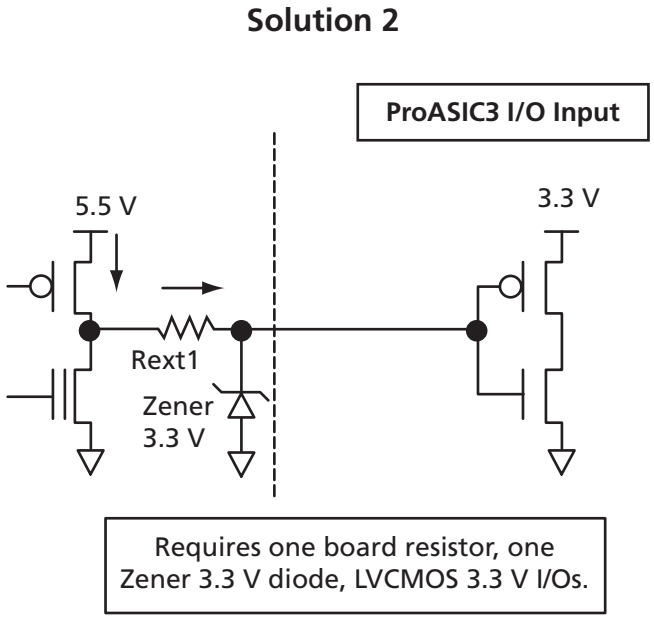


Figure 2-27 • **Solution 2**

Solution 3

The board-level design needs to ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-3 on page 3-2. This is a long-term reliability requirement.

This scheme will also work for 3.3 V PCI/PCIX configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the bus switch, as shown in Figure 2-28. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

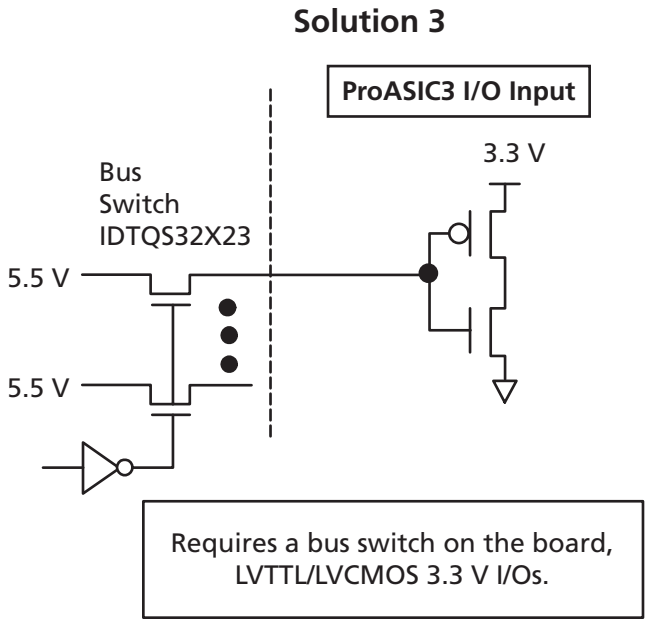


Figure 2-28 • **Solution 3**

Solution 4

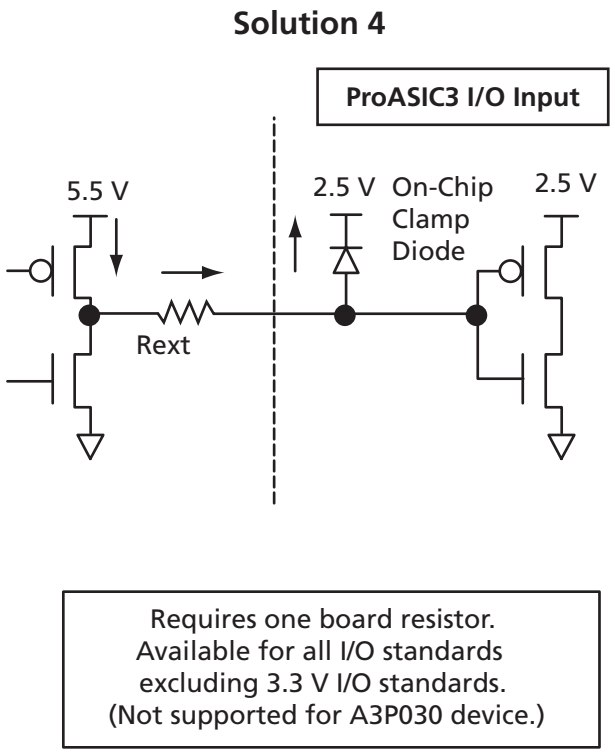


Figure 2-29 • **Solution 4**

Table 2-17 • **Comparison Table for 5 V Compliant Receiver Scheme**

Solution	Board Components	Speed	Current Limitations
1	Two resistors	Low to High[1]	Limited by transmitter's drive strength
2	Resistor and Zener 3.3 V	Medium	Limited by transmitter's drive strength
3	Bus switch	High	N/A
4	Resistor[2] R = 250 Ω at T_J = 70°C R = 500 Ω at T_J = 85°C R = 1000 Ω at T_J = 100°C	Low	Diode current 12 mA at T_J = 70°C 6 mA at T_J = 85°C 3 mA at T_J = 100°C

Notes:

1. *Speed and current consumption increase as the board resistance values decrease.*
2. *Resistor values ensure I/O diode long term reliability.*

5 V Output Tolerance

ProASIC3 I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value, and consequently cause damage to the I/O.

When set to 3.3 V LVTTL or 3.3 V LVCMOS mode, ProASIC3 I/Os can directly drive signals into 5 V TTL receivers. In fact, V_{OL} = 0.4 V and V_{OH} = 2.4 V voltages on both 3.3 V LVTTL and 3.3 V LVCMOS modes exceed the V_{IL} = 0.8 V and V_{IH} = 2 V level requirements of 5 V TTL receivers. Therefore, level '1' and level '0' will be recognized correctly by 5 V TTL receivers.

Selectable Skew between Output Buffer Enable/Disable Time

The configurable skew block is used to delay the output buffer assertion (enable) without affecting deassertion (disable) time.

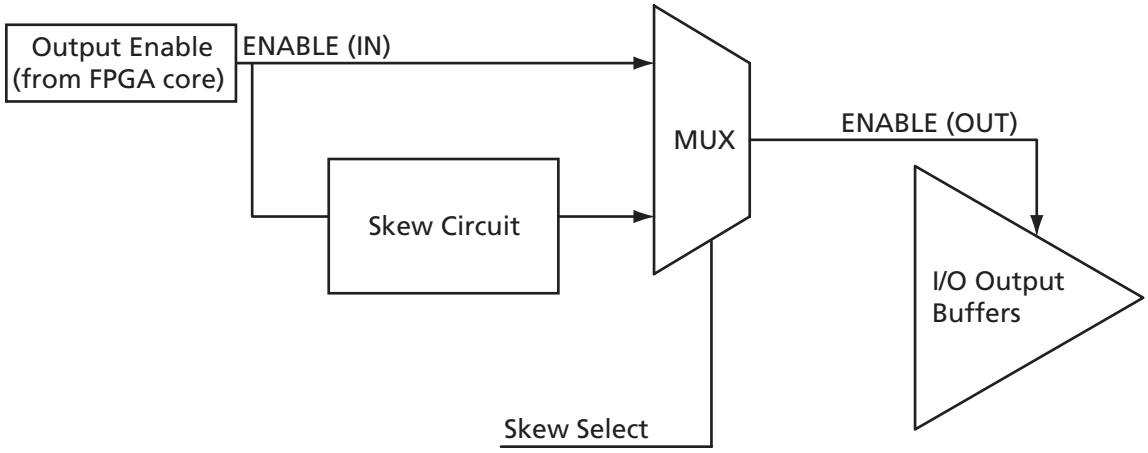


Figure 2-30 • **Block Diagram of Output Enable Path**

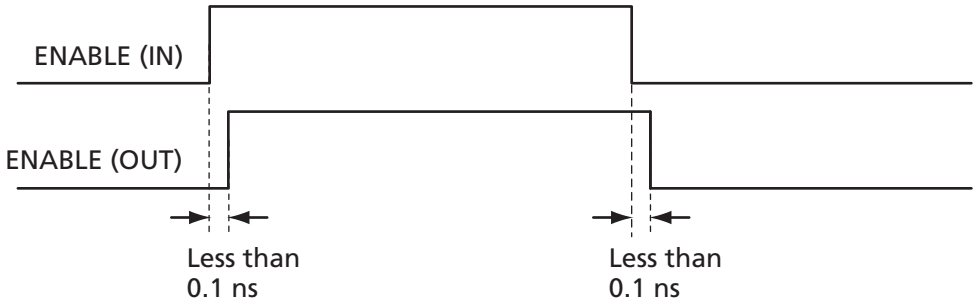


Figure 2-31 • **Timing Diagram (Option1: Bypasses Skew Circuit)**

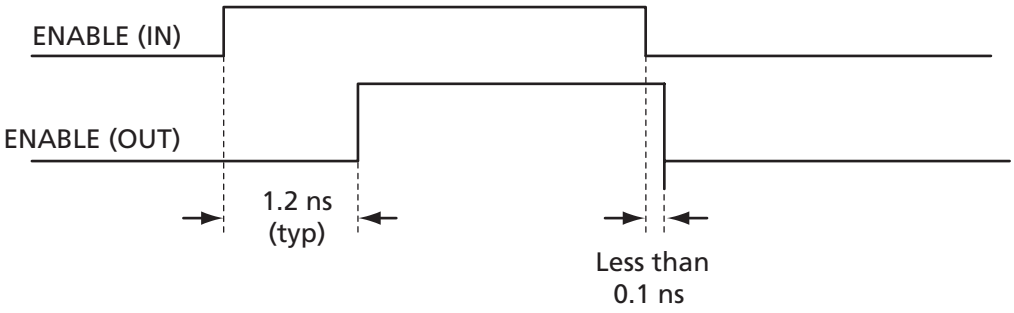


Figure 2-32 • **Timing Diagram (Option 2: With Skew Circuit Selected)**

On a system level, the skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. This circuit, when selected, provides a timing margin that can prevent bus contention and subsequent data loss and/or transmitter over-stress due to transmitter-to-transmitter current shorts. Figure 2-33 presents an example of the skew circuit implementation in a bidirectional communication system. Figure 2-34 shows how a bus contention is created, and Figure 2-35 on page 2-41 shows how it can be avoided with the skew circuit.

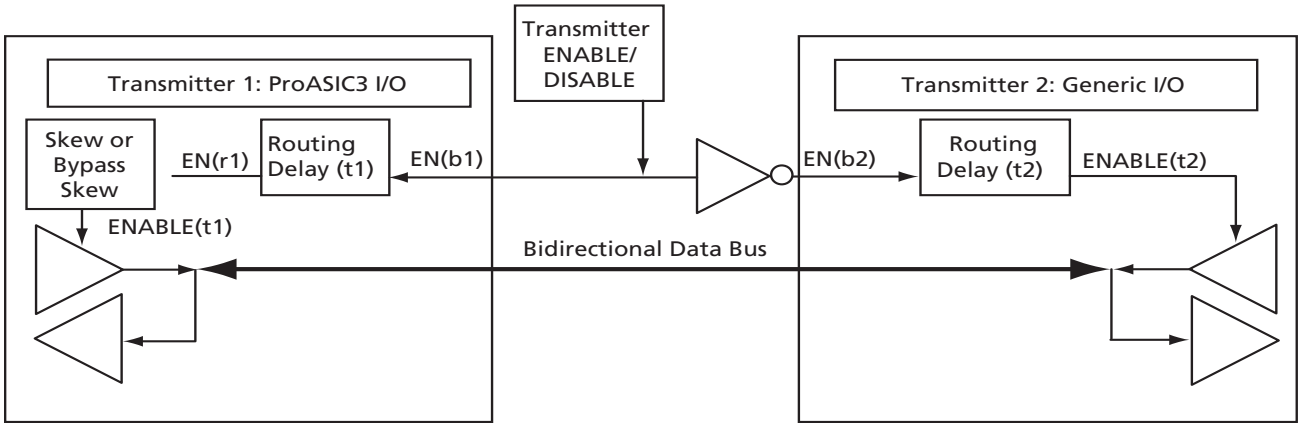


Figure 2-33 • **Example of Implementation of Skew Circuits in Bidirectional Transmission Systems Using ProASIC3 Devices**

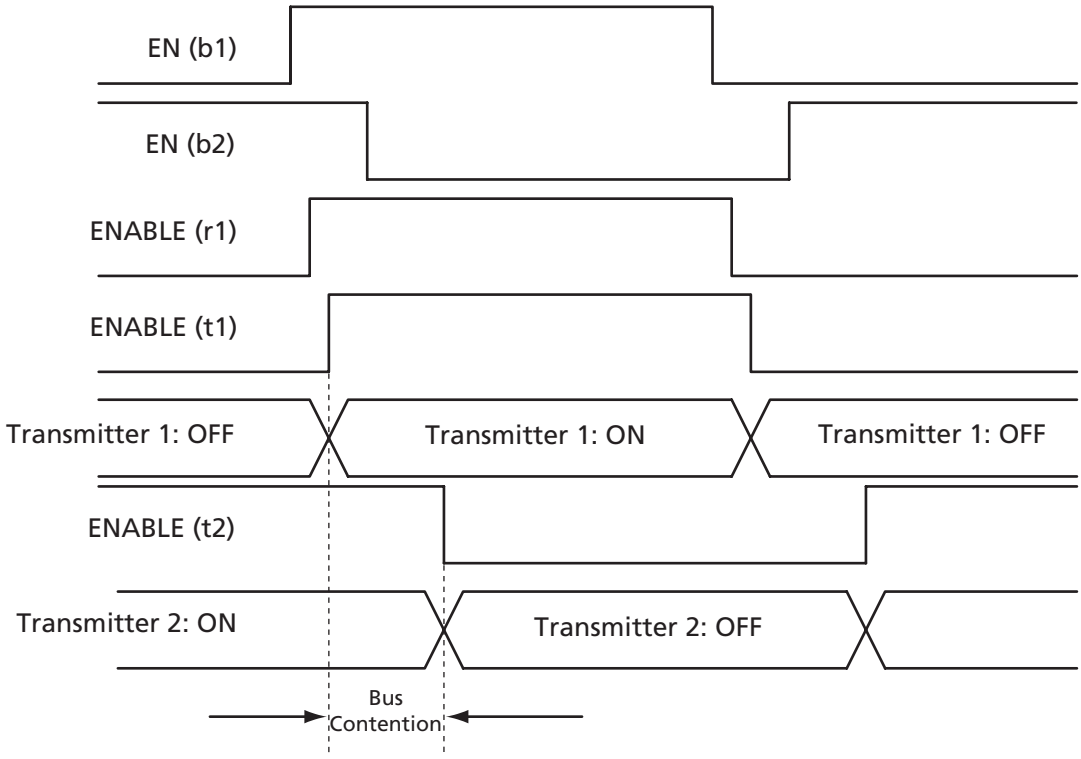
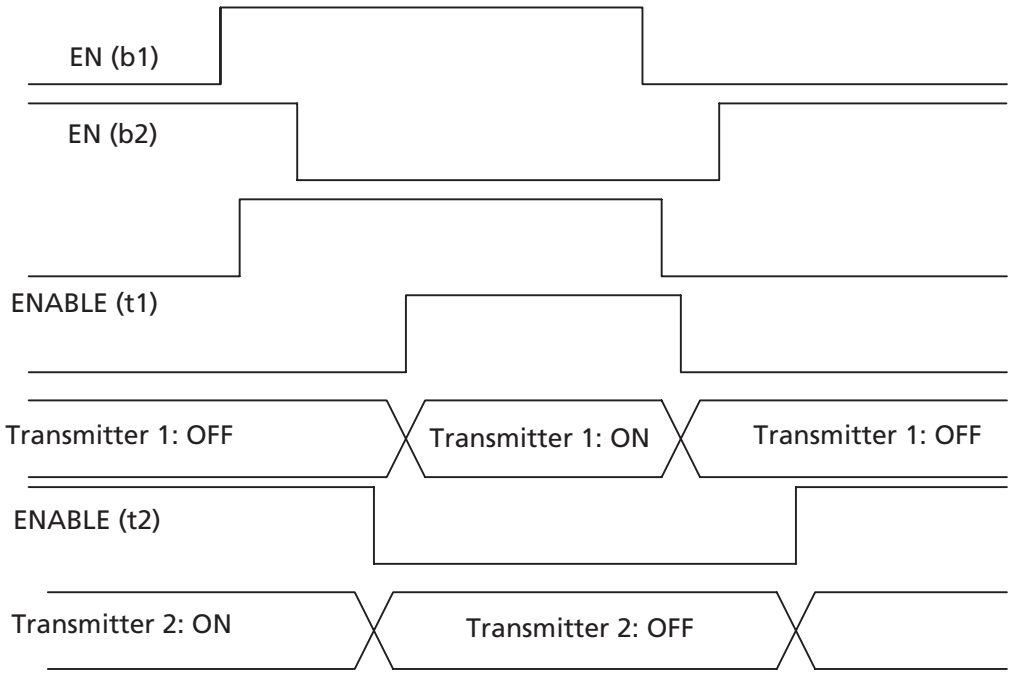


Figure 2-34 • **Timing Diagram (Bypasses Skew Circuit)**



Result: No Bus Contention

Figure 2-35 • **Timing Diagram (with Skew Circuit Selected)**

I/O Software Support

In the ProASIC3 development software, default settings have been defined for the various I/O standards that are supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. Table 2-18 lists the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in ProASIC3 support up to five different drive strengths.

Table 2-19 lists the default values for the above selectable I/O attributes as well as those that are preset for that I/O standard. See Table 2-21 on page 2-43 for SLEW and OUT_DRIVE settings.

Table 2-18 • **I/O Attributes vs. I/O Standard Applications**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓
LVCMOS 2.5 V	✓	✓	✓	✓	✓	✓
LVCMOS 2.5/5.0 V	✓	✓	✓	✓	✓	✓
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓
LVCMOS 1.5 V	✓	✓	✓	✓	✓	✓
PCI (3.3 V)			✓			✓
PCI-X (3.3 V)	✓		✓			✓
LVDS			✓			✓
LVPECL			✓			✓

Table 2-19 • **I/O Default Attributes**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW) (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	See Table 2-21 on page 2-43	See Table 2-21 on page 2-43	Off	None	35 pF	–
LVCMOS 2.5 V			Off	None	35 pF	–
LVCMOS 2.5/5.0 V			Off	None	35 pF	–
LVCMOS 1.8 V			Off	None	35 pF	–
LVCMOS 1.5 V			Off	None	35 pF	–
PCI (3.3 V)			Off	None	10 pF	–
PCI-X (3.3 V)			Off	None	10 pF	–
LVDS			Off	None	0 pF	–
LVPECL			Off	None	0 pF	–

Weak Pull-Up and Weak Pull-Down Resistors

ProASIC3 devices support optional weak pull-up and pull-down resistors per I/O pin. When the I/O is pulled up, it is connected to the V_{CCI} of its corresponding I/O bank. When it is pulled-down it is connected to GND. Refer to Table 3-20 on page 3-16 for more information.

Slew Rate Control and Drive Strength

ProASIC3 devices support output slew rate control: high and low. The A3P030 device does not support slew rate control. The high slew rate option is recommended to minimize the propagation delay. This high-speed option may introduce noise into the system if appropriate signal integrity measures are not adopted. Selecting a low slew rate reduces this kind of noise but adds some delays in the system. A low slew rate is recommended when bus transients are expected. Drive strength should also be selected according to the design requirements and noise immunity of the system.

The output slew rate and multiple drive strength controls are available in LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V, LVCMOS 2.5 V / 5.0 V input, LVCMOS 1.8 V and LVCMOS 1.5 V. All other I/O standards have a high output slew rate by default.

For A3P030, refer to Table 2-20; for other ProASIC3 devices, refer to Table 2-21 for more information about the slew rate and drive strength specification.

Table 2-20 • **A3P030 I/O Standards—OUT_DRIVE Settings**

	OUT_DRIVE (mA)		
I/O Standards	**2**	**4**	**8**
LVTTL/LVCMOS33	✓	✓	✓
LVCMOS25	✓	✓	✓
LVCMOS25_50	✓	✓	✓
LVCMOS18	✓	✓	–
LVCMOS15	✓	✓	–

Table 2-21 • **ProASIC3 Device I/O Standards—SLEW and OUT_DRIVE Settings**

	OUT_DRIVE (mA)							
I/O Standards	**2**	**4**	**6**	**8**	**12**	**16**	**Slew**	
LVTTL/LVCMOS33	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS25	✓	✓	✓	✓	✓	–	High	Low
LVCMOS25_50	✓	✓	✓	✓	✓	–	High	Low
LVCMOS18	✓	✓	✓	✓	–	–	High	Low
LVCMOS15	✓	✓	–	–	–	–	High	Low

User I/O Naming Convention

Due to the comprehensive and flexible nature of the ProASIC3 device user I/Os, a naming scheme is used to show the details of the I/O (Figure 2-36 and Figure 2-37 on page 2-45). The name identifies to which I/O bank it belongs, as well as the pairing and pin polarity for differential I/Os.

I/O Nomenclature = Gmn/IOuxwBy

Gmn is only used for I/Os that also have CCC access – i.e., global pins.

G = Global

m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle).

n = Global input MUX and pin number of the associated Global location m, either A0, A1,A2, B0, B1, B2, C0, C1, or C2. Figure 2-15 on page 2-16 shows the three input pins per each clock source MUX at the CCC location m.

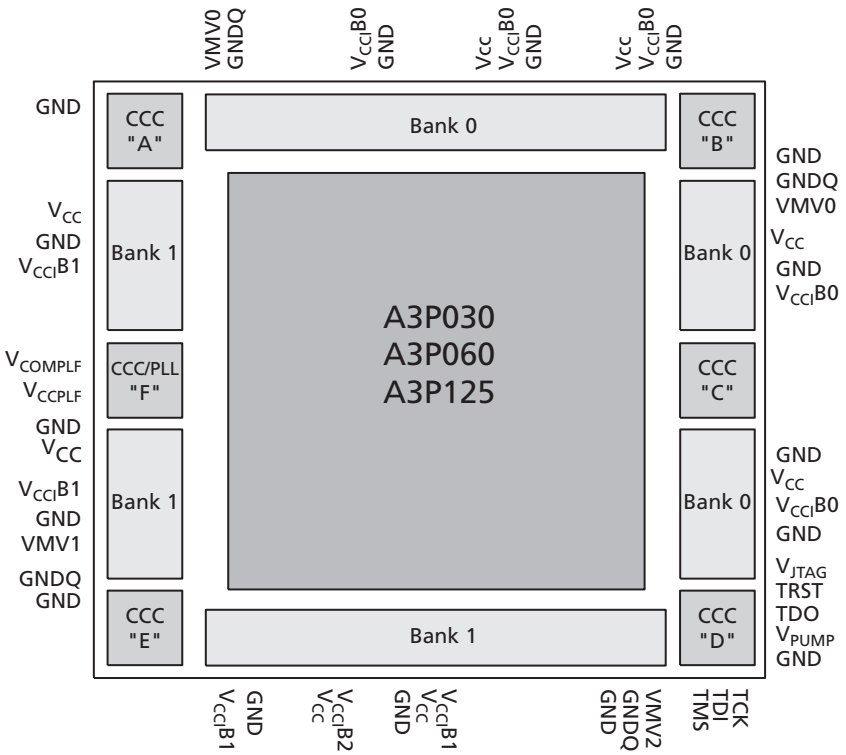
u = I/O pair number in the bank, starting at 00 from the northwest I/O bank in a clockwise direction.

x = P (Positive) or N (Negative) for differential pairs, or S (Single-Ended) for the I/O that support single-ended and voltage-referenced I/O standards only

w = D (Differential Pair) or P (Pair) or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

B = Bank

y = Bank number [0..3]. Bank number starting at 0 from the northwest I/O bank in a clockwise direction.



Note: *The A3P030 device does not support PLL (V_{COMPLF} and V_{CCPLF} pins).*

Figure 2-36 • **Naming Conventions of ProASIC3 Devices with Two I/O Banks**

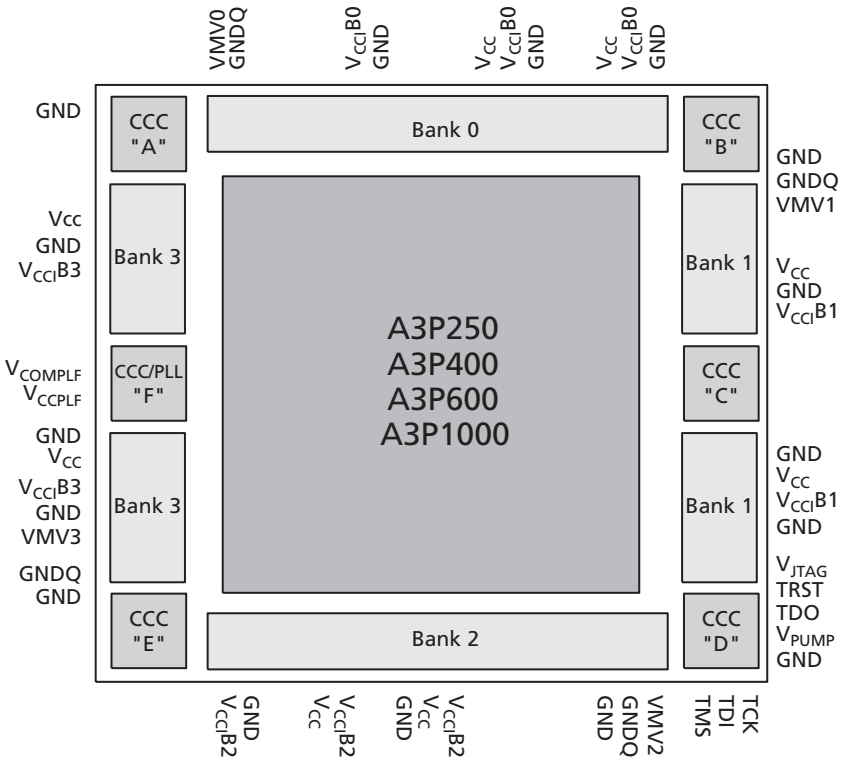


Figure 2-37 • **Naming Conventions of ProASIC3 Devices with Four I/O Banks**

Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (Quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package, and improves input signal integrity. GNDQ needs to always be connected on the board to GND.

V_{CC} **Core Supply Voltage**

Supply voltage to the FPGA core, nominal 1.5 V.

V_{CCI}Bx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are eight I/O banks on ProASIC3 devices plus a dedicated V_{JTAG} bank. Each bank can have a separate V_{CCI} connection. All I/Os in a bank will run off the same V_{CCI}Bx supply. V_{CCI} can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V nominal voltage. Unused I/O banks should have their corresponding V_{CCI} pins tied to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. X is the bank number. Within the package, the VMV plane is decoupled from the simultaneous switching noise originated from the output buffer V_{CCI} domain. This minimizes the noise transfer within the package, and improves input signal integrity. Each bank must have at least one VMV connection. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and V_{CCI} should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding V_{CCI} pins of the same bank (i.e. VMV0 to V_{CCI}B0, VMV1 to V_{CCI}B1, etc.).

V_{CCPLF} **PLL Supply Voltage**[6]

Supply voltage to analog PLL. If unused, V_{CCPLF} should be tied to GND.

V_{COMPLF} **PLL Ground**[6]

Ground to analog PLL. Unused V_{COMPL} pins should be connected to GND.

V_{JTAG} **JTAG Supply Voltage**

ProASIC3 devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and printed circuit board design.

V_{PUMP} **Programming Supply Voltage**

ProASIC3 devices support single-voltage ISP programming of the configuration Flash and FROM. For programming, V_{PUMP} should be 3.3 V nominal. During normal device operation, V_{PUMP} can be left floating or can be tied (pulled up) to any voltage between 0 V and 3.6 V.

Global Pins

GL **Globals**

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as I/Os, since they have identical capabilities. See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits" section on page 2-13.

Refer to the "User I/O Naming Convention" section on page 2-44 for a description of naming of global pins.

JTAG Pins

TCK **Test Clock**

Test clock input for the JTAG boundary-scan, ISP, and UJTAG usage. Per the (JTAG) IEEE1532 specification, it is recommended that TCK be tied to GND or V_{JTAG} when not used. This prevents a possible totem-pole current on the input buffer stage. The TCK pin does not have an internal weak pull-up resistor.

TDI **Test data Input**

Serial input for JTAG boundary-scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO **Test Data Output**

Serial output for JTAG boundary-scan, ISP, and UJTAG usage. The TDO pin does not have an internal weak pull-up resistor.

6. The A3P030 device does not support this feature.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK,TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST **Boundary Scan Reset Pin**

The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. In the operating mode, a 100 Ω external pull-down resistor should be placed between TRST and GND to ensure that the chip does not switch into a different mode.

Special Function Pins

NC **No connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Don't connect**

This pin should not be connected to any signals on the printed circuit board (PCB). These pins should be left un-connected.

Software Tools

Overview of Tools Flow

The ProASIC3 family of FPGAs is fully supported by both Actel Libero IDE and Designer FPGA Development software. Actel Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see the *Libero IDE flow diagram* located on the Actel website). Libero IDE includes Synplify® AE from Synplicity®, ViewDraw® AE from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ AE from SynaptiCAD®, PALACE™ Physical Synthesis from Magma Design Automation™, and Designer software from Actel.

Actel Designer software is a place-and-route tool and provides a comprehensive suite of back-end support tools for FPGA development. The Designer software includes the following:

- Timer – a world-class integrated static timing analyzer and constraints editor that supports timing-driven place-and-route
- NetlistViewer – a design netlist schematic viewer
- ChipPlanner – a graphical floorplanner viewer and editor
- SmartPower – tool which enables the designer to quickly estimate the power consumption of a design
- PinEditor – a graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor – tool which displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, Actel back-annotation flow is compatible with all the major simulators. Another tool included in the Designer software is the ACTgen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Actel Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors, such as Mentor Graphics, Synplicity, Synopsys, and Cadence®. The Designer software is available for both the Windows® and UNIX operating systems.

Programming

Programming can be performed using various programming tools, such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Actel).

The user can generate *.stp programming files from the Designer software and can use these files to program a device.

ProASIC3 devices can be programmed in system. For more information on ISP of ProASIC3 devices, refer to the *In-System Programming (ISP) in ProASIC3/E Using FlashPro3* and *Programming a ProASIC3/E Using a Microprocessor* application notes.

Security

ProASIC3 devices have a built-in 128-bit AES decryption core (except the A3P030 device). The decryption core facilitates secure, in-system programming of the FPGA core array fabric and the FROM. The FROM and the FPGA core fabric can be programmed independently from each other, allowing the FROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (Flash). The AES master key can be preloaded into parts in a secure programming environment (such as the Actel in-house programming center) and then "blank" parts can be

shipped to an untrusted programming or manufacturing center for final personalization with an AES encrypted bitstream. Late stage product changes or personalization can be implemented easily and securely by simply sending a STAPL file with AES encrypted data. Secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES encrypted data.

128-Bit AES Decryption[7]

The 128-bit AES standard (FIPS-192) block cipher is the NIST (National Institute of Standards and Technology) replacement for the DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It will replace the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has $3.4x10^{38}$ possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (securely) in ProASIC3 devices in nonvolatile Flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of ProASIC3 devices remain secure.

AES decryption can also be used on the 1,024-bit FROM to allow for secure remote updates of the FROM contents. This allows for easy, secure support for subscription model products. See the application note, *ProASIC3/E Security*, for more details.

ISP

ProASIC3 devices support IEEE1532 ISP via JTAG and require a single V_{PUMP} voltage of 3.3 V during programming. In addition, programming via a Microcontroller (MCU) in a target system can be achieved. See the application note *In-System Programming (ISP) in ProASIC3/E Using FlashPro3* for more details.

JTAG 1532

Programming

ProASIC3 devices support the JTAG-based IEEE1532 standard for ISP. As part of this support, when a ProASIC3 device is in an unprogrammed state, all user I/O pins are disabled. This is achieved by keeping the global IO_EN signal deactivated, which also has the effect of disabling the input buffers. Consequently, the SAMPLE instruction will have no effect while the ProASIC3 device is in this unprogrammed state. This is different behavior from that observed in the ProASIC^{PLUS} device family. This lack of effect is necessitated by the fact that SAMPLE is defined in the IEEE1532 specification as a noninvasive instruction. If the input buffers were to be enabled by SAMPLE temporarily turning on the I/Os, then it would not truly be a noninvasive instruction, hence the lack of effect when the ProASIC3 device is in this unprogrammed state. Refer to the standard or the *In-System Programming (ISP) in ProASIC3/E Using FlashPro3* application note for more details.

Boundary Scan

ProASIC3 devices are compatible with IEEE Standard 1149.1, which defines a hardware architecture and the set of mechanisms for boundary-scan testing. The basic ProASIC3 boundary-scan logic circuit is composed of the TAP (test access port) controller, test data registers, and instruction register (Figure 2-38 on page 2-49). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS) and the optional IDCODE instruction (Table 2-22 on page 2-49).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI, and TDO (test data input and output), TMS (test mode selector), and TRST (test reset input). TMS, TDI, and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary-scan test usage. Actel recommends that a nominal 20 kΩ pull-up resistor be added to TDO and TCK pins. The TAP controller is a 4-bit state machine (16 states) that operates as shown in Figure 2-38 on page 2-49. The 1s and 0s represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

ProASIC3 devices have to be programmed at least once for complete boundary-scan functionality to be available. If boundary-scan functionality is required prior to partial programming, refer to online technical support on the Actel website and search for ProASIC3 BSDL.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles. The TRST pin

7. *The A3P030 device does not support AES decryption.*

may also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

ProASIC3 devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number, and version). The boundary-scan register observes and controls the state of each I/O pin. Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin.

The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary-scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

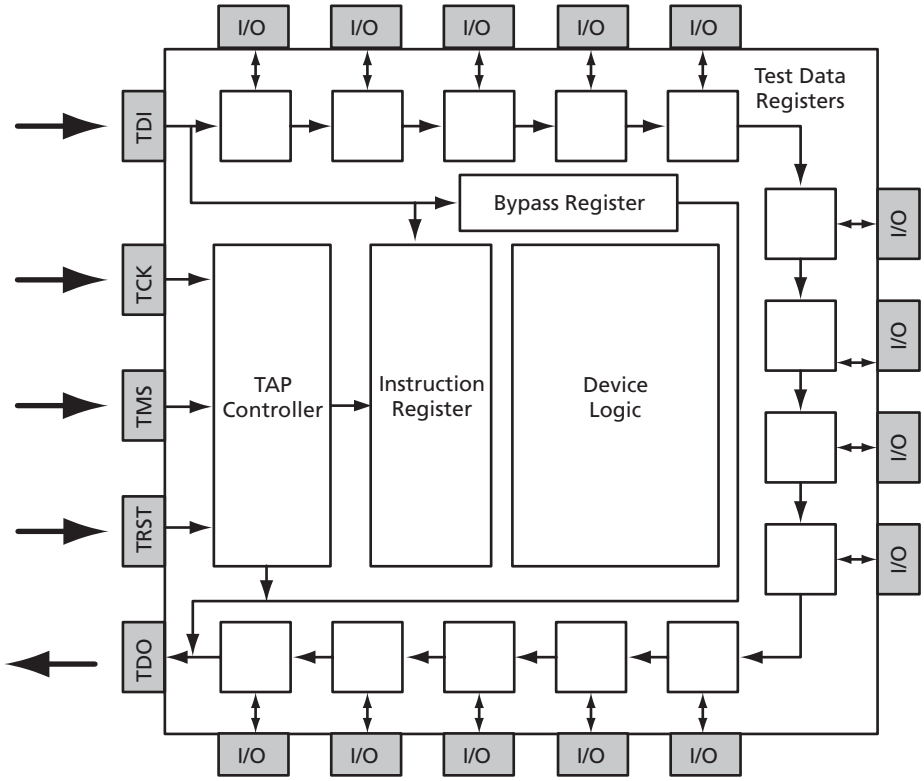


Figure 2-38 • **Boundary-Scan Chain in ProASIC3**

Table 2-22 • **Boundary-Scan Opcodes**

	Hex Opcode
EXTEST	00
HIGHZ	07
USERCODE	0E
SAMPLE/PRELOAD	01
IDCODE	0F
CLAMP	05
BYPASS	FF

DC and Switching Characteristics

General Specifications

DC and switching characteristics for –F speed grade targets based only on simulation.

The characteristics provided for –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in commercial temperature range.

Operating Conditions

Stresses beyond those listed in the Table 3-1 may cause permanent damage to the device.

Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating ranges specified in Table 3-2 on page 3-2.

Table 3-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
V_{CC}	DC core supply voltage	–0.3 to 1.65	V
V_{JTAG}	JTAG DC voltage	–0.3 to 3.75	V
V_{PUMP}	Programming voltage	–0.3 to 3.75	V
V_{CCPLL}	Analog power supply (PLL)	–0.3 to 1.65	V
V_{CCI}	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VMV	DC I/O input buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (V_{CCI} + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V

Notes:

1. *Device performance is not guaranteed if storage temperature exceeds 110°C.*
2. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-3 on page 3-2.*

Table 3-2 • **Recommended Operating Conditions**

Symbol	Parameter		Commercial	Industrial	Units
T_a	Ambient temperature		0 to +70	-40 to +85	°C
V_{CC}	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
V_{JTAG}	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
V_{PUMP}	Programming voltage	Programming Mode	3.0 to 3.6	3.0 to 3.6	V
		Operation[3]	0 to 3.6	0 to 3.6	V
V_{CCPLL}	Analog power supply (PLL)		1.4 to 1.6	1.4 to 1.6	V
V_{CCI} and VMV	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 3-13 on page 3-14. VMV and V_{CCI} should be at the same voltage within a given I/O bank.*
2. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
3. *V_{PUMP} can be left floating during operation (not programming mode).*

Table 3-3 • **Overshoot and Undershoot Limits (as measured on quiet I/Os)[1]**

V_{CCI} and VMV	Average V_{CCI}-GND Overshoot or Undershoot Duration as Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one cycle out of six clock cycles (estimated SSO density over cycles). If the overshoot/undershoot occurs at one out of two cycles, then the maximum overshoot/undershoot has to be reduced by 0.15 V.*

Table 3-4 • **Flash Programming, Storage, and Operating Limits**

Product Grade	Programming Cycles	Program Retention	Storage Temperature		Maximum Operating Junction Temperature T_J (°C)
			Min.	Max.	
Commercial	500	20 years	0	110	110
Industrial	500	20 years	–40	110	110

Note: *This is a stress rating only. Functional operation at any other condition other than those indicated is not implied.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power-up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 3-1.

There are five regions to consider during power-up.

ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. V_{CC} and V_{CCI} are above the minimum specified trip points (Figure 3-1)
2. $V_{CCI} > V_{CC} – 0.75$ V (Typ)
3. Chip is in the operating mode

V_{CCI} Trip Point:
Ramping up: 0.6 V < trip_point_up <1.2 V

Ramping down: 0.5 V < trip_point_down < 1.1 V

V_{CC} Trip Point:
Ramping up: 0.6 V < trip_point_up <1.1 V

Ramping down: 0.5 V < trip_point_down < 1 V

V_{CC} and V_{CCI} ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to V_{CCI}.
- JTAG supply, PLL power supplies, and charge pump V_{PUMP} supply have no influence on I/O behavior.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers: after 200 ns delay from input buffer activation.

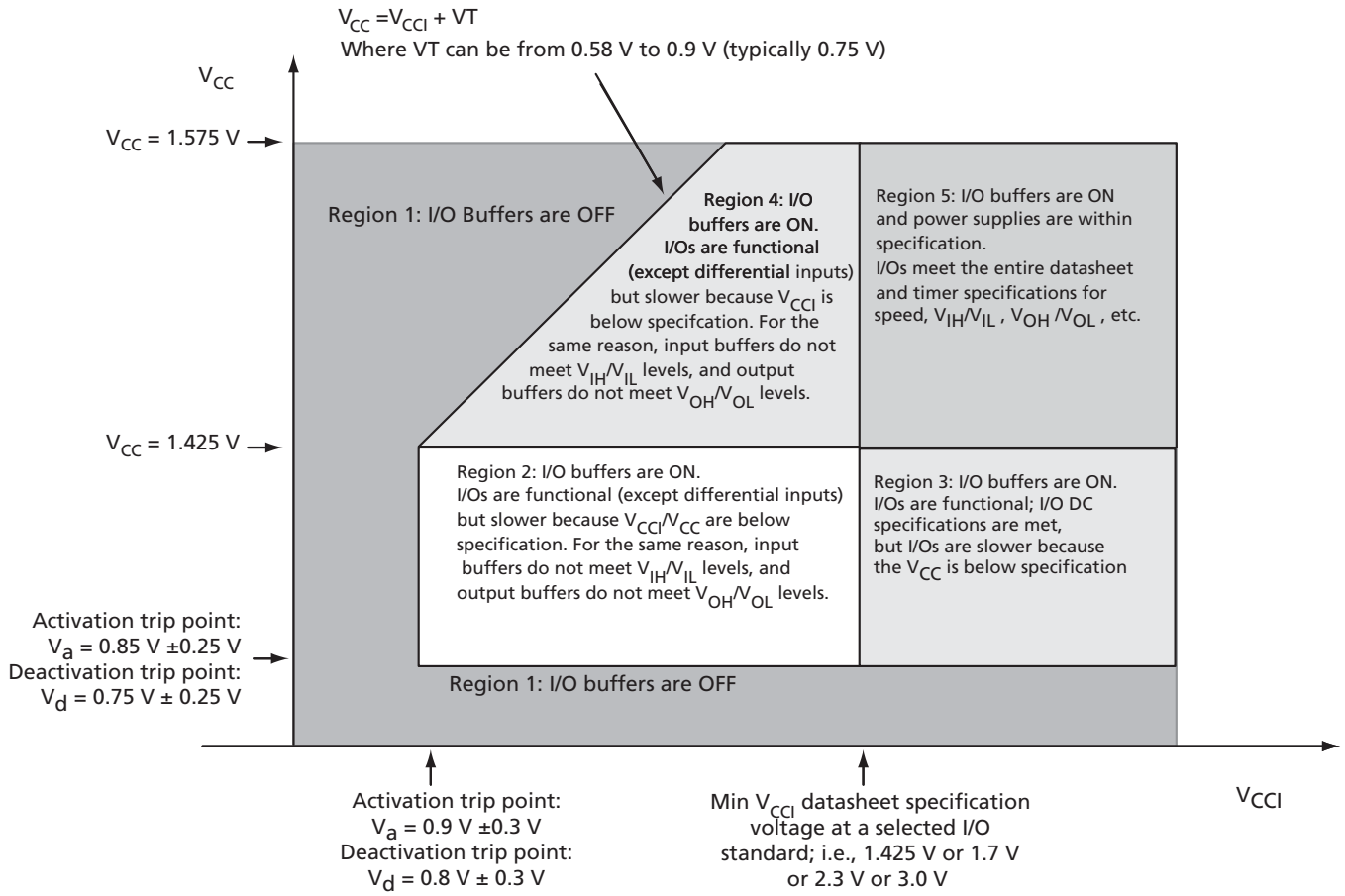


Figure 3-1 • **I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in the Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 3-1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_a \qquad \textit{EQ 3-1}$$

Where T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 3-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 3-2 shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{150\text{°C} - 70\text{°C}}{20.5\text{°C/W}} = 3.90\ \text{W} \qquad \textit{EQ 3-2}$$

Table 3-5 • **Package Thermal Resistivities**

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	200 ft./min.	500 ft./min.	
Quad Flat No Lead (QFN)	132	13.2	28.9	24.6	23.1	C/W
Very Thin Quad Flat Pack (VQFP)	100	10.0	35.3	29.4	27.1	C/W
Thin Quad Flat Pack (TQFP)	144	11.0	33.5	28.0	25.7	C/W
Plastic Quad Flat Package (PQFP)	208	8.0	26.1	22.5	20.8	C/W
Plastic Quad Flat Package (PQFP) with embedded heat spreader	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	C/W
	256	3.8	26.6	22.8	21.5	C/W
	484	3.2	20.5	17.0	15.9	C/W

Temperature and Voltage Derating Factors

Table 3-6 • **Temperature and Voltage Derating Factors for Timing Delays (Normalized to T_J = 70°C, V_{CC} = 1.425 V)**

Array Voltage V_{CC} (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	110°C
1.425	0.88	0.93	0.95	1.00	1.02	1.05
1.500	0.83	0.87	0.89	0.94	0.96	0.98
1.575	0.79	0.84	0.86	0.91	0.92	0.94

Calculating Power Dissipation

Quiescent Supply Current

Table 3-7 • **Quiescent Supply Current Characteristics**

	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
Static I_{DD} [1]	10 mA	10 mA	10 mA	20 mA	20 mA	30 mA	70 mA

Notes:

1. *I_{DD} Includes V_{CC}, V_{PUMP}, V_{CCI}, and VMV currents in industrial temperature ranges (junction temperature from –40°C to 85°C). Values do not include I/O static contribution, which is shown in Table 3-8 and Table 3-9.*
2. *–F speed grade devices may experience higher standby I_{DD} of up to five times the standard I_{DD} and higher I/O leakage.*

Power Per I/O Pin

Table 3-8 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings**

	VMV (V)	Static Power P_{DC2} (mW)[1]	Dynamic Power P_{AC9} (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.69
2.5 V LVCMOS	2.5	–	5.12
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.45
3.3 V PCI	3.3	–	18.11
3.3 V PCI-X	3.3	–	18.11
Differential			
LVDS	2.5	2.26	1.20
LVPECL	3.3	5.72	1.87

Notes:

1. *P_{DC2} is the static power (where applicable) measured on VMV.*
2. *P_{AC9} is the total dynamic power measured on V_{CC} and VMV.*

Table 3-9 • **Summary of I/O Output Buffer Power (Per Pin) – Default I/O Software Settings[1]**

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC3} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	468.67
2.5 V LVCMOS	35	2.5	–	267.48
1.8 V LVCMOS	35	1.8	–	138.32
1.5 V LVCMOS (JESD8-11)	35	1.5	–	96.13
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	88.92
LVPECL	–	3.3	19.54	166.52

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC3} is the static power (where applicable) measured on V_{CCI}.*
3. *P_{AC10} is the total dynamic power measured on V_{CC} and V_{CCI}.*

Power Consumption of Various Internal Resources

Table 3-10 • **Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices**

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)
A3P250		
P_{AC1}	Clock contribution of a Global Rib	100
P_{AC2}	Clock contribution of a Global Spine	10
P_{AC3}	Clock contribution of a VersaTile row	1.00
P_{AC4}	Clock contribution of a VersaTile used as a sequential module	0.00
P_{AC5}	First contribution of a VersaTile used as a sequential module	0.07
P_{AC6}	Second contribution of a VersaTile used as a sequential module	0.29
P_{AC7}	Contribution of a VersaTile used as a combinatorial Module	0.29
P_{AC8}	Average contribution of a routing net	0.70
P_{AC9}	Contribution of an I/O input pin (standard dependent)	See Table 3-7 on page 3-5.
P_{AC10}	Contribution of an I/O output pin. (standard dependent)	See Table 3-8 on page 3-5
P_{AC11}	Average contribution of a RAM block during a read operation	25.00
P_{AC12}	Average contribution of a RAM block during a write operation	30.00
P_{AC13}	First contribution of a PLL	4.00
P_{AC14}	Second Contribution of a PLL	2.00

Note: **For a different output load, drive strength, or slew rate, Actel recommends using the Actel Power spreadsheet calculator or SmartPower tool in Libero IDE software.*

Power Calculation Methodology

The section below describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Actel Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 3-11 on page 3-9
- Enable rates of output buffers—guidelines are provided for typical applications in Table 3-12 on page 3-9
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 3-12 on page 3-9. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

$P_{STAT} = P_{DC1} + N_{INPUTS} * P_{DC2} + N_{OUTPUTS} * P_{DC3}$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guideline are provided in Table 3-11 on page 3-9.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in Table 3-11 on page 3-9.

F_{CLK} is the global clock signal frequency.

If the number of spines and rows is not known, use the simplified formula below:

$P_{CLOCK} = (P_{AC1} + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

F_{CLK} is the global clock signal frequency.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + \alpha_1 * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-11 on page 3-9.

F_{CLK} is the global clock signal frequency.

Combinational Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha 1 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-11 on page 3-9.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-11 on page 3-9.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-11 on page 3-9.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-11 on page 3-9.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 3-12 on page 3-9.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 the RAM enable rate for write operations—guidelines are provided in Table 3-12 on page 3-9.

PLL/CCC Contribution—P_{PLL}

$P_{PLL} = P_{AC13} * F_{CLKIN} + \Sigma P_{AC14} * F_{CLKOUT}$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift-register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - The average toggle rate is = (100% + 50% + 25% + 12.5% +...0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 3-11 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 3-12 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

User I/O Characteristics

Timing Model

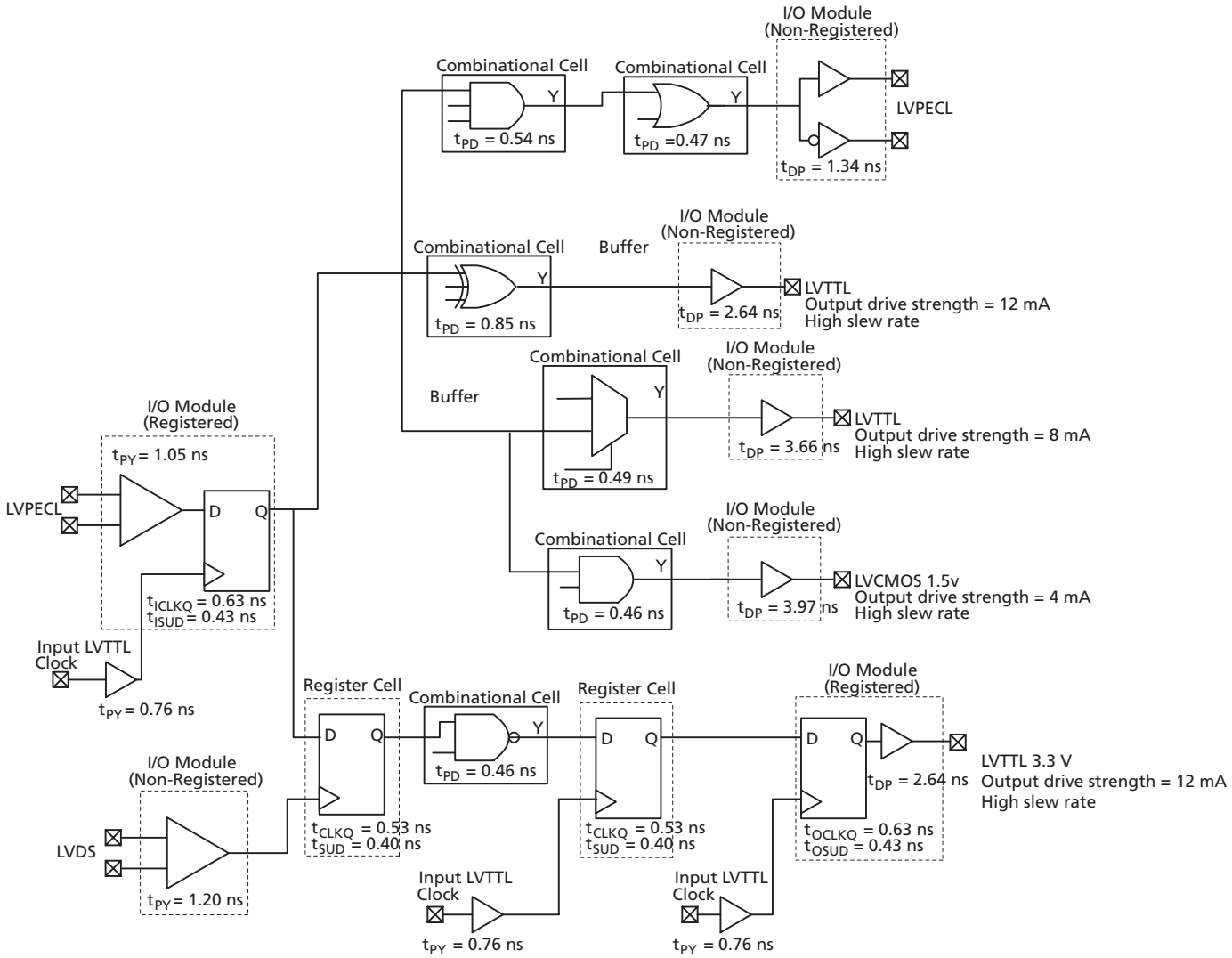
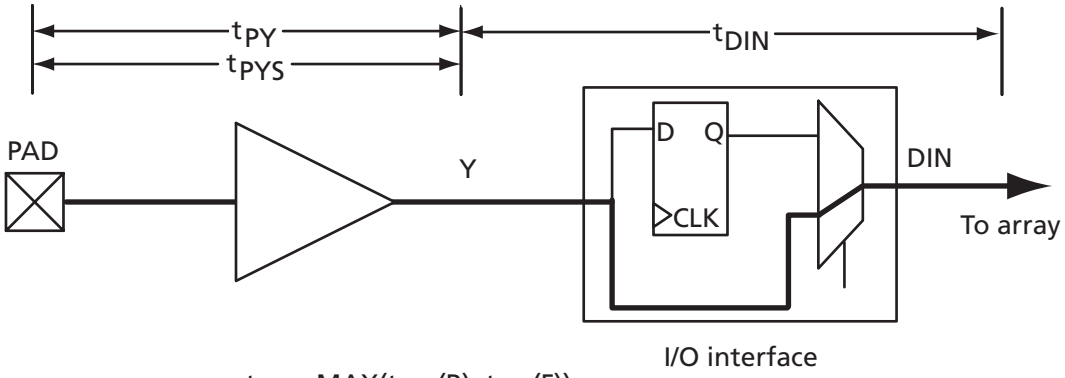


Figure 3-2 • **Timing Model**
Operating Conditions: –2 Speed, Commercial Temperature Range (T_J = 70°C), Worst Case V_{CC} =1.425 V



$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$

$t_{PYS} = MAX(t_{PYS}(R), t_{PYS}(F))$

$t_{DIN} = MAX(t_{DIN}(R), t_{DIN}(F))$

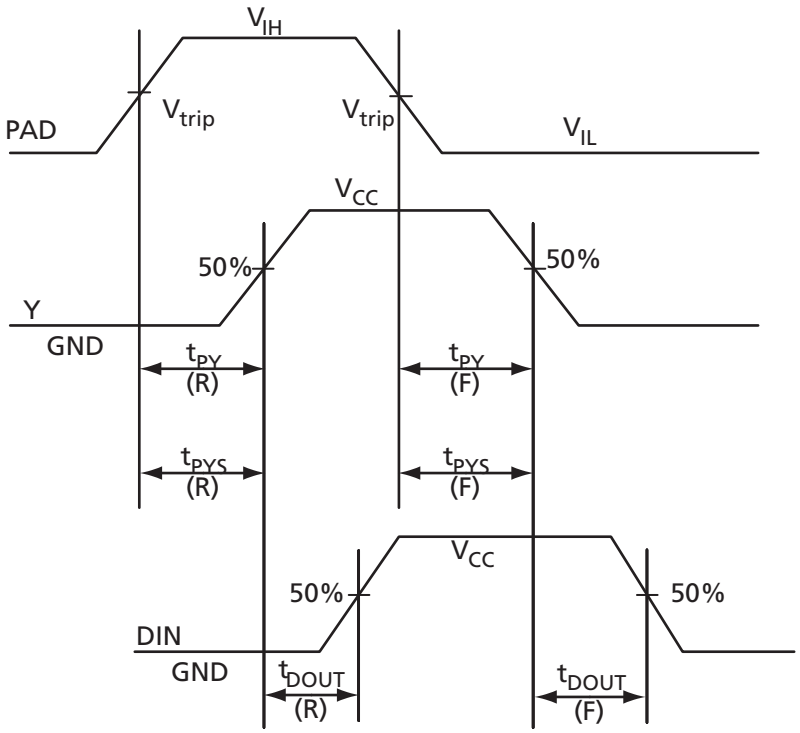


Figure 3-3 • **Input Buffer Timing Model and Delays (example)**

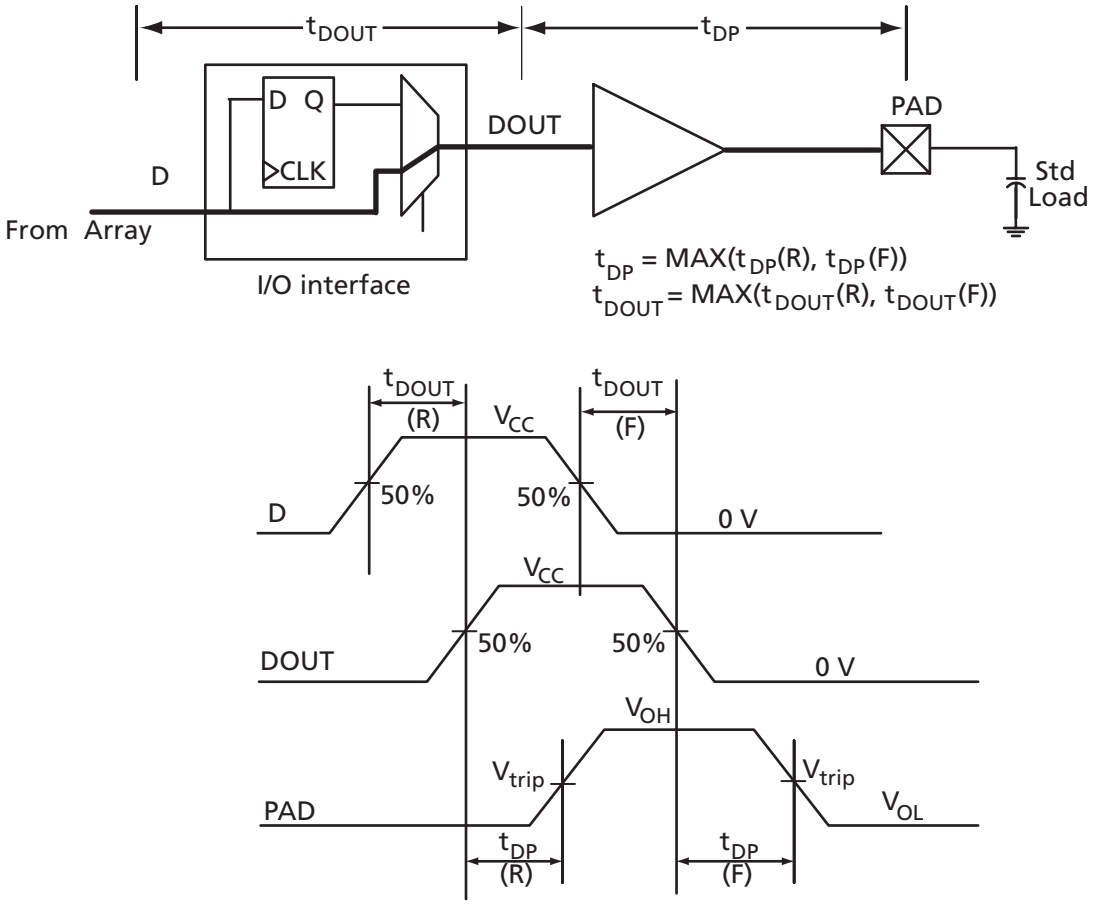


Figure 3-4 • **Output Buffer Model and Delays (example)**

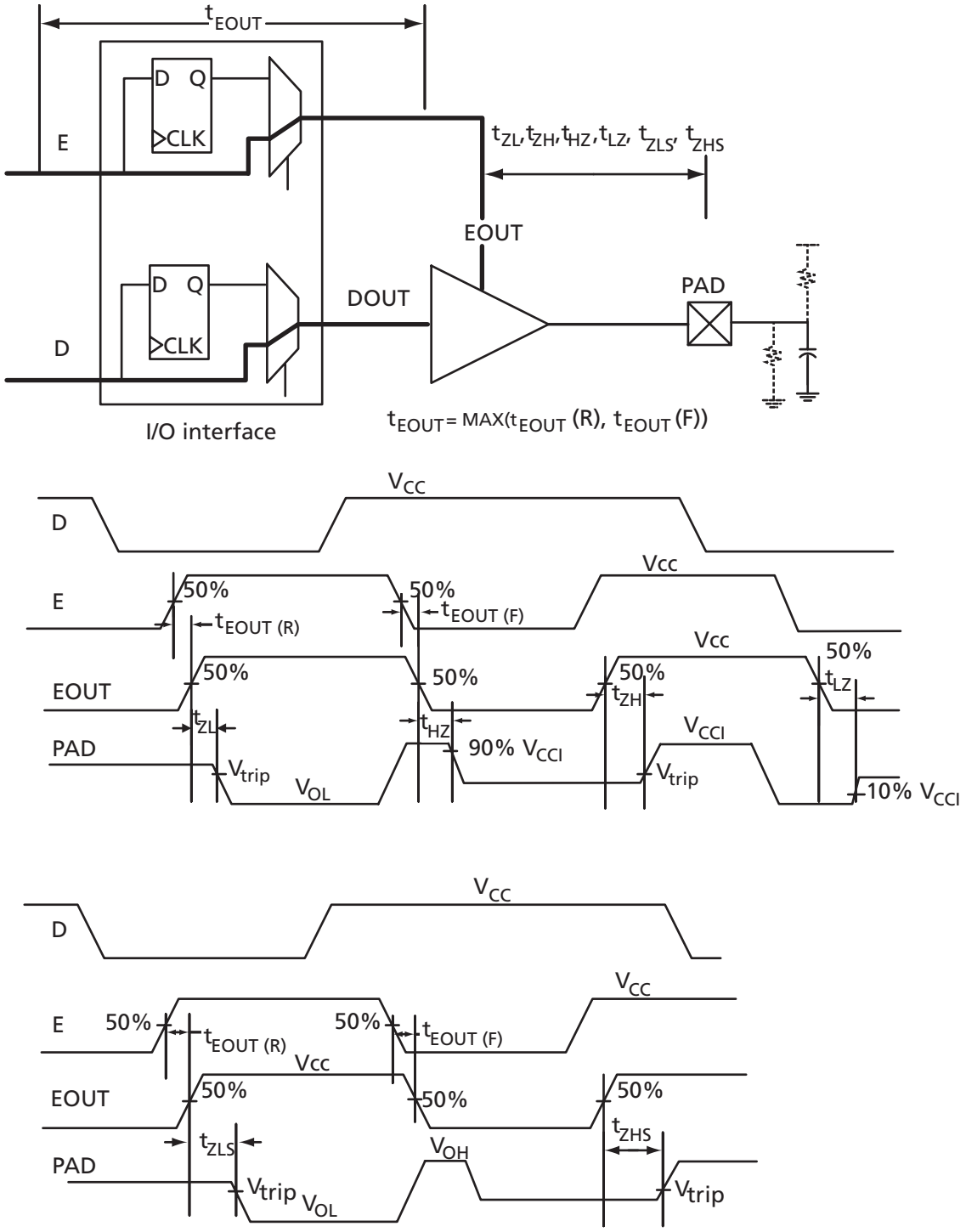


Figure 3-5 • **Tristate Output Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 3-13 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions**

I/O Standard	Drive Strength	Slew Rate	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	8	8
1.5 V LVCMOS	4 mA	High	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: *Currents are measured at 85°C junction temperature.*

Table 3-14 • **Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions**

DC I/O Standards	Commercial[1]		Industrial[2]	
	I_{IL}	I_{IH}	I_{IL}	I_{IH}
	µA	µA	µA	µA
3.3 V LVTTL /3.3V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15

Notes:

1. *Commercial range (0°C < T_J < 70°C)*
2. *Industrial range (–40°C < T_J < 85°C)*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 3-15 • **Summary of AC Measuring Points**

Standard	Measuring Trip Point (V_{trip})
3.3 V LVTTL / 3.3 V LVCMOS	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
3.3 V PCI	0.285 * V_{CCI} (RR)
	0.615 * V_{CCI} (FF)
3.3 V PCI-X	0.285 * V_{CCI} (RR)
	0.615 * V_{CCI} (FF)

Table 3-16 • **I/O AC Parameter Definitions**

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—high to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to high
t_{LZ}	Enable to Pad delay through the Output Buffer—low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to high
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to low

Table 3-17 • **Summary of I/O Timing Characteristics—Software Default Settings**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	tEOUT	t_{ZL}	tZH	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35 pF	-	0.45	2.64	0.03	0.76	0.32	2.69	2.11	2.40	2.67	4.36	3.78	ns
2.5 V LVCMOS	12 mA	High	35pF	-	0.45	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
1.8 V LVCMOS	8 mA	High	35pF	-	0.45	3.32	0.03	0.91	0.32	3.12	3.32	2.63	2.52	4.79	4.99	ns
1.5 V LVCMOS	4 mA	High	35pF	-	0.45	3.97	0.03	1.07	0.32	3.62	3.97	2.79	2.54	5.29	5.64	ns
3.3 V PCI	Per PCI spec	High	10pF	25 [2]	0.45	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.67	2.04	1.46	ns
3.3 V PCI-X	Per PCI-X spec	High	10pF	25 [2]	0.45	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.67	2.04	1.46	ns
LVDS	24 mA	High	-	-	0.45	1.36	0.03	1.20	-	-	-	-	-	-	-	ns
LVPECL	24 mA	High	-	-	0.45	1.34	0.03	1.05	-	-	-	-	-	-	-	ns

Notes:

1. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 3-10 on page 3-26 for connectivity. This resistor is not required during normal operation.*

Detailed I/O DC Characteristics

Table 3-18 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input Capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

Table 3-19 • **I/O Output Buffer Maximum Resistances[1]**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{OHspec}$

Table 3-20 • **I/O Weak Pull-Up/Pull-Down Resistances**
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

V_{CCI}	$R_{(WEAK\ PULL\text{-}UP)}$[1] ($\Omega$)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] ($\Omega$)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (V_{OLspec}) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$

Table 3-21 • **I/O Short Currents I_{OSH}/I_{OSL}**

	Drive Strength	I_{OSH} (mA)*	I_{OSL} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	103	109
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	8 mA	35	44
1.5 V LCMOS	2 mA	13	16
	4 mA	25	33

Note: **T_J = 100°C*

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 3-22 • **Short Current Event Duration before Failure**

Temperature	Time Before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months

Table 3-23 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (Min.)	Input Rise/fall Time (Max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns (or more *)	20 years (110°C)
LVDS/LVPECL	No requirement	10 ns (or more *)	10 years (100°C)

Note: **This limitation is related only to the noise induced into input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Single Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor-Transistor Logic (LVTTL) is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 3-24 • **Minimum and Maximum DC Input and Output Levels**

3.3 V LVTTL/ 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min,V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	109	103	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

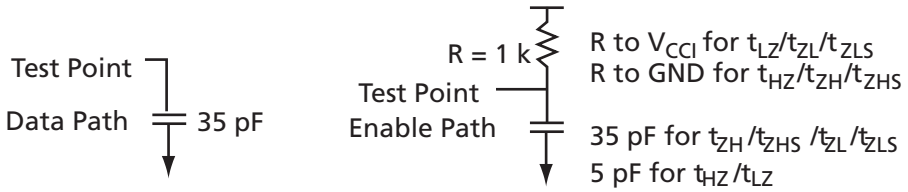


Figure 3-6 • **AC Loading**

Table 3-25 • **AC Waveforms, Measuring Points and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	35

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-14 for a complete table of trip points.*

Timing Characteristics

Table 3-26 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.72	12.32	0.05	1.22	0.51	12.55	10.69	3.18	2.95	15.23	13.37	ns
	Std.	0.60	10.26	0.04	1.02	0.43	10.45	8.90	2.64	2.46	12.68	11.13	ns
	–1	0.51	8.72	0.04	0.86	0.36	8.88	7.57	2.25	2.09	10.79	9.47	ns
	–2	0.45	7.66	0.03	0.76	0.32	7.80	6.64	1.98	1.83	9.47	8.31	ns
8 mA	–F	0.72	8.74	0.05	1.22	0.51	8.90	7.55	3.58	3.65	11.59	10.23	ns
	Std.	0.60	7.27	0.04	1.02	0.43	7.41	6.28	2.98	3.04	9.64	8.52	ns
	–1	0.51	6.19	0.04	0.86	0.36	6.30	5.34	2.54	2.59	8.20	7.25	ns
	–2	0.45	5.43	0.03	0.76	0.32	5.53	4.69	2.23	2.27	7.20	6.36	ns
12 mA	–F	0.72	6.70	0.05	1.22	0.51	6.83	5.85	3.85	4.10	9.51	8.54	ns
	Std.	0.60	5.58	0.04	1.02	0.43	5.68	4.87	3.21	3.42	7.92	7.11	ns
	–1	0.51	4.75	0.04	0.86	0.36	4.83	4.14	2.73	2.90	6.74	6.04	ns
	–2	0.45	4.17	0.03	0.76	0.32	4.24	3.64	2.39	2.55	5.91	5.31	ns
16 mA	–F	0.72	6.70	0.05	1.22	0.51	6.83	5.85	3.85	4.10	9.51	8.54	ns
	Std.	0.60	5.58	0.04	1.02	0.43	5.68	4.87	3.21	3.42	7.92	7.11	ns
	–1	0.51	4.75	0.04	0.86	0.36	4.83	4.14	2.73	2.90	6.74	6.04	ns
	–2	0.45	4.17	0.03	0.76	0.32	4.24	3.64	2.39	2.55	5.91	5.31	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-27 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.72	9.20	0.05	1.22	0.51	9.37	7.91	3.18	3.14	12.05	10.60	ns
	Std.	0.60	7.66	0.04	1.02	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	–1	0.51	6.51	0.04	0.86	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	–2	0.45	5.72	0.03	0.76	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
8 mA	–F	0.72	5.89	0.05	1.22	0.51	6.00	4.89	3.59	3.85	8.69	7.57	ns
	Std.	0.60	4.91	0.04	1.02	0.43	5.00	4.07	2.98	3.20	7.23	6.30	ns
	–1	0.51	4.17	0.04	0.86	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	–2	0.45	3.66	0.03	0.76	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
12 mA	–F	0.72	4.24	0.05	1.22	0.51	4.32	3.39	3.86	4.30	7.01	6.08	ns
	Std.	0.60	3.53	0.04	1.02	0.43	3.60	2.82	3.21	3.58	5.83	5.06	ns
	–1	0.51	3.00	0.04	0.86	0.36	3.06	2.40	2.73	3.05	4.96	4.30	ns
	–2	0.45	2.64	0.03	0.76	0.32	2.69	2.11	2.40	2.67	4.36	3.78	ns
16 mA	–F	0.72	4.24	0.05	1.22	0.51	4.32	3.39	3.86	4.30	7.01	6.08	ns
	Std.	0.60	3.53	0.04	1.02	0.43	3.60	2.82	3.21	3.58	5.83	5.06	ns
	–1	0.51	3.00	0.04	0.86	0.36	3.06	2.40	2.73	3.05	4.96	4.30	ns
	–2	0.45	2.64	0.03	0.76	0.32	2.69	2.11	2.40	2.67	4.36	3.78	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 2.5 V applications. It uses a 5-V-tolerant input buffer and push-pull output buffer.

Table 3-28 • **Minimum and Maximum DC Input and Output Levels**

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

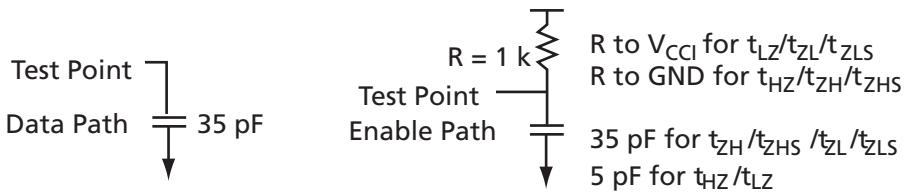


Figure 3-7 • **AC Loading**

Table 3-29 • **AC Waveforms, Measuring Points and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	2.5	1.2	35

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-14 for a complete table of trip points.*

Timing Characteristics

Table 3-30 • **2.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.72	13.69	0.05	1.57	0.51	13.47	13.69	3.22	2.65	16.16	16.38	ns
	Std.	0.60	11.40	0.04	1.31	0.43	11.22	11.40	2.68	2.20	13.45	13.63	ns
	–1	0.51	9.69	0.04	1.11	0.36	9.54	9.69	2.28	1.88	11.44	11.60	ns
	–2	0.45	8.51	0.03	0.98	0.32	8.38	8.51	2.00	1.65	10.05	10.18	ns
8 mA	–F	0.72	9.56	0.05	1.57	0.51	9.74	9.39	3.66	3.47	12.43	12.07	ns
	Std.	0.60	7.96	0.04	1.31	0.43	8.11	7.81	3.05	2.89	10.34	10.05	ns
	–1	0.51	6.77	0.04	1.11	0.36	6.90	6.65	2.59	2.46	8.80	8.55	ns
	–2	0.45	5.94	0.03	0.98	0.32	6.05	5.83	2.28	2.16	7.72	7.50	ns
12 mA	–F	0.72	7.42	0.05	1.57	0.51	7.56	7.11	3.97	3.99	10.25	9.79	ns
	Std.	0.60	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	–1	0.51	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.25	6.94	ns
	–2	0.45	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-31 • **2.5 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.72	10.41	0.05	1.57	0.51	9.41	10.41	3.21	2.77	12.09	13.09	ns
	Std.	0.60	8.66	0.04	1.31	0.43	7.83	8.66	2.68	2.30	10.07	10.90	ns
	–1	0.51	7.37	0.04	1.11	0.36	6.66	7.37	2.28	1.96	8.56	9.27	ns
	–2	0.45	6.47	0.03	0.98	0.32	5.85	6.47	2.00	1.72	7.52	8.14	ns
8 mA	–F	0.72	6.21	0.05	1.57	0.51	6.05	6.21	3.66	3.60	8.73	8.89	ns
	Std.	0.60	5.17	0.04	1.31	0.43	5.04	5.17	3.05	3.00	7.27	7.40	ns
	–1	0.51	4.39	0.04	1.11	0.36	4.28	4.39	2.59	2.55	6.19	6.30	ns
	–2	0.45	3.86	0.03	0.98	0.32	3.76	3.86	2.28	2.24	5.43	5.53	ns
12 mA	–F	0.72	4.28	0.05	1.57	0.51	4.36	4.12	3.97	4.13	7.04	6.81	ns
	Std.	0.60	3.56	0.04	1.31	0.43	3.62	3.43	3.30	3.44	5.86	5.67	ns
	–1	0.51	3.03	0.04	1.11	0.36	3.08	2.92	2.81	2.92	4.99	4.82	ns
	–2	0.45	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.8 V applications. It uses 1.8 V input buffer and push-pull output buffer.

Table 3-32 • **Minimum and Maximum DC Input and Output Levels**

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	4	4	22	17	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	8	8	44	35	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

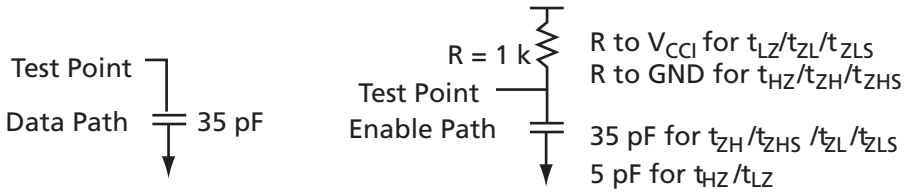


Figure 3-8 • **AC Loading**

Table 3-33 • **AC Waveforms, Measuring Points and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.8	0.9	35

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-14 for a complete table of trip points.*

Timing Characteristics

Table 3-34 • **1.8 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.7 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.72	14.25	0.05	1.46	0.51	10.97	14.25	3.33	1.99	13.66	16.94	ns
	Std.	0.60	11.86	0.04	1.22	0.43	9.13	11.86	2.77	1.66	11.37	14.10	ns
	–1	0.51	10.09	0.04	1.03	0.36	7.77	10.09	2.36	1.41	9.67	11.99	ns
	–2	0.45	8.86	0.03	0.91	0.32	6.82	8.86	2.07	1.24	8.49	10.53	ns
4 mA	–F	0.72	8.31	0.05	1.46	0.51	7.04	8.31	3.87	3.41	9.73	10.99	ns
	Std.	0.60	6.91	0.04	1.22	0.43	5.86	6.91	3.22	2.84	8.10	9.15	ns
	–1	0.51	5.88	0.04	1.03	0.36	4.99	5.88	2.74	2.41	6.89	7.78	ns
	–2	0.45	5.16	0.03	0.91	0.32	4.38	5.16	2.40	2.12	6.05	6.83	ns
6 mA	–F	0.72	5.34	0.05	1.46	0.51	5.02	5.34	4.24	4.06	7.71	8.03	ns
	Std.	0.60	4.45	0.04	1.22	0.43	4.18	4.45	3.53	3.38	6.42	6.68	ns
	–1	0.51	3.78	0.04	1.03	0.36	3.56	3.78	3.00	2.88	5.46	5.68	ns
	–2	0.45	3.32	0.03	0.91	0.32	3.12	3.32	2.63	2.52	4.79	4.99	ns
8mA	–F	0.72	14.25	0.05	1.46	0.51	10.97	14.25	3.33	1.99	13.66	16.94	ns
	Std.	0.60	11.86	0.04	1.22	0.43	9.13	11.86	2.77	1.66	11.37	14.10	ns
	–1	0.51	10.09	0.04	1.03	0.36	7.77	10.09	2.36	1.41	9.67	11.99	ns
	–2	0.45	8.86	0.03	0.91	0.32	6.82	8.86	2.07	1.24	8.49	10.53	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-35 • **1.8 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.7 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.72	18.66	0.05	1.46	0.51	16.95	18.66	3.34	1.92	19.64	21.34	ns
	Std.	0.60	15.53	0.04	1.22	0.43	14.11	15.53	2.78	1.60	16.35	17.77	ns
	–1	0.51	13.21	0.04	1.03	0.36	12.01	13.21	2.36	1.36	13.91	15.11	ns
	–2	0.45	11.60	0.03	0.91	0.32	10.54	11.60	2.07	1.19	12.21	13.27	ns
4 mA	–F	0.72	12.58	0.05	1.46	0.51	12.51	12.58	3.88	3.28	15.19	15.27	ns
	Std.	0.60	10.47	0.04	1.22	0.43	10.41	10.47	3.23	2.73	12.64	12.71	ns
	–1	0.51	8.91	0.04	1.03	0.36	8.86	8.91	2.75	2.33	10.76	10.81	ns
	–2	0.45	7.82	0.03	0.91	0.32	7.77	7.82	2.41	2.04	9.44	9.49	ns
6 mA	–F	0.72	9.67	0.05	1.46	0.51	9.85	9.42	4.25	3.93	12.53	12.11	ns
	Std.	0.60	8.05	0.04	1.22	0.43	8.20	7.84	3.54	3.27	10.43	10.08	ns
	–1	0.51	6.85	0.04	1.03	0.36	6.97	6.67	3.01	2.78	8.88	8.57	ns
	–2	0.45	6.01	0.03	0.91	0.32	6.12	5.86	2.64	2.44	7.79	7.53	ns
8 mA	–F	0.72	18.66	0.05	1.46	0.51	16.95	18.66	3.34	1.92	19.64	21.34	ns
	Std.	0.60	15.53	0.04	1.22	0.43	14.11	15.53	2.78	1.60	16.35	17.77	ns
	–1	0.51	13.21	0.04	1.03	0.36	12.01	13.21	2.36	1.36	13.91	15.11	ns
	–2	0.45	11.60	0.03	0.91	0.32	10.54	11.60	2.07	1.19	12.21	13.27	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

1.5 V LVCMOS (JESD8-11)

Low-voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.5V applications. It uses 1.5 V input buffer and push-pull output buffer.

Table 3-36 • **Minimum and Maximum DC Input and Output Levels**

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
2 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	16	13	10	10
4 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4	33	25	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

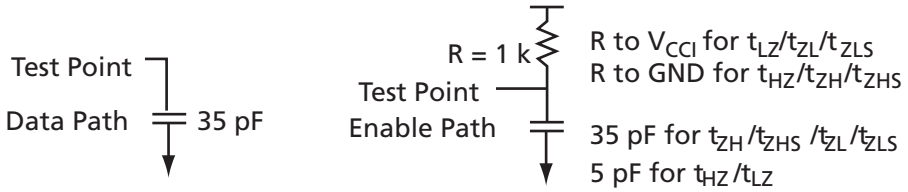


Figure 3-9 • **AC Loading**

Table 3-37 • **AC Waveforms, Measuring Points and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	35

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-14 for a complete table of trip points.*

Timing Characteristics

Table 3-38 • **1.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.4 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.72	15.36	0.05	1.73	0.51	15.39	15.36	4.08	3.18	18.07	18.04	ns
	Std.	0.60	12.78	0.04	1.44	0.43	12.81	12.78	3.40	2.64	15.04	15.02	ns
	–1	0.51	10.87	0.04	1.22	0.36	10.90	10.87	2.89	2.25	12.80	12.78	ns
	–2	0.45	9.55	0.03	1.07	0.32	9.56	9.55	2.54	1.97	11.23	11.21	ns
4 mA	–F	0.72	12.02	0.05	1.73	0.51	12.25	11.47	4.50	3.93	14.93	14.15	ns
	Std.	0.60	10.01	0.04	1.44	0.43	10.19	9.55	3.75	3.27	12.43	11.78	ns
	–1	0.51	8.51	0.04	1.22	0.36	8.67	8.12	3.19	2.78	10.57	10.02	ns
	–2	0.45	7.47	0.03	1.07	0.32	7.61	7.13	2.80	2.44	9.28	8.80	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-39 • **1.5 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.4 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.72	10.04	0.05	1.73	0.51	8.20	10.04	4.07	3.32	10.88	12.73	ns
	Std.	0.60	8.36	0.04	1.44	0.43	6.82	8.36	3.39	2.77	9.06	10.60	ns
	–1	0.51	7.11	0.04	1.22	0.36	5.80	7.11	2.88	2.35	7.71	9.02	ns
	–2	0.45	6.24	0.03	1.07	0.32	5.09	6.24	2.53	2.06	6.76	7.91	ns
4 mA	–F	0.72	6.38	0.05	1.73	0.51	5.83	6.38	4.49	4.09	8.51	9.07	ns
	Std.	0.60	5.31	0.04	1.44	0.43	4.85	5.31	3.74	3.40	7.09	7.55	ns
	–1	0.51	4.52	0.04	1.22	0.36	4.12	4.52	3.18	2.89	6.03	6.42	ns
	–2	0.45	3.97	0.03	1.07	0.32	3.62	3.97	2.79	2.54	5.29	5.64	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 3-40 • **Minimum and Maximum DC Input and Output Levels**

3.3 V PCI/PCI-X	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
Per PCI specification	Per PCI curves										10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the data path; Actel loadings for enable path characterization are described in Figure 3-10.

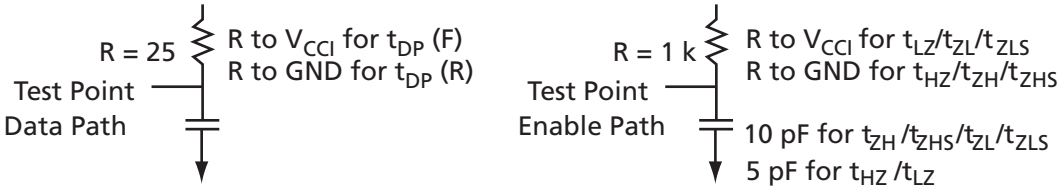


Figure 3-10 • **AC Loading**

AC loading are defined per PCI/PCI-X specifications for the data path; Actel loading for tristate is described in Table 3-41.

Table 3-41 • **AC Waveforms, Measuring Points and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	0.285 * V_{CCI} for $t_{DP(R)}$ 0.615 * V_{CCI} for $t_{DP(F)}$	10

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-14 for a complete table of trip points.*

Timing Characteristics

Table 3-42 • **3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.72	3.22	0.05	1.04	0.51	3.28	2.34	3.86	4.3	3.28	2.34	ns
Std.	0.60	2.68	0.04	0.86	0.43	2.73	1.95	3.21	3.58	2.73	1.95	ns
–1	0.51	2.28	0.04	0.73	0.36	2.32	1.66	2.73	3.05	2.32	1.66	ns
–2	0.45	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.67	2.04	1.46	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with these standards.

LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit is carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 3-11. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation, because the output standard specifications are different.

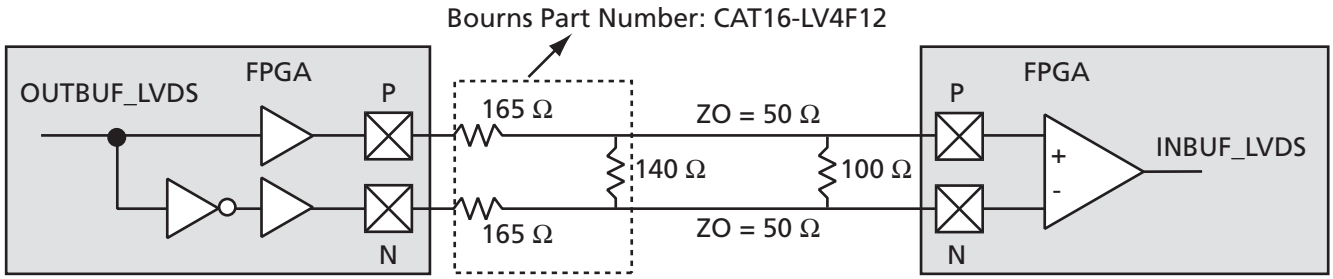


Figure 3-11 • **LVDS Circuit Diagram and Board-Level Implementation**

Table 3-43 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
V_{CCI}	Supply Voltage	2.375	2.5	2.625	V
V_{OL}	Output Low Voltage	0.9	1.075	1.25	V
V_{OH}	Output High Voltage	1.25	1.425	1.6	V
V_I	Input Voltage	0		2.925	V
V_{ODIFF}	Differential Output Voltage	250	350	450	mV
V_{OCM}	Output Common Mode Voltage	1.125	1.25	1.375	V
V_{ICM}	Input Common Mode Voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input Differential Voltage	100	350		mV

Notes:

1. *± 5%*
2. *Differential input voltage = ± 350 mV.*

Table 3-44 • **AC Waveforms, Measuring Points and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-14 for a complete table of trip points.*

Timing Characteristics

Table 3-45 • **LVDS**

Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
–F	0.72	2.2	0.05	1.92	ns
Std.	0.60	1.83	0.04	1.60	ns
–1	0.51	1.55	0.04	1.36	ns
–2	0.45	1.36	0.03	1.20	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit is carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 3-12. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation, because the output standard specifications are different.

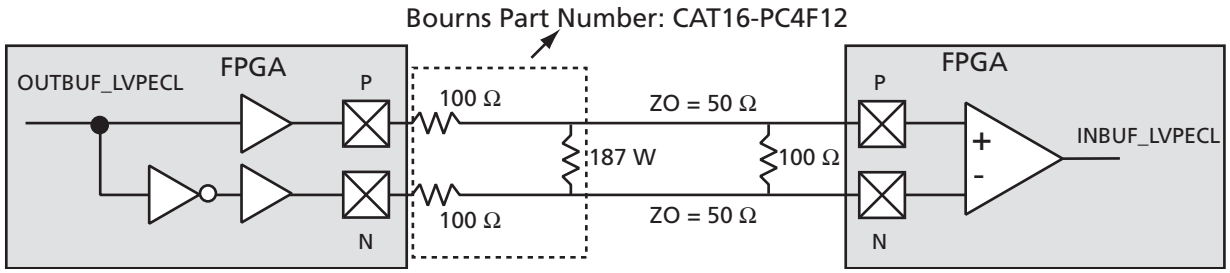


Figure 3-12 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 3-46 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{CCI}	Supply Voltage	3.0		3.3		3.6		V
V_{OL}	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{OH}	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{IL}, V_{IH}	Input Low, Input High voltages	0	3.3	0	3.6	0	3.9	V
V_{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V_{OCM}	Output Common Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V_{ICM}	Input Common Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V_{IDIFF}	Input Differential Voltage	300		300		300		mV

Table 3-47 • **AC Waveforms, Measuring Points and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-14 for a complete table of trip points.*

Timing Characteristics

Table 3-48 • **LVPECL**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
–F	0.72	2.16	0.05	1.69	ns
Std.	0.60	1.80	0.04	1.40	ns
–1	0.51	1.53	0.04	1.19	ns
–2	0.45	1.34	0.03	1.05	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

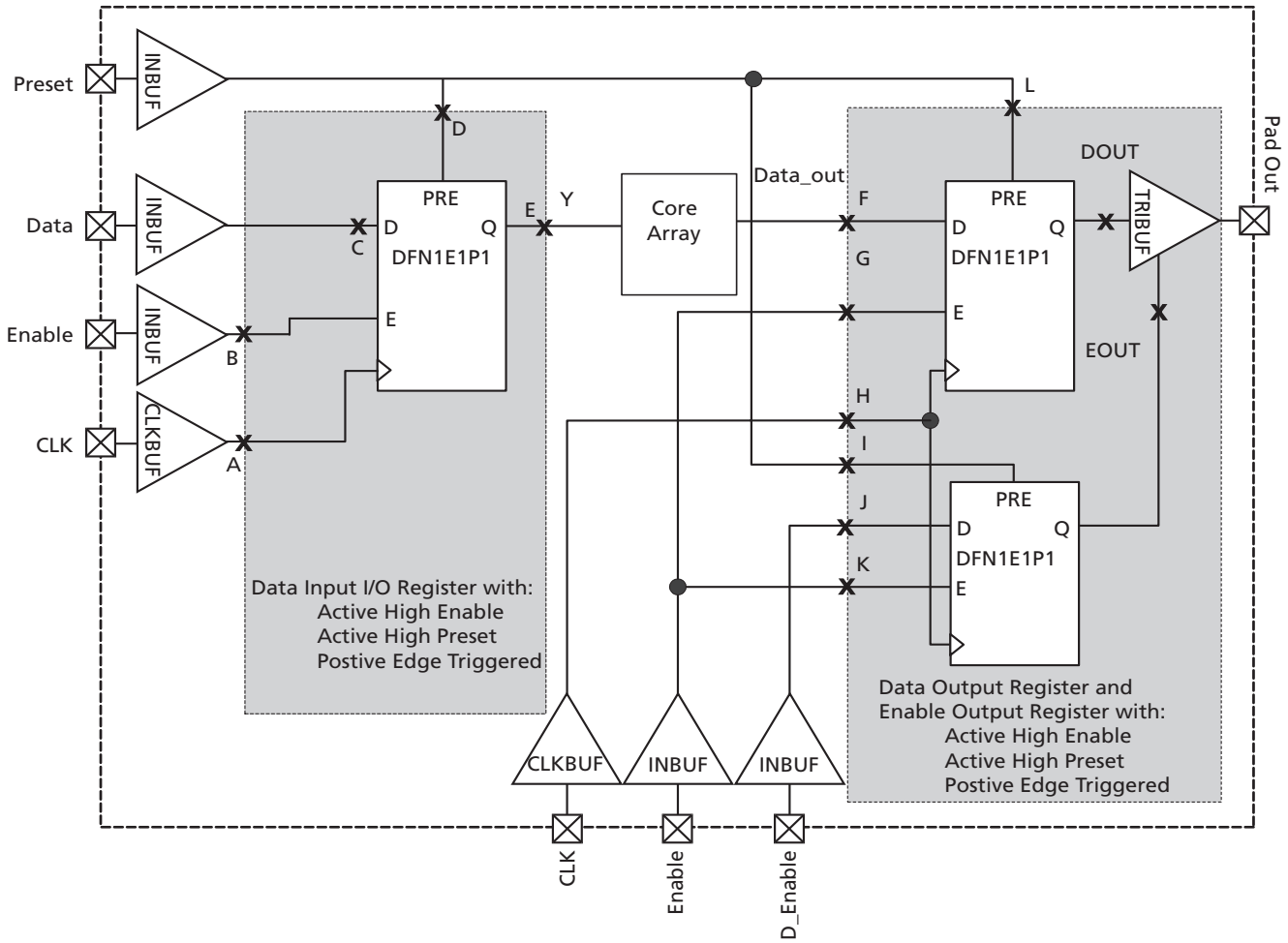


Figure 3-13 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Table 3-49 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup time for the Output Data Register	F, H
t_{OHD}	Data Hold time for the Output Data Register	F, H
t_{OSUE}	Enable Setup time for the Output Data Register	G, H
t_{OHE}	Enable Hold time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset removal time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup time for the Output Enable Register	J, H
t_{OEHD}	Data Hold time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup time for the Input Data Register	C, A
t_{IHD}	Data Hold time for the Input Data Register	C, A
t_{ISUE}	Enable Setup time for the Input Data Register	B, A
t_{IHE}	Enable Hold time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery time for the Input Data Register	D, A

Note: **See Figure 3-13 on page 3-30 for more information.*

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

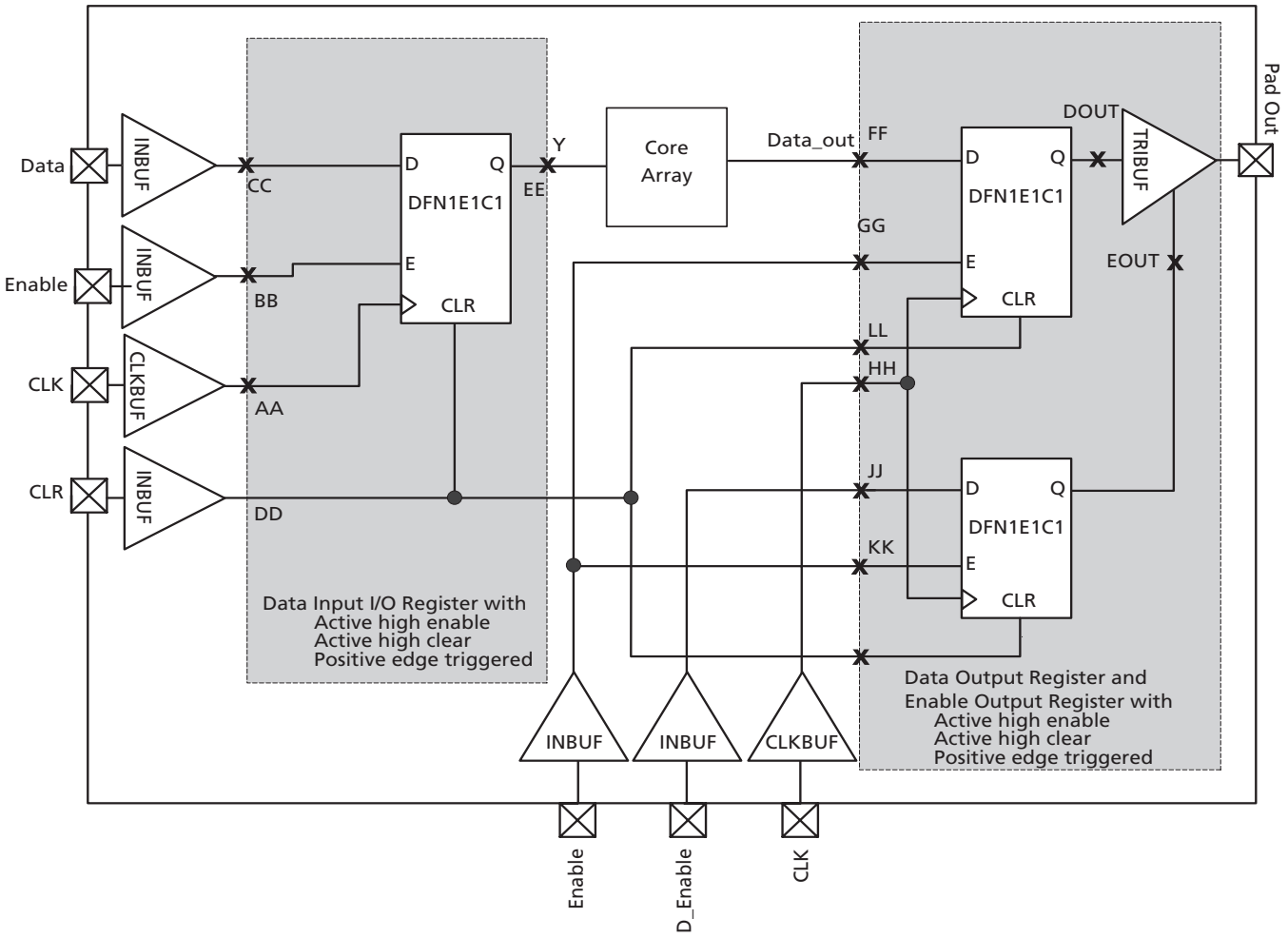


Figure 3-14 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Table 3-50 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)*
tOCLKQ	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup time for the Output Data Register	FF, HH
t_{OHD}	Data Hold time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup time for the Input Data Register	CC, AA
t_{IHD}	Data Hold time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery time for the Input Data Register	DD, AA

Note: **See Figure 3-14 on page 3-32 for more information.*

Input Register

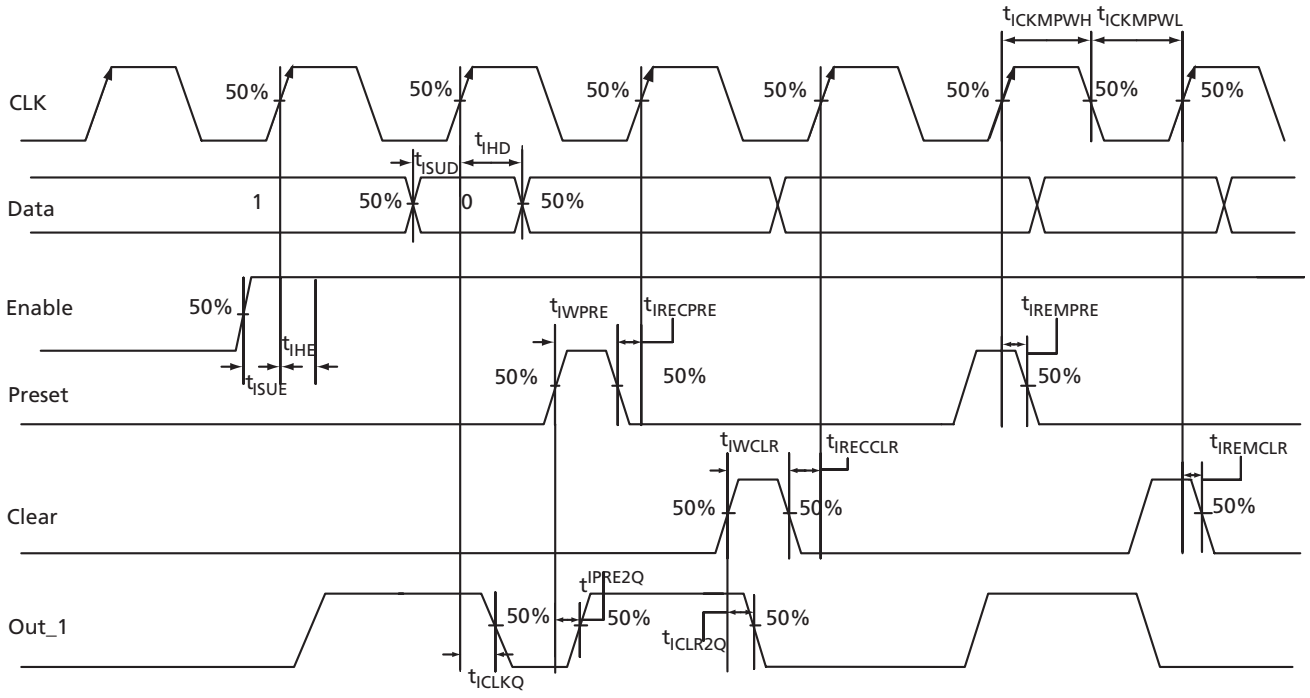


Figure 3-15 • **Input Register Timing Diagram**

Timing Characteristics

Table 3-51 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.63	0.71	0.84	1.01	ns
t_{ISUD}	Data Setup time for the Input Data Register	0.43	0.49	0.57	0.69	ns
t_{IHD}	Data Hold time for the Input Data Register	0.00	0.00	0.00	0.00	ns
t_{ISUE}	Enable Setup time for the Input Data Register	0.43	0.49	0.57	0.69	ns
t_{IHE}	Enable Hold time for the Input Data Register	0.00	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.57	0.65	0.76	1.01	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.51	0.60	0.72	ns
$t_{IREMCLR}$	Asynchronous Clear Removal time for the Input Data Register	0.00	0.00	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery time for the Input Data Register	0.10	0.10	0.10	0.10	ns
$t_{IREMPRE}$	Asynchronous Preset Removal time for the Input Data Register	0.00	0.00	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery time for the Input Data Register	0.10	0.10	0.10	0.10	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.25	0.28	0.33	0.40	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.25	0.28	0.33	0.40	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.41	0.48	0.58	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.41	0.46	0.54	0.65	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Output Register

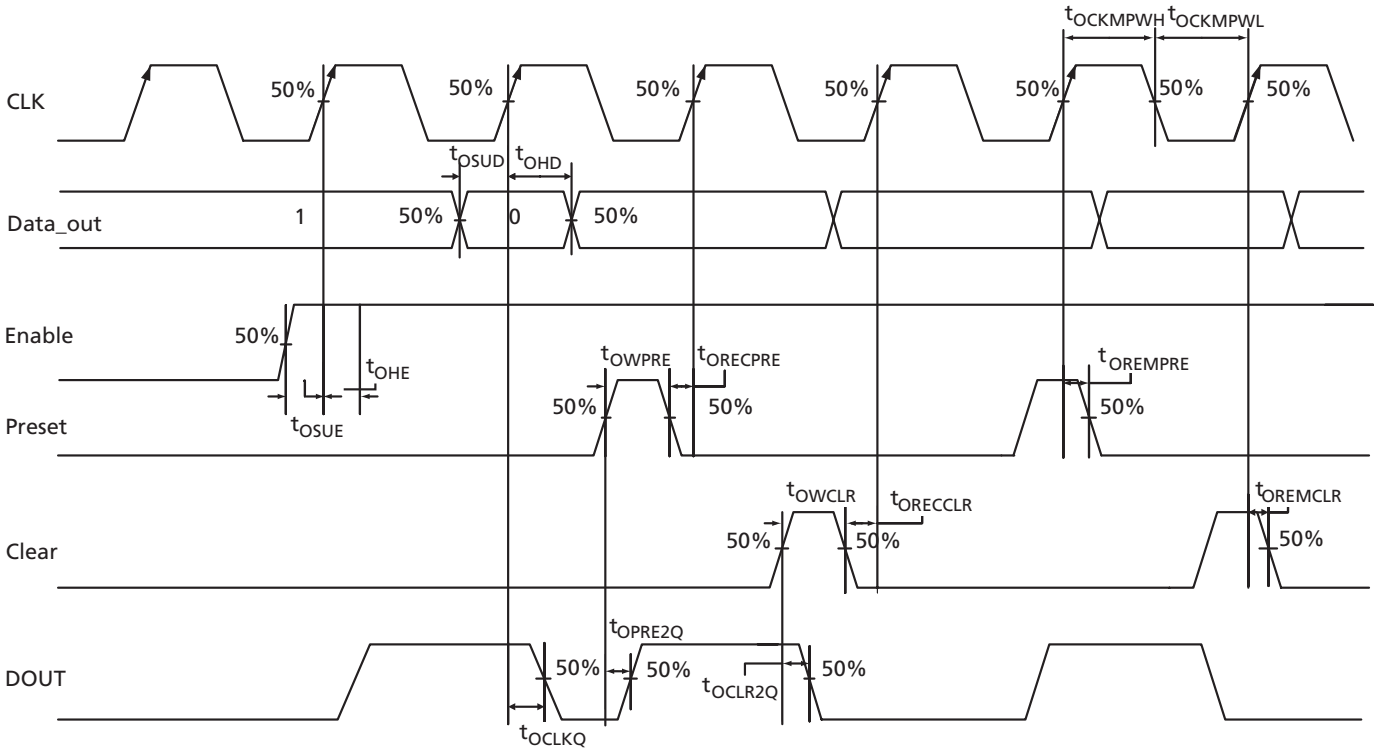


Figure 3-16 • **Output Register Timing Diagram**

Timing Characteristics

Table 3-52 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.63	0.71	0.84	1.01	ns
t_{OSUD}	Data Setup time for the Output Data Register	0.43	0.49	0.57	0.69	ns
t_{OHD}	Data Hold time for the Output Data Register	0.00	0.00	0.00	0.00	ns
t_{OSUE}	Enable Setup time for the Output Data Register	0.43	0.49	0.57	0.69	ns
t_{OHE}	Enable Hold time for the Output Data Register	0.00	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.57	0.65	0.76	1.01	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.45	0.51	0.60	0.72	ns
$t_{OREMCLR}$	Asynchronous Clear Removal time for the Output Data Register	0.00	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery time for the Output Data Register	0.24	0.27	0.32	0.38	ns
$t_{OREMPRE}$	Asynchronous Preset Removal time for the Output Data Register	0.00	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery time for the Output Data Register	0.24	0.27	0.32	0.38	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.26	0.29	0.34	0.41	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.26	0.29	0.34	0.41	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.38	0.43	0.51	0.61	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.43	0.49	0.57	0.69	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Output Enable Register

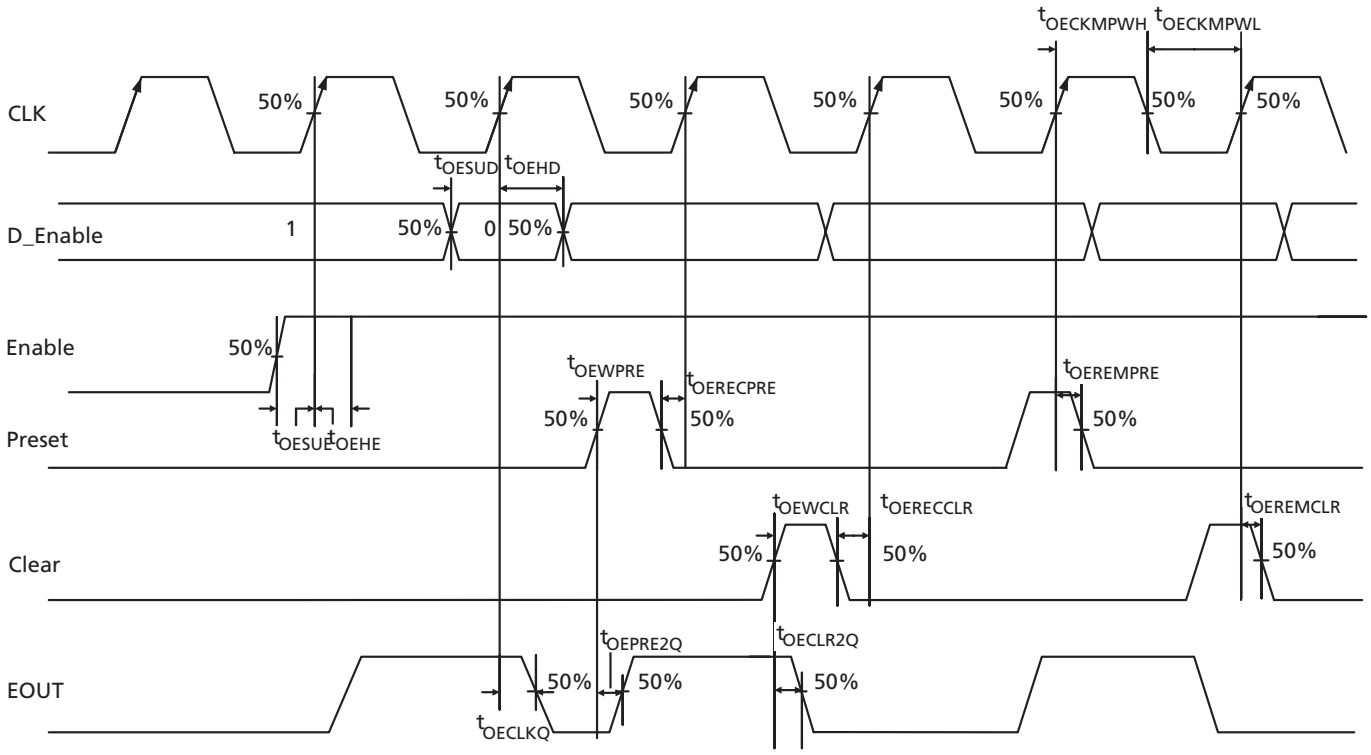


Figure 3-17 • **Output Enable Register Timing Diagram**

Timing Characteristics

Table 3-53 • **Output Enable Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.63	0.71	0.84	1.01	ns
t_{OESUD}	Data Setup time for the Output Enable Register	0.43	0.49	0.57	0.69	ns
t_{OEHD}	Data Hold time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
t_{OESUE}	Enable Setup time for the Output Enable Register	0.43	0.49	0.57	0.69	ns
t_{OEHE}	Enable Hold time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.57	0.65	0.76	1.01	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.45	0.51	0.60	0.72	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery time for the Output Enable Register	0.24	0.27	0.32	0.38	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery time for the Output Enable Register	0.24	0.27	0.32	0.38	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.26	0.29	0.34	0.41	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.26	0.29	0.34	0.41	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.38	0.43	0.51	0.61	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.43	0.49	0.57	0.69	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

DDR Module Specifications

Input DDR Module

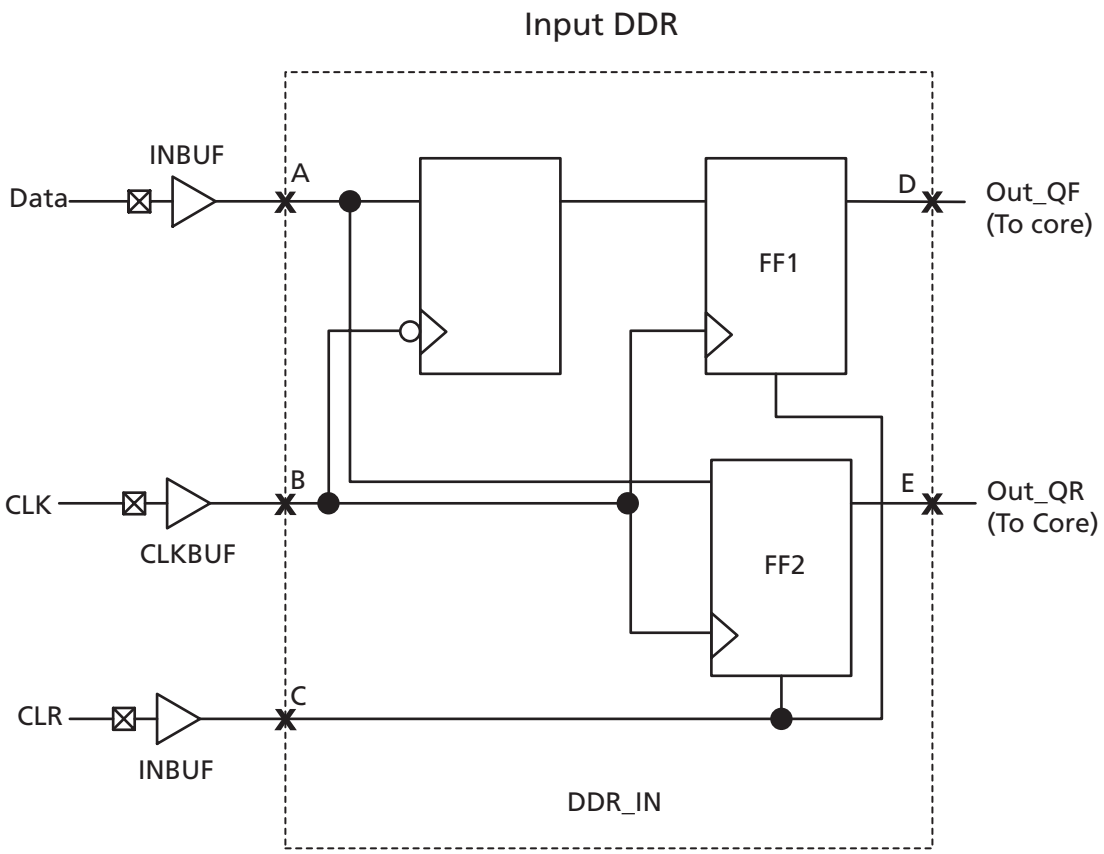


Figure 3-18 • **Input DDR Timing Model**

Table 3-54 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup time of DDR input	A, B
t_{DDRIHD}	Data Hold time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

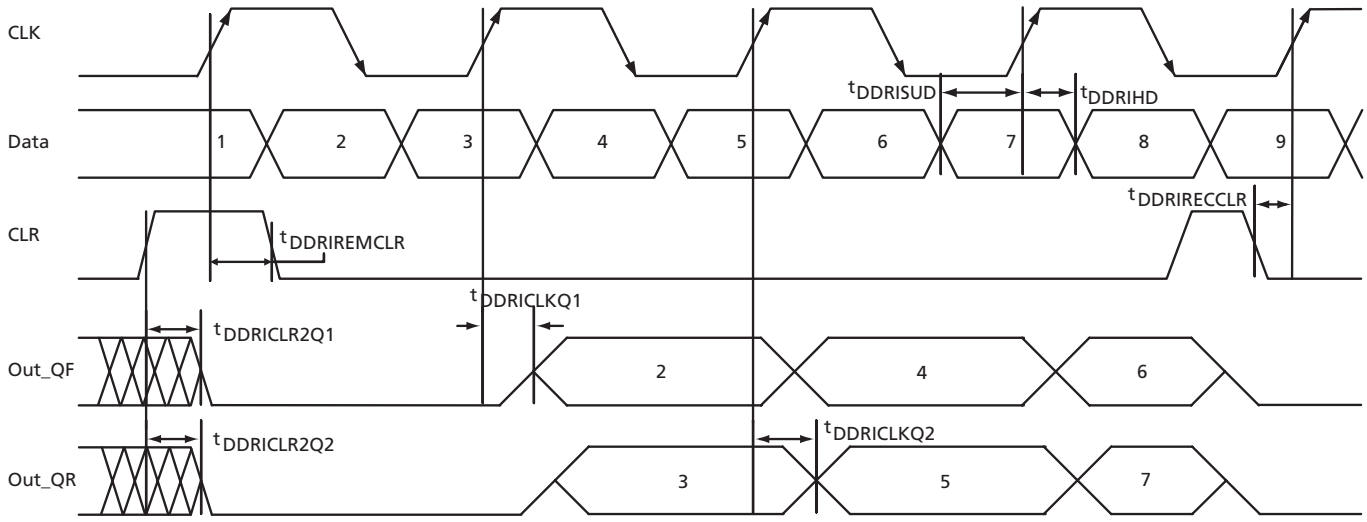


Table 3-55 • **Input DDR Timing Diagram**

Timing Characteristics

Table 3-56 • **Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.63	0.71	0.84	1.01	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.63	0.71	0.84	0.91	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.43	0.49	0.57	0.86	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear to out Out_QR for Input DDR	0.57	0.65	0.76	0.91	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear to out Out_QF for Input DDR	0.57	0.65	0.76	0.91	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal time for Input DDR	0.00	0.00	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery time for Input DDR	0.10	0.10	0.10	0.10	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR					ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR					ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR					ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR					MHz

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Output DDR Module

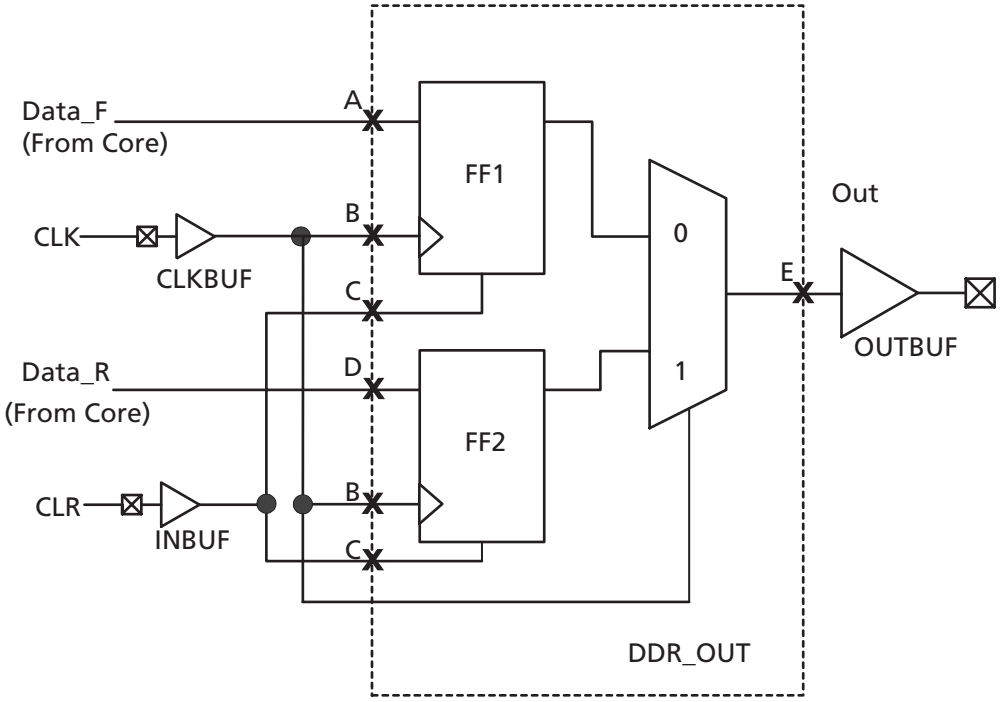


Figure 3-19 • **Output DDR Timing Model**

Table 3-57 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
tDDRORECCLR	Clear Recovery	C, B
tDDROSUD1	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

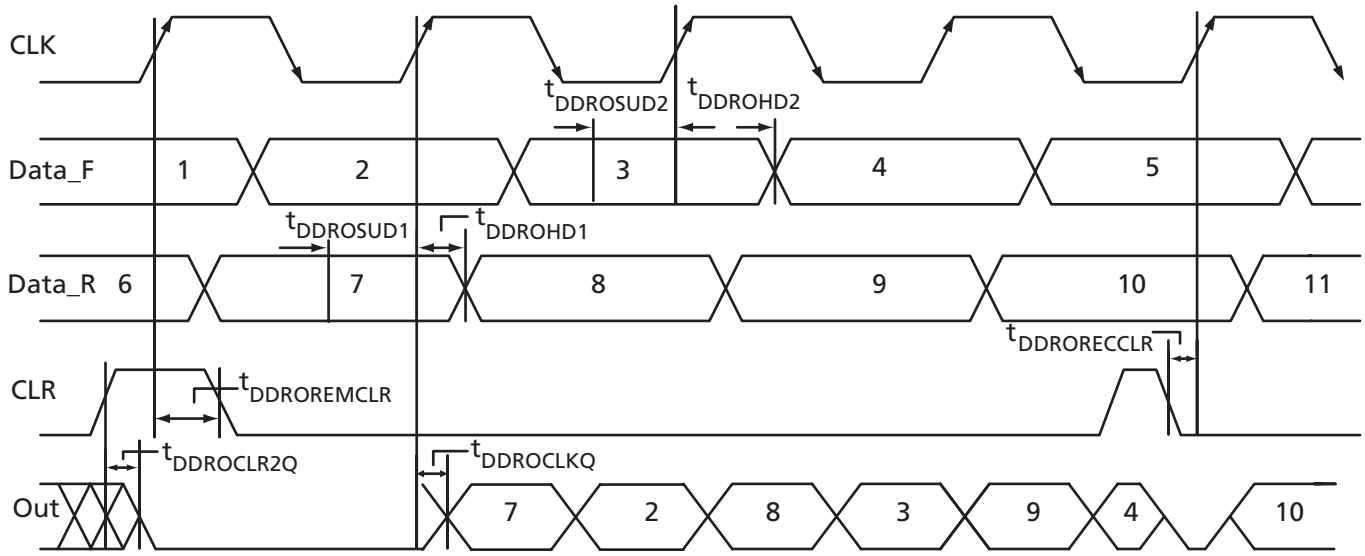


Figure 3-20 • **Output DDR Timing Diagram**

Timing Characteristics

Table 3-58 • **Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.63	0.71	0.84	1.01	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.43	0.49	0.57	0.69	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.43	0.49	0.57	0.69	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear to out for Output DDR	0.57	0.65	0.76	0.91	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal time for Output DDR	0.00	0.00	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery time for Output DDR	0.10	0.10	0.10	0.10	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR					ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR					ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR					ns
F_{DDOMAX}	Maximum Frequency for the Output DDR					MHz

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *ProASIC3/E Macro Library Guide*.

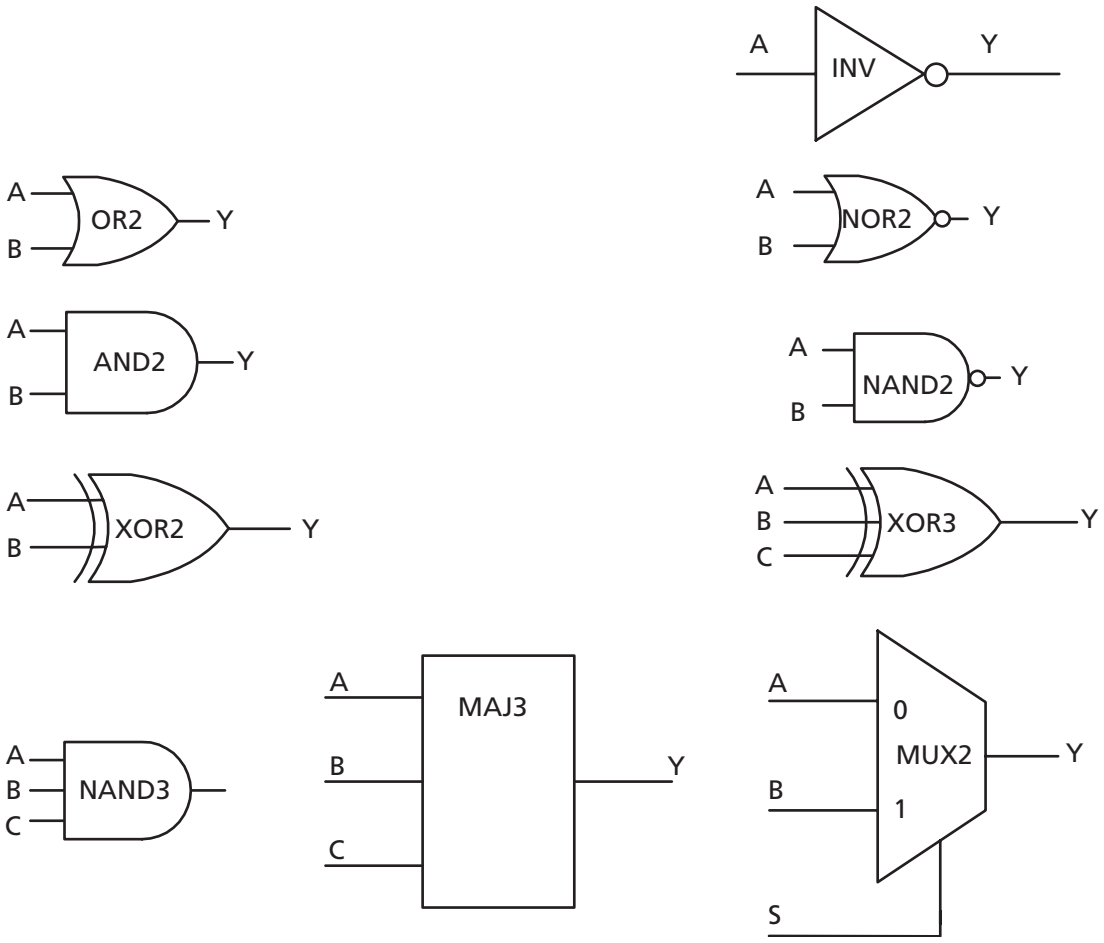


Figure 3-21 • **Sample of Combinatorial Cells**

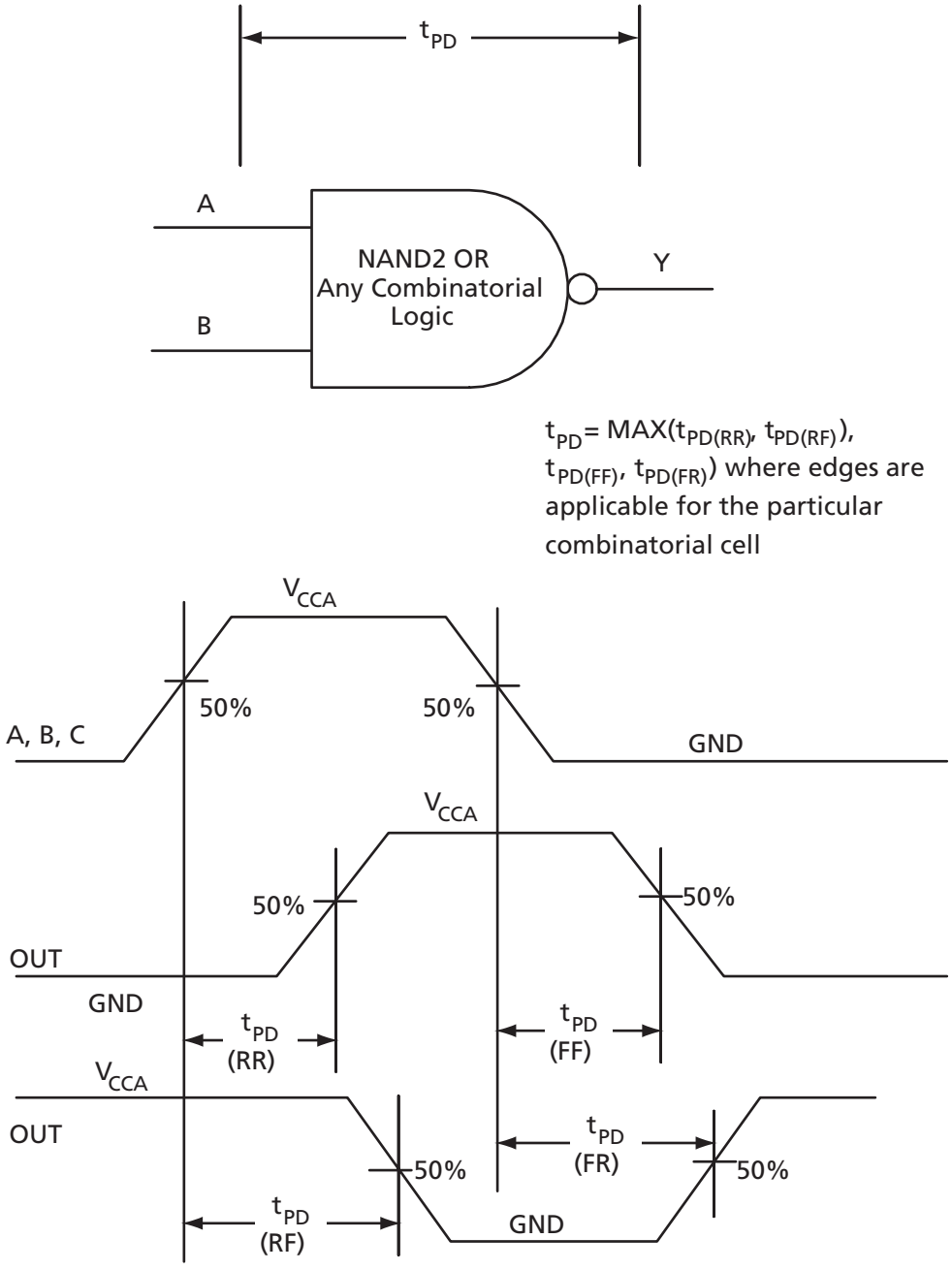


Figure 3-22 • **Timing Model and Waveforms**

Timing Characteristics

Table 3-59 • **Combinatorial Cell Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Combinatorial Cell	Equation	Parameter	–2	–1	Std.	–F	Units
INV	Y = !A	t_{PD}	0.40	0.45	0.53	0.64	ns
AND2	Y = A . B	t_{PD}	0.46	0.52	0.62	0.74	ns
NAND2	Y = !(A . B)	t_{PD}	0.46	0.52	0.62	0.74	ns
OR2	Y = A + B	t_{PD}	0.47	0.54	0.63	0.76	ns
NOR2	Y = !(A + B)	t_{PD}	0.47	0.54	0.63	0.76	ns
XOR2	Y = A ⊕ B	t_{PD}	0.72	0.82	0.96	1.15	ns
MAJ3	Y = MAJ (A , B, C)	t_{PD}	0.67	0.76	0.90	1.08	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.85	0.97	1.14	1.37	ns
MUX2	Y = A !S + B S	t_{PD}	0.49	0.56	0.65	0.79	ns
AND3	Y = A . B . C	t_{PD}	0.54	0.62	0.73	0.87	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

VersaTile Specifications as a Sequential Module

The ProASIC3 library offers a wide variety of sequential cells including flip-flops and latches. Each have a data input and optional Enable, Clear, or Preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *ProASIC3/E Macro Library Guide*.

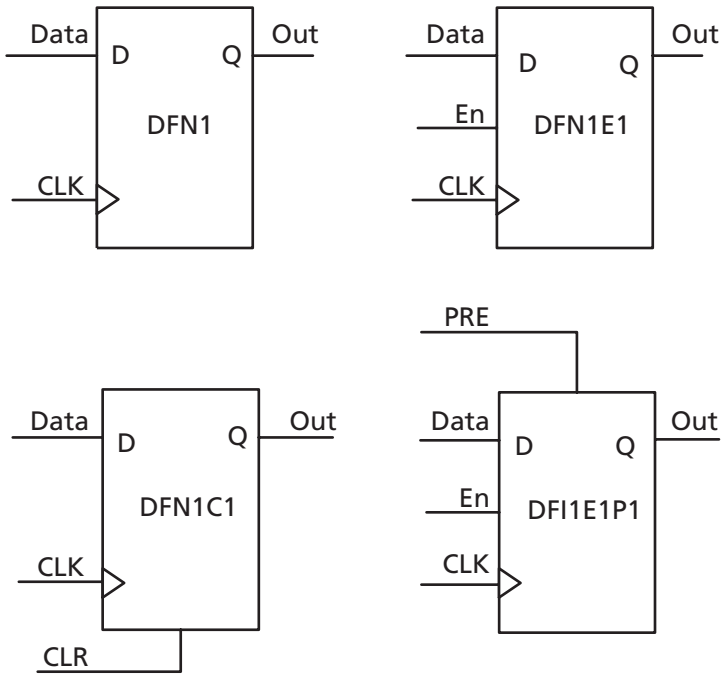


Figure 3-23 • **Sample of Sequential Cells**

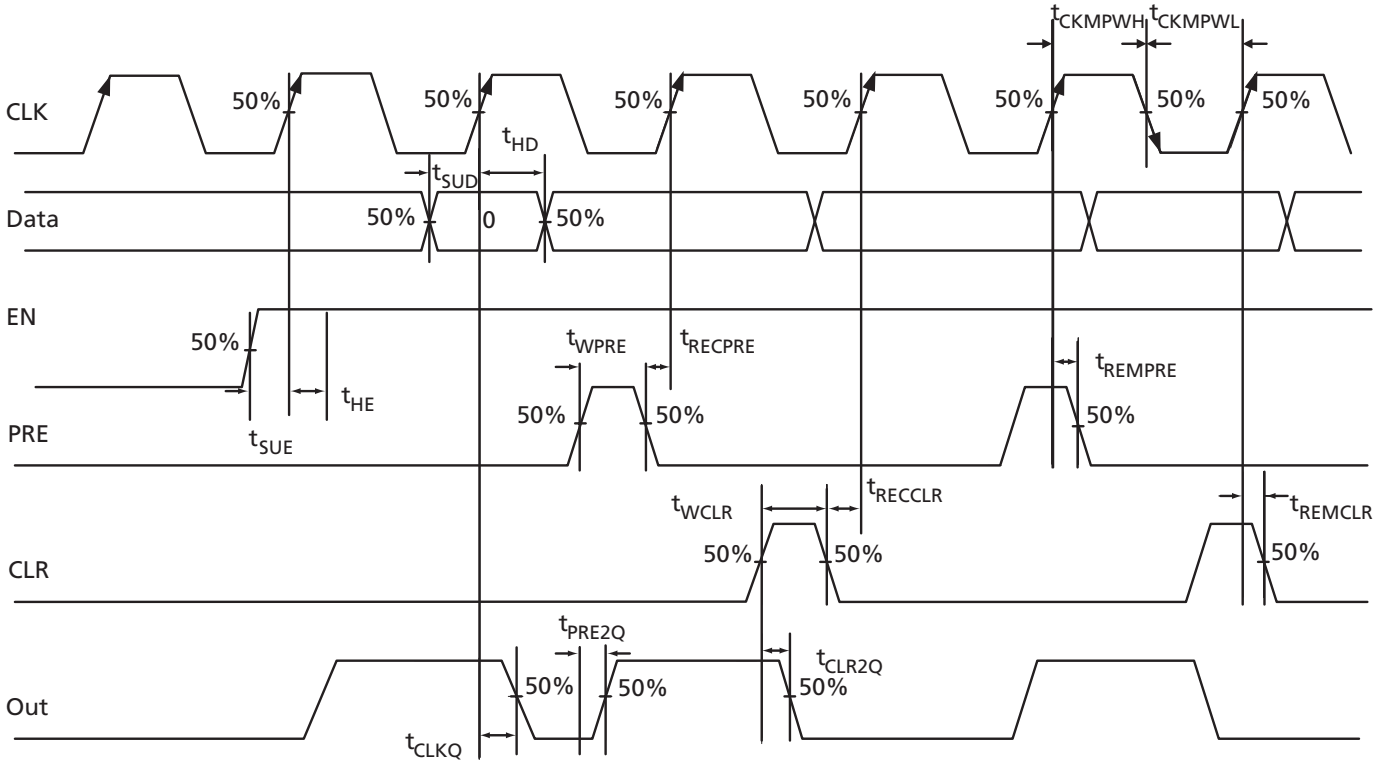


Figure 3-24 • **Timing Model and Waveforms**

Timing Characteristics

Table 3-60 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.54	0.61	0.72	0.86	ns
t_{SUD}	Data Setup time for the Core Register	0.40	0.46	0.54	0.65	ns
t_{HD}	Data Hold time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{SUE}	Enable Setup time for the Core Register	0.43	0.49	0.57	0.69	ns
t_{HE}	Enable Hold time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.40	0.45	0.53	0.64	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.40	0.45	0.53	0.64	ns
t_{REMCLR}	Asynchronous Clear Removal time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery time for the Core Register	0.24	0.27	0.32	0.38	ns
t_{REMPRE}	Asynchronous Preset Removal time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery time for the Core Register	0.24	0.27	0.32	0.38	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.26	0.29	0.34	0.41	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.26	0.29	0.34	0.41	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.38	0.43	0.51	0.61	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.43	0.49	0.57	0.69	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Global Resource Characteristics

A3P250 Clock Tree Topology

Clock delays are device-specific. Figure 3-25 is an example of a global tree used for clock routing. The global tree presented in Figure 3-25 is driven by a CCC located on the west side of the A3P250 device. It is used to drive all D-flip-flops in the device.

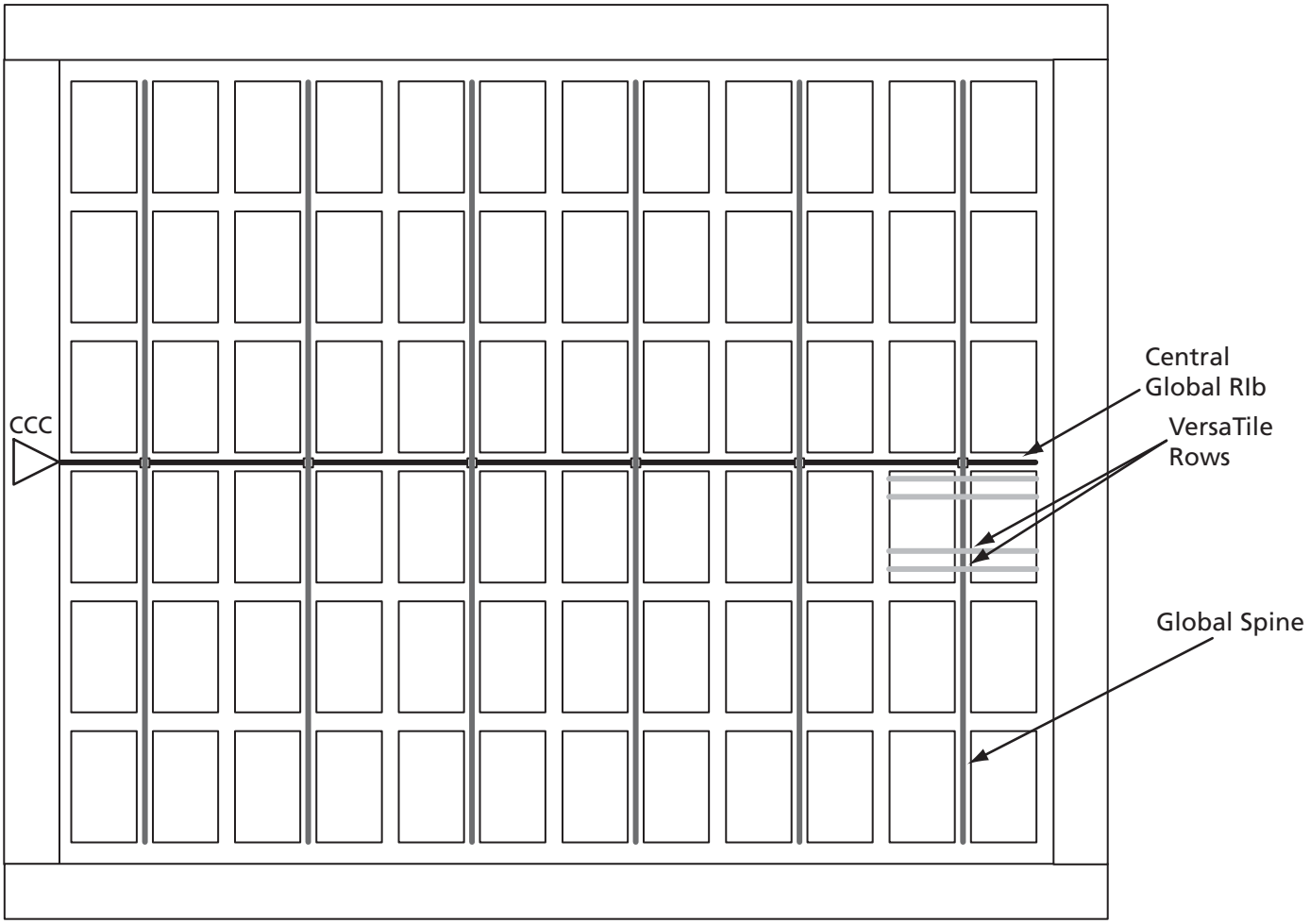


Figure 3-25 • **Example of Global Tree Use in an A3P250 Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard dependent and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to "Clock Conditioning Circuits" section on page 2-13. Table 3-61 to Table 3-67 on page 3-49 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

Table 3-61 • **A3P030 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		–F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock									ns
t_{RCKH}	Input High Delay for Global Clock									ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock									ns
F_{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-62 • **A3P060 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		–F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.05	1.18	1.02	1.34	1.20	1.58	1.44	1.91	ns
t_{RCKH}	Input High Delay for Global Clock	1.07	1.19	1.02	1.36	1.21	1.60	1.45	1.91	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock		0.14		0.34		0.40		0.47	ns
F_{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-63 • **A3P125 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		–F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.10	1.23	1.08	1.40	1.26	1.64	1.52	1.99	ns
t_{RCKH}	Input High Delay for Global Clock	1.12	1.24	1.07	1.41	1.26	1.66	1.52	1.98	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock		0.14		0.34		0.40		0.47	ns
F_{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-64 • **A3P250 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425V

Parameter	Description	–2		–1		Std.		–F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.10	1.22	1.07	1.40	1.26	1.64	1.52	1.99	ns
t_{RCKH}	Input High Delay for Global Clock	1.11	1.24	1.07	1.41	1.26	1.65	1.52	1.98	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock		0.14		0.34		0.39		0.47	ns
F_{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-65 • **A3P400 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		–F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.15	1.27	1.13	1.45	1.33	1.70	1.59	2.06	ns
t_{RCKH}	Input High Delay for Global Clock	1.16	1.28	1.12	1.46	1.32	1.72	1.59	2.05	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock		0.13		0.34		0.40		0.47	ns
F_{RMAX}	Maximum Frequency for Global Clock									Mhz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-66 • **A3P600 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		–F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.15	1.27	1.13	1.45	1.33	1.70	1.59	2.06	ns
t_{RCKH}	Input High Delay for Global Clock	1.16	1.28	1.12	1.46	1.32	1.72	1.59	2.05	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock		0.13		0.34		0.40		0.47	ns
F_{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-67 • **A3P1000 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		–F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.19	1.32	1.18	1.50	1.39	1.76	1.67	2.13	ns
t_{RCKH}	Input High Delay for Global Clock	1.20	1.32	1.18	1.51	1.38	1.77	1.66	2.12	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock		0.13		0.33		0.39		0.47	ns
F_{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Embedded SRAM and FIFO Characteristics

SRAM

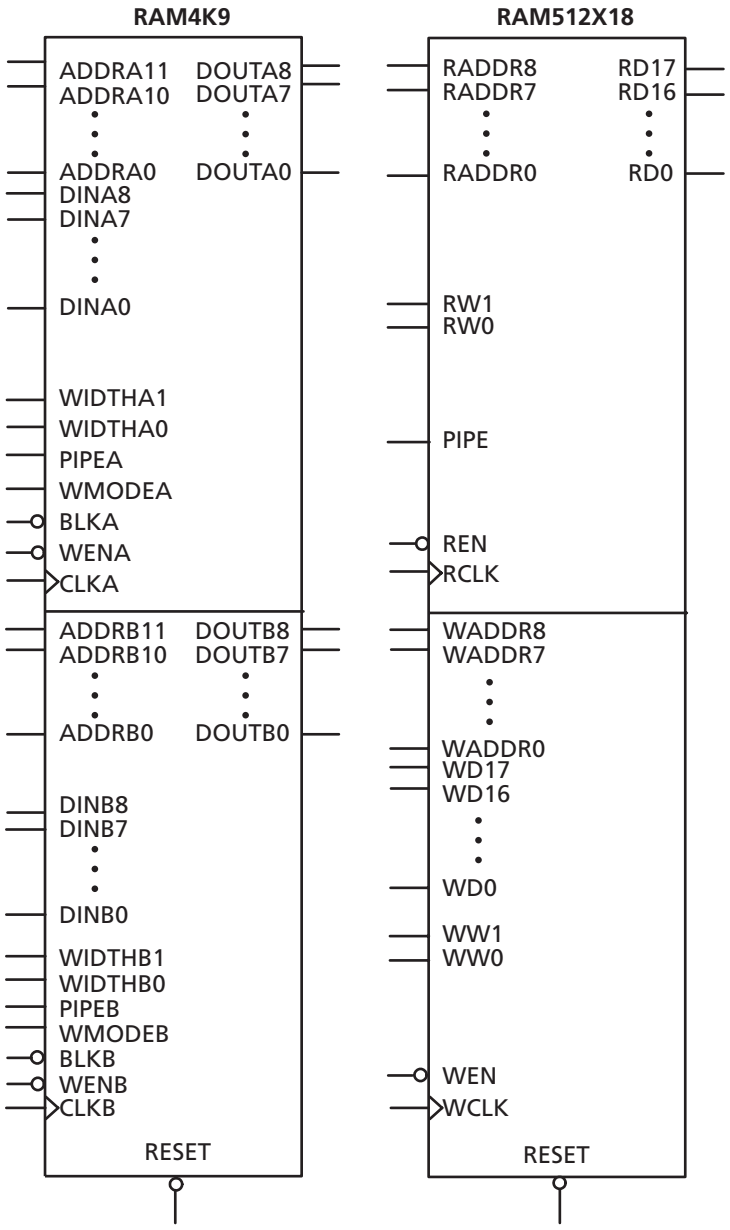


Figure 3-26 • **RAM Models**

Timing Waveforms

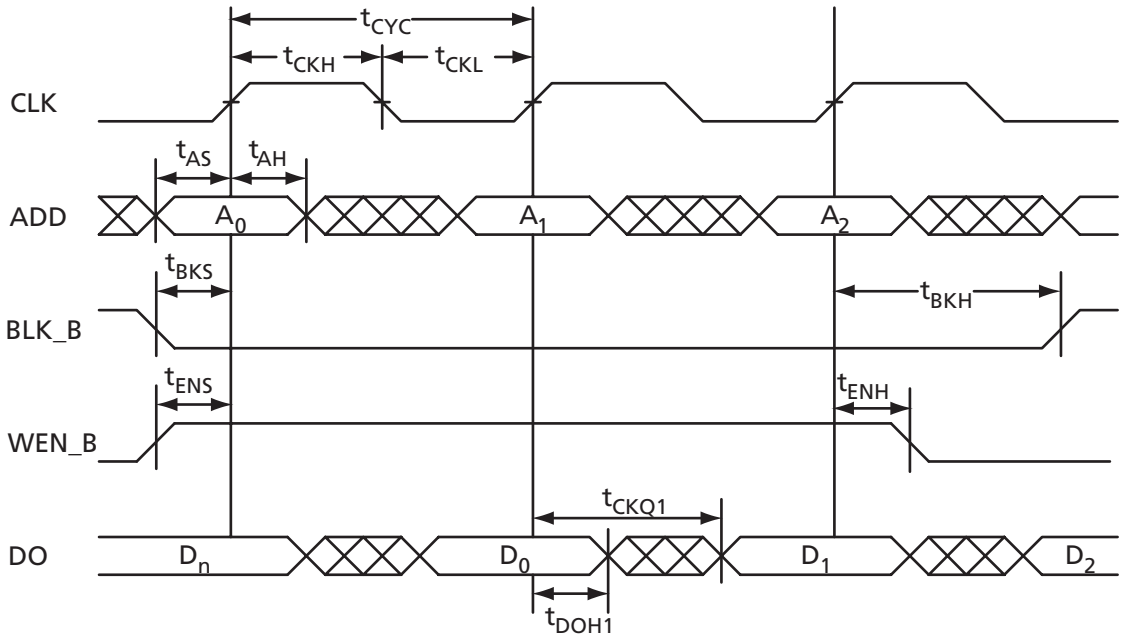


Figure 3-27 • **RAM Read for Flow-Through Output**

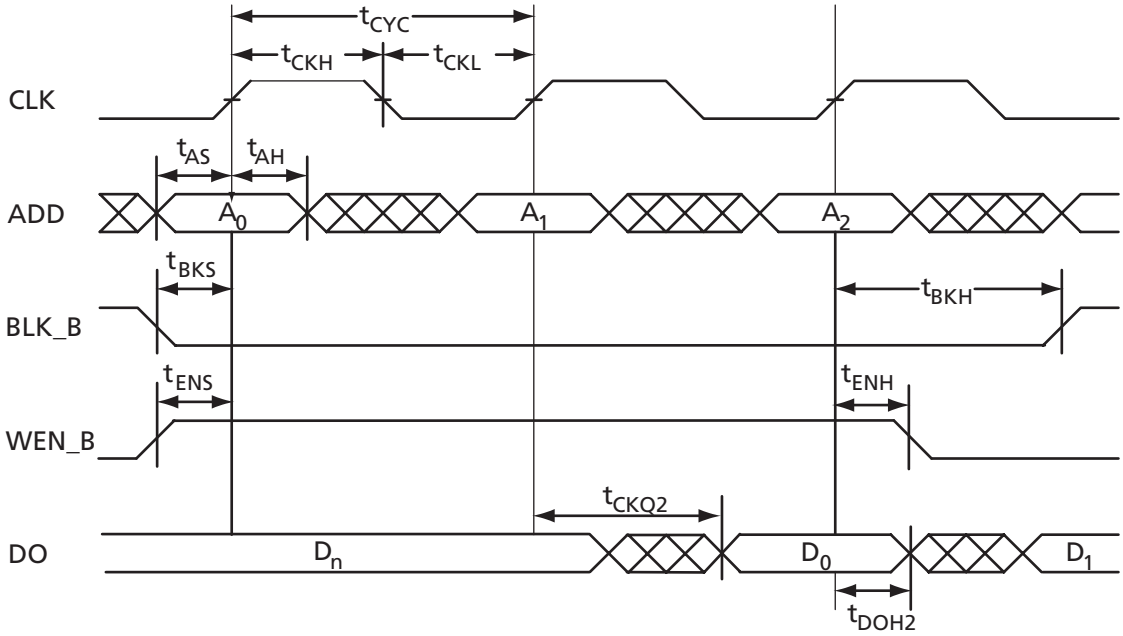


Figure 3-28 • **RAM Read for Pipelined Output**

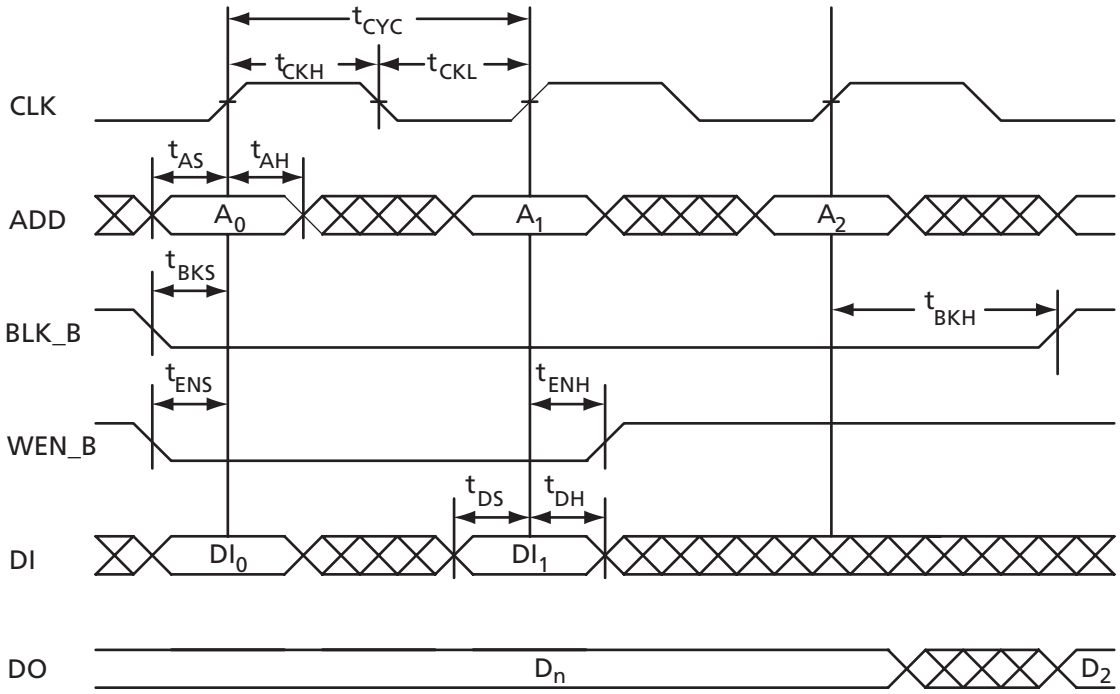


Figure 3-29 • **RAM Write, Output Retained (WMODE = 0)**

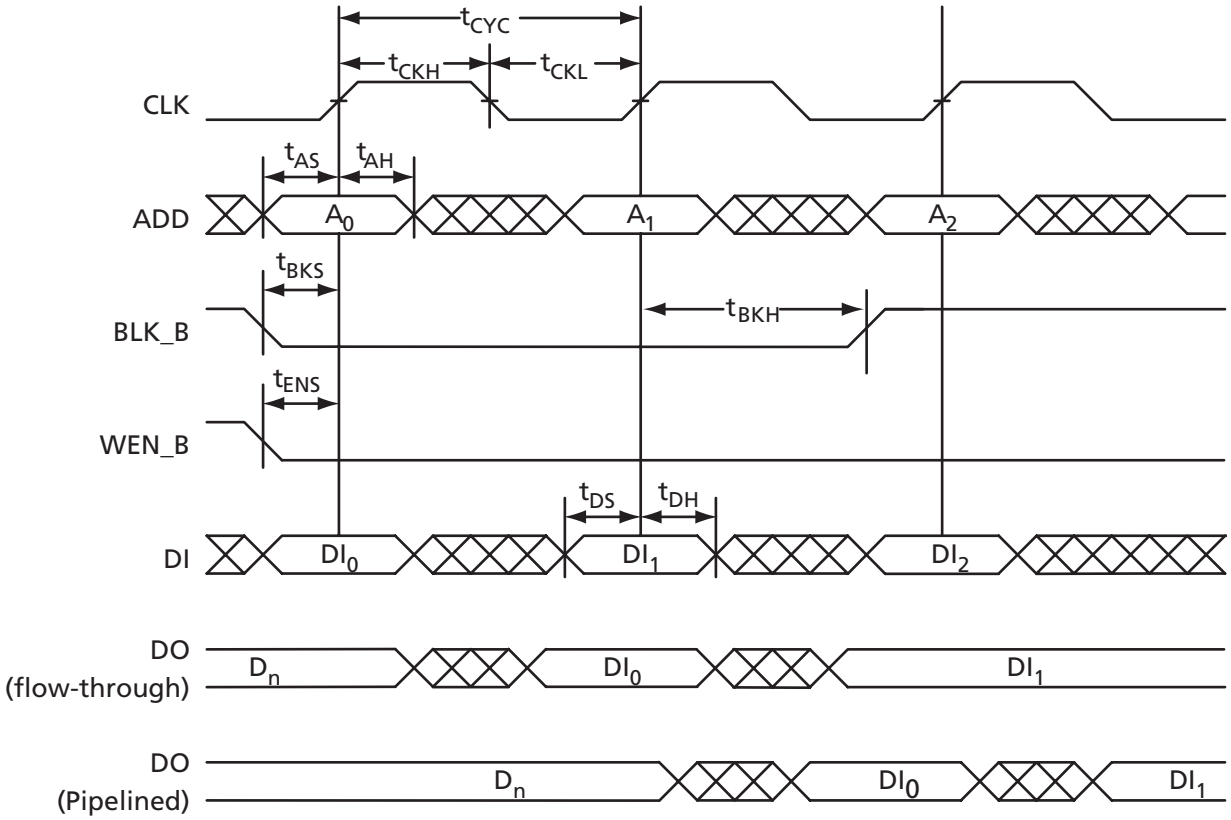


Figure 3-30 • **RAM Write, Output as Write Data (WMODE = 1)**

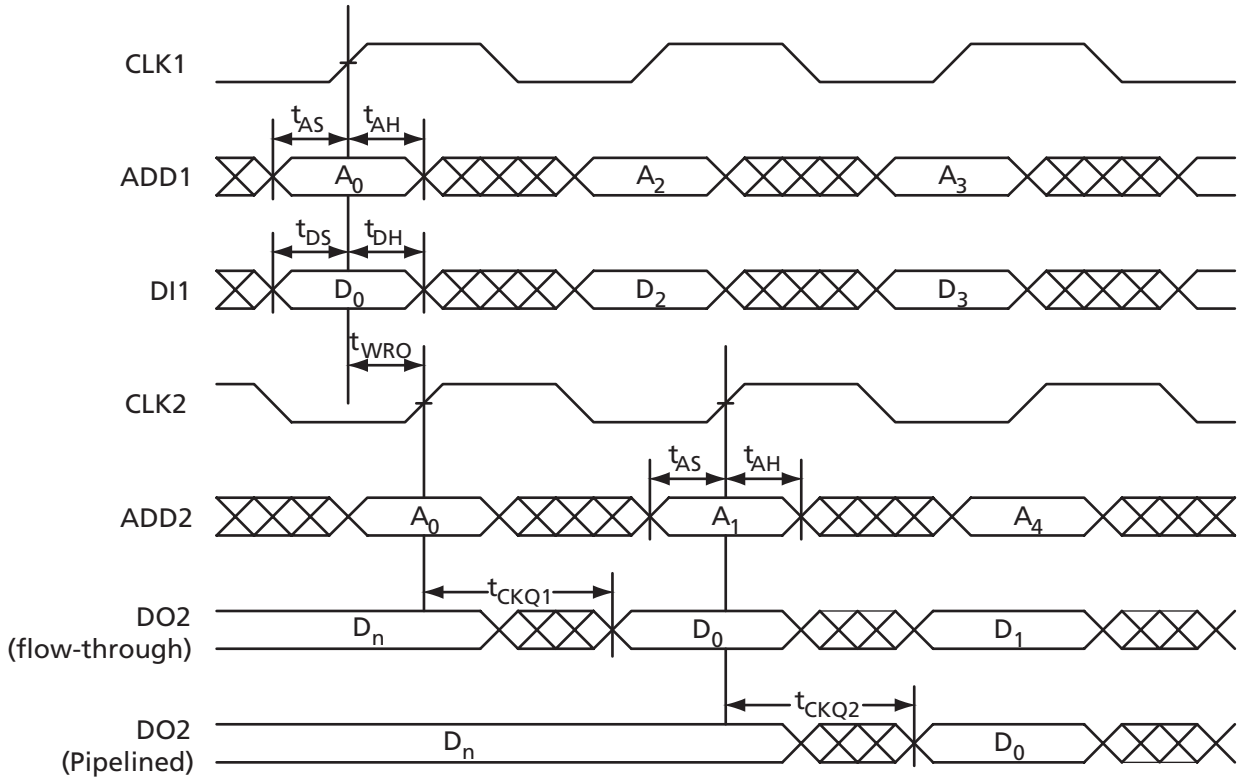


Figure 3-31 • **One Port Write/Other Port Read Same**

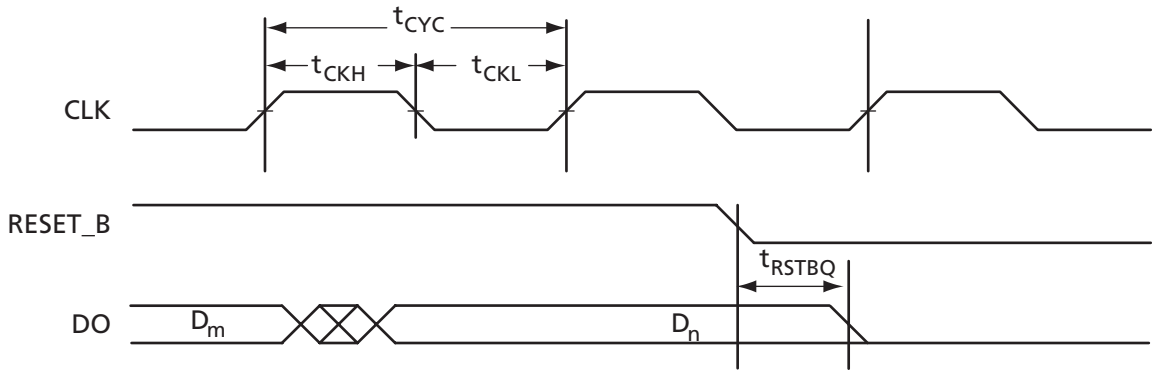


Figure 3-32 • **RAM Reset**

Timing Characteristics

Table 3-68 • **RAM4K9**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{AS}	Address Setup time	0.30	0.34	0.40	0.48	ns
t_{AH}	Address Hold time	0.00	0.00	0.00	0.00	ns
t_{ENS}	REN_B,WEN_B Setup time	0.20	0.22	0.26	0.32	ns
t_{ENH}	REN_B, WEN_B Hold time	0.03	0.03	0.04	0.05	ns
t_{BKS}	BLK_B Setup time	0.00	0.00	0.00	0.00	ns
t_{BKH}	BLK_B Hold time	0.06	0.07	0.08	0.10	ns
t_{DS}	Input data (DI) Setup time	0.24	0.27	0.32	0.38	ns
t_{DH}	Input data (DI) Hold time	0.00	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DO (output retained, WMODE = 0)	1.73	1.97	2.32	2.79	ns
	Clock High to New Data Valid on DO (flow-through, WMODE =1)	2.28	2.60	3.05	3.67	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	0.85	0.97	1.14	1.37	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (flow through)	0.98	1.12	1.31	1.57	ns
	RESET_B Low to Data Out Low on DO (pipelined)	0.98	1.12	1.31	1.57	ns
$t_{REMRSTB}$	RESET_B Removal	0.00	0.00	0.00	0.00	ns
$t_{RECRSTB}$	RESET_B Recovery	0.10	0.10	0.10	0.10	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.22	0.25	0.29	0.35	ns
t_{CYC}	Clock Cycle time	2.10	2.38	2.80	3.36	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-69 • **RAM512X18**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{AS}	Address Setup time	0.30	0.34	0.40	0.48	ns
t_{AH}	Address Hold time	0.00	0.00	0.00	0.00	ns
t_{ENS}	REN_B,WEN_B Setup time	0.14	0.16	0.19	0.23	ns
t_{ENH}	REB_B, WEN_B Hold time	0.02	0.03	0.03	0.04	ns
t_{DS}	Input data (DI) Setup time	0.22	0.25	0.30	0.36	ns
tD H	Input data (DI) Hold time	0.00	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DO (output retained, WMODE =0)	2.08	2.37	2.79	3.35	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	0.85	0.97	1.14	1.37	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (flow through)	0.98	1.12	1.31	1.57	ns
	RESET_B Low to Data Out Low on DO (pipelined)	0.98	1.12	1.31	1.57	ns
$t_{REMRSTB}$	RESET_B Removal	0.00	0.00	0.00	0.00	ns
$t_{RECRSTB}$	RESET_B Recovery	0.10	0.10	0.10	0.10	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.22	0.25	0.29	0.35	ns
t_{CYC}	Clock Cycle time	2.10	2.38	2.80	3.36	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

FIFO

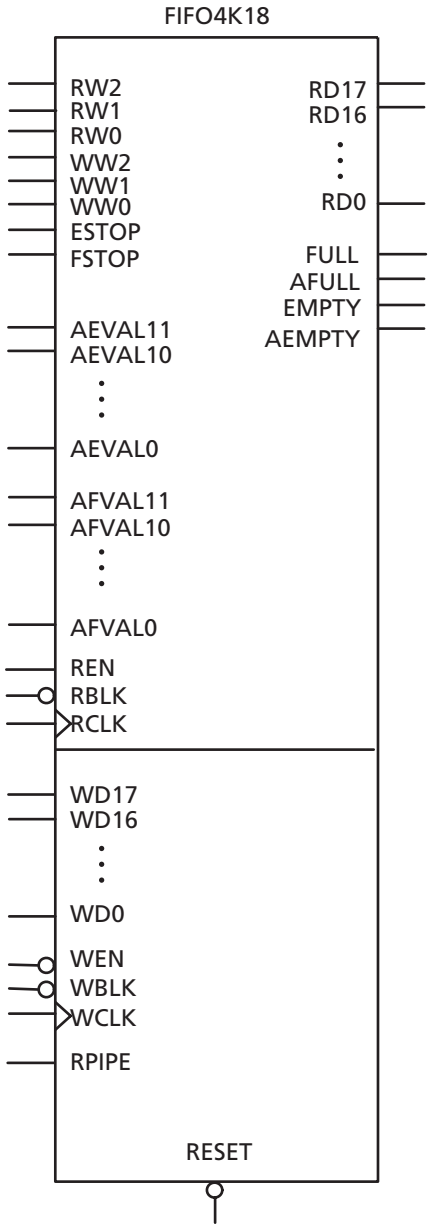


Figure 3-33 • **FIFO Model**

Timing Waveforms

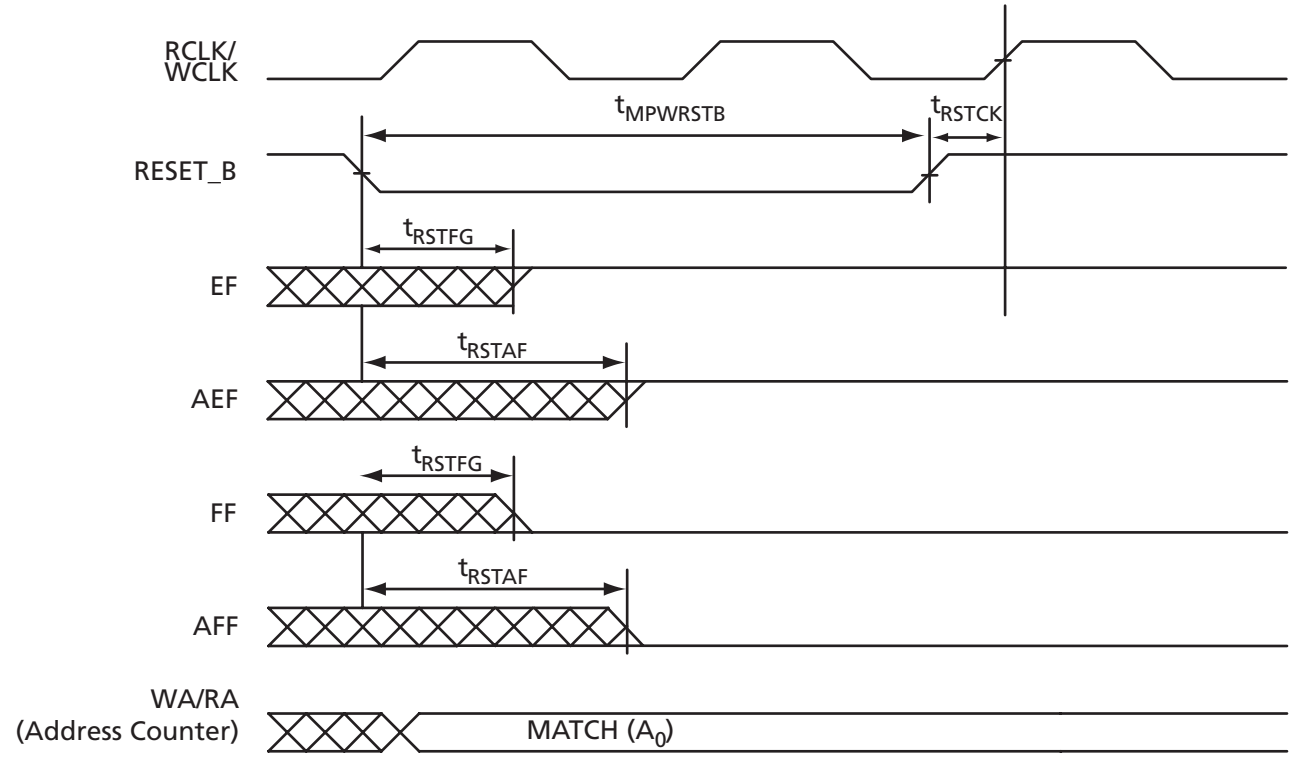


Figure 3-34 • **FIFO Reset**

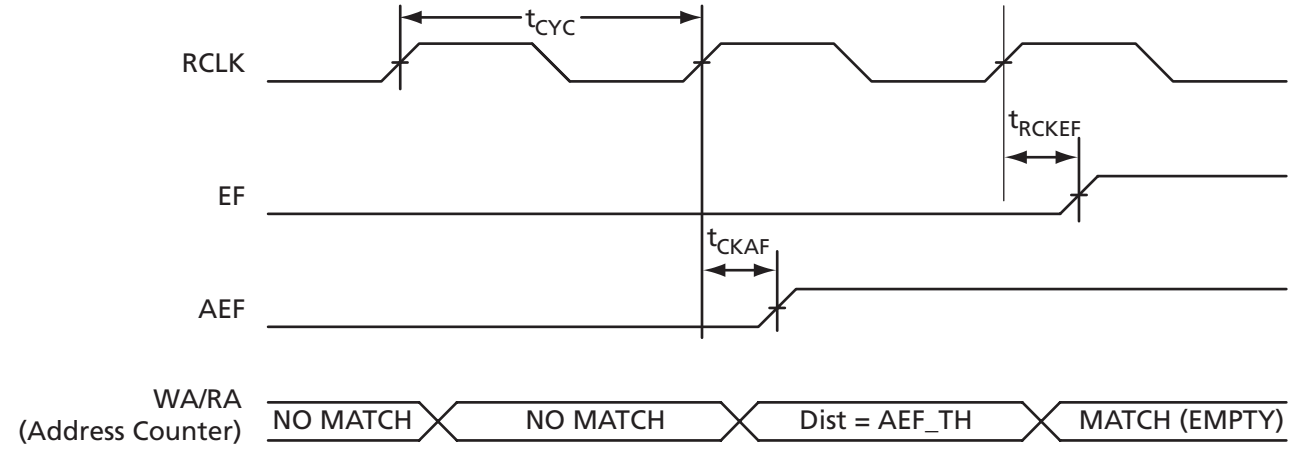


Figure 3-35 • **FIFO Reset, Empty Flag, and Almost-Empty Flag**

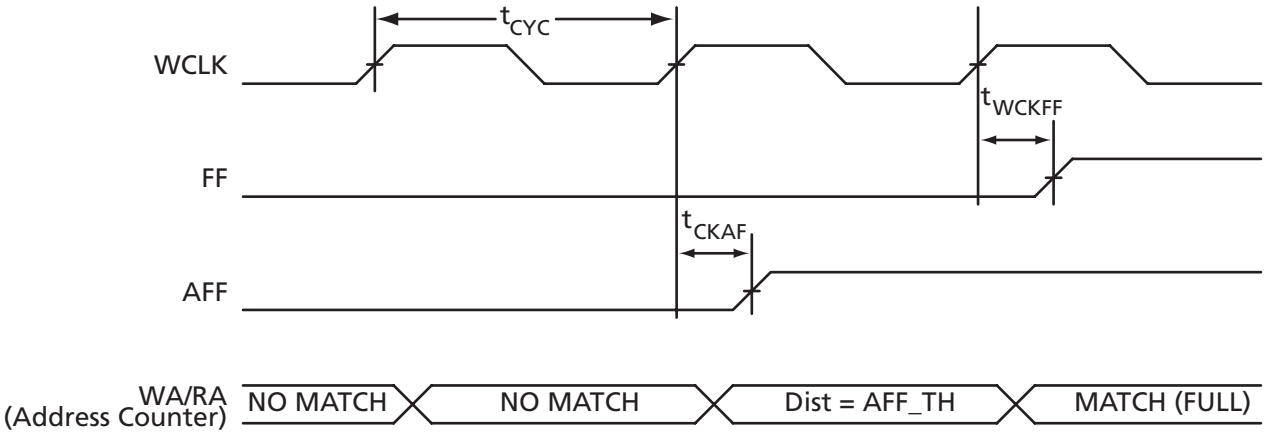


Figure 3-36 • **FIFO FULL and AFULL Flag**

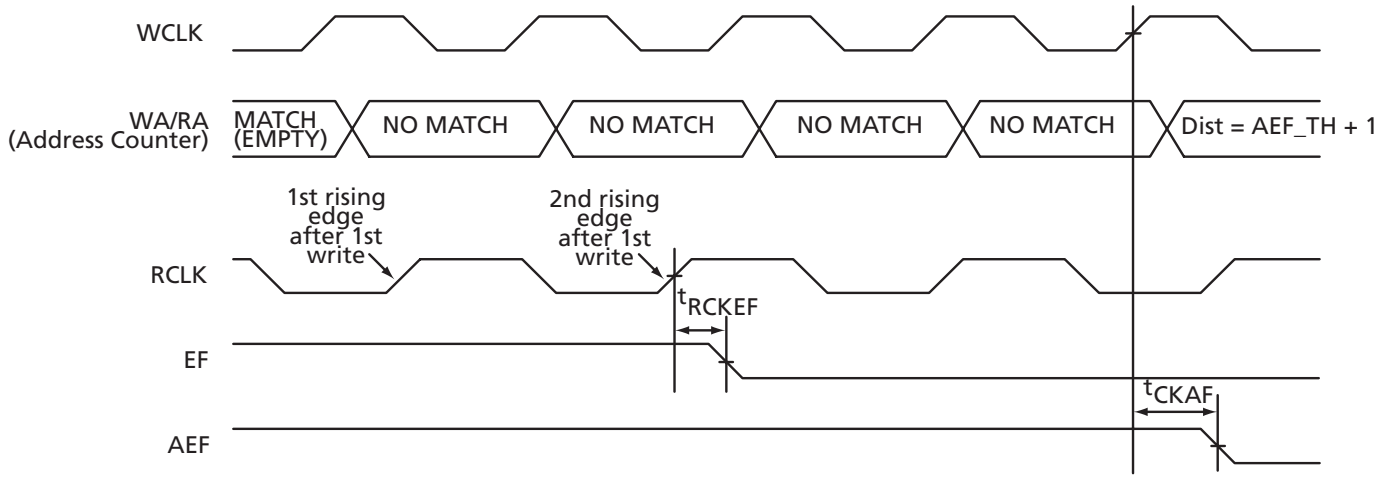


Figure 3-37 • **EMPTY Flag and AEMPTY Flag Deassertion**

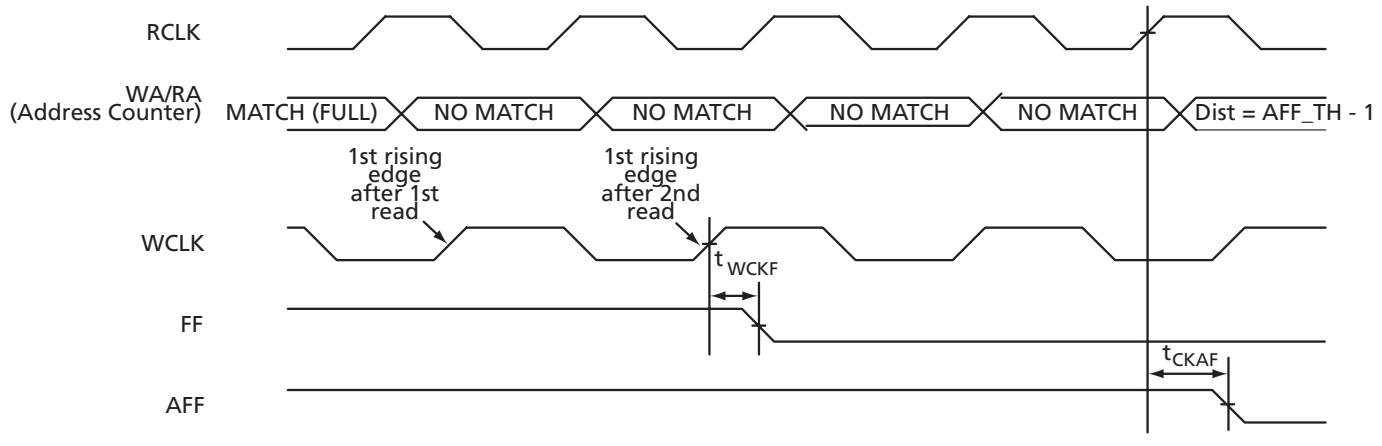


Figure 3-38 • **FULL and ALFULL Deassertion**

Timing Characteristics

Table 3-70 • **FIFO**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{ENS}	REN_B,WEN_B Setup time	0.14	0.16	0.19	0.23	ns
t_{ENH}	REN_B, WEN_B Hold time	0.06	0.07	0.08	0.10	ns
t_{BKS}	BLK_B Setup time	0.25	0.29	0.34	0.40	ns
t_{BKH}	BLK_B Hold time	0.00	0.00	0.00	0.00	ns
t_{DS}	Input data (DI) Setup time	0.22	0.25	0.30	0.36	ns
t_{DH}	Input data (DI) Hold time	0.00	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DO (flow-through)	2.28	2.60	3.05	3.67	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	0.85	0.97	1.14	1.37	ns
t_{RCKEF}	RCLK High to Empty flag Valid	1.69	1.92	2.26	2.71	ns
t_{WCKFF}	WCLK High to Full flag Valid	1.61	1.83	2.15	2.58	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	3.62	4.12	4.85	5.82	ns
t_{RSTFG}	RESET_B Low to Empty/Full flag valid	1.71	1.94	2.28	2.74	ns
t_{RSTAF}	RESET_B Low to Almost-Empty/Full Flag Valid	3.58	4.08	4.80	5.77	ns
t_{RSTBQ}	RESET_B Low to Data out Low on DO (flow through)	0.98	1.12	1.31	1.57	ns
	RESET_B Low to Data out Low on DO (pipelined)	0.98	1.12	1.31	1.57	ns
$t_{REMRSTB}$	RESET_B Removal	0.00	0.00	0.00	0.00	ns
$t_{RECRSTB}$	RESET_B Recovery	0.10	0.10	0.10	0.10	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.21	0.24	0.29	0.34	ns
t_{CYC}	Clock Cycle time	2.06	2.33	2.75	3.29	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Embedded FROM Characteristics

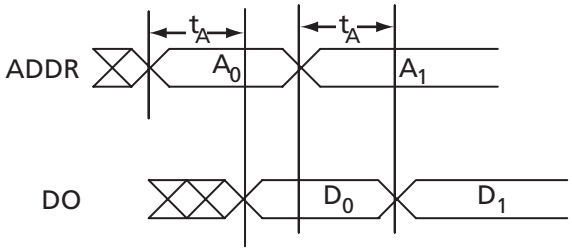


Figure 3-39 • **Timing Diagram**

Timing Characteristics

Table 3-71 • **Embedded FROM Access Time**

Parameter	Description	–2	–1	Std.	Units
t_A	Data Access Time	10	10	10	ns

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected, refer to the I/O Timing characteristics for more details.

Timing Characteristics

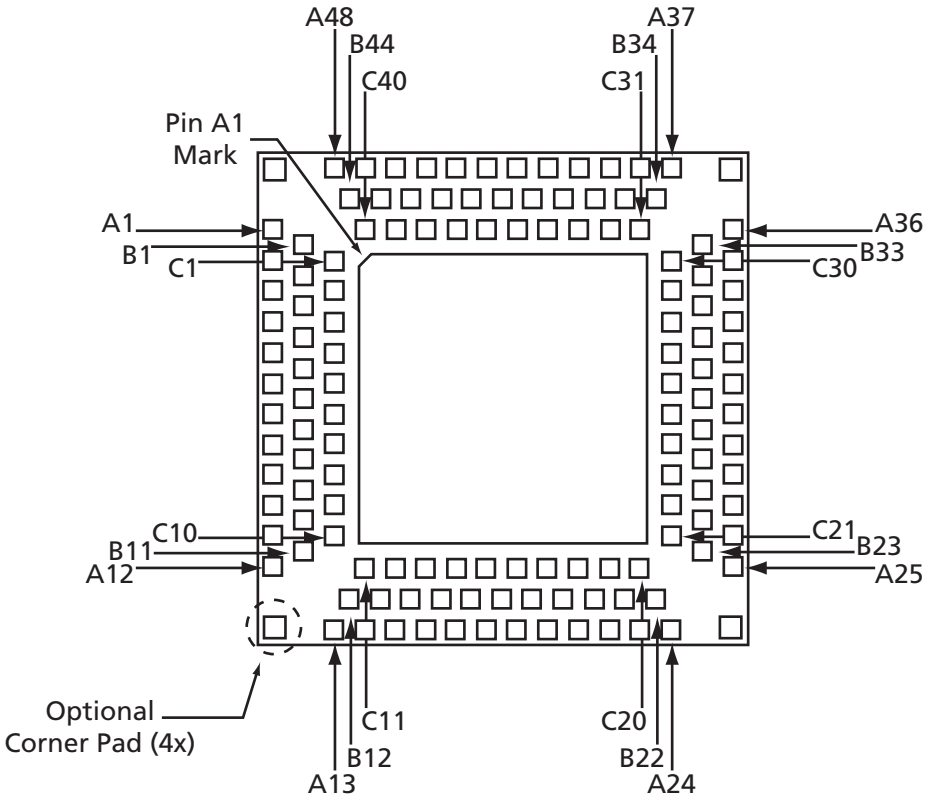
Table 3-72 • **JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, worst-case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time				ns
t_{DIHD}	Test Data Input Hold Time				ns
t_{TMSSU}	Test Mode Select Setup Time				ns
t_{TMDHD}	Test Mode Select Hold Time				ns
t_{TCK2Q}	Clock to Q (Data Out)				ns
t_{RSTB2Q}	Reset to Q (Data Out)				ns
F_{TCKMAX}	TCK maximum frequency	20/40	20/40	20/40	MHz
$t_{TRSTREM}$	ResetB Removal time				ns
$t_{TRSTREC}$	ResetB Recovery time				ns
$t_{TRSTMPW}$	ResetB minimum pulse				ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Package Pin Assignments

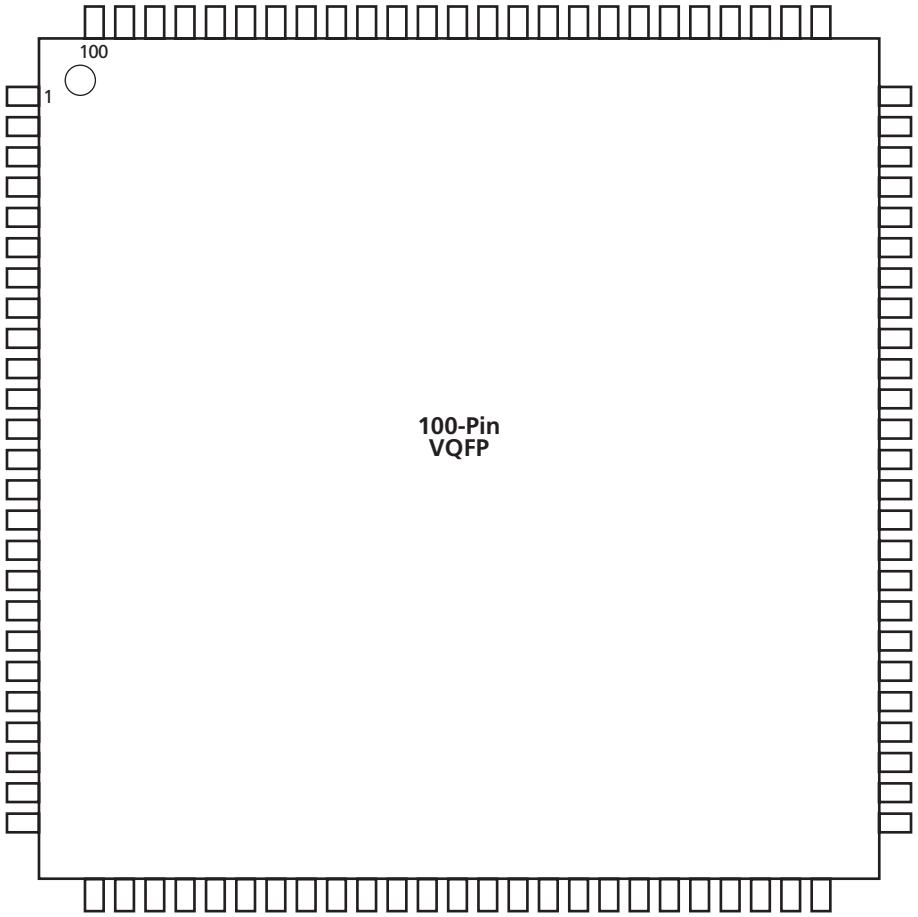
132-Pin QFN



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

100-Pin VQFP



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

100-Pin VQFP*	
Pin Number	**A3P060 Function**
1	GND
2	GAA2/IO51RSB1
3	IO52RSB1
4	GAB2/IO53RSB1
5	IO95RSB1
6	GAC2/IO94RSB1
7	IO93RSB1
8	IO92RSB1
9	GND
10	GFB1/IO87RSB1
11	GFB0/IO86RSB1
12	V_{COMPLF}
13	GFA0/IO85RSB1
14	V_{CCPLF}
15	GFA1/IO84RSB1
16	GFA2/IO83RSB1
17	V_{CC}
18	V_{CCI}B1
19	GEC1/IO77RSB1
20	GEB1/IO75RSB1
21	GEB0/IO74RSB1
22	GEA1/IO73RSB1
23	GEA0/IO72RSB1
24	VMV1
25	GNDQ
26	GEA2/IO71RSB1
27	GEB2/IO70RSB1
28	GEC2/IO69RSB1
29	IO68RSB1
30	IO67RSB1
31	IO66RSB1
32	IO65RSB1
33	IO64RSB1
34	IO63RSB1
35	IO62RSB1
36	IO61RSB1

100-Pin VQFP*	
Pin Number	**A3P060 Function**
37	V_{CC}
38	GND
39	V_{CCI}B1
40	IO60RSB1
41	IO59RSB1
42	IO58RSB1
43	GDC2/IO57RSB1
44	GDB2/IO56RSB1
45	GDA2/IO55RSB1
46	IO54RSB1
47	TCK
48	TDI
49	TMS
50	NC
51	GND
52	V_{PUMP}
53	NC
54	TDO
55	TRST
56	V_{JTAG}
57	GDA1/IO49RSB0
58	GDC0/IO46RSB0
59	GDC1/IO45RSB0
60	IO44RSB0
61	GCB2/IO42RSB0
62	GCA0/IO40RSB0
63	GCA1/IO39RSB0
64	GCC0/IO36RSB0
65	GCC1/IO35RSB0
66	V_{CCI}B0
67	GND
68	V_{CC}
69	IO31RSB0
70	GBC2/IO29RSB0
71	GBB2/IO27RSB0
72	IO26RSB0

100-Pin VQFP*	
Pin Number	**A3P060 Function**
73	GBA2/IO25RSB0
74	VMV0
75	GNDQ
76	GBA1/IO24RSB0
77	GBA0/IO23RSB0
78	GBB1/IO22RSB0
79	GBB0/IO21RSB0
80	GBC1/IO20RSB0
81	GBC0/IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO15RSB0
85	IO13RSB0
86	IO11RSB0
87	V_{CCI}B0
88	GND
89	V_{CC}
90	IO10RSB0
91	IO09RSB0
92	IO08RSB0
93	GAC1/IO07RSB0
94	GAC0/IO06RSB0
95	GAB1/IO05RSB0
96	GAB0/IO04RSB0
97	GAA1/IO03RSB0
98	GAA0/IO02RSB0
99	IO01RSB0
100	IO00RSB0

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

100-Pin VQFP*	
Pin Number	**A3P125 Function**
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	V_{COMPLF}
13	GFA0/IO122RSB1
14	V_{CCPLF}
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	V_{CC}
18	V_{CCI}B1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1
36	IO93RSB1
37	V_{CC}
38	GND

100-Pin VQFP*	
Pin Number	**A3P125 Function**
39	V_{CCI}B1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	V_{PUMP}
53	NC
54	TDO
55	TRST
56	V_{JTAG}
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	V_{CCI}B0
67	GND
68	V_{CC}
69	IO47RSB0
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0
72	IO42RSB0
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0

100-Pin VQFP*	
Pin Number	**A3P125 Function**
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	V_{CCI}B0
88	GND
89	V_{CC}
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

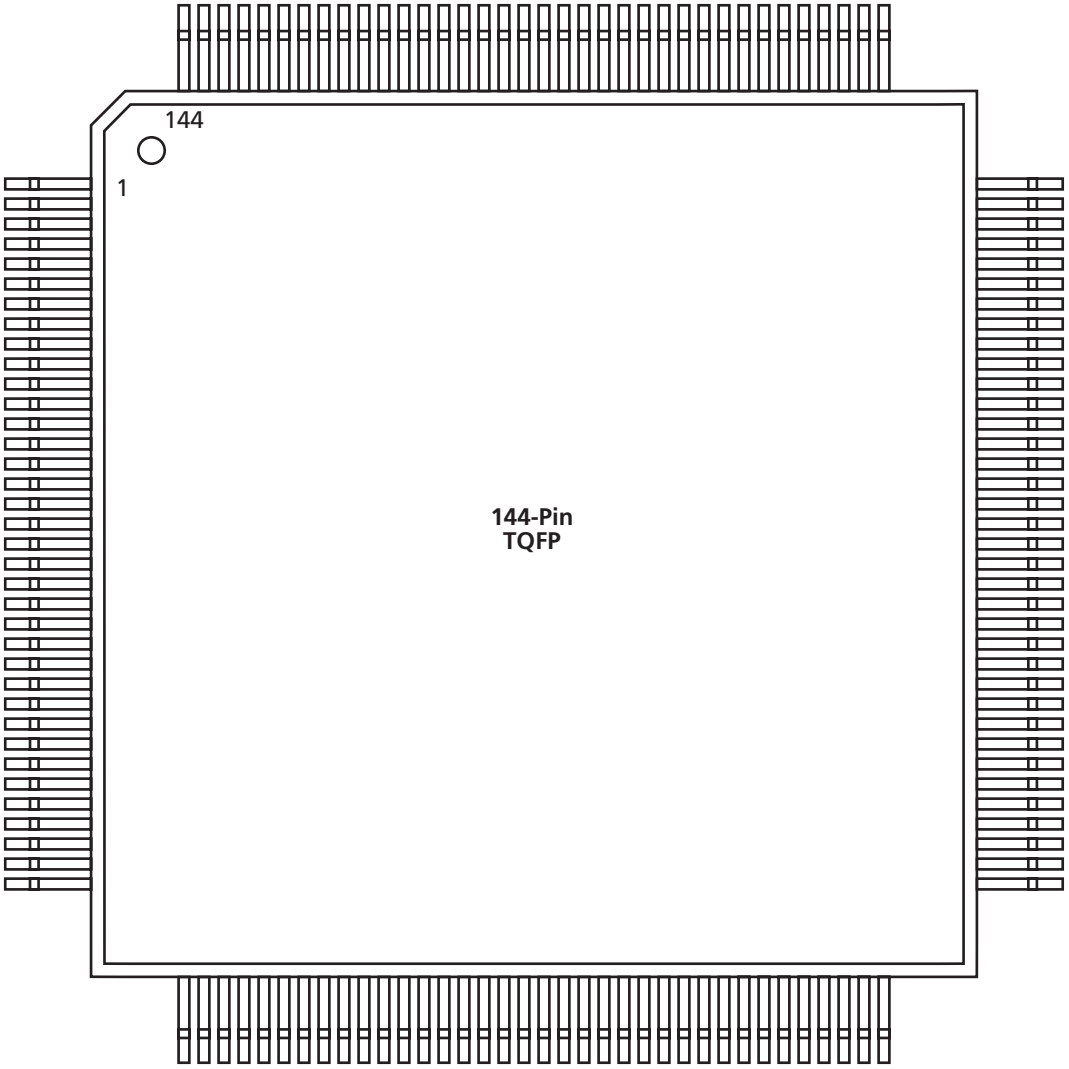
100-Pin VQFP*	
Pin Number	**A3P250 Function**
1	GND
2	GAA2/IO118PDB3
3	IO118NDB3
4	GAB2/IO117PDB3
5	IO117NDB3
6	GAC2/IO116PDB3
7	IO116NDB3
8	IO112PSB3
9	GND
10	GFB1/IO109PDB3
11	GFB0/IO109NDB3
12	V_{COMPLF}
13	GFA0/IO108NPB3
14	V_{CCPLF}
15	GFA1/IO108PPB3
16	GFA2/IO107PSB3
17	V_{CC}
18	V_{CCI}B3
19	GFC2/IO105PSB3
20	GEC1/IO100PDB3
21	GEC0/IO100NDB3
22	GEA1/IO98PDB3
23	GEA0/IO98NDB3
24	VMV3
25	GNDQ
26	GEA2/IO97RSB2
27	GEB2/IO96RSB2
28	GEC2/IO95RSB2
29	IO93RSB2
30	IO92RSB2
31	IO91RSB2
32	IO90RSB2
33	IO88RSB2
34	IO86RSB2
35	IO85RSB2
36	IO84RSB2

100-Pin VQFP*	
Pin Number	**A3P250 Function**
37	V_{CC}
38	GND
39	V_{CCI}B2
40	IO77RSB2
41	IO74RSB2
42	IO71RSB2
43	GDC2/IO63RSB2
44	GDB2/IO62RSB2
45	GDA2/IO61RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	V_{PUMP}
53	NC
54	TDO
55	TRST
56	V_{JTAG}
57	GDA1/IO60PSB1
58	GDC0/IO58NDB1
59	GDC1/IO58PDB1
60	IO52NDB1
61	GCB2/IO52PDB1
62	GCA1/IO50PDB1
63	GCA0/IO50NDB1
64	GCC0/IO48NDB1
65	GCC1/IO48PDB1
66	V_{CCI}B1
67	GND
68	V_{CC}
69	IO43NDB1
70	GBC2/IO43PDB1
71	GBB2/IO42PSB1
72	IO41NDB1

100-Pin VQFP*	
Pin Number	**A3P250 Function**
73	GBA2/IO41PDB1
74	VMV1
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO29RSB0
83	IO27RSB0
84	IO25RSB0
85	IO23RSB0
86	IO21RSB0
87	V_{CCI}B0
88	GND
89	V_{CC}
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

144-Pin TQFP



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

144-Pin TQFP*	
Pin Number	**A3P060 Function**
1	GAA2/IO51RSB1
2	IO52RSB1
3	GAB2/IO53RSB1
4	IO95RSB1
5	GAC2/IO94RSB1
6	IO93RSB1
7	IO92RSB1
8	IO91RSB1
9	V_{CC}
10	GND
11	V_{CCI}B1
12	IO90RSB1
13	GFC1/IO89RSB1
14	GFC0/IO88RSB1
15	GFB1/IO87RSB1
16	GFB0/IO86RSB1
17	V_{COMPLF}
18	GFA0/IO85RSB1
19	V_{CCPLF}
20	GFA1/IO84RSB1
21	GFA2/IO83RSB1
22	GFB2/IO82RSB1
23	GFC2/IO81RSB1
24	IO80RSB1
25	IO79RSB1
26	IO78RSB1
27	GND
28	V_{CCI}B1
29	GEC1/IO77RSB1
30	GEC0/IO76RSB1
31	GEB1/IO75RSB1
32	GEB0/IO74RSB1
33	GEA1/IO73RSB1
34	GEA0/IO72RSB1
35	VMV1
36	GNDQ

144-Pin TQFP*	
Pin Number	**A3P060 Function**
37	NC
38	GEA2/IO71RSB1
39	GEB2/IO70RSB1
40	GEC2/IO69RSB1
41	IO68RSB1
42	IO67RSB1
43	IO66RSB1
44	IO65RSB1
45	V_{CC}
46	GND
47	V_{CCI}B1
48	NC
49	IO64RSB1
50	NC
51	IO63RSB1
52	NC
53	IO62RSB1
54	NC
55	IO61RSB1
56	NC
57	NC
58	IO60RSB1
59	IO59RSB1
60	IO58RSB1
61	GDC2/IO57RSB1
62	NC
63	GND
64	NC
65	GDB2/IO56RSB1
66	GDA2/IO55RSB1
67	IO54RSB1
68	GNDQ
69	TCK
70	TDI
71	TMS
72	VMV1

144-Pin TQFP*	
Pin Number	**A3P060 Function**
73	V_{PUMP}
74	NC
75	TDO
76	TRST
77	V_{JTAG}
78	GDA0/IO50RSB0
79	GDB0/IO48RSB0
80	GDB1/IO47RSB0
81	V_{CCI}B0
82	GND
83	IO44RSB0
84	GCC2/IO43RSB0
85	GCB2/IO42RSB0
86	GCA2/IO41RSB0
87	GCA0/IO40RSB0
88	GCA1/IO39RSB0
89	GCB0/IO38RSB0
90	GCB1/IO37RSB0
91	GCC0/IO36RSB0
92	GCC1/IO35RSB0
93	IO34RSB0
94	IO33RSB0
95	NC
96	NC
97	NC
98	V_{CCI}B0
99	GND
100	V_{CC}
101	IO30RSB0
102	GBC2/IO29RSB0
103	IO28RSB0
104	GBB2/IO27RSB0
105	IO26RSB0
106	GBA2/IO25RSB0
107	VMV0
108	GNDQ

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

144-Pin TQFP*	
Pin Number	**A3P060 Function**
109	NC
110	NC
111	GBA1/IO24RSB0
112	GBA0/IO23RSB0
113	GBB1/IO22RSB0
114	GBB0/IO21RSB0
115	GBC1/IO20RSB0
116	GBC0/IO19RSB0
117	V_{CCI}B0
118	GND
119	V_{CC}
120	IO18RSB0
121	IO17RSB0
122	IO16RSB0
123	IO15RSB0
124	IO14RSB0
125	IO13RSB0
126	IO12RSB0
127	IO11RSB0
128	NC
129	IO10RSB0
130	IO09RSB0
131	IO08RSB0
132	GAC1/IO07RSB0
133	GAC0/IO06RSB0
134	NC
135	GND
136	NC
137	GAB1/IO05RSB0
138	GAB0/IO04RSB0
139	GAA1/IO03RSB0
140	GAA0/IO02RSB0
141	IO01RSB0
142	IO00RSB0
143	GNDQ
144	VMV0

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

144_Pin TQFP*	
Pin Number	**A3P125 Function**
1	GAA2/IO67RSB1
2	IO68RSB1
3	GAB2/IO69RSB1
4	IO132RSB1
5	GAC2/IO131RSB1
6	IO130RSB1
7	IO129RSB1
8	IO128RSB1
9	V_{CC}
10	GND
11	V_{CCI}B1
12	IO127RSB1
13	GFC1/IO126RSB1
14	GFC0/IO125RSB1
15	GFB1/IO124RSB1
16	GFB0/IO123RSB1
17	V_{COMPLF}
18	GFA0/IO122RSB1
19	V_{CCPLF}
20	GFA1/IO121RSB1
21	GFA2/IO120RSB1
22	GFB2/IO119RSB1
23	GFC2/IO118RSB1
24	IO117RSB1
25	IO116RSB1
26	IO115RSB1
27	GND
28	V_{CCI}B1
29	GEC1/IO112RSB1
30	GEC0/IO111RSB1
31	GEB1/IO110RSB1
32	GEB0/IO109RSB1
33	GEA1/IO108RSB1
34	GEA0/IO107RSB1
35	VMV1
36	GNDQ

144_Pin TQFP*	
Pin Number	**A3P125 Function**
37	NC
38	GEA2/IO106RSB1
39	GEB2/IO105RSB1
40	GEC2/IO104RSB1
41	IO103RSB1
42	IO102RSB1
43	IO101RSB1
44	IO100RSB1
45	V_{CC}
46	GND
47	V_{CCI}B1
48	IO99RSB1
49	IO97RSB1
50	IO95RSB1
51	IO93RSB1
52	IO92RSB1
53	IO90RSB1
54	IO88RSB1
55	IO86RSB1
56	IO84RSB1
57	IO83RSB1
58	IO82RSB1
59	IO81RSB1
60	IO80RSB1
61	IO79RSB1
62	V_{CC}
63	GND
64	V_{CCI}B1
65	GDC2/IO72RSB1
66	GDB2/IO71RSB1
67	GDA2/IO70RSB1
68	GNDQ
69	TCK
70	TDI
71	TMS
72	VMV1

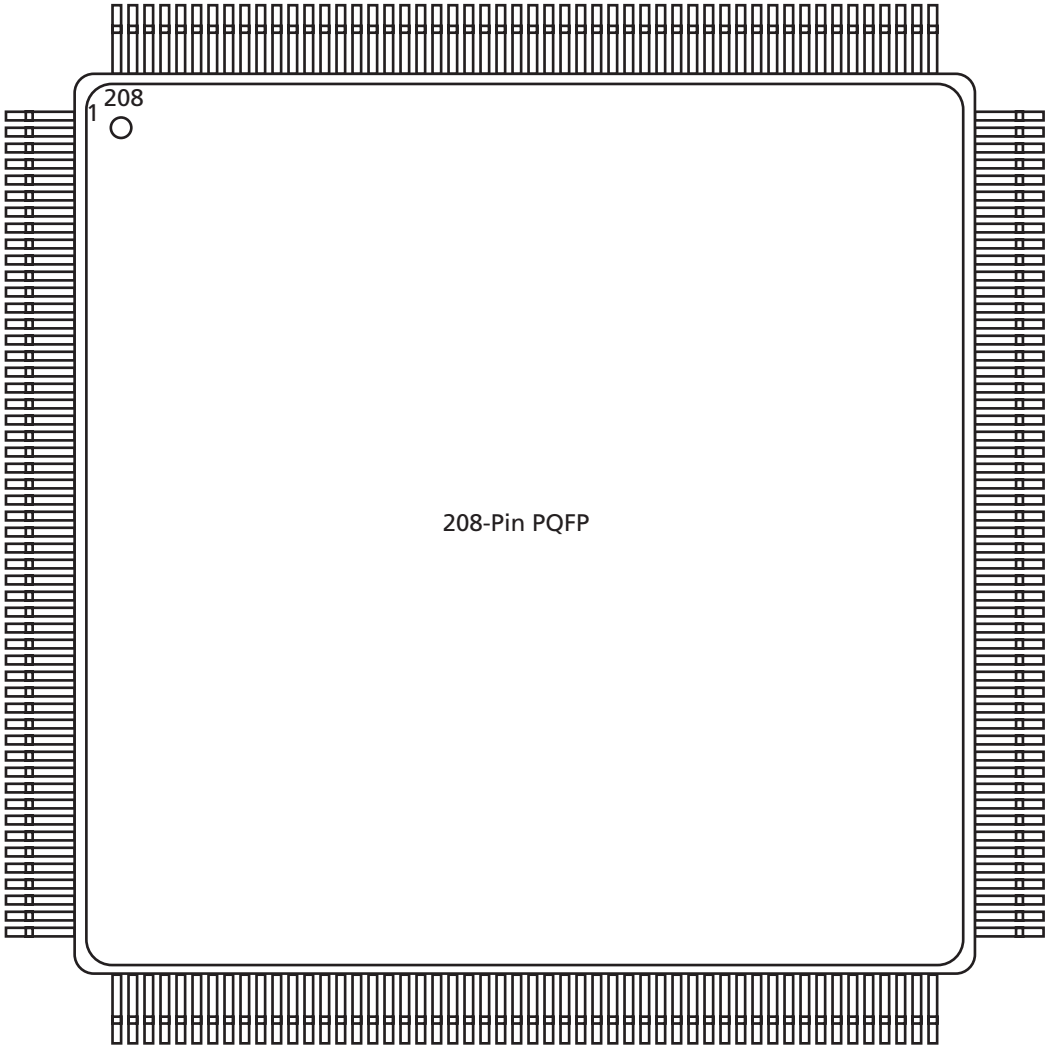
144_Pin TQFP*	
Pin Number	**A3P125 Function**
73	V_{PUMP}
74	NC
75	TDO
76	TRST
77	V_{JTAG}
78	GDA0/IO66RSB0
79	GDB0/IO64RSB0
80	GDB1/IO63RSB0
81	V_{CCI}B0
82	GND
83	IO60RSB0
84	GCC2/IO59RSB0
85	GCB2/IO58RSB0
86	GCA2/IO57RSB0
87	GCA0/IO56RSB0
88	GCA1/IO55RSB0
89	GCB0/IO54RSB0
90	GCB1/IO53RSB0
91	GCC0/IO52RSB0
92	GCC1/IO51RSB0
93	IO50RSB0
94	IO49RSB0
95	NC
96	NC
97	NC
98	V_{CCI}B0
99	GND
100	V_{CC}
101	IO47RSB0
102	GBC2/IO45RSB0
103	IO44RSB0
104	GBB2/IO43RSB0
105	IO42RSB0
106	GBA2/IO41RSB0
107	VMV0
108	GNDQ

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

144_Pin TQFP*	
Pin Number	**A3P125 Function**
109	GBA1/IO40RSB0
110	GBA0/IO39RSB0
111	GBB1/IO38RSB0
112	GBB0/IO37RSB0
113	GBC1/IO36RSB0
114	GBC0/IO35RSB0
115	IO34RSB0
116	IO33RSB0
117	V_{CCI}B0
118	GND
119	V_{CC}
120	IO29RSB0
121	IO28RSB0
122	IO27RSB0
123	IO25RSB0
124	IO23RSB0
125	IO21RSB0
126	IO19RSB0
127	IO17RSB0
128	IO16RSB0
129	IO14RSB0
130	IO12RSB0
131	IO10RSB0
132	IO08RSB0
133	IO06RSB0
134	V_{CCI}B0
135	GND
136	V_{CC}
137	GAC1/IO05RSB0
138	GAC0/IO04RSB0
139	GAB1/IO03RSB0
140	GAB0/IO02RSB0
141	GAA1/IO01RSB0
142	GAA0/IO00RSB0
143	GNDQ
144	VMV0

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

208-Pin PQFP



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

208-Pin PQFP*	
Pin Number	**A3P125 Function**
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	NC
8	NC
9	IO130RSB1
10	IO129RSB1
11	NC
12	IO128RSB1
13	NC
14	NC
15	NC
16	V_{CC}
17	GND
18	V_{CCI}B1
19	IO127RSB1
20	NC
21	GFC1/IO126RSB1
22	GFC0/IO125RSB1
23	GFB1/IO124RSB1
24	GFB0/IO123RSB1
25	V_{COMPLF}
26	GFA0/IO122RSB1
27	V_{CCPLF}
28	GFA1/IO121RSB1
29	GND
30	GFA2/IO120RSB1
31	NC
32	GFB2/IO119RSB1
33	NC
34	GFC2/IO118RSB1
35	IO117RSB1
36	NC
37	IO116RSB1
38	IO115RSB1

208-Pin PQFP*	
Pin Number	**A3P125 Function**
39	NC
40	V_{CCI}B1
41	GND
42	IO114RSB1
43	IO113RSB1
44	GEC1/IO112RSB1
45	GEC0/IO111RSB1
46	GEB1/IO110RSB1
47	GEB0/IO109RSB1
48	GEA1/IO108RSB1
49	GEA0/IO107RSB1
50	VMV1
51	GNDQ
52	GND
53	NC
54	NC
55	GEA2/IO106RSB1
56	GEB2/IO105RSB1
57	GEC2/IO104RSB1
58	IO103RSB1
59	IO102RSB1
60	IO101RSB1
61	IO100RSB1
62	V_{CCI}B1
63	IO99RSB1
64	IO98RSB1
65	GND
66	IO97RSB1
67	IO96RSB1
68	IO95RSB1
69	IO94RSB1
70	IO93RSB1
71	V_{CC}
72	V_{CCI}B1
73	IO92RSB1
74	IO91RSB1
75	IO90RSB1
76	IO89RSB1

208-Pin PQFP*	
Pin Number	**A3P125 Function**
77	IO88RSB1
78	IO87RSB1
79	IO86RSB1
80	IO85RSB1
81	GND
82	IO84RSB1
83	IO83RSB1
84	IO82RSB1
85	IO81RSB1
86	IO80RSB1
87	IO79RSB1
88	V_{CC}
89	V_{CCI}B1
90	IO78RSB1
91	IO77RSB1
92	IO76RSB1
93	IO75RSB1
94	IO74RSB1
95	IO73RSB1
96	GDC2/IO72RSB1
97	GND
98	GDB2/IO71RSB1
99	GDA2/IO70RSB1
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV1
105	GND
106	V_{PUMP}
107	NC
108	TDO
109	TRST
110	V_{JTAG}
111	GDA0/IO66RSB0
112	GDA1/IO65RSB0
113	GDB0/IO64RSB0
114	GDB1/IO63RSB0

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

208-Pin PQFP*	
Pin Number	**A3P125 Function**
115	GDC0/IO62RSB0
116	GDC1/IO61RSB0
117	NC
118	NC
119	NC
120	NC
121	NC
122	GND
123	V_{CCI}B0
124	NC
125	NC
126	V_{CC}
127	IO60RSB0
128	GCC2/IO59RSB0
129	GCB2/IO58RSB0
130	GND
131	GCA2/IO57RSB0
132	GCA0/IO56RSB0
133	GCA1/IO55RSB0
134	GCB0/IO54RSB0
135	GCB1/IO53RSB0
136	GCC0/IO52RSB0
137	GCC1/IO51RSB0
138	IO50RSB0
139	IO49RSB0
140	V_{CCI}B0
141	GND
142	V_{CC}
143	IO48RSB0
144	IO47RSB0
145	IO46RSB0
146	NC
147	NC
148	NC
149	GBC2/IO45RSB0
150	IO44RSB0
151	GBB2/IO43RSB0
152	IO42RSB0

208-Pin PQFP*	
Pin Number	**A3P125 Function**
153	GBA2/IO41RSB0
154	VMV0
155	GNDQ
156	GND
157	NC
158	GBA1/IO40RSB0
159	GBA0/IO39RSB0
160	GBB1/IO38RSB0
161	GBB0/IO37RSB0
162	GND
163	GBC1/IO36RSB0
164	GBC0/IO35RSB0
165	IO34RSB0
166	IO33RSB0
167	IO32RSB0
168	IO31RSB0
169	IO30RSB0
170	V_{CCI}B0
171	V_{CC}
172	IO29RSB0
173	IO28RSB0
174	IO27RSB0
175	IO26RSB0
176	IO25RSB0
177	IO24RSB0
178	GND
179	IO23RSB0
180	IO22RSB0
181	IO21RSB0
182	IO20RSB0
183	IO19RSB0
184	IO18RSB0
185	IO17RSB0
186	V_{CCI}B0
187	V_{CC}
188	IO16RSB0
189	IO15RSB0
190	IO14RSB0

208-Pin PQFP*	
Pin Number	**A3P125 Function**
191	IO13RSB0
192	IO12RSB0
193	IO11RSB0
194	IO10RSB0
195	GND
196	IO09RSB0
197	IO08RSB0
198	IO07RSB0
199	IO06RSB0
200	V_{CCI}B0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

208-Pin PQFP*	
Pin Number	**A3P250 Function**
1	GND
2	GAA2/IO118PDB3
3	IO118NDB3
4	GAB2/IO117PDB3
5	IO117NDB3
6	GAC2/IO116PDB3
7	IO116NDB3
8	IO115PDB3
9	IO115NDB3
10	IO114PDB3
11	IO114NDB3
12	IO113PDB3
13	IO113NDB3
14	IO112PDB3
15	IO112NDB3
16	V_{CC}
17	GND
18	V_{CCI}B3
19	IO111PDB3
20	IO111NDB3
21	GFC1/IO110PDB3
22	GFC0/IO110NDB3
23	GFB1/IO109PDB3
24	GFB0/IO109NDB3
25	V_{COMPLF}
26	GFA0/IO108NPB3
27	V_{CCPLF}
28	GFA1/IO108PPB3
29	GND
30	GFA2/IO107PDB3
31	IO107NDB3
32	GFB2/IO106PDB3
33	IO106NDB3
34	GFC2/IO105PDB3
35	IO105NDB3
36	NC
37	IO104PDB3
38	IO104NDB3

208-Pin PQFP*	
Pin Number	**A3P250 Function**
39	IO103PSB3
40	V_{CCI}B3
41	GND
42	IO101PDB3
43	IO101NDB3
44	GEC1/IO100PDB3
45	GEC0/IO100NDB3
46	GEB1/IO99PDB3
47	GEB0/IO99NDB3
48	GEA1/IO98PDB3
49	GEA0/IO98NDB3
50	VMV3
51	GNDQ
52	GND
53	NC
54	NC
55	GEA2/IO97RSB2
56	GEB2/IO96RSB2
57	GEC2/IO95RSB2
58	IO94RSB2
59	IO93RSB2
60	IO92RSB2
61	IO91RSB2
62	V_{CCI}B2
63	IO90RSB2
64	IO89RSB2
65	GND
66	IO88RSB2
67	IO87RSB2
68	IO86RSB2
69	IO85RSB2
70	IO84RSB2
71	V_{CC}
72	V_{CCI}B2
73	IO83RSB2
74	IO82RSB2
75	IO81RSB2
76	IO80RSB2

208-Pin PQFP*	
Pin Number	**A3P250 Function**
77	IO79RSB2
78	IO78RSB2
79	IO77RSB2
80	IO76RSB2
81	GND
82	IO75RSB2
83	IO74RSB2
84	IO73RSB2
85	IO72RSB2
86	IO71RSB2
87	IO70RSB2
88	V_{CC}
89	V_{CCI}B2
90	IO69RSB2
91	IO68RSB2
92	IO67RSB2
93	IO66RSB2
94	IO65RSB2
95	IO64RSB2
96	GDC2/IO63RSB2
97	GND
98	GDB2/IO62RSB2
99	GDA2/IO61RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	V_{PUMP}
107	NC
108	TDO
109	TRST
110	V_{JTAG}
111	GDA0/IO60NDB1
112	GDA1/IO60PDB1
113	GDB0/IO59NDB1
114	GDB1/IO59PDB1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

208-Pin PQFP*	
Pin Number	**A3P250 Function**
115	GDC0/IO58NDB1
116	GDC1/IO58PDB1
117	IO57NDB1
118	IO57PDB1
119	IO56NDB1
120	IO56PDB1
121	IO55RSB1
122	GND
123	V_{CCI}B1
124	NC
125	NC
126	V_{CC}
127	IO53NDB1
128	GCC2/IO53PDB1
129	GCB2/IO52PSB1
130	GND
131	GCA2/IO51PSB1
132	GCA1/IO50PDB1
133	GCA0/IO50NDB1
134	GCB0/IO49NDB1
135	GCB1/IO49PDB1
136	GCC0/IO48NDB1
137	GCC1/IO48PDB1
138	IO47NDB1
139	IO47PDB1
140	V_{CCI}B1
141	GND
142	V_{CC}
143	IO46RSB1
144	IO45NDB1
145	IO45PDB1
146	IO44NDB1
147	IO44PDB1
148	IO43NDB1
149	GBC2/IO43PDB1
150	IO42NDB1
151	GBB2/IO42PDB1
152	IO41NDB1

208-Pin PQFP*	
Pin Number	**A3P250 Function**
153	GBA2/IO41PDB1
154	VMV1
155	GNDQ
156	GND
157	NC
158	GBA1/IO40RSB0
159	GBA0/IO39RSB0
160	GBB1/IO38RSB0
161	GBB0/IO37RSB0
162	GND
163	GBC1/IO36RSB0
164	GBC0/IO35RSB0
165	IO34RSB0
166	IO33RSB0
167	IO32RSB0
168	IO31RSB0
169	IO30RSB0
170	V_{CCI}B0
171	V_{CC}
172	IO29RSB0
173	IO28RSB0
174	IO27RSB0
175	IO26RSB0
176	IO25RSB0
177	IO24RSB0
178	GND
179	IO23RSB0
180	IO22RSB0
181	IO21RSB0
182	IO20RSB0
183	IO19RSB0
184	IO18RSB0
185	IO17RSB0
186	V_{CCI}B0
187	V_{CC}
188	IO16RSB0
189	IO15RSB0
190	IO14RSB0

208-Pin PQFP*	
Pin Number	**A3P250 Function**
191	IO13RSB0
192	IO12RSB0
193	IO11RSB0
194	IO10RSB0
195	GND
196	IO09RSB0
197	IO08RSB0
198	IO07RSB0
199	IO06RSB0
200	V_{CCI}B0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

208-Pin PQFP*	
Pin Number	**A3P400 Function**
1	GND
2	GAA2/IO155PDB3
3	IO155NDB3
4	GAB2/IO154PDB3
5	IO154NDB3
6	GAC2/IO153PDB3
7	IO153NDB3
8	IO152PDB3
9	IO152NDB3
10	IO151PDB3
11	IO151NDB3
12	IO150PDB3
13	IO150NDB3
14	IO149PDB3
15	IO149NDB3
16	V_{CC}
17	GND
18	V_{CCI}B3
19	IO148PDB3
20	IO148NDB3
21	GFC1/IO147PDB3
22	GFC0/IO147NDB3
23	GFB1/IO146PDB3
24	GFB0/IO146NDB3
25	V_{COMPLF}
26	GFA0/IO145NPB3
27	V_{CCPLF}
28	GFA1/IO145PPB3
29	GND
30	GFA2/IO144PDB3
31	IO144NDB3
32	GFB2/IO143PDB3
33	IO143NDB3
34	GFC2/IO142PDB3
35	IO142NDB3
36	NC
37	IO141PDB3
38	IO141NDB3

208-Pin PQFP*	
Pin Number	**A3P400 Function**
39	IO140PSB3
40	V_{CCI}B3
41	GND
42	IO138PDB3
43	IO138NDB3
44	GEC1/IO137PDB3
45	GEC0/IO137NDB3
46	GEB1/IO136PDB3
47	GEB0/IO136NDB3
48	GEA1/IO135PDB3
49	GEA0/IO135NDB3
50	VMV3
51	GNDQ
52	GND
53	NC
54	NC
55	GEA2/IO134RSB2
56	GEB2/IO133RSB2
57	GEC2/IO132RSB2
58	IO131RSB2
59	IO130RSB2
60	IO129RSB2
61	IO128RSB2
62	V_{CCI}B2
63	IO126RSB2
64	IO124RSB2
65	GND
66	IO122RSB2
67	IO120RSB2
68	IO118RSB2
69	IO116RSB2
70	IO114RSB2
71	V_{CC}
72	V_{CCI}B2
73	IO112RSB2
74	IO111RSB2
75	IO110RSB2
76	IO109RSB2

208-Pin PQFP*	
Pin Number	**A3P400 Function**
77	IO108RSB2
78	IO107RSB2
79	IO106RSB2
80	IO103RSB2
81	GND
82	IO102RSB2
83	IO101RSB2
84	IO100RSB2
85	IO99RSB2
86	IO98RSB2
87	IO97RSB2
88	V_{CC}
89	V_{CCI}B2
90	IO94RSB2
91	IO92RSB2
92	IO90RSB2
93	IO88RSB2
94	IO86RSB2
95	IO84RSB2
96	GDC2/IO82RSB2
97	GND
98	GDB2/IO81RSB2
99	GDA2/IO80RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	V_{PUMP}
107	NC
108	TDO
109	TRST
110	V_{JTAG}
111	GDA0/IO79NDB1
112	GDA1/IO79PDB1
113	GDB0/IO78NDB1
114	GDB1/IO78PDB1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

208-Pin PQFP*	
Pin Number	**A3P400 Function**
115	GDC0/IO77NDB1
116	GDC1/IO77PDB1
117	IO76NDB1
118	IO76PDB1
119	IO75NDB1
120	IO75PDB1
121	IO74RSB1
122	GND
123	V_{CCI}B1
124	NC
125	NC
126	V_{CC}
127	IO73PSB1
128	GCC2/IO72PSB1
129	GCB2/IO71PSB1
130	GND
131	GCA2/IO70PSB1
132	GCA1/IO69PDB1
133	GCA0/IO69NDB1
134	GCB0/IO68NDB1
135	GCB1/IO68PDB1
136	GCC0/IO67NDB1
137	GCC1/IO67PDB1
138	IO66NDB1
139	IO66PDB1
140	V_{CCI}B1
141	GND
142	V_{CC}
143	IO65RSB1
144	IO64NDB1
145	IO64PDB1
146	IO63NDB1
147	IO63PDB1
148	IO62NDB1
149	GBC2/IO62PDB1
150	IO61NDB1
151	GBB2/IO61PDB1
152	IO60NDB1

208-Pin PQFP*	
Pin Number	**A3P400 Function**
153	GBA2/IO60PDB1
154	VMV1
155	GNDQ
156	GND
157	NC
158	GBA1/IO59RSB0
159	GBA0/IO58RSB0
160	GBB1/IO57RSB0
161	GBB0/IO56RSB0
162	GND
163	GBC1/IO55RSB0
164	GBC0/IO54RSB0
165	IO52RSB0
166	IO50RSB0
167	IO48RSB0
168	IO46RSB0
169	IO44RSB0
170	V_{CCI}B0
171	V_{CC}
172	IO37RSB0
173	IO36RSB0
174	IO35RSB0
175	IO34RSB0
176	IO33RSB0
177	IO32RSB0
178	GND
179	IO31RSB0
180	IO30RSB0
181	IO29RSB0
182	IO28RSB0
183	IO27RSB0
184	IO25RSB0
185	IO23RSB0
186	V_{CCI}B0
187	V_{CC}
188	IO19RSB0
189	IO17RSB0
190	IO15RSB0

208-Pin PQFP*	
Pin Number	**A3P400 Function**
191	IO13RSB0
192	IO12RSB0
193	IO11RSB0
194	IO10RSB0
195	GND
196	IO09RSB0
197	IO08RSB0
198	IO07RSB0
199	IO06RSB0
200	V_{CCI}B0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

208-Pin PQFP*	
Pin Number	**A3P600 Function**
1	GND
2	GAA2/IO170PDB3
3	IO170NDB3
4	GAB2/IO169PDB3
5	IO169NDB3
6	GAC2/IO168PDB3
7	IO168NDB3
8	IO167PDB3
9	IO167NDB3
10	IO166PDB3
11	IO166NDB3
12	IO165PDB3
13	IO165NDB3
14	IO164PDB3
15	IO164NDB3
16	V_{CC}
17	GND
18	V_{CCI}B3
19	IO163PDB3
20	IO163NDB3
21	GFC1/IO161PDB3
22	GFC0/IO161NDB3
23	GFB1/IO160PDB3
24	GFB0/IO160NDB3
25	V_{COMPLF}
26	GFA0/IO159NPB3
27	V_{CCPLF}
28	GFA1/IO159PPB3
29	GND
30	GFA2/IO158PDB3
31	IO158NDB3
32	GFB2/IO157PDB3
33	IO157NDB3
34	GFC2/IO156PDB3
35	IO156NDB3
36	V_{CC}
37	IO147PDB3
38	IO147NDB3

208-Pin PQFP*	
Pin Number	**A3P600 Function**
39	IO146PSB3
40	V_{CCI}B3
41	GND
42	IO145PDB3
43	IO145NDB3
44	GEC1/IO144PDB3
45	GEC0/IO144NDB3
46	GEB1/IO143PDB3
47	GEB0/IO143NDB3
48	GEA1/IO142PDB3
49	GEA0/IO142NDB3
50	VMV3
51	GNDQ
52	GND
53	NC
54	GEA2/IO141RSB2
55	GEB2/IO140RSB2
56	GEC2/IO139RSB2
57	IO138RSB2
58	IO137RSB2
59	IO136RSB2
60	IO135RSB2
61	IO134RSB2
62	V_{CCI}B2
63	IO133RSB2
64	IO131RSB2
65	GND
66	IO129RSB2
67	IO127RSB2
68	IO125RSB2
69	IO123RSB2
70	IO121RSB2
71	V_{CC}
72	V_{CCI}B2
73	IO118RSB2
74	IO117RSB2
75	IO116RSB2
76	IO115RSB2

208-Pin PQFP*	
Pin Number	**A3P600 Function**
77	IO114RSB2
78	IO113RSB2
79	IO112RSB2
80	IO110RSB2
81	GND
82	IO109RSB2
83	IO108RSB2
84	IO107RSB2
85	IO106RSB2
86	IO105RSB2
87	IO104RSB2
88	V_{CC}
89	V_{CCI}B2
90	IO102RSB2
91	IO100RSB2
92	IO98RSB2
93	IO96RSB2
94	IO94RSB2
95	IO90RSB2
96	GDC2/IO89RSB2
97	GND
98	GDB2/IO88RSB2
99	GDA2/IO87RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	V_{PUMP}
107	GNDQ
108	TDO
109	TRST
110	V_{JTAG}
111	GDA0/IO86NDB1
112	GDA1/IO86PDB1
113	GDB0/IO85NDB1
114	GDB1/IO85PDB1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

208-Pin PQFP*	
Pin Number	**A3P600 Function**
115	GDC0/IO84NDB1
116	GDC1/IO84PDB1
117	IO82NDB1
118	IO82PDB1
119	IO80NDB1
120	IO80PDB1
121	IO79PSB1
122	GND
123	V_{CCI}B1
124	IO75NDB1
125	IO75PDB1
126	NC
127	IO73NDB1
128	GCC2/IO73PDB1
129	GCB2/IO72PSB1
130	GND
131	GCA2/IO71PSB1
132	GCA1/IO70PDB1
133	GCA0/IO70NDB1
134	GCB0/IO69NDB1
135	GCB1/IO69PDB1
136	GCC0/IO68NDB1
137	GCC1/IO68PDB1
138	IO66NDB1
139	IO66PDB1
140	V_{CCI}B1
141	GND
142	V_{CC}
143	IO65PSB1
144	IO64NDB1
145	IO64PDB1
146	IO63NDB1
147	IO63PDB1
148	IO62NDB1
149	GBC2/IO62PDB1
150	IO61NDB1
151	GBB2/IO61PDB1
152	IO60NDB1

208-Pin PQFP*	
Pin Number	**A3P600 Function**
153	GBA2/IO60PDB1
154	VMV1
155	GNDQ
156	GND
157	NC
158	GBA1/IO59RSB0
159	GBA0/IO58RSB0
160	GBB1/IO57RSB0
161	GBB0/IO56RSB0
162	GND
163	GBC1/IO55RSB0
164	GBC0/IO54RSB0
165	IO52RSB0
166	IO50RSB0
167	IO48RSB0
168	IO46RSB0
169	IO44RSB0
170	V_{CCI}B0
171	V_{CC}
172	IO36RSB0
173	IO35RSB0
174	IO34RSB0
175	IO33RSB0
176	IO32RSB0
177	IO31RSB0
178	GND
179	IO29RSB0
180	IO28RSB0
181	IO27RSB0
182	IO26RSB0
183	IO25RSB0
184	IO24RSB0
185	IO23RSB0
186	V_{CCI}B0
187	V_{CC}
188	IO20RSB0
189	IO19RSB0
190	IO18RSB0

208-Pin PQFP*	
Pin Number	**A3P600 Function**
191	IO17RSB0
192	IO16RSB0
193	IO14RSB0
194	IO12RSB0
195	GND
196	IO10RSB0
197	IO09RSB0
198	IO08RSB0
199	IO07RSB0
200	V_{CCI}B0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

208-Pin PQFP*	
Pin Number	**A3P1000 Function**
1	GND
2	GAA2/IO219PDB3
3	IO219NDB3
4	GAB2/IO218PDB3
5	IO218NDB3
6	GAC2/IO217PDB3
7	IO217NDB3
8	IO216PDB3
9	IO216NDB3
10	IO215PDB3
11	IO215NDB3
12	IO214PDB3
13	IO214NDB3
14	IO213PDB3
15	IO213NDB3
16	V_{CC}
17	GND
18	V_{CCI}B3
19	IO211PDB3
20	IO211NDB3
21	GFC1/IO206PDB3
22	GFC0/IO206NDB3
23	GFB1/IO205PDB3
24	GFB0/IO205NDB3
25	V_{COMPLF}
26	GFA0/IO204NPB3
27	V_{CCPLF}
28	GFA1/IO204PPB3
29	GND
30	GFA2/IO203PDB3
31	IO203NDB3
32	GFB2/IO202PDB3
33	IO202NDB3
34	GFC2/IO201PDB3
35	IO201NDB3
36	V_{CC}
37	IO191PDB3
38	IO191NDB3

208-Pin PQFP*	
Pin Number	**A3P1000 Function**
39	IO189PSB3
40	V_{CCI}B3
41	GND
42	IO188PDB3
43	IO188NDB3
44	GEC1/IO187PDB3
45	GEC0/IO187NDB3
46	GEB1/IO186PDB3
47	GEB0/IO186NDB3
48	GEA1/IO185PDB3
49	GEA0/IO185NDB3
50	VMV3
51	GNDQ
52	GND
53	NC
54	GEA2/IO184RSB2
55	GEB2/IO183RSB2
56	GEC2/IO182RSB2
57	IO181RSB2
58	IO180RSB2
59	IO179RSB2
60	IO178RSB2
61	IO177RSB2
62	V_{CCI}B2
63	IO175RSB2
64	IO173RSB2
65	GND
66	IO171RSB2
67	IO169RSB2
68	IO167RSB2
69	IO165RSB2
70	IO163RSB2
71	V_{CC}
72	V_{CCI}B2
73	IO159RSB2
74	IO157RSB2
75	IO155RSB2
76	IO153RSB2

208-Pin PQFP*	
Pin Number	**A3P1000 Function**
77	IO151RSB2
78	IO149RSB2
79	IO147RSB2
80	IO145RSB2
81	GND
82	IO140RSB2
83	IO138RSB2
84	IO136RSB2
85	IO134RSB2
86	IO132RSB2
87	IO130RSB2
88	V_{CC}
89	V_{CCI}B2
90	IO125RSB2
91	IO123RSB2
92	IO121RSB2
93	IO119RSB2
94	IO117RSB2
95	IO115RSB2
96	GDC2/IO113RSB2
97	GND
98	GDB2/IO112RSB2
99	GDA2/IO111RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	V_{PUMP}
107	GNDQ
108	TDO
109	TRST
110	V_{JTAG}
111	GDA0/IO110NDB1
112	GDA1/IO110PDB1
113	GDB0/IO109NDB1
114	GDB1/IO109PDB1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

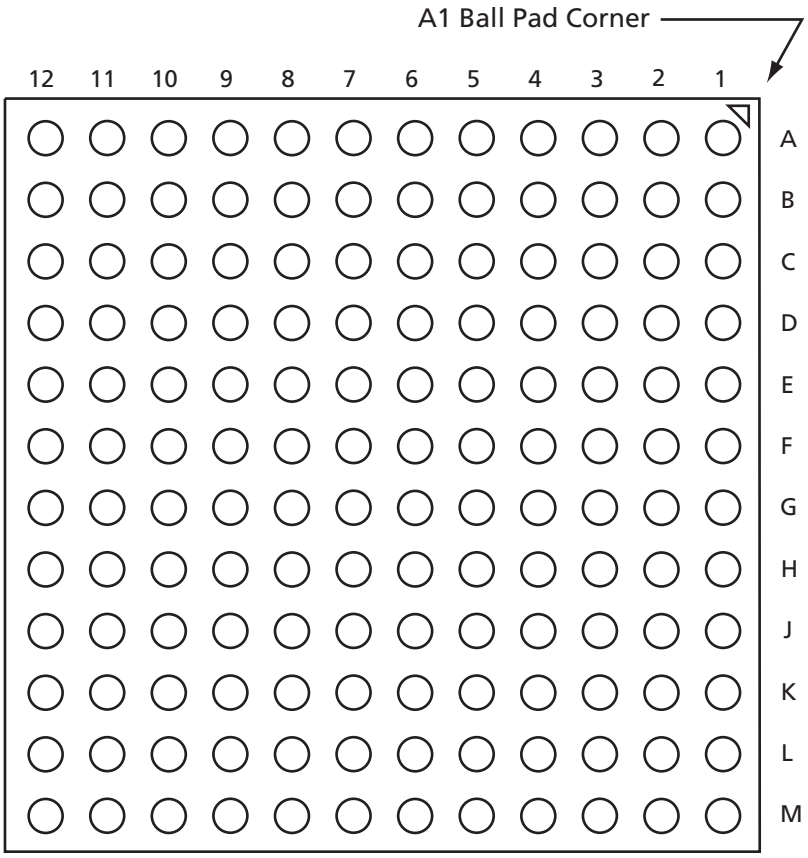
208-Pin PQFP*	
Pin Number	**A3P1000 Function**
115	GDC0/IO108NDB1
116	GDC1/IO108PDB1
117	IO106NDB1
118	IO106PDB1
119	IO104NDB1
120	IO104PDB1
121	IO102PSB1
122	GND
123	V_{CCI}B1
124	IO97NDB1
125	IO97PDB1
126	NC
127	IO93NDB1
128	GCC2/IO93PDB1
129	GCB2/IO92PSB1
130	GND
131	GCA2/IO91PSB1
132	GCA1/IO90PDB1
133	GCA0/IO90NDB1
134	GCB0/IO89NDB1
135	GCB1/IO89PDB1
136	GCC0/IO88NDB1
137	GCC1/IO88PDB1
138	IO85NDB1
139	IO85PDB1
140	V_{CCI}B1
141	GND
142	V_{CC}
143	IO83PSB1
144	IO82NDB1
145	IO82PDB1
146	IO81NDB1
147	IO81PDB1
148	IO80NDB1
149	GBC2/IO80PDB1
150	IO79NDB1
151	GBB2/IO79PDB1
152	IO78NDB1

208-Pin PQFP*	
Pin Number	**A3P1000 Function**
153	GBA2/IO78PDB1
154	VMV1
155	GNDQ
156	GND
157	NC
158	GBA1/IO77RSB0
159	GBA0/IO76RSB0
160	GBB1/IO75RSB0
161	GBB0/IO74RSB0
162	GND
163	GBC1/IO73RSB0
164	GBC0/IO72RSB0
165	IO70RSB0
166	IO67RSB0
167	IO63RSB0
168	IO60RSB0
169	IO57RSB0
170	V_{CCI}B0
171	V_{CC}
172	IO54RSB0
173	IO51RSB0
174	IO48RSB0
175	IO45RSB0
176	IO42RSB0
177	IO40RSB0
178	GND
179	IO38RSB0
180	IO35RSB0
181	IO33RSB0
182	IO31RSB0
183	IO29RSB0
184	IO27RSB0
185	IO25RSB0
186	V_{CCI}B0
187	V_{CC}
188	IO22RSB0
189	IO20RSB0
190	IO18RSB0

208-Pin PQFP*	
Pin Number	**A3P1000 Function**
191	IO16RSB0
192	IO15RSB0
193	IO14RSB0
194	IO13RSB0
195	GND
196	IO12RSB0
197	IO11RSB0
198	IO10RSB0
199	IO09RSB0
200	V_{CCI}B0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

144-Pin FBGA



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

144-Pin FBGA*	
Pin Number	**A3P060 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO04RSB0
A4	GAB1/IO05RSB0
A5	IO08RSB0
A6	GND
A7	IO11RSB0
A8	V_{CC}
A9	IO16RSB0
A10	GBA0/IO23RSB0
A11	GBA1/IO24RSB0
A12	GNDQ
B1	GAB2/IO53RSB1
B2	GND
B3	GAA0/IO02RSB0
B4	GAA1/IO03RSB0
B5	IO00RSB0
B6	IO10RSB0
B7	IO12RSB0
B8	IO14RSB0
B9	GBB0/IO21RSB0
B10	GBB1/IO22RSB0
B11	GND
B12	VMV0
C1	IO95RSB1
C2	GFA2/IO83RSB1
C3	GAC2/IO94RSB1
C4	V_{CC}
C5	IO01RSB0
C6	IO09RSB0
C7	IO13RSB0
C8	IO15RSB0
C9	IO17RSB0
C10	GBA2/IO25RSB0
C11	IO26RSB0
C12	GBC2/IO29RSB0

144-Pin FBGA*	
Pin Number	**A3P060 Function**
D1	IO91RSB1
D2	IO92RSB1
D3	IO93RSB1
D4	GAA2/IO51RSB1
D5	GAC0/IO06RSB0
D6	GAC1/IO07RSB0
D7	GBC0/IO19RSB0
D8	GBC1/IO20RSB0
D9	GBB2/IO27RSB0
D10	IO18RSB0
D11	IO28RSB0
D12	GCB1/IO37RSB0
E1	V_{CC}
E2	GFC0/IO88RSB1
E3	GFC1/IO89RSB1
E4	V_{CCI}B1
E5	IO52RSB1
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	GCC1/IO35RSB0
E9	V_{CCI}B0
E10	V_{CC}
E11	GCA0/IO40RSB0
E12	IO30RSB0
F1	GFB0/IO86RSB1
F2	V_{COMPLF}
F3	GFB1/IO87RSB1
F4	IO90RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO36RSB0
F9	GCB0/IO38RSB0
F10	GND
F11	GCA1/IO39RSB0
F12	GCA2/IO41RSB0

144-Pin FBGA*	
Pin Number	**A3P060 Function**
G1	GFA1/IO84RSB1
G2	GND
G3	V_{CCPLF}
G4	GFA0/IO85RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO45RSB0
G9	IO32RSB0
G10	GCC2/IO43RSB0
G11	IO31RSB0
G12	GCB2/IO42RSB0
H1	V_{CC}
H2	GFB2/IO82RSB1
H3	GFC2/IO81RSB1
H4	GEC1/IO77RSB1
H5	V_{CC}
H6	IO34RSB0
H7	IO44RSB0
H8	GDB2/IO56RSB1
H9	GDC0/IO46RSB0
H10	V_{CCI}B0
H11	IO33RSB0
H12	V_{CC}
J1	GEB1/IO75RSB1
J2	IO78RSB1
J3	V_{CCI}B1
J4	GEC0/IO76RSB1
J5	IO79RSB1
J6	IO80RSB1
J7	V_{CC}
J8	TCK
J9	GDA2/IO55RSB1
J10	TDO
J11	GDA1/IO49RSB0
J12	GDB1/IO47RSB0

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

144-Pin FBGA*	
Pin Number	**A3P060 Function**
K1	GEB0/IO74RSB1
K2	GEA1/IO73RSB1
K3	GEA0/IO72RSB1
K4	GEA2/IO71RSB1
K5	IO65RSB1
K6	IO64RSB1
K7	GND
K8	IO54RSB1
K9	GDC2/IO57RSB1
K10	GND
K11	GDA0/IO50RSB0
K12	GDB0/IO48RSB0
L1	GND
L2	VMV1
L3	GEB2/IO70RSB1
L4	IO67RSB1
L5	V_{CCI}B1
L6	IO62RSB1
L7	IO59RSB1
L8	IO58RSB1
L9	TMS
L10	V_{JTAG}
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO69RSB1
M3	IO68RSB1
M4	IO66RSB1
M5	IO63RSB1
M6	IO61RSB1
M7	IO60RSB1
M8	NC
M9	TDI
M10	V_{CCI}B1
M11	V_{PUMP}
M12	GNDQ

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

144-Pin FBGA*	
Pin Number	**A3P250 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO16RSB0
A6	GND
A7	IO29RSB0
A8	V_{CC}
A9	IO33RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO117PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO14RSB0
B6	IO19RSB0
B7	IO22RSB0
B8	IO30RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV1
C1	IO117NDB3
C2	GFA2/IO107PPB3
C3	GAC2/IO116PDB3
C4	V_{CC}
C5	IO12RSB0
C6	IO17RSB0
C7	IO24RSB0
C8	IO31RSB0
C9	IO34RSB0
C10	GBA2/IO41PDB1
C11	IO41NDB1
C12	GBC2/IO43PPB1

144-Pin FBGA*	
Pin Number	**A3P250 Function**
D1	IO112NDB3
D2	IO112PDB3
D3	IO116NDB3
D4	GAA2/IO118PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO42PDB1
D10	IO42NDB1
D11	IO43NPB1
D12	GCB1/IO49PPB1
E1	V_{CC}
E2	GFC0/IO110NDB3
E3	GFC1/IO110PDB3
E4	V_{CCI}B3
E5	IO118NPB3
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	GCC1/IO48PDB1
E9	V_{CCI}B1
E10	V_{CC}
E11	GCA0/IO50NDB1
E12	IO51NDB1
F1	GFB0/IO109NPB3
F2	V_{COMPLF}
F3	GFB1/IO109PPB3
F4	IO107NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO48NDB1
F9	GCB0/IO49NPB1
F10	GND
F11	GCA1/IO50PDB1
F12	GCA2/IO51PDB1

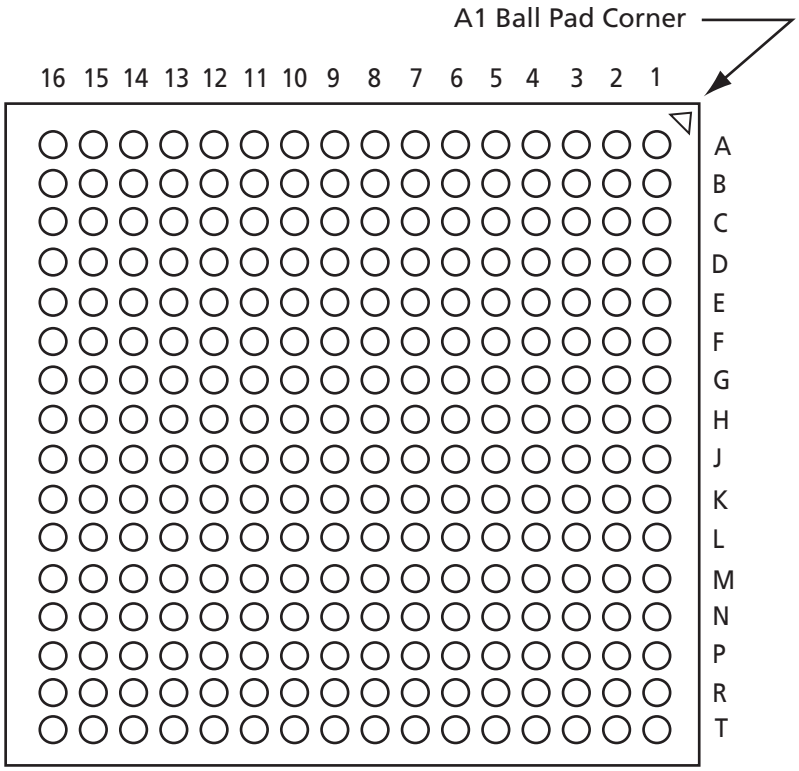
144-Pin FBGA*	
Pin Number	**A3P250 Function**
G1	GFA1/IO108PPB3
G2	GND
G3	V_{CCPLF}
G4	GFA0/IO108NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO58PPB1
G9	IO53NDB1
G10	GCC2/IO53PDB1
G11	IO52NDB1
G12	GCB2/IO52PDB1
H1	V_{CC}
H2	GFB2/IO106PDB3
H3	GFC2/IO105PSB3
H4	GEC1/IO100PDB3
H5	V_{CC}
H6	IO79RSB2
H7	IO65RSB2
H8	GDB2/IO62RSB2
H9	GDC0/IO58NPB1
H10	V_{CCI}B1
H11	IO54PSB1
H12	V_{CC}
J1	GEB1/IO99PDB3
J2	IO106NDB3
J3	V_{CCI}B3
J4	GEC0/IO100NDB3
J5	IO88RSB2
J6	IO81RSB2
J7	V_{CC}
J8	TCK
J9	GDA2/IO61RSB2
J10	TDO
J11	GDA1/IO60PDB1
J12	GDB1/IO59PDB1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

144-Pin FBGA*	
Pin Number	**A3P250 Function**
K1	GEB0/IO99NDB3
K2	GEA1/IO98PDB3
K3	GEA0/IO98NDB3
K4	GEA2/IO97RSB2
K5	IO90RSB2
K6	IO84RSB2
K7	GND
K8	IO66RSB2
K9	GDC2/IO63RSB2
K10	GND
K11	GDA0/IO60NDB1
K12	GDB0/IO59NDB1
L1	GND
L2	VMV3
L3	GEB2/IO96RSB2
L4	IO91RSB2
L5	V_{CCI}B2
L6	IO82RSB2
L7	IO80RSB2
L8	IO72RSB2
L9	TMS
L10	V_{JTAG}
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO95RSB2
M3	IO92RSB2
M4	IO89RSB2
M5	IO87RSB2
M6	IO85RSB2
M7	IO78RSB2
M8	IO76RSB2
M9	TDI
M10	V_{CCI}B2
M11	V_{PUMP}
M12	GNDQ

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

256-Pin FBGA



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

256-Pin FBGA*	
Pin Number	**A3P250 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO07RSB0
A6	IO10RSB0
A7	IO11RSB0
A8	IO15RSB0
A9	IO20RSB0
A10	IO25RSB0
A11	IO29RSB0
A12	IO33RSB0
A13	GBB1/IO38RSB0
A14	GBA0/IO39RSB0
A15	GBA1/IO40RSB0
A16	GND
B1	GAB2/IO117PDB3
B2	GAA2/IO118PDB3
B3	NC
B4	GAB1/IO03RSB0
B5	IO06RSB0
B6	IO09RSB0
B7	IO12RSB0
B8	IO16RSB0
B9	IO21RSB0
B10	IO26RSB0
B11	IO30RSB0
B12	GBC1/IO36RSB0
B13	GBB0/IO37RSB0
B14	NC
B15	GBA2/IO41PDB1
B16	IO41NDB1
C1	IO117NDB3
C2	IO118NDB3
C3	NC
C4	NC
C5	GAC0/IO04RSB0

256-Pin FBGA*	
Pin Number	**A3P250 Function**
C6	GAC1/IO05RSB0
C7	IO13RSB0
C8	IO17RSB0
C9	IO22RSB0
C10	IO27RSB0
C11	IO31RSB0
C12	GBC0/IO35RSB0
C13	IO34RSB0
C14	NC
C15	IO42NPB1
C16	IO44PDB1
D1	IO114NDB3
D2	IO114PDB3
D3	GAC2/IO116PDB3
D4	NC
D5	GNDQ
D6	IO08RSB0
D7	IO14RSB0
D8	IO18RSB0
D9	IO23RSB0
D10	IO28RSB0
D11	IO32RSB0
D12	GNDQ
D13	NC
D14	GBB2/IO42PPB1
D15	NC
D16	IO44NDB1
E1	IO113PDB3
E2	NC
E3	IO116NDB3
E4	IO115PDB3
E5	VMV0
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	IO19RSB0
E9	IO24RSB0
E10	V_{CCI}B0

256-Pin FBGA*	
Pin Number	**A3P250 Function**
E11	V_{CCI}B0
E12	VMV1
E13	GBC2/IO43PDB1
E14	IO46RSB1
E15	NC
E16	IO45PDB1
F1	IO113NDB3
F2	IO112PPB3
F3	NC
F4	IO115NDB3
F5	V_{CCI}B3
F6	GND
F7	V_{CC}
F8	V_{CC}
F9	V_{CC}
F10	V_{CC}
F11	GND
F12	V_{CCI}B1
F13	IO43NDB1
F14	NC
F15	IO47PPB1
F16	IO45NDB1
G1	IO111NDB3
G2	IO111PDB3
G3	IO112NPB3
G4	GFC1/IO110PPB3
G5	V_{CCI}B3
G6	V_{CC}
G7	GND
G8	GND
G9	GND
G10	GND
G11	V_{CC}
G12	V_{CCI}B1
G13	GCC1/IO48PPB1
G14	IO47NPB1
G15	IO54PDB1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

256-Pin FBGA*	
Pin Number	**A3P250 Function**
G16	IO54NDB1
H1	GFB0/IO109NPB3
H2	GFA0/IO108NDB3
H3	GFB1/IO109PPB3
H4	V_{COMPLF}
H5	GFC0/IO110NPB3
H6	V_{CC}
H7	GND
H8	GND
H9	GND
H10	GND
H11	V_{CC}
H12	GCC0/IO48NPB1
H13	GCB1/IO49PPB1
H14	GCA0/IO50NPB1
H15	NC
H16	GCB0/IO49NPB1
J1	GFA2/IO107PPB3
J2	GFA1/IO108PDB3
J3	V_{CCPLF}
J4	IO106NDB3
J5	GFB2/IO106PDB3
J6	V_{CC}
J7	GND
J8	GND
J9	GND
J10	GND
J11	V_{CC}
J12	GCB2/IO52PPB1
J13	GCA1/IO50PPB1
J14	GCC2/IO53PPB1
J15	NC
J16	GCA2/IO51PDB1
K1	GFC2/IO105PDB3
K2	IO107NPB3
K3	IO104PPB3
K4	NC

256-Pin FBGA*	
Pin Number	**A3P250 Function**
K5	$V_{CCI}B3$
K6	V_{CC}
K7	GND
K8	GND
K9	GND
K10	GND
K11	V_{CC}
K12	$V_{CCI}B1$
K13	IO52NPB1
K14	IO55RSB1
K15	IO53NPB1
K16	IO51NDB1
L1	IO105NDB3
L2	IO104NPB3
L3	NC
L4	IO102RSB3
L5	$V_{CCI}B3$
L6	GND
L7	V_{CC}
L8	V_{CC}
L9	V_{CC}
L10	V_{CC}
L11	GND
L12	$V_{CCI}B1$
L13	GDB0/IO59NPB1
L14	IO57NDB1
L15	IO57PDB1
L16	IO56PDB1
M1	IO103PDB3
M2	NC
M3	IO101NPB3
M4	GEC0/IO100NPB3
M5	VMV3
M6	$V_{CCI}B2$
M7	$V_{CCI}B2$
M8	NC
M9	IO74RSB2

256-Pin FBGA*	
Pin Number	**A3P250 Function**
M10	$V_{CCI}B2$
M11	$V_{CCI}B2$
M12	VMV2
M13	NC
M14	GDB1/IO59PPB1
M15	GDC1/IO58PDB1
M16	IO56NDB1
N1	IO103NDB3
N2	IO101PPB3
N3	GEC1/IO100PPB3
N4	NC
N5	GNDQ
N6	GEA2/IO97RSB2
N7	IO86RSB2
N8	IO82RSB2
N9	IO75RSB2
N10	IO69RSB2
N11	IO64RSB2
N12	GNDQ
N13	NC
N14	V_{JTAG}
N15	GDC0/IO58NDB1
N16	GDA1/IO60PDB1
P1	GEB1/IO99PDB3
P2	GEB0/IO99NDB3
P3	NC
P4	NC
P5	IO92RSB2
P6	IO89RSB2
P7	IO85RSB2
P8	IO81RSB2
P9	IO76RSB2
P10	IO71RSB2
P11	IO66RSB2
P12	NC
P13	TCK
P14	V_{PUMP}

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

256-Pin FBGA*	
Pin Number	**A3P250 Function**
P15	TRST
P16	GDA0/IO60NDB1
R1	GEA1/IO98PDB3
R2	GEA0/IO98NDB3
R3	NC
R4	GEC2/IO95RSB2
R5	IO91RSB2
R6	IO88RSB2
R7	IO84RSB2
R8	IO80RSB2
R9	IO77RSB2
R10	IO72RSB2
R11	IO68RSB2
R12	IO65RSB2
R13	GDB2/IO62RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO94RSB2
T3	GEB2/IO96RSB2
T4	IO93RSB2
T5	IO90RSB2
T6	IO87RSB2
T7	IO83RSB2
T8	IO79RSB2
T9	IO78RSB2
T10	IO73RSB2
T11	IO70RSB2
T12	GDC2/IO63RSB2
T13	IO67RSB2
T14	GDA2/IO61RSB2
T15	TMS
T16	GND

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

256-Pin FBGA*	
Pin Number	**A3P400 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO14RSB0
A6	IO18RSB0
A7	IO22RSB0
A8	IO27RSB0
A9	IO30RSB0
A10	IO39RSB0
A11	IO41RSB0
A12	IO46RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO154PDB3
B2	GAA2/IO155PPB3
B3	IO10RSB0
B4	GAB1/IO03RSB0
B5	IO12RSB0
B6	IO16RSB0
B7	IO21RSB0
B8	IO26RSB0
B9	IO31RSB0
B10	IO37RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO48RSB0
B15	GBA2/IO60PPB1
B16	IO50RSB0
C1	IO154NDB3
C2	IO08RSB0
C3	IO07RSB0
C4	IO06RSB0
C5	GAC0/IO04RSB0

256-Pin FBGA*	
Pin Number	**A3P400 Function**
C6	GAC1/IO05RSB0
C7	IO20RSB0
C8	IO25RSB0
C9	IO32RSB0
C10	IO38RSB0
C11	IO44RSB0
C12	GBC0/IO54RSB0
C13	IO51RSB0
C14	IO52RSB0
C15	IO53RSB0
C16	IO60NPB1
D1	IO152NPB3
D2	IO155NPB3
D3	GAC2/IO153PDB3
D4	IO09RSB0
D5	GNDQ
D6	IO15RSB0
D7	IO19RSB0
D8	IO24RSB0
D9	IO33RSB0
D10	IO40RSB0
D11	IO43RSB0
D12	GNDQ
D13	IO49RSB0
D14	GBB2/IO61PDB1
D15	IO63NDB1
D16	IO64NDB1
E1	IO151PDB3
E2	IO152PPB3
E3	IO153NDB3
E4	IO11RSB0
E5	VMV0
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	IO28RSB0
E9	IO35RSB0
E10	V_{CCI}B0

256-Pin FBGA*	
Pin Number	**A3P400 Function**
E11	V_{CCI}B0
E12	VMV1
E13	GBC2/IO62PDB1
E14	IO61NDB1
E15	IO63PDB1
E16	IO64PDB1
F1	IO151NDB3
F2	IO150PPB3
F3	NC
F4	IO148PPB3
F5	V_{CCI}B3
F6	GND
F7	V_{CC}
F8	V_{CC}
F9	V_{CC}
F10	V_{CC}
F11	GND
F12	V_{CCI}B1
F13	IO62NDB1
F14	NC
F15	IO65RSB1
F16	IO73NDB1
G1	IO150NPB3
G2	IO149PDB3
G3	IO149NDB3
G4	GFC1/IO147PPB3
G5	V_{CCI}B3
G6	V_{CC}
G7	GND
G8	GND
G9	GND
G10	GND
G11	V_{CC}
G12	V_{CCI}B1
G13	GCC1/IO67PPB1
G14	IO66NDB1
G15	IO66PDB1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

256-Pin FBGA*	
Pin Number	**A3P400 Function**
G16	IO73PDB1
H1	GFB0/IO146NPB3
H2	GFA0/IO145NDB3
H3	GFB1/IO146PPB3
H4	V_{COMPLF}
H5	GFC0/IO147NPB3
H6	V_{CC}
H7	GND
H8	GND
H9	GND
H10	GND
H11	V_{CC}
H12	GCC0/IO67NPB1
H13	GCB1/IO68PPB1
H14	GCA0/IO69NPB1
H15	NC
H16	GCB0/IO68NPB1
J1	GFA2/IO144PPB3
J2	GFA1/IO145PDB3
J3	V_{CCPLF}
J4	IO148NPB3
J5	GFB2/IO143PPB3
J6	V_{CC}
J7	GND
J8	GND
J9	GND
J10	GND
J11	V_{CC}
J12	GCB2/IO71PPB1
J13	GCA1/IO69PPB1
J14	GCC2/IO72PDB1
J15	NC
J16	GCA2/IO70PDB1
K1	GFC2/IO142PDB3
K2	IO144NPB3
K3	IO143NPB3
K4	IO138PDB3

256-Pin FBGA*	
Pin Number	**A3P400 Function**
K5	V_{CCI}B3
K6	V_{CC}
K7	GND
K8	GND
K9	GND
K10	GND
K11	V_{CC}
K12	V_{CCI}B1
K13	IO71NPB1
K14	IO72NDB1
K15	IO74RSB1
K16	IO70NDB1
L1	IO142NDB3
L2	IO140NDB3
L3	IO139RSB3
L4	IO138NDB3
L5	V_{CCI}B3
L6	GND
L7	V_{CC}
L8	V_{CC}
L9	V_{CC}
L10	V_{CC}
L11	GND
L12	V_{CCI}B0
L13	GDB0/IO78NPB1
L14	IO75NDB1
L15	IO75PDB1
L16	IO76PDB1
M1	IO141NDB3
M2	IO140PDB3
M3	IO127RSB2
M4	GEC0/IO137NPB3
M5	VMV3
M6	V_{CCI}B2
M7	V_{CCI}B2
M8	IO106RSB2
M9	IO99RSB2

256-Pin FBGA*	
Pin Number	**A3P400 Function**
M10	V_{CCI}B2
M11	V_{CCI}B2
M12	VMV2
M13	IO85RSB2
M14	GDB1/IO78PPB1
M15	GDC1/IO77PDB1
M16	IO76NDB1
N1	IO141PDB3
N2	IO131RSB2
N3	GEC1/IO137PPB3
N4	IO128RSB2
N5	GNDQ
N6	GEA2/IO134RSB2
N7	IO113RSB2
N8	IO109RSB2
N9	IO100RSB2
N10	IO95RSB2
N11	IO90RSB2
N12	GNDQ
N13	IO83RSB2
N14	V_{JTAG}
N15	GDC0/IO77NDB1
N16	GDA1/IO79PDB1
P1	GEB1/IO136PDB3
P2	GEB0/IO136NDB3
P3	IO130RSB2
P4	IO129RSB2
P5	IO126RSB2
P6	IO121RSB2
P7	IO115RSB2
P8	IO108RSB2
P9	IO101RSB2
P10	IO94RSB2
P11	IO88RSB2
P12	IO84RSB2
P13	TCK
P14	V_{PUMP}

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

256-Pin FBGA*	
Pin Number	**A3P400 Function**
P15	TRST
P16	GDA0/IO79NDB1
R1	GEA1/IO135PDB3
R2	GEA0/IO135NDB3
R3	IO125RSB2
R4	GEC2/IO132RSB2
R5	IO122RSB2
R6	IO118RSB2
R7	IO112RSB2
R8	IO107RSB2
R9	IO102RSB2
R10	IO96RSB2
R11	IO91RSB2
R12	IO87RSB2
R13	GDB2/IO81RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO124RSB2
T3	GEB2/IO133RSB2
T4	IO123RSB2
T5	IO120RSB2
T6	IO116RSB2
T7	IO111RSB2
T8	IO105RSB2
T9	IO103RSB2
T10	IO97RSB2
T11	IO93RSB2
T12	GDC2/IO82RSB2
T13	IO86RSB2
T14	GDA2/IO80RSB2
T15	TMS
T16	GND

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

256-Pin FBGA*	
Pin Number	**A3P600 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO12RSB0
A6	IO14RSB0
A7	IO19RSB0
A8	IO26RSB0
A9	IO31RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO47RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO169PDB3
B2	GAA2/IO170PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO10RSB0
B6	IO15RSB0
B7	IO18RSB0
B8	IO24RSB0
B9	IO32RSB0
B10	IO40RSB0
B11	IO43RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO49RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO169NDB3
C2	IO170NDB3
C3	VMV3
C4	IO06RSB0
C5	GAC0/IO04RSB0

256-Pin FBGA*	
Pin Number	**A3P600 Function**
C6	GAC1/IO05RSB0
C7	IO17RSB0
C8	IO25RSB0
C9	IO33RSB0
C10	IO38RSB0
C11	IO42RSB0
C12	GBC0/IO54RSB0
C13	IO52RSB0
C14	IO51RSB0
C15	IO50RSB0
C16	IO61NPB1
D1	IO166NDB3
D2	IO166PDB3
D3	GAC2/IO168PDB3
D4	IO168NDB3
D5	GNDQ
D6	IO13RSB0
D7	IO16RSB0
D8	IO22RSB0
D9	IO36RSB0
D10	IO39RSB0
D11	IO46RSB0
D12	GNDQ
D13	IO53RSB0
D14	GBB2/IO61PPB1
D15	IO63PPB1
D16	IO65PDB1
E1	IO165NDB3
E2	IO165PDB3
E3	IO167PDB3
E4	IO167NDB3
E5	VMV0
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	IO29RSB0
E9	IO30RSB0
E10	V_{CCI}B0

256-Pin FBGA*	
Pin Number	**A3P600 Function**
E11	V_{CCI}B0
E12	VMV1
E13	GBC2/IO62PDB1
E14	IO63NPB1
E15	IO64PPB1
E16	IO65NDB1
F1	IO154PSB3
F2	IO162PPB3
F3	IO164PDB3
F4	IO164NDB3
F5	V_{CCI}B3
F6	GND
F7	V_{CC}
F8	V_{CC}
F9	V_{CC}
F10	V_{CC}
F11	GND
F12	V_{CCI}B1
F13	IO62NDB1
F14	IO64NPB1
F15	IO66PPB1
F16	IO67PPB1
G1	IO155NDB3
G2	IO155PDB3
G3	IO162NPB3
G4	GFC1/IO161PPB3
G5	V_{CCI}B3
G6	V_{CC}
G7	GND
G8	GND
G9	GND
G10	GND
G11	V_{CC}
G12	V_{CCI}B1
G13	GCC1/IO68PPB1
G14	IO66NPB1
G15	IO67NPB1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

256-Pin FBGA*	
Pin Number	**A3P600 Function**
G16	IO71NPB1
H1	GFB0/IO160NPB3
H2	GFA0/IO159NDB3
H3	GFB1/IO160PPB3
H4	V_{COMPLF}
H5	GFC0/IO161NPB3
H6	V_{CC}
H7	GND
H8	GND
H9	GND
H10	GND
H11	V_{CC}
H12	GCC0/IO68NPB1
H13	GCB1/IO69PPB1
H14	GCA0/IO70NPB1
H15	IO73NPB1
H16	GCB0/IO69NPB1
J1	GFA2/IO158PPB3
J2	GFA1/IO159PDB3
J3	V_{CCPLF}
J4	IO157NDB3
J5	GFB2/IO157PDB3
J6	V_{CC}
J7	GND
J8	GND
J9	GND
J10	GND
J11	V_{CC}
J12	GCB2/IO72PPB1
J13	GCA1/IO70PPB1
J14	GCC2/IO73PPB1
J15	IO77PPB1
J16	GCA2/IO71PPB1
K1	GFC2/IO156PPB3
K2	IO158NPB3
K3	IO151PDB3
K4	IO151NDB3

256-Pin FBGA*	
Pin Number	**A3P600 Function**
K5	V_{CCI}B3
K6	V_{CC}
K7	GND
K8	GND
K9	GND
K10	GND
K11	V_{CC}
K12	V_{CCI}B1
K13	IO72NPB1
K14	IO82PDB1
K15	IO79PDB1
K16	IO77NPB1
L1	IO149PDB3
L2	IO156NPB3
L3	IO147PDB3
L4	IO147NDB3
L5	V_{CCI}B3
L6	GND
L7	V_{CC}
L8	V_{CC}
L9	V_{CC}
L10	V_{CC}
L11	GND
L12	V_{CCI}B1
L13	GDB0/IO85NPB1
L14	IO82NDB1
L15	IO79NDB1
L16	IO80PDB1
M1	IO149NDB3
M2	IO146PDB3
M3	IO146NDB3
M4	GEC0/IO144NPB3
M5	VMV3
M6	V_{CCI}B2
M7	V_{CCI}B2
M8	IO111RSB2
M9	IO110RSB2

256-Pin FBGA*	
Pin Number	**A3P600 Function**
M10	V_{CCI}B2
M11	V_{CCI}B2
M12	VMV2
M13	IO81NDB1
M14	GDB1/IO85PPB1
M15	GDC1/IO84PDB1
M16	IO80NDB1
N1	IO145PDB3
N2	IO145NDB3
N3	GEC1/IO144PPB3
N4	IO137RSB2
N5	GNDQ
N6	GEA2/IO141RSB2
N7	IO120RSB2
N8	IO113RSB2
N9	IO106RSB2
N10	IO99RSB2
N11	IO94RSB2
N12	GNDQ
N13	IO81PDB1
N14	V_{JTAG}
N15	GDC0/IO84NDB1
N16	GDA1/IO86PDB1
P1	GEB1/IO143PDB3
P2	GEB0/IO143NDB3
P3	IO138RSB2
P4	IO135RSB2
P5	IO134RSB2
P6	IO128RSB2
P7	IO121RSB2
P8	IO115RSB2
P9	IO108RSB2
P10	IO100RSB2
P11	IO95RSB2
P12	VMV1
P13	TCK
P14	V_{PUMP}

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

256-Pin FBGA*	
Pin Number	**A3P600 Function**
P15	TRST
P16	GDA0/IO86NDB1
R1	GEA1/IO142PDB3
R2	GEA0/IO142NDB3
R3	IO136RSB2
R4	GEC2/IO139RSB2
R5	IO130RSB2
R6	IO125RSB2
R7	IO119RSB2
R8	IO114RSB2
R9	IO107RSB2
R10	IO101RSB2
R11	IO96RSB2
R12	IO90RSB2
R13	GDB2/IO88RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO133RSB2
T3	GEB2/IO140RSB2
T4	IO132RSB2
T5	IO127RSB2
T6	IO123RSB2
T7	IO117RSB2
T8	IO112RSB2
T9	IO109RSB2
T10	IO102RSB2
T11	IO97RSB2
T12	GDC2/IO89RSB2
T13	IO91RSB2
T14	GDA2/IO87RSB2
T15	TMS
T16	GND

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

256-Pin FBGA*	
Pin Number	**A3P1000 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO17RSB0
A6	IO22RSB0
A7	IO28RSB0
A8	IO34RSB0
A9	IO44RSB0
A10	IO50RSB0
A11	IO56RSB0
A12	IO62RSB0
A13	GBB1/IO75RSB0
A14	GBA0/IO76RSB0
A15	GBA1/IO77RSB0
A16	GND
B1	GAB2/IO218PDB3
B2	GAA2/IO219PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO26RSB0
B8	IO35RSB0
B9	IO45RSB0
B10	IO52RSB0
B11	IO57RSB0
B12	GBC1/IO73RSB0
B13	GBB0/IO74RSB0
B14	IO69RSB0
B15	GBA2/IO78PDB1
B16	IO78NDB1
C1	IO218NDB3
C2	IO219NDB3
C3	VMV3
C4	IO06RSB0
C5	GAC0/IO04RSB0

256-Pin FBGA*	
Pin Number	**A3P1000 Function**
C6	GAC1/IO05RSB0
C7	IO27RSB0
C8	IO33RSB0
C9	IO43RSB0
C10	IO51RSB0
C11	IO58RSB0
C12	GBC0/IO72RSB0
C13	IO70RSB0
C14	IO71RSB0
C15	IO81PDB1
C16	IO81NDB1
D1	IO215NDB3
D2	IO215PDB3
D3	GAC2/IO217PDB3
D4	IO217NDB3
D5	GNDQ
D6	IO21RSB0
D7	IO25RSB0
D8	IO31RSB0
D9	IO46RSB0
D10	IO53RSB0
D11	IO59RSB0
D12	GNDQ
D13	IO80NDB1
D14	GBB2/IO79PDB1
D15	IO82PDB1
D16	IO82NDB1
E1	IO210PDB3
E2	IO213NDB3
E3	IO213PDB3
E4	IO216PDB3
E5	VMV0
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	IO38RSB0
E9	IO47RSB0
E10	V_{CCI}B0

256-Pin FBGA*	
Pin Number	**A3P1000 Function**
E11	V_{CCI}B0
E12	VMV1
E13	GBC2/IO80PDB1
E14	IO79NDB1
E15	IO83PDB1
E16	IO83NDB1
F1	IO210NDB3
F2	IO211NDB3
F3	IO211PDB3
F4	IO216NDB3
F5	V_{CCI}B3
F6	GND
F7	V_{CC}
F8	V_{CC}
F9	V_{CC}
F10	V_{CC}
F11	GND
F12	V_{CCI}B1
F13	IO85PDB1
F14	IO85NDB1
F15	IO86PDB1
F16	IO86NDB1
G1	IO200PSB3
G2	IO208NDB3
G3	IO208PDB3
G4	GFC1/IO206PPB3
G5	V_{CCI}B3
G6	V_{CC}
G7	GND
G8	GND
G9	GND
G10	GND
G11	V_{CC}
G12	V_{CCI}B1
G13	GCC1/IO88PPB1
G14	IO87PDB1
G15	IO87NDB1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

256-Pin FBGA*	
Pin Number	**A3P1000 Function**
G16	IO94PSB1
H1	GFB0/IO205NPB3
H2	GFA0/IO204NDB3
H3	GFB1/IO205PPB3
H4	V_{COMPLF}
H5	GFC0/IO206NPB3
H6	V_{CC}
H7	GND
H8	GND
H9	GND
H10	GND
H11	V_{CC}
H12	GCC0/IO88NPB1
H13	GCB1/IO89PPB1
H14	GCA0/IO90NPB1
H15	IO91NPB1
H16	GCB0/IO89NPB1
J1	GFA2/IO203PPB3
J2	GFA1/IO204PDB3
J3	V_{CCPLF}
J4	IO202NDB3
J5	GFB2/IO202PDB3
J6	V_{CC}
J7	GND
J8	GND
J9	GND
J10	GND
J11	V_{CC}
J12	GCB2/IO92PPB1
J13	GCA1/IO90PPB1
J14	GCC2/IO93PDB1
J15	IO93NDB1
J16	GCA2/IO91PPB1
K1	GFC2/IO201PSB3
K2	IO203NPB3
K3	IO197PDB3
K4	IO197NDB3

256-Pin FBGA*	
Pin Number	**A3P1000 Function**
K5	$V_{CCI}B3$
K6	V_{CC}
K7	GND
K8	GND
K9	GND
K10	GND
K11	V_{CC}
K12	$V_{CCI}B1$
K13	IO92NPB1
K14	IO100NDB1
K15	IO100PDB1
K16	IO102PDB1
L1	IO195PDB3
L2	IO195NDB3
L3	IO194PDB3
L4	IO194NDB3
L5	$V_{CCI}B3$
L6	GND
L7	V_{CC}
L8	V_{CC}
L9	V_{CC}
L10	V_{CC}
L11	GND
L12	$V_{CCI}B1$
L13	GDB0/IO109NPB1
L14	IO103NDB1
L15	IO103PDB1
L16	IO102NDB1
M1	IO191PDB3
M2	IO190PDB3
M3	IO190NDB3
M4	GEC0/IO187NPB3
M5	VMV3
M6	$V_{CCI}B2$
M7	$V_{CCI}B2$
M8	IO144RSB2
M9	IO133RSB2

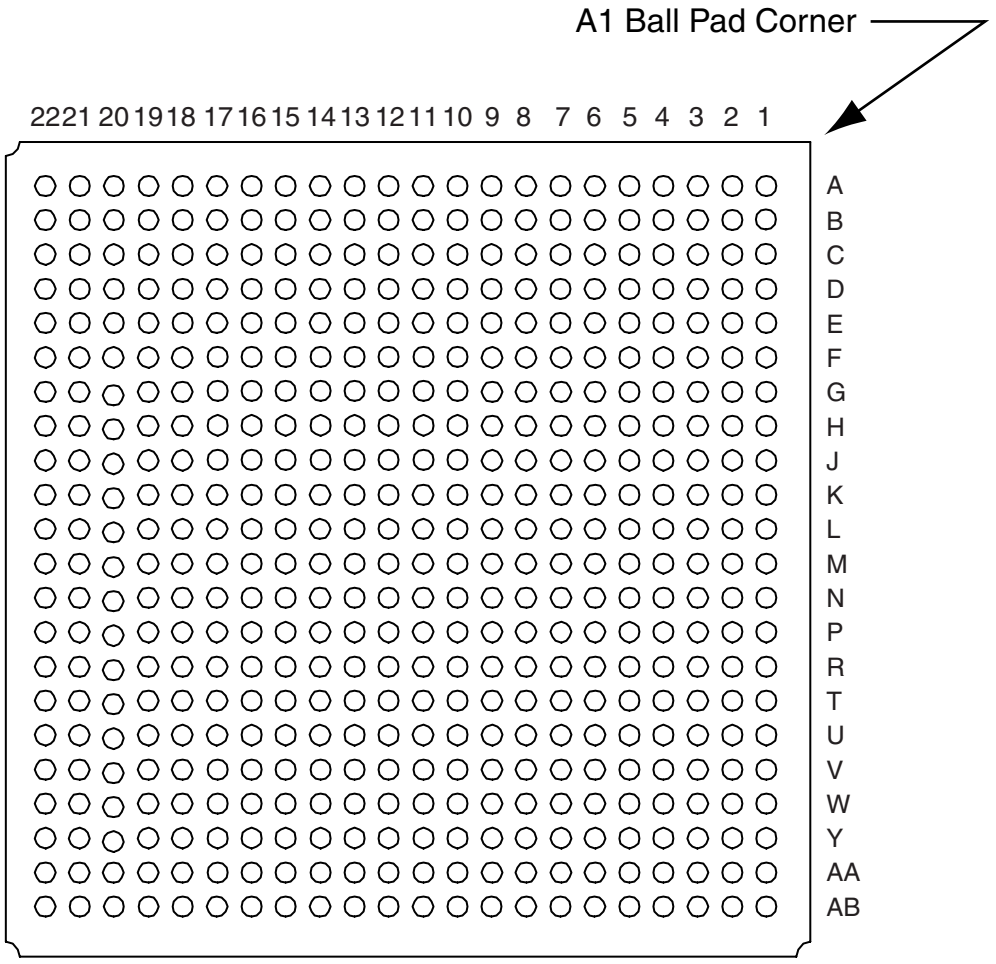
256-Pin FBGA*	
Pin Number	**A3P1000 Function**
M10	$V_{CCI}B2$
M11	$V_{CCI}B2$
M12	VMV2
M13	IO107PDB1
M14	GDB1/IO109PPB1
M15	GDC1/IO108PDB1
M16	IO106PSB1
N1	IO191NDB3
N2	IO188PPB3
N3	GEC1/IO187PPB3
N4	IO188NPB3
N5	GNDQ
N6	GEA2/IO184RSB2
N7	IO153RSB2
N8	IO146RSB2
N9	IO134RSB2
N10	IO126RSB2
N11	IO121RSB2
N12	GNDQ
N13	IO107NDB1
N14	V_{JTAG}
N15	GDC0/IO108NDB1
N16	GDA1/IO110PDB1
P1	GEB1/IO186PDB3
P2	GEB0/IO186NDB3
P3	IO181RSB2
P4	IO178RSB2
P5	IO166RSB2
P6	IO159RSB2
P7	IO154RSB2
P8	IO148RSB2
P9	IO138RSB2
P10	IO131RSB2
P11	IO124RSB2
P12	VMV1
P13	TCK
P14	V_{PUMP}

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

256-Pin FBGA*	
Pin Number	**A3P1000 Function**
P15	TRST
P16	GDA0/IO110NDB1
R1	GEA1/IO185PDB3
R2	GEA0/IO185NDB3
R3	IO177RSB2
R4	GEC2/IO182RSB2
R5	IO167RSB2
R6	IO160RSB2
R7	IO155RSB2
R8	IO150RSB2
R9	IO139RSB2
R10	IO130RSB2
R11	IO127RSB2
R12	IO119RSB2
R13	GDB2/IO112RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO176RSB2
T3	GEB2/IO183RSB2
T4	IO170RSB2
T5	IO164RSB2
T6	IO158RSB2
T7	IO152RSB2
T8	IO145RSB2
T9	IO137RSB2
T10	IO132RSB2
T11	IO125RSB2
T12	GDC2/IO113RSB2
T13	IO117RSB2
T14	GDA2/IO111RSB2
T15	TMS
T16	GND

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

484-Pin FBGA*	
Pin Number	**A3P400 Function**
A1	GND
A2	GND
A3	V_{CCI}B0
A4	NC
A5	NC
A6	IO13RSB0
A7	IO17RSB0
A8	NC
A9	NC
A10	IO23RSB0
A11	IO29RSB0
A12	IO34RSB0
A13	IO36RSB0
A14	NC
A15	NC
A16	IO45RSB0
A17	IO47RSB0
A18	NC
A19	NC
A20	V_{CCI}B0
A21	GND
A22	GND
B1	GND
B2	V_{CCI}B3
B3	NC
B4	NC
B5	NC
B6	NC
B7	NC
B8	NC
B9	NC
B10	NC
B11	NC
B12	NC
B13	NC
B14	NC

484-Pin FBGA*	
Pin Number	**A3P400 Function**
B15	NC
B16	NC
B17	NC
B18	NC
B19	NC
B20	NC
B21	V_{CCI}B1
B22	GND
C1	V_{CCI}B3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	V_{CC}
C9	V_{CC}
C10	NC
C11	NC
C12	NC
C13	NC
C14	V_{CC}
C15	V_{CC}
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	V_{CCI}B1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0

484-Pin FBGA*	
Pin Number	**A3P400 Function**
D7	GAB0/IO02RSB0
D8	IO14RSB0
D9	IO18RSB0
D10	IO22RSB0
D11	IO27RSB0
D12	IO30RSB0
D13	IO39RSB0
D14	IO41RSB0
D15	IO46RSB0
D16	GBB1/IO57RSB0
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO154PDB3
E5	GAA2/IO155PPB3
E6	IO10RSB0
E7	GAB1/IO03RSB0
E8	IO12RSB0
E9	IO16RSB0
E10	IO21RSB0
E11	IO26RSB0
E12	IO31RSB0
E13	IO37RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO48RSB0
E18	GBA2/IO60PPB1
E19	IO50RSB0
E20	GND

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA*	
Pin Number	**A3P400 Function**
E21	NC
E22	NC
F1	NC
F2	NC
F3	NC
F4	IO154NDB3
F5	IO08RSB0
F6	IO07RSB0
F7	IO06RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO20RSB0
F11	IO25RSB0
F12	IO32RSB0
F13	IO38RSB0
F14	IO44RSB0
F15	GBC0/IO54RSB0
F16	IO51RSB0
F17	IO52RSB0
F18	IO53RSB0
F19	IO60NPB1
F20	NC
F21	NC
F22	NC
G1	NC
G2	NC
G3	NC
G4	IO152NPB3
G5	IO155NPB3
G6	GAC2/IO153PDB3
G7	IO09RSB0
G8	GNDQ
G9	IO15RSB0
G10	IO19RSB0
G11	IO24RSB0
G12	IO33RSB0

484-Pin FBGA*	
Pin Number	**A3P400 Function**
G13	IO40RSB0
G14	IO43RSB0
G15	GNDQ
G16	IO49RSB0
G17	GBB2/IO61PDB1
G18	IO63NDB1
G19	IO64NDB1
G20	NC
G21	NC
G22	NC
H1	NC
H2	NC
H3	V_{CC}
H4	IO151PDB3
H5	IO152PPB3
H6	IO153NDB3
H7	IO11RSB0
H8	VMV0
H9	V_{CCI}B0
H10	V_{CCI}B0
H11	IO28RSB0
H12	IO35RSB0
H13	V_{CCI}B0
H14	V_{CCI}B0
H15	VMV1
H16	GBC2/IO62PDB1
H17	IO61NDB1
H18	IO63PDB1
H19	IO64PDB1
H20	V_{CC}
H21	NC
H22	NC
J1	NC
J2	NC
J3	NC
J4	IO151NDB3

484-Pin FBGA*	
Pin Number	**A3P400 Function**
J5	IO150PPB3
J6	NC
J7	IO148PPB3
J8	V_{CCI}B3
J9	GND
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	GND
J15	V_{CCI}B1
J16	IO62NDB1
J17	NC
J18	IO65RSB1
J19	IO73NDB1
J20	NC
J21	NC
J22	NC
K1	NC
K2	NC
K3	NC
K4	IO150NPB3
K5	IO149PDB3
K6	IO149NDB3
K7	GFC1/IO147PPB3
K8	V_{CCI}B3
K9	V_{CC}
K10	GND
K11	GND
K12	GND
K13	GND
K14	V_{CC}
K15	V_{CCI}B1
K16	GCC1/IO67PPB1
K17	IO66NDB1
K18	IO66PDB1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA*	
Pin Number	**A3P400 Function**
K19	IO73PDB1
K20	NC
K21	NC
K22	NC
L1	NC
L2	NC
L3	NC
L4	GFB0/IO146NPB3
L5	GFA0/IO145NDB3
L6	GFB1/IO146PPB3
L7	V_{COMPLF}
L8	GFC0/IO147NPB3
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	V_{CC}
L15	GCC0/IO67NPB1
L16	GCB1/IO68PPB1
L17	GCA0/IO69NPB1
L18	NC
L19	GCB0/IO68NPB1
L20	NC
L21	NC
L22	NC
M1	NC
M2	NC
M3	NC
M4	GFA2/IO144PPB3
M5	GFA1/IO145PDB3
M6	V_{CCPLF}
M7	IO148NPB3
M8	GFB2/IO143PPB3
M9	V_{CC}
M10	GND

484-Pin FBGA*	
Pin Number	**A3P400 Function**
M11	GND
M12	GND
M13	GND
M14	V_{CC}
M15	GCB2/IO71PPB1
M16	GCA1/IO69PPB1
M17	GCC2/IO72PDB1
M18	NC
M19	GCA2/IO70PDB1
M20	NC
M21	NC
M22	NC
N1	NC
N2	NC
N3	NC
N4	GFC2/IO142PDB3
N5	IO144NPB3
N6	IO143NPB3
N7	IO138PDB3
N8	$V_{CCI}B3$
N9	V_{CC}
N10	GND
N11	GND
N12	GND
N13	GND
N14	V_{CC}
N15	$V_{CCI}B1$
N16	IO71NPB1
N17	IO72NDB1
N18	IO74RSB1
N19	IO70NDB1
N20	NC
N21	NC
N22	NC
P1	NC
P2	NC

484-Pin FBGA*	
Pin Number	**A3P400 Function**
P3	NC
P4	IO142NDB3
P5	IO140NDB3
P6	IO139RSB3
P7	IO138NDB3
P8	$V_{CCI}B3$
P9	GND
P10	V_{CC}
P11	V_{CC}
P12	V_{CC}
P13	V_{CC}
P14	GND
P15	$V_{CCI}B1$
P16	GDB0/IO78NPB1
P17	IO75NDB1
P18	IO75PDB1
P19	IO76PDB1
P20	NC
P21	NC
P22	NC
R1	NC
R2	NC
R3	V_{CC}
R4	IO141NDB3
R5	IO140PDB3
R6	IO127RSB2
R7	GEC0/IO137NPB3
R8	VMV3
R9	$V_{CCI}B2$
R10	$V_{CCI}B2$
R11	IO106RSB2
R12	IO99RSB2
R13	$V_{CCI}B2$
R14	$V_{CCI}B2$
R15	VMV2
R16	IO85RSB2

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA*	
Pin Number	**A3P400 Function**
R17	GDB1/IO78PPB1
R18	GDC1/IO77PDB1
R19	IO76NDB1
R20	V_{CC}
R21	NC
R22	NC
T1	NC
T2	NC
T3	NC
T4	IO141PDB3
T5	IO131RSB2
T6	GEC1/IO137PPB3
T7	IO128RSB2
T8	GNDQ
T9	GEA2/IO134RSB2
T10	IO113RSB2
T11	IO109RSB2
T12	IO100RSB2
T13	IO95RSB2
T14	IO90RSB2
T15	GNDQ
T16	IO83RSB2
T17	V_{JTAG}
T18	GDC0/IO77NDB1
T19	GDA1/IO79PDB1
T20	NC
T21	NC
T22	NC
U1	NC
U2	NC
U3	NC
U4	GEB1/IO136PDB3
U5	GEB0/IO136NDB3
U6	IO130RSB2
U7	IO129RSB2
U8	IO126RSB2

484-Pin FBGA*	
Pin Number	**A3P400 Function**
U9	IO121RSB2
U10	IO115RSB2
U11	IO108RSB2
U12	IO101RSB2
U13	IO94RSB2
U14	IO88RSB2
U15	IO84RSB2
U16	TCK
U17	V_{PUMP}
U18	TRST
U19	GDA0/IO79NDB1
U20	NC
U21	NC
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO135PDB3
V5	GEA0/IO135NDB3
V6	IO125RSB2
V7	GEC2/IO132RSB2
V8	IO122RSB2
V9	IO118RSB2
V10	IO112RSB2
V11	IO107RSB2
V12	IO102RSB2
V13	IO96RSB2
V14	IO91RSB2
V15	IO87RSB2
V16	GDB2/IO81RSB2
V17	TDI
V18	NC
V19	TDO
V20	GND
V21	NC
V22	NC

484-Pin FBGA*	
Pin Number	**A3P400 Function**
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO124RSB2
W6	GEB2/IO133RSB2
W7	IO123RSB2
W8	IO120RSB2
W9	IO116RSB2
W10	IO111RSB2
W11	IO105RSB2
W12	IO103RSB2
W13	IO97RSB2
W14	IO93RSB2
W15	GDC2/IO82RSB2
W16	IO86RSB2
W17	GDA2/IO80RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	V_{CCI}B3
Y2	NC
Y3	NC
Y4	NC
Y5	GND
Y6	NC
Y7	NC
Y8	V_{CC}
Y9	V_{CC}
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	V_{CC}

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA*	
Pin Number	**A3P400 Function**
Y15	V_{CC}
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	V_{CCI}B1
AA1	GND
AA2	V_{CCI}B3
AA3	NC
AA4	NC
AA5	NC
AA6	NC
AA7	NC
AA8	NC
AA9	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC
AA15	NC
AA16	NC
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	V_{CCI}B1
AA22	GND
AB1	GND
AB2	GND
AB3	V_{CCI}B2
AB4	NC
AB5	NC
AB6	IO119RSB2

484-Pin FBGA*	
Pin Number	**A3P400 Function**
AB7	IO117RSB2
AB8	IO114RSB2
AB9	IO110RSB2
AB10	NC
AB11	NC
AB12	IO104RSB2
AB13	IO98RSB2
AB14	NC
AB15	NC
AB16	IO92RSB2
AB17	IO89RSB2
AB18	NC
AB19	NC
AB20	V_{CCI}B2
AB21	GND
AB22	GND

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA*	
Pin Number	**A3P600 Function**
A1	GND
A2	GND
A3	V_{CCI}B0
A4	NC
A5	NC
A6	IO08RSB0
A7	IO09RSB0
A8	NC
A9	NC
A10	IO21RSB0
A11	IO23RSB0
A12	IO27RSB0
A13	IO28RSB0
A14	NC
A15	NC
A16	IO35RSB0
A17	IO45RSB0
A18	NC
A19	NC
A20	V_{CCI}B0
A21	GND
A22	GND
B1	GND
B2	V_{CCI}B3
B3	NC
B4	NC
B5	NC
B6	IO07RSB0
B7	IO11RSB0
B8	NC
B9	NC
B10	IO20RSB0
B11	NC
B12	NC
B13	IO34RSB0
B14	NC

484-Pin FBGA*	
Pin Number	**A3P600 Function**
B15	NC
B16	IO44RSB0
B17	IO48RSB0
B18	NC
B19	NC
B20	NC
B21	V_{CCI}B1
B22	GND
C1	V_{CCI}B3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	V_{CC}
C9	V_{CC}
C10	NC
C11	NC
C12	NC
C13	NC
C14	V_{CC}
C15	V_{CC}
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	V_{CCI}B1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0

484-Pin FBGA*	
Pin Number	**A3P600 Function**
D7	GAB0/IO02RSB0
D8	IO12RSB0
D9	IO14RSB0
D10	IO19RSB0
D11	IO26RSB0
D12	IO31RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO47RSB0
D16	GBB1/IO57RSB0
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO169PDB3
E5	GAA2/IO170PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO10RSB0
E9	IO15RSB0
E10	IO18RSB0
E11	IO24RSB0
E12	IO32RSB0
E13	IO40RSB0
E14	IO43RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO49RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA*	
Pin Number	**A3P600 Function**
E21	NC
E22	NC
F1	NC
F2	NC
F3	NC
F4	IO169NDB3
F5	IO170NDB3
F6	VMV3
F7	IO06RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO17RSB0
F11	IO25RSB0
F12	IO33RSB0
F13	IO38RSB0
F14	IO42RSB0
F15	GBC0/IO54RSB0
F16	IO52RSB0
F17	IO51RSB0
F18	IO50RSB0
F19	IO61NPB1
F20	NC
F21	NC
F22	NC
G1	IO163NDB3
G2	IO163PDB3
G3	NC
G4	IO166NDB3
G5	IO166PDB3
G6	GAC2/IO168PDB3
G7	IO168NDB3
G8	GNDQ
G9	IO13RSB0
G10	IO16RSB0
G11	IO22RSB0
G12	IO36RSB0

484-Pin FBGA*	
Pin Number	**A3P600 Function**
G13	IO39RSB0
G14	IO46RSB0
G15	GNDQ
G16	IO53RSB0
G17	GBB2/IO61PPB1
G18	IO63PPB1
G19	IO65PDB1
G20	NC
G21	NC
G22	NC
H1	NC
H2	NC
H3	V_{CC}
H4	IO165NDB3
H5	IO165PDB3
H6	IO167PDB3
H7	IO167NDB3
H8	VMV0
H9	V_{CCI}B0
H10	V_{CCI}B0
H11	IO29RSB0
H12	IO30RSB0
H13	V_{CCI}B0
H14	V_{CCI}B0
H15	VMV1
H16	GBC2/IO62PDB1
H17	IO63NPB1
H18	IO64PPB1
H19	IO65NDB1
H20	V_{CC}
H21	NC
H22	NC
J1	IO153PDB3
J2	IO154NDB3
J3	NC
J4	IO154PDB3

484-Pin FBGA*	
Pin Number	**A3P600 Function**
J5	IO162PPB3
J6	IO164PDB3
J7	IO164NDB3
J8	V_{CCI}B3
J9	GND
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	GND
J15	V_{CCI}B1
J16	IO62NDB1
J17	IO64NPB1
J18	IO66PPB1
J19	IO67PPB1
J20	NC
J21	IO74PDB1
J22	IO74NDB1
K1	IO153NDB3
K2	NC
K3	NC
K4	IO155NDB3
K5	IO155PDB3
K6	IO162NPB3
K7	GFC1/IO161PPB3
K8	V_{CCI}B3
K9	V_{CC}
K10	GND
K11	GND
K12	GND
K13	GND
K14	V_{CC}
K15	V_{CCI}B1
K16	GCC1/IO68PPB1
K17	IO66NPB1
K18	IO67NPB1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA*	
Pin Number	**A3P600 Function**
K19	IO71NPB1
K20	NC
K21	NC
K22	IO75PDB1
L1	NC
L2	IO152PDB3
L3	NC
L4	GFB0/IO160NPB3
L5	GFA0/IO159NDB3
L6	GFB1/IO160PPB3
L7	V_{COMPLF}
L8	GFC0/IO161NPB3
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	V_{CC}
L15	GCC0/IO68NPB1
L16	GCB1/IO69PPB1
L17	GCA0/IO70NPB1
L18	IO73NPB1
L19	GCB0/IO69NPB1
L20	NC
L21	NC
L22	IO75NDB1
M1	NC
M2	IO152NDB3
M3	NC
M4	GFA2/IO158PPB3
M5	GFA1/IO159PDB3
M6	V_{CCPLF}
M7	IO157NDB3
M8	GFB2/IO157PDB3
M9	V_{CC}
M10	GND

484-Pin FBGA*	
Pin Number	**A3P600 Function**
M11	GND
M12	GND
M13	GND
M14	V_{CC}
M15	GCB2/IO72PPB1
M16	GCA1/IO70PPB1
M17	GCC2/IO73PPB1
M18	IO77PPB1
M19	GCA2/IO71PPB1
M20	NC
M21	IO76PDB1
M22	NC
N1	IO150PPB3
N2	NC
N3	NC
N4	GFC2/IO156PPB3
N5	IO158NPB3
N6	IO151PDB3
N7	IO151NDB3
N8	$V_{CCI}B3$
N9	V_{CC}
N10	GND
N11	GND
N12	GND
N13	GND
N14	V_{CC}
N15	$V_{CCI}B1$
N16	IO72NPB1
N17	IO82PDB1
N18	IO79PDB1
N19	IO77NPB1
N20	NC
N21	IO76NDB1
N22	NC
P1	NC
P2	IO150NPB3

484-Pin FBGA*	
Pin Number	**A3P600 Function**
P3	NC
P4	IO149PDB3
P5	IO156NPB3
P6	IO147PDB3
P7	IO147NDB3
P8	$V_{CCI}B3$
P9	GND
P10	V_{CC}
P11	V_{CC}
P12	V_{CC}
P13	V_{CC}
P14	GND
P15	$V_{CCI}B1$
P16	GDB0/IO85NPB1
P17	IO82NDB1
P18	IO79NDB1
P19	IO80PDB1
P20	NC
P21	NC
P22	IO78PDB1
R1	NC
R2	IO148PDB3
R3	V_{CC}
R4	IO149NDB3
R5	IO146PDB3
R6	IO146NDB3
R7	GEC0/IO144NPB3
R8	VMV3
R9	$V_{CCI}B2$
R10	$V_{CCI}B2$
R11	IO111RSB2
R12	IO110RSB2
R13	$V_{CCI}B2$
R14	$V_{CCI}B2$
R15	VMV2
R16	IO81NDB1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA*	
Pin Number	**A3P600 Function**
R17	GDB1/IO85PPB1
R18	GDC1/IO84PDB1
R19	IO80NDB1
R20	V_{CC}
R21	IO83PDB1
R22	IO78NDB1
T1	NC
T2	IO148NDB3
T3	NC
T4	IO145PDB3
T5	IO145NDB3
T6	GEC1/IO144PPB3
T7	IO137RSB2
T8	GNDQ
T9	GEA2/IO141RSB2
T10	IO120RSB2
T11	IO113RSB2
T12	IO106RSB2
T13	IO99RSB2
T14	IO94RSB2
T15	GNDQ
T16	IO81PDB1
T17	V_{JTAG}
T18	GDC0/IO84NDB1
T19	GDA1/IO86PDB1
T20	NC
T21	IO83NDB1
T22	NC
U1	NC
U2	NC
U3	NC
U4	GEB1/IO143PDB3
U5	GEB0/IO143NDB3
U6	IO138RSB2
U7	IO135RSB2
U8	IO134RSB2

484-Pin FBGA*	
Pin Number	**A3P600 Function**
U9	IO128RSB2
U10	IO121RSB2
U11	IO115RSB2
U12	IO108RSB2
U13	IO100RSB2
U14	IO95RSB2
U15	VMV1
U16	TCK
U17	V_{PUMP}
U18	TRST
U19	GDA0/IO86NDB1
U20	NC
U21	NC
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO142PDB3
V5	GEA0/IO142NDB3
V6	IO136RSB2
V7	GEC2/IO139RSB2
V8	IO130RSB2
V9	IO125RSB2
V10	IO119RSB2
V11	IO114RSB2
V12	IO107RSB2
V13	IO101RSB2
V14	IO96RSB2
V15	IO90RSB2
V16	GDB2/IO88RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	NC

484-Pin FBGA*	
Pin Number	**A3P600 Function**
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO133RSB2
W6	GEB2/IO140RSB2
W7	IO132RSB2
W8	IO127RSB2
W9	IO123RSB2
W10	IO117RSB2
W11	IO112RSB2
W12	IO109RSB2
W13	IO102RSB2
W14	IO97RSB2
W15	GDC2/IO89RSB2
W16	IO91RSB2
W17	GDA2/IO87RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	V_{CCI}B3
Y2	NC
Y3	NC
Y4	NC
Y5	GND
Y6	NC
Y7	NC
Y8	V_{CC}
Y9	V_{CC}
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	V_{CC}

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA*	
Pin Number	**A3P600 Function**
Y15	V_{CC}
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	V_{CCI}B1
AA1	GND
AA2	V_{CCI}B3
AA3	NC
AA4	NC
AA5	NC
AA6	IO131RSB2
AA7	IO126RSB2
AA8	NC
AA9	NC
AA10	IO116RSB2
AA11	NC
AA12	NC
AA13	IO103RSB2
AA14	NC
AA15	NC
AA16	IO93RSB2
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	V_{CCI}B1
AA22	GND
AB1	GND
AB2	GND
AB3	V_{CCI}B2
AB4	NC
AB5	NC
AB6	IO129RSB2

484-Pin FBGA*	
Pin Number	**A3P600 Function**
AB7	IO124RSB2
AB8	IO122RSB2
AB9	IO118RSB2
AB10	NC
AB11	NC
AB12	IO105RSB2
AB13	IO104RSB2
AB14	NC
AB15	NC
AB16	IO98RSB2
AB17	IO92RSB2
AB18	NC
AB19	NC
AB20	V_{CCI}B2
AB21	GND
AB22	GND

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA*	
Pin Number	**A3P1000 Function**
A1	GND
A2	GND
A3	V_{CCI}B0
A4	IO08RSB0
A5	IO10RSB0
A6	IO12RSB0
A7	IO16RSB0
A8	IO19RSB0
A9	IO24RSB0
A10	IO32RSB0
A11	IO39RSB0
A12	IO40RSB0
A13	IO48RSB0
A14	IO54RSB0
A15	IO60RSB0
A16	IO63RSB0
A17	IO65RSB0
A18	IO67RSB0
A19	NC
A20	V_{CCI}B0
A21	GND
A22	GND
AA1	GND
AA2	V_{CCI}B3
AA3	NC
AA4	IO179RSB2
AA5	IO174RSB2
AA6	IO171RSB2
AA7	IO165RSB2
AA8	IO162RSB2
AA9	IO157RSB2
AA10	IO149RSB2
AA11	IO142RSB2
AA12	IO135RSB2
AA13	IO129RSB2
AA14	NC

484-Pin FBGA*	
Pin Number	**A3P1000 Function**
AA15	NC
AA16	IO118RSB2
AA17	IO115RSB2
AA18	NC
AA19	NC
AA20	NC
AA21	V_{CCI}B1
AA22	GND
AB1	GND
AB2	GND
AB3	V_{CCI}B2
AB4	IO175RSB2
AB5	IO172RSB2
AB6	IO168RSB2
AB7	IO163RSB2
AB8	IO161RSB2
AB9	IO156RSB2
AB10	IO147RSB2
AB11	IO141RSB2
AB12	IO140RSB2
AB13	IO128RSB2
AB14	IO123RSB2
AB15	IO122RSB2
AB16	IO120RSB2
AB17	IO116RSB2
AB18	IO114RSB2
AB19	NC
AB20	V_{CCI}B2
AB21	GND
AB22	GND
B1	GND
B2	V_{CCI}B3
B3	NC
B4	IO07RSB0
B5	IO09RSB0
B6	IO11RSB0

484-Pin FBGA*	
Pin Number	**A3P1000 Function**
B7	IO14RSB0
B8	IO18RSB0
B9	IO23RSB0
B10	IO30RSB0
B11	IO37RSB0
B12	IO41RSB0
B13	IO49RSB0
B14	IO55RSB0
B15	IO61RSB0
B16	IO64RSB0
B17	IO66RSB0
B18	IO68RSB0
B19	NC
B20	NC
B21	V_{CCI}B1
B22	GND
C1	V_{CCI}B3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	IO13RSB0
C8	V_{CC}
C9	V_{CC}
C10	IO29RSB0
C11	IO36RSB0
C12	IO42RSB0
C13	NC
C14	V_{CC}
C15	V_{CC}
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA*	
Pin Number	**A3P1000 Function**
C21	NC
C22	V_{CCI}B1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO17RSB0
D9	IO22RSB0
D10	IO28RSB0
D11	IO34RSB0
D12	IO44RSB0
D13	IO50RSB0
D14	IO56RSB0
D15	IO62RSB0
D16	GBB1/IO75RSB0
D17	GBA0/IO76RSB0
D18	GBA1/IO77RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO218PDB3
E5	GAA2/IO219PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO15RSB0
E9	IO20RSB0
E10	IO26RSB0
E11	IO35RSB0
E12	IO45RSB0

484-Pin FBGA*	
Pin Number	**A3P1000 Function**
E13	IO52RSB0
E14	IO57RSB0
E15	GBC1/IO73RSB0
E16	GBB0/IO74RSB0
E17	IO69RSB0
E18	GBA2/IO78PDB1
E19	IO78NDB1
E20	GND
E21	NC
E22	NC
F1	NC
F2	IO214NDB3
F3	IO214PDB3
F4	IO218NDB3
F5	IO219NDB3
F6	VMV3
F7	IO06RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO27RSB0
F11	IO33RSB0
F12	IO43RSB0
F13	IO51RSB0
F14	IO58RSB0
F15	GBC0/IO72RSB0
F16	IO70RSB0
F17	IO71RSB0
F18	IO81PDB1
F19	IO81NDB1
F20	NC
F21	NC
F22	NC
G1	IO212NDB3
G2	IO212PDB3
G3	NC
G4	IO215NDB3

484-Pin FBGA*	
Pin Number	**A3P1000 Function**
G5	IO215PDB3
G6	GAC2/IO217PDB3
G7	IO217NDB3
G8	GNDQ
G9	IO21RSB0
G10	IO25RSB0
G11	IO31RSB0
G12	IO46RSB0
G13	IO53RSB0
G14	IO59RSB0
G15	GNDQ
G16	IO80NDB1
G17	GBB2/IO79PDB1
G18	IO82PDB1
G19	IO82NDB1
G20	IO84PDB1
G21	IO84NDB1
G22	NC
H1	NC
H2	NC
H3	V_{CC}
H4	IO210PDB3
H5	IO213NDB3
H6	IO213PDB3
H7	IO216PDB3
H8	VMV0
H9	V_{CCI}B0
H10	V_{CCI}B0
H11	IO38RSB0
H12	IO47RSB0
H13	V_{CCI}B0
H14	V_{CCI}B0
H15	VMV1
H16	GBC2/IO80PDB1
H17	IO79NDB1
H18	IO83PDB1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA*	
Pin Number	**A3P1000 Function**
H19	IO83NDB1
H20	V_{CC}
H21	NC
H22	NC
J1	IO209NDB3
J2	IO209PDB3
J3	NC
J4	IO210NDB3
J5	IO211NDB3
J6	IO211PDB3
J7	IO216NDB3
J8	V_{CCI}B3
J9	GND
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	GND
J15	V_{CCI}B1
J16	IO85PDB1
J17	IO85NDB1
J18	IO86PDB1
J19	IO86NDB1
J20	NC
J21	IO95PDB1
J22	IO95NDB1
K1	IO207NDB3
K2	IO207PDB3
K3	NC
K4	IO200PPB3
K5	IO208NDB3
K6	IO208PDB3
K7	GFC1/IO206PPB3
K8	V_{CCI}B3
K9	V_{CC}
K10	GND

484-Pin FBGA*	
Pin Number	**A3P1000 Function**
K11	GND
K12	GND
K13	GND
K14	V_{CC}
K15	V_{CCI}B1
K16	GCC1/IO88PPB1
K17	IO87PDB1
K18	IO87NDB1
K19	IO94PDB1
K20	IO94NDB1
K21	NC
K22	IO97PDB1
L1	NC
L2	IO199PDB3
L3	IO200NPB3
L4	GFB0/IO205NPB3
L5	GFA0/IO204NDB3
L6	GFB1/IO205PPB3
L7	V_{COMPLF}
L8	GFC0/IO206NPB3
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	V_{CC}
L15	GCC0/IO88NPB1
L16	GCB1/IO89PPB1
L17	GCA0/IO90NPB1
L18	IO91NPB1
L19	GCB0/IO89NPB1
L20	IO96PDB1
L21	IO96NDB1
L22	IO97NDB1
M1	NC
M2	IO199NDB3

484-Pin FBGA*	
Pin Number	**A3P1000 Function**
M3	IO201NPB3
M4	GFA2/IO203PPB3
M5	GFA1/IO204PDB3
M6	V_{CCPLF}
M7	IO202NDB3
M8	GFB2/IO202PDB3
M9	V_{CC}
M10	GND
M11	GND
M12	GND
M13	GND
M14	V_{CC}
M15	GCB2/IO92PPB1
M16	GCA1/IO90PPB1
M17	GCC2/IO93PDB1
M18	IO93NDB1
M19	GCA2/IO91PPB1
M20	IO98PDB1
M21	IO98NDB1
M22	NC
N1	IO198PDB3
N2	IO198NDB3
N3	NC
N4	GFC2/IO201PPB3
N5	IO203NPB3
N6	IO197PDB3
N7	IO197NDB3
N8	V_{CCI}B3
N9	V_{CC}
N10	GND
N11	GND
N12	GND
N13	GND
N14	V_{CC}
N15	V_{CCI}B1
N16	IO92NPB1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA*	
Pin Number	**A3P1000 Function**
N17	IO100NDB1
N18	IO100PDB1
N19	IO102PDB1
N20	NC
N21	IO101PDB1
N22	IO99PDB1
P1	NC
P2	IO196PDB3
P3	IO196NDB3
P4	IO195PDB3
P5	IO195NDB3
P6	IO194PDB3
P7	IO194NDB3
P8	V_{CCI}B3
P9	GND
P10	V_{CC}
P11	V_{CC}
P12	V_{CC}
P13	V_{CC}
P14	GND
P15	V_{CCI}B1
P16	GDB0/IO109NPB1
P17	IO103NDB1
P18	IO103PDB1
P19	IO102NDB1
P20	NC
P21	IO101NDB1
P22	IO99NDB1
R1	NC
R2	IO193PPB3
R3	V_{CC}
R4	IO191PDB3
R5	IO190PDB3
R6	IO190NDB3
R7	GEC0/IO187NPB3
R8	VMV3

484-Pin FBGA*	
Pin Number	**A3P1000 Function**
R9	V_{CCI}B2
R10	V_{CCI}B2
R11	IO144RSB2
R12	IO133RSB2
R13	V_{CCI}B2
R14	V_{CCI}B2
R15	VMV2
R16	IO107PDB1
R17	GDB1/IO109PPB1
R18	GDC1/IO108PDB1
R19	IO106PPB1
R20	V_{CC}
R21	IO104NDB1
R22	IO104PDB1
T1	IO193NPB3
T2	IO192PPB3
T3	NC
T4	IO191NDB3
T5	IO188PPB3
T6	GEC1/IO187PPB3
T7	IO188NPB3
T8	GNDQ
T9	GEA2/IO184RSB2
T10	IO153RSB2
T11	IO146RSB2
T12	IO134RSB2
T13	IO126RSB2
T14	IO121RSB2
T15	GNDQ
T16	IO107NDB1
T17	V_{JTAG}
T18	GDC0/IO108NDB1
T19	GDA1/IO110PDB1
T20	NC
T21	IO106NPB1
T22	IO105PDB1

484-Pin FBGA*	
Pin Number	**A3P1000 Function**
U1	IO192NPB3
U2	IO189PDB3
U3	IO189NDB3
U4	GEB1/IO186PDB3
U5	GEB0/IO186NDB3
U6	IO181RSB2
U7	IO178RSB2
U8	IO166RSB2
U9	IO159RSB2
U10	IO154RSB2
U11	IO148RSB2
U12	IO138RSB2
U13	IO131RSB2
U14	IO124RSB2
U15	VMV1
U16	TCK
U17	V_{PUMP}
U18	TRST
U19	GDA0/IO110NDB1
U20	NC
U21	NC
U22	IO105NDB1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO185PDB3
V5	GEA0/IO185NDB3
V6	IO177RSB2
V7	GEC2/IO182RSB2
V8	IO167RSB2
V9	IO160RSB2
V10	IO155RSB2
V11	IO150RSB2
V12	IO139RSB2
V13	IO130RSB2
V14	IO127RSB2

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

484-Pin FBGA*	
Pin Number	**A3P1000 Function**
V15	IO119RSB2
V16	GDB2/IO112RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	NC
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO176RSB2
W6	GEB2/IO183RSB2
W7	IO170RSB2
W8	IO164RSB2
W9	IO158RSB2
W10	IO152RSB2
W11	IO145RSB2
W12	IO137RSB2
W13	IO132RSB2
W14	IO125RSB2
W15	GDC2/IO113RSB2
W16	IO117RSB2
W17	GDA2/IO111RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	V_{CCI}B3
Y2	NC
Y3	NC
Y4	IO180RSB2
Y5	GND
Y6	IO173RSB2
Y7	IO169RSB2
Y8	V_{CC}
Y9	V_{CC}
Y10	IO151RSB2
Y11	IO143RSB2
Y12	IO136RSB2
Y13	NC
Y14	V_{CC}
Y15	V_{CC}
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	V_{CCI}B1

Note: **Refer to the "User I/O Naming Convention" section on page 2-44.*

Datasheet Information

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Web-only." The definition of these categories are as follows:

Product Brief

The product brief is a summarized version of a advanced datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

Unmarked (production)

This datasheet version contains information that is considered to be final.

International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR)

The products described in this datasheet are subject to the International Traffic in Arms Regulations (ITAR) or the Export Administration Regulations (EAR). They may require an approved export license prior to their export. An export can include a release or disclosure to a foreign national inside or outside the United States.

http://www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.

Dunlop House, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
Phone +44 (0) 1276 401 450
Fax +44 (0) 1276 401 490

Actel Japan
www.jp.actel.com

EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668

Actel Hong Kong
www.actel.com.cn

Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488

51700012-1/1.05