CIRRUS LOGIC

CL-SH260

Data Sheet

FEATURES

- Fully hardware- and software-compatible with PC XT/AT computers
- Provides direct bus interface logic with on-chip 24mA drivers
- Contains the logic for daisy chaining two embedded disk controller drives on a PC AT
- Supports host data transfer under DMA or Programmed I/O for both PC XT and PC AT modes
- Fast microcontroller interface — 16-MHz 8051, 12-MHz 68HC11
- Provides logic to speed up PC AT command response
- Provides on-chip registers to emulate the IBM® Task File for PC AT, IBM Command Descriptor Block for PC XT
- 84-pin PLCC or 100-pin QFP
- Low-power CMOS technology 84-pin PLCC or 100-pin QFP

Supports:

- direct buffer memory addressing up to 64 KBytes of static RAM
- any XT/AT interface speed with programmable and auto-inserted wait states
- interrupt or polled microcontroller interface

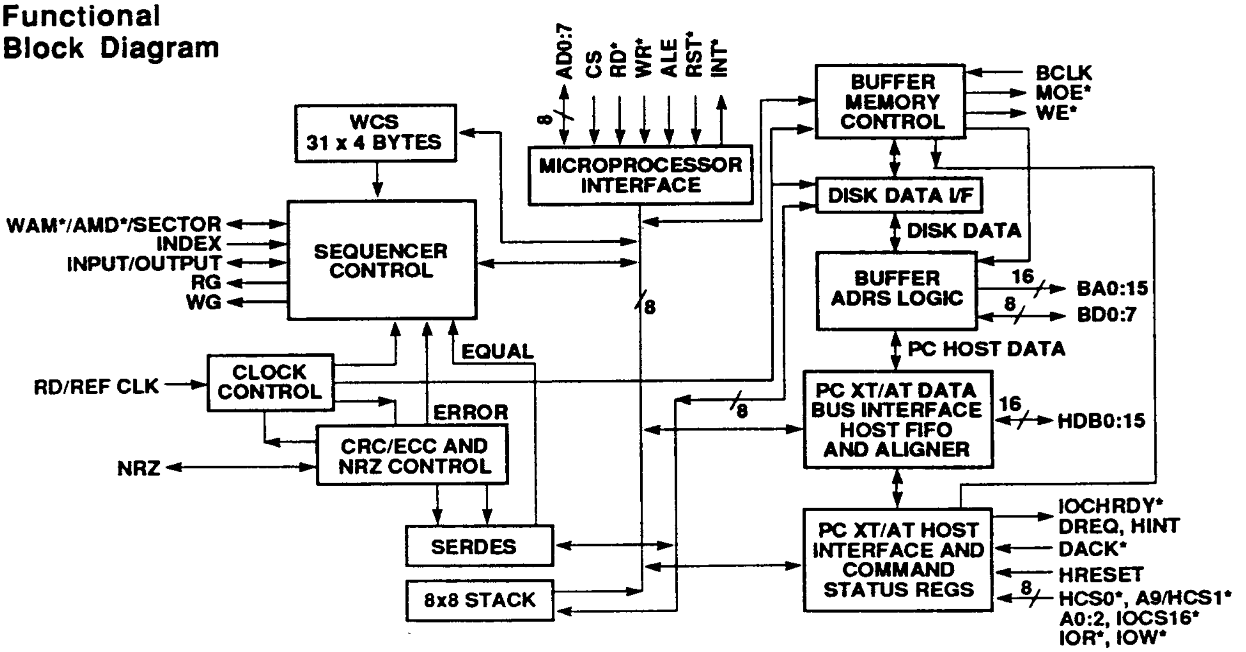
Enhanced PC XT/AT Disk Controller

OVERVIEW

The highly integrated CL–SH260 provides a large portion of the hardware necessary to build a Winchester disk controller for the PC XT/AT or other compatible interface. The CL-SH260 includes an advanced Winchester Disk Formatter, a dual-port Buffer Manager, and a host bus interface.

The CL-SH260 supports disk data rates up to 20 Mbits/sec., a requirement in high-performance disk drives. The CL-SH260's Disk Formatter consists of a serializer/deserializer, a flexible RAM-based Sequencer, and CRC/ECC generation circuitry. The industry standard 16-bit CCITT-CRC, conventional

Functional Block Diagram



January 1991

OVERVIEW (cont.)

The CL-SH260's Disk Formatter consists of a serializer/deserializer, a flexible RAM-based Sequencer, and CRC/ECC generation circuitry. The industry standard 16-bit CCITT-CRC, conventional 32-bit AT ECC polynomial, and a computer-generated 56-bit ECC polynomial are all supported in hardware. The ECC circuitry includes hardware correction assist logic to speed the correction process. The CL-SH260 Buffer Manager will control up to 64 KBytes of SRAM buffer memory as a dual port circular buffer.

The CL-SH260 works with a local microcontroller; it has a multiplexed address and data bus similar to that provided by the Intel® 8051 family of microcontrollers and the Motorola® 68HC11. It supports both interrupt and polled processor interfaces. The maskable interrupts include 11 disk and host interface events.

ADVANTAGES

Unique Features	**Benefits**
• *Provides automatic wait states or pre-programmed wait states for extended cycle transfers*	Can be compatible with any host CPU speeds. Prevents host overrun or underrun conditions.
• *Provides logic for daisy-chaining two embedded controller drives on the AT bus in a Master/Slave configuration*	Allows the use of two embedded disk controllers in a system.
• *Supports 8 MBytes/sec buffer memory throughput*	Can be used in high-performance applications.
• *31 Words of Writable Control Store*	Provides great flexibility to implement various formats and defect management schemes.
• *Computer-generated 56/32-bit ECC polynomial embedded in hardware*	Single-burst error correction up to 23 bits. Probability of miscorrection as low as 10^{-14} per bit corrected with the 56-bit polynomial.
• *ECC circuitry provides logic to speed up the correction process*	Hardware correction with minimal MPU intervention. Can correct within a single sector time.
• *Data rate up to 20 Mbits/sec.*	Can be used in high-performance applications.
• *Maskable microcontroller interrupt capability*	Relieves the microcontroller from polling to perform other tasks. Provides status information to the microprocessor when interrupts are disabled.
• *Sector Size Counter*	Reads and writes sectors larger than 512 bytes without microcontroller intervention.
• *Provides on-chip 24 mA-drivers with 300-pF drive capability for XT/AT interface*	Eliminates external hardware interface drivers.

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TABLES

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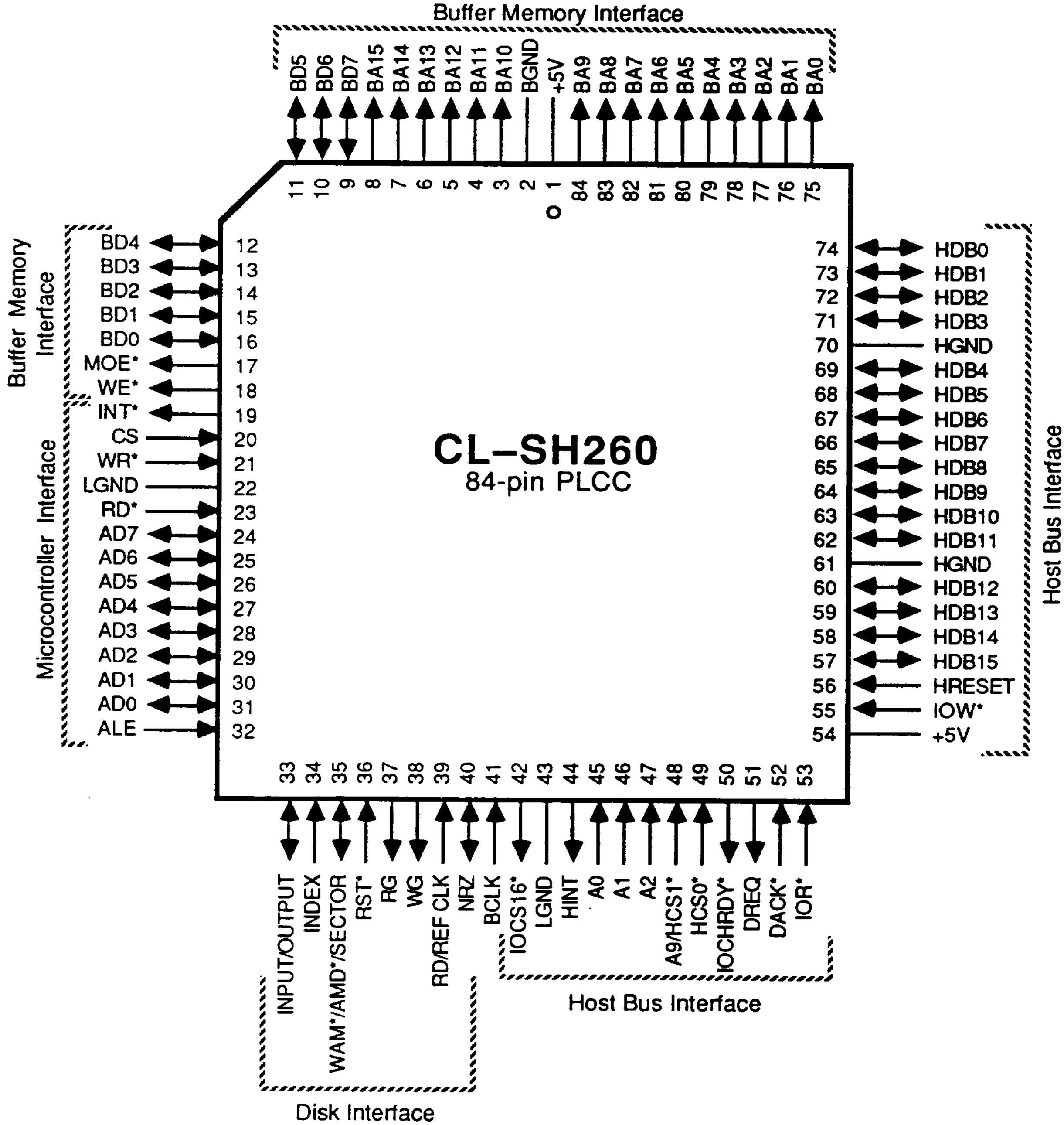
1. PIN INFORMATION

The CL-SH260 is available in either an 84-pin Plastic Leaded Chip Carrier (PLCC) or a 100-pin Quad Flat Pack (QFP) package. Pin numbers mentioned throughout the text refer to the 84-pin PLCC package unless otherwise noted. The diagram below shows the pin-out of the 84-pin package. All unused inputs must be tied to their inactive state to VCC or GND respectively.

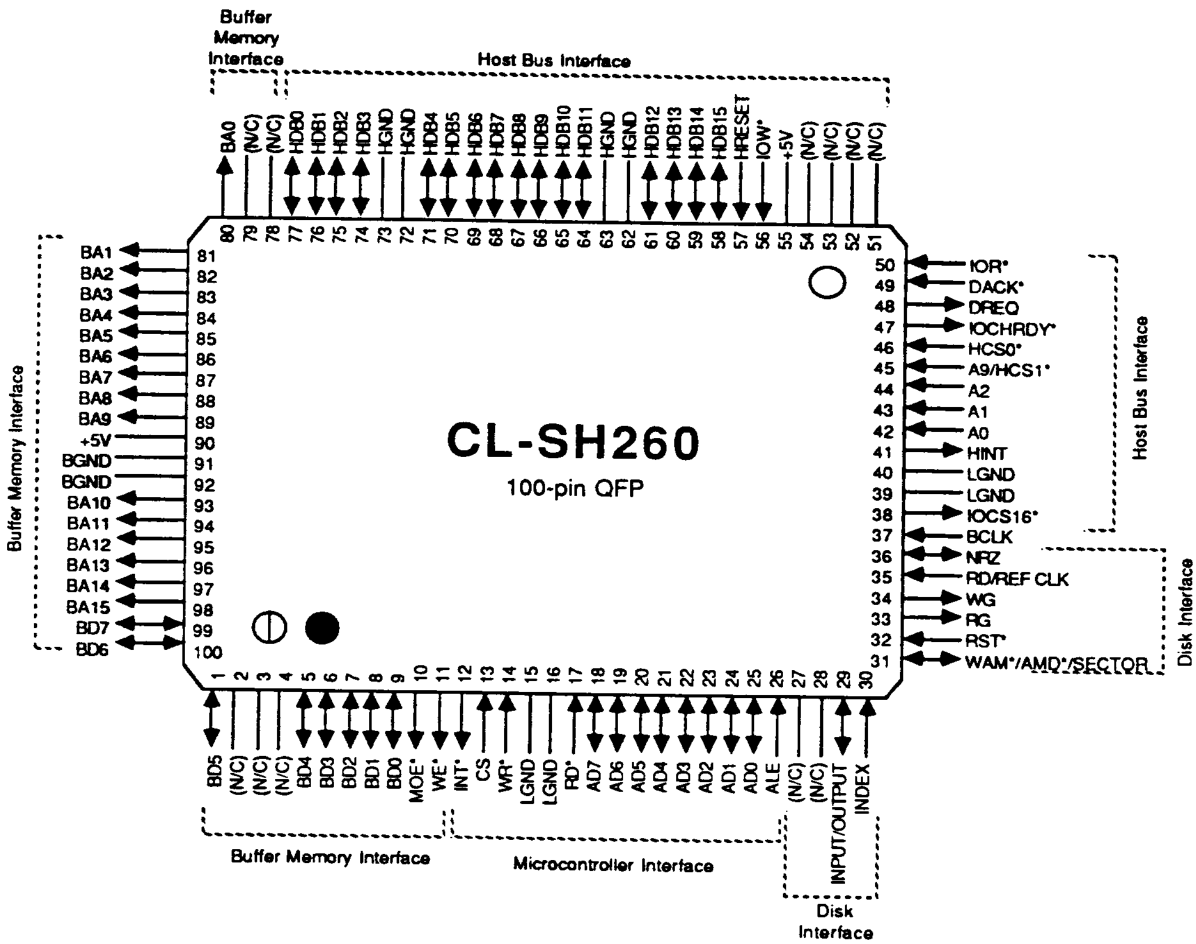
1.1 Pin Diagram for the 84-Pin Leaded Chip Carrier (PLCC)



*Denotes negative true signal

1.2 Pin Diagram for the 100-Pin Quad Flat Pack (QFP)

The CL-SH260 is available in either an 84-pin Plastic Leaded Chip Carrier (PLCC) or a 100-pin Quad Flat Pack (QFP) package. **Pin numbers mentioned throughout the text refer to the 84-pin PLCC package unless otherwise noted.** The diagram below shows the pin-out of the 100-pin package. All unused inputs must be tied to their inactive state to VCC or GND respectively.



*Denotes negative true signal.

1.3 Pin Assignments

The following conventions are used on the pin assignment tables. An asterisk (*) denotes a negative true signal. An (I) indicates an input pin. An (O) indicates an output pin. An input/output pin is indicated by (I/O). A (Z) indicates a tri-state output or input/output pin. Open drain output pins are indicated by (OD). The pin numbers throughout this data sheet refer to the 84-pin PLCC package unless otherwise noted.

BUFFER MEMORY INTERFACE PINS

SYMBOL	PIN NUMBER PLCC	QFP	TYPE	DESCRIPTION
BA0:15	75-84, 3-8	80-89, 93-98	O	**BUFFER MEMORY ADDRESS LINES**: Bits 0-15.
BD7:0	9-16	99-100,1,5-9	I/O	**BUFFER MEMORY DATA BUS:** These eight signals are Bits 0-7 of the 8-bit parallel data lines to/from the buffer memory.
MOE*	17	10	O	**MEMORY OUTPUT ENABLE**: This signal is asserted low when a buffer memory operation is active.
WE*	18	11	O	**WRITE ENABLE**: This signal is asserted low when a buffer memory Write operation is active.
BCLK	41	37	I	**SYSTEM CLOCK**: This is a clock input which is used to generate buffer memory access cycles.

MICROCONTROLLER INTERFACE PINS

SYMBOL	PIN NUMBER PLCC	QFP	TYPE	DESCRIPTION
INT*	19	12	O,OD	LOCAL MICROCONTROLLER INTERRUPT: This signal is programmable for either push-pull or open-drain output circuitry.
CS	20	13	I	**CHIP SELECT**: This signal must be asserted to access the CL–SH260 registers.
WR*	21	14	I	**WRITE**: When the WR* signal (Pin 21) is asserted low and the CHIP SELECT signal (Pin 20) is asserted high, the data on the A/D lines will be written into the specified register.
RD*	23	17	I	**READ**: When the RD* signal (Pin 23) is asserted low and the CHIP SELECT signal (Pin 20) is asserted high, the data from the specified register will be read on to the A/D lines.
AD7:0	24-31	18-25	I/O	**LOCAL MICROCONTROLLER ADDRESS/ DATA**: These are tri-state Address/Data lines which interface with a multiplexed microcontroller Address/Data bus.
ALE	32	26	I	**ADDRESS LATCH ENABLE**: This control signal latches the address on the A/D lines.

1.3 Pin Assignments *(cont.)*

MICROCONTROLLER INTERFACE PINS *(cont.)*

SYMBOL	PIN NUMBER PLCC	PIN NUMBER QFP	TYPE	DESCRIPTION
RST*	36	32	I	**RESET:** When this signal is asserted low, it stops all operations within the chip and deasserts the READ GATE (Pin 37) and the WRITE GATE (Pin 38) signals. All I/O signals and Host outputs are set to a high-impedance state. See the section on register intialization (Section 5.3).

DISK INTERFACE PINS

SYMBOL	PIN NUMBER PLCC	PIN NUMBER QFP	TYPE	DESCRIPTION
INPUT/ OUTPUT	33	29	/O	**INPUT/OUTPUT**: This is a general purpose control and status signal. It can be configured to be an input or an output in the SEQUENCER OUT ENABLE bit (Bit 6) of the FORMATTER MODE SELECTION Register (77H). When configured as an input, this signal is available to synchronize the Sector Format Sequencer to an external event. When configured as an output, this signal is controlled by Bit 2 of the CONTROL FIELD (A0H thru BEH) of the Writable Control Store (WCS). At power-on, this signal is configured as an input.
INDEX	34	30		**INDEX** : This is input for the INDEX pulse received from the disk drive.
WAM*/ AMD*/ SECTOR	35	31	I/O	**WRITE ADDRESS MARK / ADDRESS MARK DETECT/ SECTOR**: This signal can be configured to operate in Hard or Soft Sector mode by initializing the HARD SOFT* SECTOR MODE CONTROL bit (Bit 7) of the FORMATTER MODE SELECTION Register (77H). The default is Soft Sector mode. Also, in Soft Sector mode, when the READ GATE signal (Pin 37) is asserted, a low level input on this signal indicates Address Mark detected. In Hard Sector mode, this is the input for the SECTOR pulse.
RG	37	33	O	**READ GATE**: This signal is asserted when the CL-SH260 is reading NRZ data from the disk interface.
WG	38	34	O	**WRITE GATE**: This signal is asserted when the CL–SH260 is writing NRZ data to the disk interface.
RD/REF CLK	39	35	I	**READ/REFERENCE CLOCK**: This signal is used in conjunc - tion with the NRZ signal (Pin 40) to clock data in and out of the chip.
NRZ	40	36	I/O	**NRZ**: Read data input from the disk when the READ GATE signal (Pin 37) is asserted; write data output to the disk when the WRITE GATE signal (Pin 38) is asserted.

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1.3 Pin Assignments *(cont.)*

HOST BUS PINS

SYMBOL	PIN NUMBER PLCC	PIN NUMBER QFP	TYPE	DESCRIPTION
IOCS16*	42	38	OD	**16 BIT DATA TRANSFER**: This signal indicates that a 16-bit sector buffer transfer is active on the PC bus.
HINT	44	41	O,Z	**HOST INTERRUPT**: This signal is asserted to indicate to the Host that the disk controller needs attention.
A0:2	45-47	42-44	I	**HOST ADDRESS LINES**: The Host address lines A0:2 and A9 are used to access the various PC AT/XT control, status, and data registers. Only the A0:1 lines are used for PC XT operation.
A9/HCS1*	48	45	I	**A9/HCS1***: This is a multiplexed input signal. When the HCSI MODE ENABLE bit (Register 52H, Bit 3) is reset, this input is HOST ADDRESS LINE A9. When the HCSI MODE ENABLE bit (Register 52H, Bit 3) is set, this input is HOST CHIP SELECT 1. When this signal is configured as HCS1*, this input is ignored when the DACK* signal (Pin 52) is asserted low.
HCS0*	49	46	I	**HOST CHIP SELECT 0**: When this signal is asserted low, this input selects access to the control, status and data registers. This input is ignored when the DACK* signal (Pin 52) is asserted low.
IOCHRDY*	50	47	O,Z	**I/O CHANNEL READY**: This signal is asserted low to extend Host transfer cycles when the disk controller is not ready to respond.
DREQ	51	48	O,Z	**DMA REQUEST**: This signal is used during DMA transfer between the Host and the CL-SH260.
DACK*	52	49	I	**DMA ACKNOWLEDGE**: This signal is used during DMA to complete the DMA handshake for data transfer between the Host and the CL-SH260. In a typical AT application, this input signal is not used and should be pulled up to power through a 10 Kohm resistor.
IOR*	53	50	I	**INPUT READ SELECT**: This signal is asserted low by the Host during a Host Read operation. When this signal is asserted low with the HCS0*/HCS1* or the DACK* signal (Pin 52), status or data is enabled on to the Host data bus.
IOW*	55	56	I	**INPUT WRITE SELECT**: This signal is asserted low by the Host during a Host Write operation. When this signal is asserted low with the HCS0*/HCS1* or the DACK* signal (Pin 52), data from the Host data bus is strobed in to the CL-SH260.
HRESET	56	57	I	**HOST RESET**: When this signal is asserted, it initializes the Control/Status Registers and stops any command in process. See the section on register initialization (Section 5.3).

1.3 Pin Assignments *(cont.)*

HOST BUS PINS *(cont.)*

SYMBOL	PIN NUMBER PLCC	QFP	TYPE	DESCRIPTION
HDB[15:0]	57-60, 62-69, 71-74	58-61 64-71 74-77	I/O	**HOST DATA BUS**: During PC AT operations, Host signals HDB0:15 are used for word transfers between the buffer memory and the Host data bus signals HDB0:7 are used for control, status, and ECC byte access. During PC XT operation only the HDB0:7 lines are used; the HDB0:15 lines are tri-state.

POWER AND GROUND PINS

SYMBOL	PIN NUMBER PLCC	QFP	TYPE	DESCRIPTION
+5V	1,54	55,90	N/A	**POWER SUPPLY (+5).**
BGND	2	91-92	N/A	**BUFFER BUS GROUND.**
LGND	22,43	15-16, 39-40	N/A	**LOGIC GROUND.**
HGND	61,70	62-63,72-73	N/A	**HOST GROUND PINS.**

2. MICROCONTROLLER-ACCESSIBLE REGISTER TABLES

2.1 Buffer Manager and PC Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
50H	R	HOST INTERRUPT STATUS
51H	R/W	HOST INTERRUPT ENABLE
52H	R/W	UNIQUE FEATURES CONTROL/STATUS
53H	R/W	DMA CONTROL
54H	R/W	BUFFER SIZE
58H	R/W	PC MODE CONTROL
59H	R/W	BUFFER MANAGER/PC RESET CONTROL
5AH, 5BH	R/W	READ ADDRESS POINTER (RAP) (16 bits)
5CH, 5DH	R/W	WRITE ADDRESS POINTER (WAP) (16 bits)
5EH, 5FH	R/W	PC STOP POINTER (PC-SP) (16 bits)

2.2 Formatter Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
4EH	R/W	SECTOR SIZE
71H	R/W	ECC CONTROL
72H	R/W	ECC CORRECTION SHIFT-REGISTER/COUNTER
73H - 76H	R	ECC STATUS
77H	R/W	FORMATTER MODE SELECTION
78H	R	NEXT ACTIVE SEQUENCER ADDRESS
78H	W	BRANCH ADDRESS
79H	R	SEQUENCER STATUS
79H	W	SEQUENCER START ADDRESS
7AH	R/W	OPERATION CONTROL / STATUS
7BH	R/W	WAM CONTROL
7CH	R/W	SYNC PATTERN
7DH	R	FORMATTER INTERRUPT STATUS
7EH	R/W	FORMATTER INTERRUPT ENABLE
7FH	R	FORMATTER STACK READ
7FH	W	CLOCK/SYNC CONTROL

2.3 External Access Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
4DH	R	SHADOW LATCH
70H	R/W	BUFFER MEMORY ACCESS

2.4 Writable Control Store (WCS)

ADDRESS	TYPE	DESCRIPTION/FUNCTION
80H-9EH	R/W	NEXT ADDRESS FIELD
A0H-BEH	R/W	CONTROL FIELD
C0H-DEH	R/W	COUNT FIELD
E0H-FEH	R/W	DATA FIELD

2.5 Sequencer Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
49H-4CH	R/W	CURRENT SEQUENCER WORD

2.6 Microcontroller–Host Interface Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
40H-47H or 60H-67H	R/W	HOST REGISTER FILE
55H-57H	R/W	HOST CONTROL/STATUS
73H	W	AUTOCOMMAND "LOCK" RELEASE

3. FUNCTIONAL DESCRIPTION

The CL-SH260 is designed to be used with a low cost microcontroller, which allows it to maintain a "loose" synchronization with the real-time disk operation. The CL-SH260 maintains "close" synchronization with the data to and from the disk drive and provides the signals necessary to control this path. Using the CL-SH260 means a lower total part count for the intelligent disk drive design with the PC XT/AT interface.

The CL-SH260 is divided into four major functional blocks:

- Microcontroller Interface
- Disk Formatter
- Buffer Memory Interface
- Host Interface

3.1 Microcontroller Interface

The microcontroller interface is based on an eight-bit multiplexed address and data bus found on popular microcontrollers such as the Intel 8085/8031/8051 and the Motorola 68HC11.

The CL-SH260 decodes addresses from 40H to FFH. In order to prevent erroneous operations, the disk controller board design should reserve the decoding of addresses 40H to FFH for the CL–SH260 only. However, the CL–SH260 does not decode addresses 68H to 6FH and the decoding of addresses 40H-47H as well as 60H-67H can be totally disabled by resetting the HOST REGISTER FILE ACCESS ENABLE bit (Register 77H, Bit 1). In that case the CL-SH260 will not decode addresses 40H-47H and 60H-67H as well.

The CL–SH260 provides a register file which the microcontroller can access to interface with the Host. This register file can be mapped to either 40H-47H or 60H-67H (when access to the register file is enabled — Register 77H, Bit 1 is set) by programming the HOST REGISTER FILE DECODE SELECT bit (Register 77H, Bit 2). Mapping these registers into address 40H-47H will disable the CL–SH260 from decoding addresses 60H-67H (they can be used for external system use). Mapping them into 60H-67H will make addresses 40H-47H available for external system use.
The definition of these registers is also different when the CL–SH260 is programmed to operate in the PC XT mode versus the PC AT mode. For detailed descriptions, see the Microcontroller Host Interface section (Section 13).

The CL-SH260 has a programmable interrupt circuit available. There are 11 interrupt sources available from both the Buffer Manager/PC Registers and from the Formatter Registers, as shown in Tables 3.1 and 3.2

Table 3.1 Buffer/PC Interrupt Sources

*PC Transfer Overrun /Underrun Detected	*Host Transfer Done
*PC Reset Detected	*PC Selection Phase Detected

Table 3.2 Formatter Interrupt Sources

*Data Transfer Detected	*Input Detected
*Sequencer Output Detected	*ECC Error
*Sequencer Stopped	*Index Past
*Sector Past	

The interrupt capability can be completely disabled (by resetting Register 77H, Bit 3), or the individual interrupt sources can be masked. Four interrupt registers provide the status and mask programmability for interrupt sources. Even when the interrupts are disabled (Register 77H, Bit 3 is reset), the Interrupt Status Registers may be used as a focal point for microcontroller control when the CL-SH260 is being used in a polled mode.

The CL-SH260 provides the microcontroller read access to external switch settings. The microcontroller accesses these switches by reading Register 70H, with the MOE* DISABLE bit (Register 52H, Bit 0) set to logical 1. The microcontroller-readable switches connect to the buffer memory data bus. These switches must be installed with relatively high impedance pull-ups and pull-downs so that the resistor impedance does not affect buffer memory performance (it is recommended to use 270 KΩ pull-up and 27 KΩ pull-down resistors and wait 25 µsec after the last buffer memory access for stability).

3.2 Disk Formatter

The operation of the Disk Formatter is controlled by the contents of the Sequencer Writable Control Store (WCS). A Sequencer program must be entered into the Writable Control Store (WCS) before the CL–SH260 Disk Formatter can function properly. Under firmware control, the Disk Formatter can be made to sequence through different types of operations, such as: Read ID, Read ID and Read Data, Read ID and Write Data, and Write ID and Write Data.

The Sequencer controls the timing relationships between the disk interface output signals and monitors disk interface input lines to branch to different Sequencer locations. The track layout, such as gap lengths, sector size, and sector data fill character, can be flexibly defined in the Writable Control Store (WCS). The CL–SH260 Disk Formatter also has other registers that can be used to control the definition of the track format such as the SYNC character or the ADDRESS MARK.

The Writable Control Store (WCS) consists of 124 bytes, organized as 31 words, each four bytes wide. The Writable Control Store (WCS) word can be broken down into DATA, COUNT, NEXT ADDRESS and CONTROL FIELDS.

The DATA FIELD contains data which may be used to initialize the track format, including gap, ID field, and sector data fill characters. This data can also be compared to the NRZ data-in to identify various fields in a sector or to execute sector data compares.

The COUNT FIELD specifies the initial value minus one of the Sequencer counter for the current word. The Sequencer counter is decremented once every eight READ/-REFERENCE CLOCK (RD/REF CLK) cycles. When the count reaches zero, the Sequencer will go to the next address.

The next address will be based on the contents of the NEXT ADDRESS FIELD of the Writable Control Store (WCS) word unless a branch condition has been programmed and met during the last byte of the current Writable Control Store (WCS) word.

If a branch condition has been programmed and met, then the next address to be executed is based on the contents of the BRANCH ADDRESS Register (78H). Thus, by programming different branch conditions which are based on external or internal events, the chip can be made to sequence through different operations.
The CONTROL FIELD is used to generate and initiate all synchronous NRZ data handling operations.
The microcontroller's control of the Sequencer revolves around the SEQUENCER START ADDRESS (Register 79H) and the BRANCH ADDRESS (Register 78H). Writing to Register 79H loads the starting address (where the Sequencer is to begin execution), and causes the four bytes at that Writable Control Store (WCS) word to be fetched and written into the Current Sequencer Word Registers (Registers 49H-4CH).

The serial data flow portion of the Disk Formatter consists of a CRC/ECC generator and a serializer/deserializer. Data to be written to the disk enters the CL–SH260 in a byte-wide format. It is serialized and processed through a CRC/ECC generator. An NRZ serial bit stream is then shifted out to the disk drive. Note that the NRZ serial bit stream will include serialized constants required for Address Marks, gaps, and ID fields, as well as the serialized data and ECC generated output.

The CL–SH260 can be programmed (in the Writable Control Store (WCS) COUNT FIELD) for CRC or an ECC polynomial. It can be fully suppressed to use external ECC circuitry.

The CRC polynomial used is the CCITT CRC code:

$$x^{16}+x^{12}+x^{5}+1$$

The CL–SH260 provides the option of using a 56-bit or a 32-bit ECC polynomial by programming the COUNT FIELD of the appropriate Writable Control Store (WCS) word. The forward and reverse 56-bit ECC polynomial is a computer-generated code provided under license from Neal Glover of Data Systems Technology, Broomfield, CO. The forward polynomial is:

$$x^{56}+x^{52}+x^{50}+x^{43}+x^{41}+x^{34}+x^{30}+x^{26}+x^{24}+x^{8}+1$$

The reverse polynomial is:

$$x^{56}+x^{48}+x^{32}+x^{30}+x^{26}+x^{22}+x^{15}+x^{13}+x^{6}+x^{4}+1$$

This polynomial can detect single burst errors up to 56 bits in length, and double-burst errors, where the combination of bursts is less than or equal to 41 bits. This polynomial can also correct single-burst errors up to 23 bits in length. The 32-bit ECC polynomial is the standard polynomial found in IBM PC AT controllers.
The forward polynomial is:

$$x^{32}+x^{28}+x^{26}+x^{19}+x^{17}+x^{10}+x^{6}+x^{2}+1$$

The reverse polynomial is:

$$x^{32}+x^{30}+x^{26}+x^{22}+x^{15}+x^{13}+x^{6}+x^{4}+1$$

The forward and reverse polynomial is selected by programming ECC CONTROL (Register 71H, Bit 7). Whichever polynomial is selected, the ECC/CRC shift registers always start preset to all 1's.

Data read from the disk enters the CL–SH260 as an NRZ serial bit stream. The input data stream is processed through the ECC generator and deserialized into a byte-wide format. The syndrome is saved in the ECC registers.

If an ECC error is detected after a Read Data operation, the microcontroller uses Registers 71H - 76H to determine if the error is correctable and to calculate the error pattern and displacement from the beginning of the sector. After this, the error can be corrected in the data bytes in the buffer memory. The CL-SH260 has hardware assist circuitry to speed up the correction process.

During a read process from the device, the CL–SH260 also has the ability to compare the data being received on a byte-by-byte basis with information either from the DATA FIELD of the Writable Control Store (WCS) (such as verifying the ID field) or from the external buffer memory (such as during a data field search operation).

The CL–SH260 also has a circular stack eight bytes deep. By enabling this (setting Bit 4 of the Writable Control Store (WCS) CONTROL FIELD) during the Read operation, information read from the disk drive can be pushed onto the stack to be examined later at a lower speed by the microcontroller (Register 7FH). This capability can be used to pass the ID field to the microcontroller for defect management, seek verification and other disk controller tasks.

3.3 Buffer Memory Interface

Byte-wide data transferred by the CL–SH260 is passed to and from the buffer memory on the BUFFER MEMORY DATA BUS (BD7:0).

The CL–SH260 is capable of controlling buffer memory sizes up to 64K bytes of static RAM. The chip provides 16 buffer memory address lines (BA0:15), along with a Memory-Output-Enable (MOE*) signal (Pin17) and a Write-Enable (WE*) signal (Pin 18) for the static buffer memory.

The period of the buffer memory access cycles is determined by programming Bits 6 and 7 of the CLOCK/SYNC CONTROL Register (7FH) and is based on the BCLK input (Pin 41). The CL–SH260 can support up to 8 MBytes/sec of buffer memory throughput. The period of the buffer memory access cycles, along with other CL–SH260 specifications, determines the access time requirement for the buffer memory. The CL-SH260 samples the data from the RAM at the falling (trailing) edge of BCLK. The equations below can be used to determine the buffer memory throughput and the RAM speeds to be used.

$$\text{Buffer Memory Throughput} = \frac{1}{\text{Period of memory access cycle}}$$

T_1 = Period of buffer memory access cycle

For Buffer Memory Read

Max. Read Access Time = $T_1 - Av_{max} - Dis_{min}$

Min. Output Enable = $T1/2 - Mv_{max} - Dis_{min}$

For Buffer Memory Write

Address set up to WE* ↑ = $T_1 - Av_{max} + Wh_{max}$

Data set up to WE* ↑ = $T1/2 - Dov_{max} + Wh_{max}$

NOTE: For Av_{max}, Dis_{min}, Mv_{max}, Wh_{max}, Dov_{max} definitions, refer to the buffer memory Read/Write timing parameters (Section 14.3 A.C. Characteristics).

Register 70H decode is provided for the microcontroller to gain access to the buffer memory. The buffer memory data bus and the microcontroller data bus are internally bridged accordingly. Register 70H should not be accessed during Host or Disk transfers with the buffer memory.

Register 70H buffer memory access locations are based upon the contents of the READ ADDRESS POINTER (RAP — Registers 5AH and 5BH) if the ROP/WOP* bit (Register 53H, Bit 4) is reset to logical 0 (WOP*); and on the contents of the WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH) if the ROP/WOP* bit (Register 53H, Bit 4) is set to logical 1 (ROP). The READ ADDRESS POINTER (RAP — Registers 5AH and 5BH) or the WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH) will not be incremented by an accesses to Register 70H.

Disk Transfer

In case of disk transfers, a byte is transferred as the Disk Formatter requires service (for a deserialized byte or a byte to serialize). The direction of the transfer is determined by the value of ROP/WOP* bit (Register 53H, Bit 4). For a Disk Read operation, the ROP/WOP* bit (Register 53H, Bit 4) is set to logical 1 and the NRZ data is deserialized and written to the buffer memory at the location specified by the contents of the WRITE ADDRESS POINTER (WAP) Registers (5CH and 5DH). For a Disk Write operation the ROP/WOP* bit (Register 53H, Bit 4) is reset to logical 0 and the data read from the buffer memory at the location specified by the contents of the READ ADDRESS POINTER (RAP) Registers (5AH and 5BH) is serialized and written to the disk.

Host Data Transfer

In case of transfers between the Host bus and the buffer memory, data is transferred under DMA or Programmed I/O (PIO) control. The direction of transfer is determined by the contents of the HOST WRITE ENABLE and the HOST READ ENABLE bits (Register 53H, Bits 2 & 3 respectively), along with the ROP/WOP* bit (Register 53H, Bit 4).

NOTE: For correct operation of the CL–SH260, the ROP/WOP* bit (Register 53H, Bit 4) MUST be set to logical 1 when the HOST READ ENABLE bit (Register 53H, Bit 3) is set. Also, the ROP/WOP* bit (Register 53H, Bit 4) MUST be reset to logical 0 when the HOST WRITE ENABLE bit (Register 53H, Bit 2) is set.

If the HOST READ ENABLE bit (Register 53H, Bit 3) and the ROP/WOP* bit (Register 53H, Bit 4) are set to logical 1, the READ ADDRESS POINTER (RAP—Registers 5AH and 5BH) is used during transfers from the buffer memory to the Host.

If the HOST WRITE ENABLE bit (Register 53H, Bit 2) is set to logical 1 and the ROP/WOP* bit (Register 53H, Bit 4) is reset to logical 0, the WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH) is used during transfers from the Host to the buffer memory.

During Host data transfers, the last buffer memory address that can be accessed is controlled by the PC STOP POINTER (Registers 5EH and 5FH). This PC STOP POINTER (Registers 5EH and 5FH) is compared with the appropriate Address Pointer (the READ ADDRESS POINTER—RAP (Registers 5AH and 5BH), or the WRITE ADDRESS POINTER —WAP (Registers 5CH and 5DH)), masked by the contents of the BUFFER SIZE Register (54H). When a match occurs, the HOST TRANSFER DONE bit (Register 53H, Bit 5) is set signifying the completion of the transfer to or from the Host.

3.4 PC Host Interface

The CL–SH260 provides the capability for direct connection to the Host bus. The drivers can sink up to 24mA current and drive a load up to 300pf.

The CL–SH260 also provides circuitry to extend the Host I/O cycle and insert Wait states by asserting low the IOCHRDY* signal (Pin 50). This circuit is only active during Programmed I/O Host transfers. The CL–SH260 inserts Wait states in the following two ways:

(1) It can be programmed in PC WAIT STATE (Register 58H, Bits 0 and 1) to insert Wait states on any Host

I/O transfer. This can be used to extend the width of the IOR*/IOW* pulse in case of a fast CPU with short IOR*/IOW* pulses.

(2) When a Wait state is enabled (Register 58H, Bit 2 is set), it will be automatically inserted by asserting low the IOCHRDY* signal (Pin 50) (only during Host I/O transfers to/from buffer memory) when the CL–SH260 is not ready for the transfer.

If programmed Wait states (as in 1) are enabled, the automatic Wait state circuit will be activated after the programmed number of Wait states have been inserted if additional Wait states are necessary.

The CL–SH260 has circuitry to speed up the performance of the disk controller by decoding Write commands requiring data transfer from the Host to the buffer memory, i.e., Format (5XH), Write Buffer (E8H), Write or Write Long (3XH). The CL–SH260 will automatically start accepting data from the Host without local microcontroller control when the AT HOST COMMAND Register is loaded by the Host. If interrupts are enabled, the CL-SH260 then generates an interrupt to the local microcontroller. The PC STOP POINTER (Registers 5EH and 5FH) is initialized to 01FFH. If the DISABLE STOP POINTER COMPARE bit (Register 52H, Bit 6) is set, the local microcontroller must initialize the PC STOP POINTER (Registers 5EH and 5FH) to enable the comparison of the WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH) with the PC STOP POINTER (Registers 5EH and 5FH). The CL–SH260 Disk Formatter will disconnect from the Buffer Manager on receiving one of these commands. It will also disable write access by the local microcontroller to Registers 53H, 5CH, 5DH, and read/write access to Register 70H. Access to these registers will be enabled when the local microcontroller writes to Register 73H. The local microcontroller must write to Register 73H to restart a transfer between the Disk Formatter and the buffer memory.

If Bit 1 of the command byte is set (for Read/Write Long commands) then all buffer memory transfers to/from the Host will exceed the PC STOP POINTER (Registers 5EH and 5FH) by the count of ECC bytes. Initially the PC STOP POINTER (Registers 5EH and 5FH) is set at the end of the data field. When the active READ ADDRESS POINTER (RAP — Registers 5AH and 5BH) or WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH) matches the PC STOP POINTER (Registers 5EH and 5FH), the internal FIFO will be emptied of the word width data. The ECC bytes will then be transferred in Byte mode and the respective Address Pointer will be incremented by the number of ECC bytes.

The CL–SH260 provides circuitry to support two embedded AT disk controller drives in a system. There are two bits (Bits 1 and 2) in Register 52H for this configuration. The MASTER/SLAVE MODE ENABLE bit (Register 52H, Bit 1) must be set to enable the two disk drive Master/Slave configuration. The MASTER/SLAVE SELECT bit (Register 52H, Bit 2) configures the disk drive as a Master or Slave. If this bit is set, the disk controller responds as a Slave (i.e., it responds when the disk drive number in the AT HOST DRIVE/HEAD Register [Port 1F6H] is set to 1). In general, the register files in both controllers (configured as Master and Slave) will be written to by the Host, no matter which disk drive is selected in the AT HOST DRIVE/HEAD Register. Only the selected disk drive, however, will execute the command. The only exception is during Power-up or Diagnostic commands. In that case, both the Master and the Slave will run the diagnostics but the Master will return the status to the Host.

4. FUNCTIONAL OPERATION

The CL–SH260 performs two basic disk operations, reading NRZ data in and writing NRZ data out. These two operations can be combined easily into the following four major functions:

- Read ID or Sector Identification
- Read ID and Write Data or Sector Write
- Read ID and Read Data or Sector Read
- Write ID and Write Data or Format Sector

These can be further modified to perform the Search Data and Verify Data functions.

Read Operation

One of the requirements of the Read operation is to synchronize the incoming data on byte boundaries and then either process the data or pass the data through to the buffer memory.

Data synchronization occurs when a specific incoming data stream compares to the sync pattern programmed in the SYNC PATTERN Register (7CH). The number of bits used in the synchronization comparison is specified by the contents of the CLOCK/SYNC CONTROL Register (7FH), Bits 0-2. The process begins when the CONTROL FIELD of the Current Sequencer Word activates the READ GATE (RG) signal (Pin 37). The serial data passes through a programmable synchronization comparator until a match is found with the contents of the SYNC PATTERN Register (7CH). If the CL-SH260 is in soft-sectored mode, the comparison must be qualified by the assertion low of the WAM*/AMD*/SECTOR signal (Pin 35) by the time the last NRZ bit of the sync pattern is read into the CL-SH260.

Typically, for soft-sectored formats, the first byte after the synchronization byte is used to differentiate between Sector ID and Data Fields. After synchronization, the Sequencer has the ability to enable the comparison of the incoming data against the DATA FIELD of the Writable Control Store (WCS) and also to capture the incoming data on the stack. The comparison and branch capability of the Sequencer allows the incoming data to be recognized and acted upon. The programmable compare capability can be used to access the correct sector automatically by recognizing the proper Sector ID. If the Sector ID does not match the DATA FIELD of the Current Sequencer Word then the Sequencer can be programmed to stop, and can be restarted by the microcontroller to find the sector again.

Write Operation

The other disk operation of the CL–SH260 is writing NRZ data. This operation begins when the CONTROL FIELD in the Current Sequencer Word activates the WRITE GATE (WG) signal (Pin 38). The WRITE GATE signal (Pin 38) is typically switched on at a specific place in the track layout: during a Write splice after the sector ID ECC (for a Write Sector Data operation), or after INDEX (for a Track Format operation). Data from the Current Sequencer Word's DATA FIELD or from the buffer memory data bus is passed through the serializer then through the ECC circuitry, and out the NRZ data signal (Pin 40).

4.1 Sector Identification

The Sector Identification function consists of reading the Sector ID field to identify to the microcontroller the current sector address. This function is typically performed with a comparison of the Sector ID field Address Mark, a capture of the Sector ID field in the stack, and finally an ECC/CRC verification of data integrity. Any of the incoming data bytes may be captured in the stack by programming the STACK ENABLE bit (Bit 4) in the Writable Control Store (WCS) CONTROL FIELD. Also, any of the incomng data bytes may be compared against the Writable Control Store (WCS) DATA FIELD by programming both the Writable Control Store (WCS) DATA FIELD and the COMPARE ENABLE bit (Bit 1) in the Writable Control Store (WCS) CONTROL FIELD.

After the Sector Identification function is completed, the microcontroller can then read the SEQUENCER STATUS Register (79H). If there was no ECC error, the microcontroller can then read the stack to identify the current sector address or it may repeat the function.

4.2 Sector Read

The Sector Read function typically consists of two parts. The first is reading and identifying the desired Sector ID field. This is described in the Sector Identification section (Section 4.1); however, the desired sector address will also be included in the comparison. A branch condition is often programmed at the end of the Sector Identification function such that if the compared bytes match and there was no ECC error, the sequencer will automatically execute the second half of the Sector Read function.

After the sector has been positively identified, the second half of the Sector Read function is to transfer the Sector Data field to the bufffer memory. After the read, the microcontroller may then read the SEQUENCER STATUS Register (79H) and determine the completion status of the Sector Read.

If the read was successful, then the microcontroller will typically program the CL–SH260 to transfer this sector from the buffer memory to the Host. If the read was not successful, the microcontroller may try to correct the data or attempt to re-read this sector.

4.3 Sector Write

The Sector Write function typically consists of two parts. The first is identical with the first part of the Sector Read; reading the Sector ID field. The same Sequencer routine should be used. The only difference is that after a successful Sector ID read, the next address should be the address of the Write Sector routine. This can usually be accomplished by changing the address in the BRANCH ADDRESS Register (78H) after a successful ID read.

After the sector has been positively identified, the second half of the Sector Write function is to transfer the data from the buffer memory to the disk as explained above in the Write operation.

4.4 Format Sector

The Format Sector function consists of a Write operation that will write both the Sector ID field and the Sector Data field. This function is normally started with the Sequencer waiting for the INDEX pulse to branch into the Write operation routine. The microcontroller can update the Sector ID field information in the Writable Control Store (WCS) while the Sector Data field is being written on the disk. This allows a full track format with a minimum of microcontroller intervention.

The CL–SH260 allows the Sector Data field to be generated from the Writable Control Store (WCS) instead of from the buffer memory, through the use of the SUPPRESS TRANSFER bit (Register 7AH, Bit 5).

4.5 Search Data

The Sector Read function can be modified into a Search Data function. When the second half of the Sector Read function is entered, the contents of the buffer memory will be compared, byte-for-byte, with the incoming data from the disk drive. This comparison of the DATA FIELD is enabled by setting the SEARCH OPERATION bit (Bit 4) of the OPERATION CONTROL/STATUS Register (7AH), and the COMPARE ENABLE bit (Bit 1) in the CONTROL FIELD of the Writable Control Store (WCS) word which starts the data transfer.

The result of this comparison is latched in to the SEQUENCER STATUS Register (79H, Bits 0 and 1). Be sure to reset both the SEARCH OPERATION bit (Register 7AH, Bit 4) and the COMPARE ENABLE bit (CONTROL FIELD, Bit 1) after the completion of the Search Data function.

4.6 Verify Sector

By setting the SUPPRESS TRANSFER bit in the OPERATION CONTROL/STATUS Register, (7AH, Bit 5) and performing a Read Sector function, the incoming data will be verified for good ECC but will not be transferred to the buffer memory.

4.7 Extended Data Handling

Variable Sector Size

The CL–SH260 has an eight-bit Sector Data field length counter loadable from the COUNT FIELD of the Writable Control Store (WCS). The COUNT FIELD is programmable. By setting it to any value from 00H to FFH, any block length up to 256 bytes can be transferred. The value of the COUNT FIELD should be one less than the actual sector length. For sector sizes greater than 256 bytes, several different methods can be used.

The simplest approach is to use as many Sequencer words as required to implement the count for the data field.

The next approach uses the INHIBIT CARRY bit in the OPERATION CONTROL/STATUS Register (7AH, Bit 7). By setting the INHIBIT CARRY bit (Register 7AH, Bit 7), before the count of the Writable Control Store (WCS) word with the DATA TRANSFER bit (CONTROL FIELD, Bit 0) set has expired, the Sequencer will be inhibited from going on to the next Writable Control Store (WCS) word, and another 256 bytes of data will be transferred.

The INHIBIT CARRY bit (Register 7AH, Bit 7) will be automatically reset on the next carry of the word with the DATA TRANSFER bit (CONTROL FIELD, Bit 0) set (underflow of the current control word's count field). By testing and setting this bit, additional counts of 256 byte segments may be transferred.

For odd-sized data fields, initialize the COUNT FIELD with the remainder and use the modulo-256 counter for the bulk of the counting. For example, for 532 bytes start with a count of 19 and set the INHIBIT CARRY bit (Register 7AH, Bit 7) twice.

The final approach uses the COUNT FIELD and the INHIBIT CARRY bit (Register 7AH, Bit 7) as well as the SECTOR SIZE Register (4EH) to program how many 256 byte counts the INHIBIT CARRY bit (Register 7AH, Bit 7) should suppress. The number initialized in the SECTOR SIZE Register (4EH) should be one less than the number of multiples of 256 byte segments to be transferred.

For example, for 532 bytes start with the SECTOR SIZE Register (4EH) initialized to 01H, an initial count of 13H in the Writable Control Store (WCS) COUNT FIELD, and set the INHIBIT CARRY bit (Register 7AH, Bit 7).

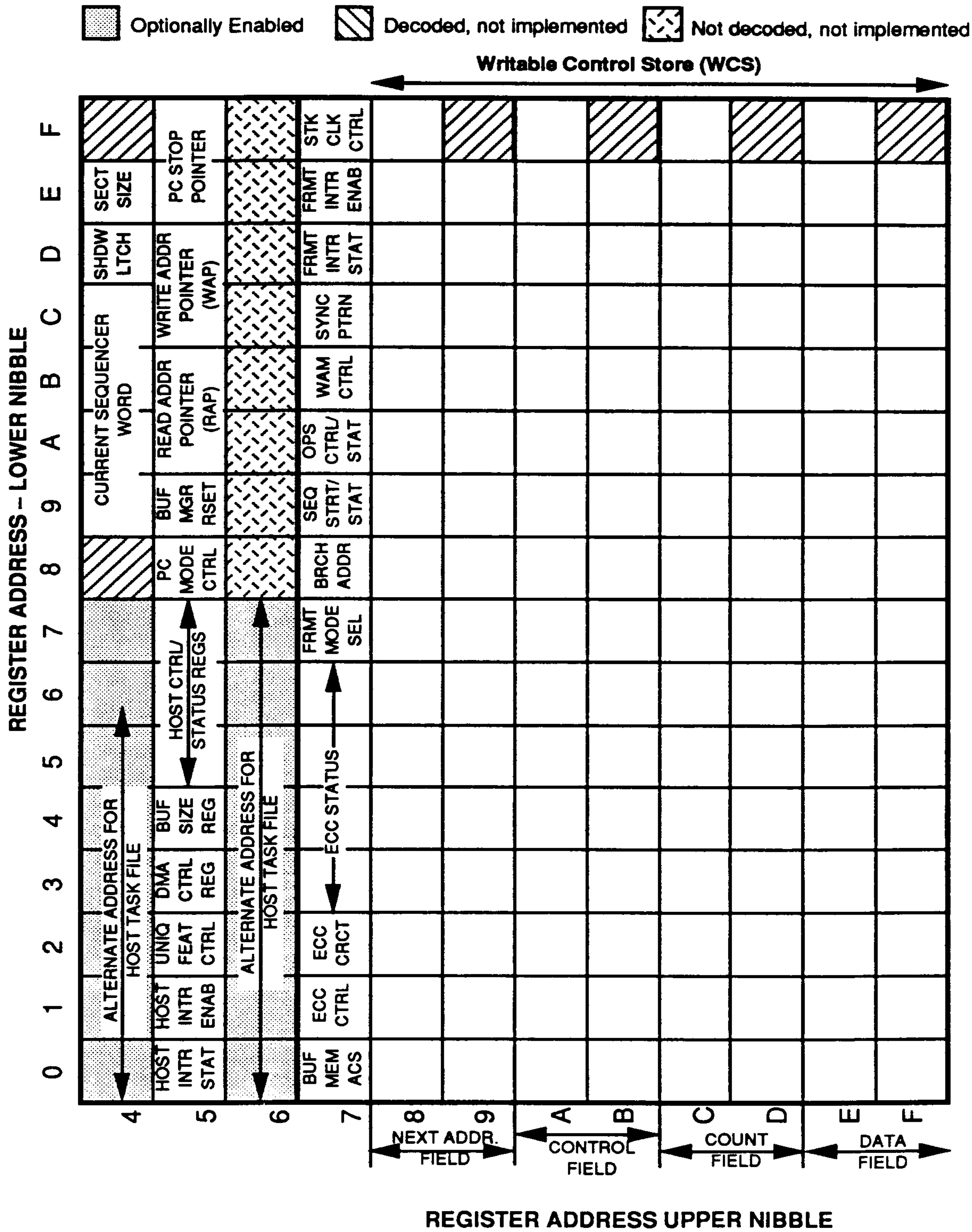
Multi Sector Read/Write Operations

Multi-sector Read or Write operations can be accomplished by two methods. The simplest method is to load the next sector ID to be accessed while the DATA TRANSFER STATUS bit (Register 79H, Bit 6) is set for the present sector, and to restart the Read or Write operation immediately after the end of the present sector.

The next approach loads multiple ID field read subroutines and a single read/write data field subroutine into the thirty-one word Writable Control Store (WCS). The BRANCH ADDRESS (Register 78H) can then be used to jump between the subroutines.

5. REGISTER ADDRESSES

5.1. Memory Map



5.2. Writable Control Store (WCS) Worksheet

Microprocessor Register Addresses

SEQUENCER ADDRESS	BRANCH ADDRESS (Reg. 78H)		NEXT ADDRESS FIELD		CONTROL FIELD		COUNT FIELD		DATA FIELD
0		80		A0		C0		E0	
1		81		A1		C1		E1	
2		82		A2		C2		E2	
3		83		A3		C3		E3	
4		84		A4		C4		E4	
5		85		A5		C5		E5	
6		86		A6		C6		E6	
7		87		A7		C7		E7	
8		88		A8		C8		E8	
9		89		A9		C9		E9	
A		8A		AA		CA		EA	
B		8B		AB		CB		EB	
C		8C		AC		CC		EC	
D		8D		AD		CD		ED	
E		8E		AE		CE		EE	
F		8F		AF		CF		EF	
10		90		B0		D0		F0	
11		91		B1		D1		F1	
12		92		B2		D2		F2	
13		93		B3		D3		F3	
14		94		B4		D4		F4	
15		95		B5		D5		F5	
16		96		B6		D6		F6	
17		97		B7		D7		F7	
18		98		B8		D8		F8	
19		99		B9		D9		F9	
1A		9A		BA		DA		FA	
1B		9B		BB		DB		FB	
1C		9C		BC		DC		FC	
1D		9D		BD		DD		FD	
1E		9E		BE		DE		FE	

BITS [0:4] = NEXT ADDRESS
BITS [5:7]

0 = DATA XFER
1 = COMP EN
2 = OUTPUT
3 = INVLD NRZ
4 = STACK EN
5 = WG OFF
6 = RG ON
7 = WG ON

BITS [0:3] = CNT
4 = CNT/CRC SELECT
5 = CNT/RESERVED
6 = CNT/PROCESS ECC
7 = CNT/AM

BITS [0:7] = DATA

If (RG • ECC) = 1
000 = CONTINUE, NEXT ADDRESS USED
001 = STOP ON ECC ERROR
010 = STOP ON COMPARISON NOT EQUAL
011 = STOP ON COMPARISON NOT EQUAL OR ECC ERROR
100 = BRANCH ON GOOD ECC AND COMPARISON EQUAL
101 = BRANCH ON ECC ERROR
110 = BRANCH ON COMPARISON NOT EQUAL
111 = BRANCH ON COMPARISON NOT EQUAL OR ECC ERROR

If (RG • ECC) = 0
000 = CONTINUE, NEXT ADDRESS USED
001 = STOP IF INPUT RISING (LEADING) EDGE DETECTED
010 = STOP IF INDEX OR SECTOR RISING (LEADING) EDGE DETECTED
011 = STOP ON COMPARISON NOT EQUAL
100 = BRANCH ON CARRY
101 = BRANCH ON INPUT RISING (LEADING) EDGE DETECTED
110 = BRANCH ON INDEX OR SECTOR RISING (LEADING) EDGE DETECTED
111 = BRANCH ON COMPARISON NOT EQUAL

5.3. Register Initialization

REG #	HRESET (Pin 56)	HOST RST* (Pin 36)	PROGRAM RESET	WRITE REG 59H	REG 59H Bit 0=1	REG 71 Bit 5=1	REGISTER VALUE 7	6	5	4	3	2	1	0
40/60							X	X	X	X	X	X	X	X
41/61							X	X	X	X	X	X	X	X
42/62							X	X	X	X	X	X	X	X
43/63							X	X	X	X	X	X	X	X
44/64							X	X	X	X	X	X	X	X
45/65							X	X	X	X	X	X	X	X
46/66	√	√	√				0	0	0	0	0	0	0	0
47/67							X	X	X	X	X	X	X	X
49		√				√	0	0	0	0	0	0	0	0
4A		√				‡	0	0	0	0	0	0	0	0
4B		√				‡	0	0	0	0	0	0	0	0
4C		√				‡	0	0	0	0	0	0	0	0
4D		√				‡	0	0	0	0	0	0	0	0
4E		√					0	0	0	0	0	0	0	0
50	√	√	‡				1††	X	X	0†††	0	0	0	0
51		√					X	X	X	0	0	0	0	0
52		√					0	X	X	0	0	0	0	0
53‡					‡		X	X	0	0	0	0	X	X
54							0	0	0	0	0	0	0	0
55XT mode	√	‡	‡				0	0	0	0	0	0	0	0
56XT mode							X	X	X	X	X	X	X	X
57XT mode	√		‡				X	X	X	X	X	X	0	0
55AT mode	√	‡	‡				1	0	0	0	-	-	-	0
56AT mode		‡					X	X	X	0	0	0	0	0
57AT mode		‡					X	X	X	0	0	0	0	0
58		‡					0	1	0	1	1	0	0	0
59		‡					X	X	X	X	X	X	X	1
5A		‡		‡	‡		0	0	0	0	0	0	0	0
5B		‡		‡	‡		0	0	0	0	0	0	0	0
5C‡‡		‡		‡	‡		0	0	0	0	0	0	0	0
5D‡‡		‡		‡	‡		0	0	0	0	0	0	0	0
5E‡‡		‡		‡	‡		1	1	1	1	1	1	1	1
5F‡‡		‡		‡	‡		0	0	0	0	0	0	0	1
70							X	X	X	X	X	X	X	X
71		‡				‡	0	0	1	0	0	0	0	0
72		‡				‡	0	0	0	0	0	0	0	0
73		‡				‡	1	1	1	1	1	1	1	1
74		‡				‡	1	1	1	1	1	1	1	1
75		‡				‡	1	1	1	1	1	1	1	1
76		‡				‡	1	1	1	1	1	1	1	1
77		‡					0	0	0	0	0	0	0	0
78		‡				‡	X	X	X	0	0	0	0	0
79R		‡				‡	0	0	0	1	0	0	0	0
7A		‡				‡	0	X	0	0	0	0	X	X
7B		‡					0	0	0	0	0	0	0	0
7C		‡					0	0	0	0	0	0	0	0
7D		‡				‡	X	0	0	0	0	0	X	X
7E		‡					X	0	0	0	0	0	0	0
7F		‡					0	0	0	X	X	0	0	0
80-9E							X	X	X	X	X	X	X	X
A0-BE							X	X	X	X	X	X	X	X
C0-DE							X	X	X	X	X	X	X	X
E0-FE							X	X	X	X	X	X	X	X

NOTE:

- X — means indeterminate. HOST PROGRAM RESET is when the XT Host writes to Port 1 or the AT Host sets the RESET bit (Bit 2) of the AT HOST FIXED DISK Register.
- ‡ — The DMA CONTROL Register (53H) is also reset on a Host write to the Command Register. An AUTO command resets all bits except Bit 2 which is set. This is true in PC AT mode only.
- ‡‡ — The WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH) is reset and the PC STOP POINTER (Registers 5EH and 5FH) is set to 01FFH on an AUTO command in the PC AT mode.
- † — Also AT Diagnostic command (90H).
- †† — Not affected by the HOST RESET signal (HRESET — Pin 56) or by the HOST PROGRAM RESET.
- ††† — Bit 4 = 0 when the RST* signal (Pin 36) is asserted low. Bit 4 = 1 when the HOST RESET signal (HRESET — Pin 56) is asserted or under HOST PROGRAM RESET.
- \- — Reset (0) only by the HOST RESET signal (HRESET — Pin 56) or by the RST* signal (Pin 36).

6. XT HOST–ACCESSIBLE REGISTERS

The CL–SH 260 has on-chip registers to interface between the XT Host and the disk over the IBM XT I/O channel. The XT Host transfers data to/from the disk controller through a combination of I/O ports and under DMA data transfers. These registers can be accessed by the XT Host when the XT/AT SELECT bit (Bit 7) in the PC MODE CONTROL Register (58H) is set. There are three read ports and four write ports. The ports are as follows: Read Data, Write Data, Status, Programmed Reset, Drive Type, and DMA/IRQ Enable.

DACK*	HCS0*	A1	A0	IOR* = 0	IOW* = 0
0	1	x	x	Read Data	Write Data
1	0	0	0	Read Data	Write Data
1	0	0	1	Status	Program Reset
1	0	1	0	Drive Type	Select
1	0	1	1	Reserved	DMA/IRQ Enable

NOTE: x = Don't Care

6.1. Port 0 – READ DATA (Read Only)

Data transferred from the disk controller to the XT Host comes from this register. Data is defined as sector bytes, configuration, and command completion information. This data is transferred by either Programmed I/O (PIO) or DMA. However, DMA data transfers may only occur if the disk controller is in the DATA phase. See the STATUS Register (Section 6.3).

6.2. Port 0 – WRITE DATA (Write Only)

Data transferred from the XT Host to the disk controller goes through this write-only register. Data is defined as command, sector bytes, and configuration information. This data is transferred either by Programmed I/O (PIO) or DMA. However, DMA transfers may only occur if the disk controller is in the DATA phase. See the STATUS Register (Section 6.3).

6.3. Port 1 – STATUS (Read Only)

This register contains information regarding the present state of the disk controller. This read-only register contains the following bits:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	INTRQ	DMARQ	BUSY	C/D*	I/O*	REQ

Bit 0	**REQ:** When this bit is set, it indicates that the disk controller wants to send or receive a byte. The type and direction of transfer depends on the state of the disk controller which is defined by the C/D* and I/O* status bits. This bit is set and cleared for each byte transferred between the Host and the disk controller. This bit is valid even if the data transfers are being done by DMA.
Bit 1	**I/O***: This bit determines the direction of transfer when the REQ bit (Bit 0) is set. See the following table.
Bit 2	**C/D***: This bit determines the type of information being transferred, either Command, Data, or Status. See the following table.
Bit 3	**BUSY**: This bit indicates that the disk controller is executing a command. When this bit is set, no new commands are accepted until the disk controller goes idle by resetting this bit. This bit is set during the Selection phase and reset at the end of the command.
Bit 4	**DMARQ**: This bit is set only during the data transfers between the Host and the disk controller, (i.e. C/D*=0, and REQ=1). In addition, the disk controller must be programmed to generate DMA transfers by setting the DMAEN bit (Bit 0) in the XT DMA/IRQ ENABLE Register (57H). This bit is the direct image of the DREQ line on the Host bus interface. When this bit is set, it indicates that the CL–SH260 is ready for a DMA transfer. It is set for each byte transfer and cleared by the Host bus signal DACK* (Pin 52).
Bit 5	**INTRQ**: This bit indicates that an interrupt has been issued to the Host. This bit directly reflects the Host bus signal HINT (Pin 44). This bit is set during the Command Completion phase. During this phase, the completion status byte is available to the Host. In order for this bit to be set, the Host must set the IRQEN bit (Bit 1) in the XT DMA/IRQ ENABLE Register (57H) before the Command Completion phase. It may be cleared by the XT Host resetting the IRQEN bit (Bit 1) in the XT DMA/IRQ ENABLE Register, or by the XT Host writing to Port 1 (Host Programmed Reset), or by asserting the HOST RESET signal (HRESET—Pin 56).
Bits 6-7 —	**RESERVED.** It will read 0.

BUSY	C/D*	I/O*	STATE OF DISK CONTROLLER	DIRECTION OF TRANSFER
0	x	x	IDLE	
1	0	0	DATA PHASE	PC to Disk Controller
1	0	1	DATA PHASE	Disk Controller to PC
1	1	0	COMMAND PHASE	PC to Disk Controller
1	1	1	STATUS PHASE	Disk Controller to PC

6.4. Port 1 – RESET (Write Only)

The XT Host may reset the disk controller at any time by writing to this register. This will immediately cause the disk controller to enter the idle state if the disk controller is busy. See the section on register initialization (Section 5.3).

6.5. Port 2 – DRIVE TYPE (Read Only)

This register contains information used by the XT Host to identify the drive characteristics. Bits 0-3 indicate the configuration of the disk drives connected to the disk controller. Bits 0 and 1 correspond to Disk Drive 0, and Bits 2 and 3 correspond to Disk Drive 1. The information contained in this register is written by the local microcontroller and is used by the XT Host BIOS driver program. The CL-SH260 does not interpret or use these bits in any respect.

6.6. Port 2 – CONTROLLER SELECT (Write Only)

Writing to this register starts the command process. When the disk controller is idle and the XT Host writes to this address, the BUSY bit (Port 1 - STATUS, Bit 3) is set and CL–SH260 enters the Command phase. Any data can be written to this register to cause the CL–SH260 to set the BUSY bit (Port 1 - STATUS, Bit 3). When the BUSY bit (Port 1 - STATUS, Bit 3) is set, a write to this port has no effect.

CIRRUS LOGIC

6.7. Port 3 – DMA/IRQ ENABLE (Write Only)

This register allows the XT Host to control both DMA transfers and interrupts to the XT Host. This write-only register can be loaded at any time. The DMAEN bit (Bit 0) in the XT DMA/IRQ ENABLE Register (57H) allows the CL–SH260 to drive the XT Host DREQ signal (Pin 51) during the "Data Transfer" phase. The DREQ signal (Pin 51) is set and cleared on each data transfer forming an interlocked handshake. The DMAEN bit (Register 57H, Bit 0) should be set right after the "Select" sequence and reset at the Command Completion phase. The IRQEN bit (Bit 1) in the XT DMA/IRQ ENABLE Register controls the enable for the tri-stated XT Host signal HINT (Pin 44). When the IRQEN bit (XT DMA/IRQ ENABLE Register, Bit 1) is reset, no interrupts will be issued to the XT Host. When the IRQEN bit (XT DMA/IRQ ENABLE Register, Bit 1) is set, it allows the disk controller to interrupt the XT Host at the Command Completion phase. To reset the interrupt once it is set, the XT Host must reset the IRQEN bit (Bit 1) in the XT DMA/IRQ ENABLE Register, or write to Port 1 (Host Programmed Reset), or assert the HOST RESET signal (HRESET—Pin 56). Bits 2-7 are "don't care" bits, but it is recommended that these bits be set to logical zero.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	X	INTEN	DMAEN

NOTE: X = Don't Care

7. AT HOST-ACCESSIBLE REGISTERS

The CL–SH260 has on-chip registers for an AT Host to communicate with a hard disk controller. Register access is accomplished through Programmed I/O (PIO) or DMA (Read/Write Data only). These registers can be accessed by the AT Host when the XT/AT SELECT bit (Bit 7) in the PC MODE CONTROL Register (58H) is reset. All registers are eight bits, except the read/write data, which can be 8/16 bits. The table below shows the state of various signals for accessing these registers when Pin 48 is programmed as A9 or as HCS1*.

HCS1* MODE DISABLED (Register 52H, Bit 3 is reset; Pin 48 is A9)

DREQ	BUSY	HCS0*	A9	A2	A1	A0	IOR*	IOW*
1	0	0	0	0	0	0	Read Data	Write Data
x	0	0	0	0	0	1	Error Status	Write Precomp.
x	0	0	0	0	1	0	Sector Count	Sector Count
x	0	0	0	0	1	1	Sector Number	Sector Number
x	0	0	0	1	0	0	Cylinder Low	Cylinder Low
x	0	0	0	1	0	1	Cylinder High	Cylinder High
x	0	0	0	1	1	0	Drive/Head Number	Drive/Head Number
x	0	0	0	1	1	1	Contr./Drive Status	Command
0	1	0	0	x	x	x	Contr./Drive Status	Not Allowed
x	x	0	1	1	1	0	Alt. Contr./Dr. Status	Fixed Disk
x	x	0	1	1	1	1	Digital Input	Reserved

x = Don't Care

HCS1* MODE ENABLED (Register 52H, Bit 3 is set; Pin 48 is HCS1*)

DREQ	BUSY	HCS0*	HCS1*	A2	A1	A0	IOR*	IOW*
1	0	0	1	0	0	0	Read Data	Write Data
x	0	0	1	0	0	1	Error Status	Write Precomp.
x	0	0	1	0	1	0	Sector Count	Sector Count
x	0	0	1	0	1	1	Sector Number	Sector Number
x	0	0	1	1	0	0	Cylinder Low	Cylinder Low
x	0	0	1	1	0	1	Cylinder High	Cylinder High
x	0	0	1	1	1	0	Drive/Head Number	Drive/Head Number
x	0	0	1	1	1	1	Contr./Drive Status	Command
0	1	0	1	x	x	x	Contr./Drive Status	Not Allowed
x	x	1	0	1	1	0	Alt. Contr./Dr. Status	Fixed Disk
x	x	1	0	1	1	1	Digital Input	Reserved

x = Don't Care

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7.1. AT HOST READ DATA

This register transfers sector and ECC data from the buffer memory to the AT Host. The register is 16 bits wide except when transferring Read ECC data, when it is eight bits. The AT Host may only access this register during data transfers in which the DREQ bit (Bit 3) is set in the AT HOST CONTROLLER/DRIVE STATUS Register.

7.2. AT HOST WRITE DATA

This register transfers sector and ECC data from the AT Host to the buffer memory. This register is 16 bits wide except when transferring Write ECC data, when it is eight bits. The AT Host may only access this register during data transfers in which the DREQ bit (Bit 3) is set in the AT HOST CONTROLLER/DRIVE STATUS Register.

7.3. AT HOST ERROR STATUS (Read Only)

The local microcontroller can write detailed error status of the last command failure to this register. This register can also be used to set disk controller diagnostic errors during the Diagnostic command or on power-up. When an error occurs, this register can be loaded by the microcontroller and the ERROR bit (Bit 0) is set in the AT HOST CONTROLLER/DRIVE STATUS Register. This register may only be read by the AT Host when the BUSY bit (Bit 7) in the AT HOST CONTROLLER/DRIVE STATUS Register is not set.

7.4. AT HOST WRITE PRECOMPENSATION (Write Only)

This register sets the boundary at which the disk controller will start precompensating the data written to the disk drive. The value in this register is the cylinder address divided by four. This register may only be written to by the AT Host when the BUSY bit (Bit 7) in the AT HOST CONTROLLER/DRIVE STATUS Register is not set.

7.5. AT HOST SECTOR COUNT (Read/Write)

This register specifies the number of sectors to be transferred during a Read/Write Sector command. This register is decremented as each sector is transferred. If this register is loaded with 0, then 256 sectors are transferred. This register may only be accessed when the BUSY bit (Bit 7) is not set in the AT HOST CONTROLLER/DRIVE STATUS Register.

7.6. AT HOST SECTOR NUMBER (Read/Write)

This register contains the starting sector number for the current Read/Write Sector command. This register is incremented as each sector is transferred between the AT Host and the disk controller. This register may only be accessed when the BUSY bit (Bit 7) is not set in the AT HOST CONTROLLER/DRIVE STATUS Register.

7.7. AT HOST CYLINDER LOW (Read/Write)

This register contains the lower eight bits of the disk cylinder address. This register, in conjunction with the AT HOST CYLINDER HIGH Register, constitutes a 16-bit cylinder address. This register may only be accessed when the BUSY bit (Bit 7) is not set in the AT HOST CONTROLLER/DRIVE STATUS Register.

7.8. AT HOST CYLINDER HIGH (Read/Write)

This register contains the upper eight bits of the disk cylinder address. This register, in conjunction with the AT HOST CYLINDER LOW Register, constitutes a 16-bit cylinder address. This register may only be accessed when the BUSY bit (Bit 7) is not set in the AT HOST CONTROLLER/DRIVE STATUS Register.

7.9. AT HOST DRIVE/HEAD (Read/Write)

This register contains the sector size, drive and head number. This register may only be accessed when the BUSY bit (Bit 7) is not set in the AT HOST CONTROLLER/DRIVE STATUS Register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	SECTOR SIZE		DRV #	HEAD NUMBER			

Bit 7 should be set to 1. This register is reset when the RST* signal (Pin 36) is asserted low, or the HOST RESET signal (HRESET—Pin 56) is asserted. It is also reset when the RESET bit (AT HOST FIXED DISK Register, Bit 2) is set or when a Diagnostic command (90H) is issued by the AT Host.

7.10. AT HOST CONTROLLER/DRIVE STATUS (Read Only)

This register specifies the state of the disk controller/drive. This register may be accessed by the AT Host at any time, however, when the BUSY bit (Bit 7) is set, no other bits in the register are valid. Also by reading this register, any pending interrupts to the AT Host are cleared.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BUSY	READY	FAULT	SKCOMPL	DREQ	CDATA	INDEX	ERROR

Bit 0	**ERROR**: This bit is set when an error occurred on the last command or power-up diagnostics. The error code is stored in the AT HOST ERROR STATUS Register.
Bit 1	**INDEX**: This bit reflects the status of INDEX signal (Pin 34) from the selected disk drive. This signal is asserted once per revolution of the disk. This bit will never set if the drive is not ready (i.e., if Bit 6 is reset).
Bit 2	**CDATA**: This bit is set whenever, on the previous read sector transfer, a sector read off the disk had a correctable ECC error which was corrected.
Bit 3	**DREQ**: This bit is set for data transfers to/from the sector buffer. This includes both sector and ECC data. The disk controller is considered "busy" whenever this bit or the BUSY bit (Bit 7) is set. When this bit is set, the AT Host may also read/write any of the AT-Host Registers, including the AT HOST COMMAND Register.
Bit 4	**SKCOMPL**: This bit indicates the state of the Seek Complete signal from the selected disk drive. This bit is set when the disk drive is not seeking.
Bit 5	**FAULT**: This bit reflects the state of the Write Fault signal from the selected disk drive. When this bit is set, it indicates that the disk drive is unsafe for read/write access.
Bit 6	**READY**: This bit reflects the state of the Ready signal from the selected disk drive. When this bit is set, the disk drive is present, but may not be ready for read/write transfers.
Bit 7	**BUSY**: When this bit is set, the disk controller is executing a command. Also, when this bit is set, the AT Host may not read or write any other registers except the AT HOST CONTROLLER/DRIVE STATUS Register, the AT HOST ALTERNATE CONTROLLER/DRIVE STATUS Register, the AT HOST FIXED DISK Register, and the AT HOST DIGITAL INPUT Register. This bit is set when the RST* signal (Pin 36) is asserted low, or the HOST RESET signal (HRESET—Pin 56) is asserted. It is also set when AT HOST FIXED DISK Register, Bit 2 is set or when the AT HOST COMMAND Register is loaded by the AT Host.

7.11. AT HOST COMMAND (Write Only)

The AT Host issues a new command to the disk controller through this register. The AT Host must ensure that the BUSY bit (Bit 7) in the AT HOST CONTROLLER/DRIVE STATUS Register is reset and all other registers must be set up prior to loading this register. The AT Host may abort the current data transfer and start a new command by writing to this register only when the DREQ bit (Bit 3) in the AT HOST CONTROLLER/DRIVE STATUS Register is set.

7.12. AT HOST ALTERNATE CONTROLLER/DRIVE STATUS

This register contains the same bit definition as the AT HOST CONTROLLER/DRIVE STATUS Register. This alternate register is used for systems that do not want to reset pending interrupts by reading the AT HOST CONTROLLER/DRIVE STATUS Register. This register may be read at any time.

7.13. AT HOST FIXED DISK (Write Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	HD3EN	RESET	INTEN*	DMAEN

Bit 0	**DMAEN**: This bit is an extra feature the CL–SH260 supports for the AT that is not part of the generic AT interface. This feature allows a DMA channel to be multiplexed between multiple peripherals directly by the AT Host without local microcontroller intervention. To enable this feature, first the AT HOST FIXED DISK REGISTER DMAENB bit (Register 52H, Bit 4) must be set and second the DMA mode must be selected (Register 58H, Bit 3). With these two control bits set, this bit controls the enabling of the DMA channel.
Bit 1	**INTEN***: When this bit is reset to logical 0, it enables the HINT (HOST INTERRUPT—Pin 44) output. When this bit is set to logical 1, the HINT (HOST INTERRUPT—Pin 44) output is tri-stated, regardless of the presence or absence of a pending interrupt. The internal signal and the status will still be valid even when reenabling the output.
Bit 2	**RESET**: The AT Host interface will be held in the Reset condition when this bit is set. If two disk drives are daisy chained, the AT Host interface on both disk drives will be reset. See the section on register initialization (Section 5.3).
Bit 3	**HEAD SELECT 3 ENABLE**: This bit selects whether the status of HEAD SELECT 3 (Register 46H/66H, Bit 3) or the status of RWC0 or RWC1 (depending on the drive selected) (Register 56H/57H, Bit 3) is returned as Bit 5 of the AT HOST DIGITAL INPUT Register. This bit can be overridden by Register 56H/57H, Bit 4. In that case the CL–SH260 always shows the status of HEAD SELECT 3.
Bits 4-7	Don't Care Bits, but it is recommended that the user program these bits to logical zero.

7.14. AT HOST DIGITAL INPUT (Read Only)

This register is a diagnostic loopback register that indicates the present state of Disk Drive Select 0/1, Head Select 0 - 2, Head Select 3/Reduced Write Current, and the WRITE GATE signal (Pin 38). The AT Host may read this register at any time. The bits in this register are negative true.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HiZ	WGATE*	H3*/RWC*	H2*	H1*	H0*	DS1*	DS0*

NOTE: HiZ denotes high impedance

Bits 0-1	**DS0*, DS1***: These two bits are Disk Drive Select 0/1. They will always be the complement of each other. The state of these bits is defined by the AT HOST DRIVE/HEAD Register, Bit 4. The relationship between these bits is shown in the following table:

AT HOST DRIVE/ HEAD REGISTER Bit 4	DS0*	DS1*
0	0	1
1	1	0

Bits 2-4	**H0*, H1*, H2***: These bits reflect the complement of the Head Number Bits (0-2) in the AT HOST DRIVE/HEAD Register.
Bit 5	**H3*/RWC***: This bit reflects either Head Number 3 (Bit 3 of the AT HOST DRIVE/HEAD Register) or Reduced Write Current (Bit 3 of the AT DRIVE 0/1 CONTROL/STATUS Registers (56H/57H)). If Bit 3 of the AT HOST FIXED DISK Register, or Bit 4 of the AT DRIVE 0/1 CONTROL/STATUS Registers (56H/57H) is set then this bit reflects the complement of the AT HOST DRIVE/HEAD Register, Bit 3. Otherwise, this bit reflects the complement of Bit 3 of the AT DRIVE 0/1 CONTROL/STATUS Registers.
Bit 6	**WRITE GATE***: This bit reflects the complement of the WRITE GATE signal (Pin 38).
Bit 7	**RESERVED**. Tri-state at the data pin when read.

8. BUFFER MANAGER AND PC REGISTERS

8.1. 50H – HOST INTERRUPT STATUS (Read Only)

This register is reset when the HOST RESET signal (HRESET—Pin 56) is asserted, when the RST* signal (Pin 36) is asserted low, or by a Host Programmed Reset. Bit 4 of this register is reset by the RST* signal (Pin 36) if the HOST RESET signal (HRESET—Pin 56) is not asserted and the Host Programmed Reset is not set. All bits, except Bit 7, are reset by a read of this register.

Bit 0	**HOST TRANSFER DONE**: When this bit is set, it indicates completion of a Host transfer (the PC STOP POINTER (Registers 5EH and 5FH) is equal to the appropriate Address Pointer (the READ ADDRESS POINTER (RAP — Registers 5AH and 5BH), or the WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH)). After this bit is set, the appropriate Address Pointer will read one byte more than the value of the PC STOP POINTER (Registers 5EH and 5FH). This bit is the same as Register 53H, Bit 5.
Bit 1	**PC TRANSFER OVERRUN/UNDERRUN DETECTED**: When this bit is set, it indicates that a data transfer between the Host and the buffer memory did not function properly. This bit is set when the IOCHRDY* signal (Pin 50) is asserted low and the rising (trailing) edge of the IOW* signal (Pin 55) or the IOR* signal (Pin 53) was detected.
Bit 2	**PC SELECTION PHASE DETECTED**: In the PC XT mode, this bit is set when the Host writes to Port 2. In PC AT mode, this bit is set when the Host writes to the AT COMMAND Register (47H/67H).
Bit 3	**RESERVED.**
Bit 4	**PC RESET DETECTED**: This bit is set by assertion of the HOST RESET signal (HRESET—Pin 56) or a Host Programmed Reset, i.e., when the XT Host writes to Port 1 or the AT Host sets the RESET bit (AT HOST FIXED DISK Register, Bit 2). It remains set for the duration of the Host Reset condition.
Bit 5	**RESERVED.**
Bit 6	**RESERVED.**
Bit 7	**INTERRUPT STATUS REGISTER SET**: This bit is the logical OR of Bits 0-6 in the FORMATTER INTERRUPT STATUS Register (7DH).

8.2. 51H - HOST INTERRUPT ENABLE (Read/Write)

This register is reset only when the RST* signal (Pin 36) is asserted low.

Bit 0	**HOST TRANSFER DONE ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the HOST TRANSFER DONE bit (Register 50H, Bit 0 and Register 53H, Bit 5) is set.
Bit 1	**PC TRANSFER OVERRUN ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the PC TRANSFER OVERRUN/UNDERRUN DETECTED bit (Register 50H, Bit 1) is set.
Bit 2	**PC SELECTION PHASE ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the PC SELECTION PHASE DETECTED bit (Register 50H, Bit 2) is set.
Bit 3	**RESERVED**.
Bit 4	**PC RESET ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the PC RESET DETECTED bit (Register 50H, Bit 4) is set.
Bit 5	**RESERVED**.
Bit 6	**RESERVED**.
Bit 7	**RESERVED**.

8.3. 52H – UNIQUE FEATURES CONTROL/STATUS (Read/Write)

This register is reset only when the RST* signal (Pin 36) is asserted low.

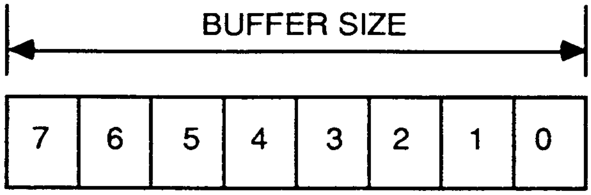
Bit 0	**MOE* DISABLE**: When this bit is set to logical 1, the MOE* signal (Pin 17) is disabled from being asserted low. This is intended to support reading switch settings (via Register 70H) on the buffer memory data bus.
Bit 1	**MASTER/SLAVE MODE ENABLE**: This bit is valid in the PC AT mode only (i.e. Register 58H, Bit 7 is reset). When this bit is set, it enables the ability to daisy chain two separate AT interface disk drives together, one configured as Master and the other as Slave. The Master responds to Disk Drive 0 Select, and the Slave responds to Disk Drive 1 Select. On a Diagnostic command both the Master and the Slave respond, but only the Master is enabled to report status to the Host.
Bit 2	**MASTER/SLAVE SELECT**: This bit is valid in the PC AT mode only (i.e. Register 58H, Bit 7 is reset) and when Bit 1 is set. When this bit is reset, the CL–SH 260 is configured as the Master. When this bit is set, the CL–SH 260 is configured as the Slave.
Bit 3	**HCS1 MODE ENABLE**: This bit is valid in the PC AT mode only (i.e., Register 58H, Bit 7 is reset). When this bit is set, Pin 48 is HCS1* input. When this bit is reset, Pin 48 is PC ADDRESS LINE 9.
Bit 4	**AT HOST FIXED DISK REGISTER DMAENB**: This bit is valid only in the PC AT mode and when the DMA mode is enabled (i.e. Register 58H, Bits 3 and 7 are reset). When this bit is set, it allows Bit 0 of the AT HOST FIXED DISK Register to control the enabling of the DMA channel. This bit should be set prior to enabling the DMA mode (Register 58H, Bit 3).
Bit 5	**AT DMAEN**: This bit reflects Bit 0 of AT HOST FIXED DISK Register. (Read Only)
Bit 6	**DISABLE STOP POINTER COMPARE**: When this bit is set, it disables the comparison of the PC STOP POINTER (Registers 5EH and 5FH) until Register 5FH is loaded.
Bit 7	**TEST MODE ENABLE**: This bit is reserved for test purposes. The user must program this bit to a logical zero.

8.4. 53H – DMA CONTROL (Read/Write)

This register is reset when the RST* signal (Pin 36) is asserted low, or when the RESET bit (Register 59H, Bit 0) is set. This register is also reset on an AT Host write to the AT HOST COMMAND Register. However, on an Auto command, all bits are reset except Bit 2, which is set.

Bit 0	**RESERVED.**
Bit 1	**RESERVED.**
Bit 2	**HOST WRITE ENABLE**: Setting this bit will start transfer from the Host to the buffer memory. In addition, the ROP/WOP* bit (Bit 4) must be reset to logical 0 when this bit is set.
Bit 3	**HOST READ ENABLE**: Setting this bit will start transfer from the buffer memory to the Host. In addition, the ROP/WOP* bit (Bit 4) must be set to logical 1 when this bit is set.
Bit 4	**ROP/WOP***: Set this bit to logical 1 for a Disk Read operation. This will cause data transfer from the disk to the buffer memory. With the HOST READ ENABLE bit (Bit 3) set, data is transferred from the buffer memory to the Host. Reset this bit to logical 0 for a Disk Write operation. This will cause data transfer from the buffer memory to the disk. With the HOST WRITE ENABLE bit (Bit 2) set, data is transferred from the Host to the buffer memory.
Bit 5	**HOST TRANSFER DONE**: When this bit is set, it indicates completion of a Host transfer (the PC STOP POINTER (Registers 5EH and 5FH) is equal to the appropriate Address Pointer (the READ ADDRESS POINTER (RAP — Registers 5AH and 5BH), or the WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH)). After this bit is set, the appropriate Address Pointer will read one byte more than the value of the PC STOP POINTER (Registers 5EH and 5FH). This bit is the same as Register 50H, Bit 0. (Read Only)
Bit 6	**RESERVED.**
Bit 7	**RESERVED.**

8.5. 54H – BUFFER SIZE (Read/Write)



00H	=	256 BYTES
01H	=	512 BYTES
03H	=	1K BYTES
07H	=	2K BYTES
0FH	=	4K BYTES
1FH	=	8K BYTES
3FH	=	16K BYTES
7FH	=	32K BYTES
FFH	=	64K BYTES

Bits 0-7	This register specifies the size of the physical buffer memory (in bytes) where the codes for a given buffer size are in the table above. The upper byte of the PC STOP POINTER (Register 5FH) is bit compared with the upper byte of the appropriate Host Address Pointer (the WRITE ADDRESS POINTER — WAP (Registers 5CH and 5DH), or the READ ADDRESS POINTER — RAP (Registers 5AH and 5BH)). The result of the bit compare is logically 'ANDed' with the contents of this register. Bit locations that are zero in this register have the bit-compare results masked. After the bit-compare masking, when the PC STOP POINTER (Registers 5EH and 5FH) equals the appropriate Host Address Pointer (the WRITE ADDRESS POINTER — WAP (Registers 5CH and 5DH), or the READ ADDRESS POINTER — RAP (Registers 5AH and 5BH)), the DMA transfer is terminated and the WAP or the RAP will be pointing to one byte higher than the PC STOP POINTER (Registers 5EH and 5FH). The HOST TRANSFER DONE bit (Register 50H, Bit 0 and Register 53H, Bit 5) will be set.

8.6. 58H – PC MODE CONTROL (Read/Write)

This register is initalized only when the RST* signal (Pin 36) is asserted low.

Bits 0-1	**PC WAIT STATE:** These bits specify the number of buffer memory cycles for which the IOCHRDY* signal (Pin 50) will be asserted low for Programmed I/O (PIO) transfers. These bits are reset when the RST* signal (Pin 36) is asserted low.
	00 = No buffer memory cycles (Disables any Wait states). 01 = 1-2 Buffer memory cycles. 10 = 2-3 Buffer memory cycles. 11 = 3-4 Buffer memory cycles.
Bit 2	**AUTO WAIT STATE GENERATION ENABLE:** When this bit is set, the IOCHRDY* signal (Pin 50) is asserted low to introduce Wait states automatically for Programmed I/O (PIO) transfers between the Host and the buffer memory when the CL-SH260 is not ready to transfer data. These Wait states are in addition to the programmed number of Wait states specified by Bits 0-1. This bit is reset when the RST* signal (Pin 36) is asserted low.
Bit 3	**PIO/DMA SELECT:** (PC AT mode only) This bit is set when the RST* signal (Pin 36) is asserted low. When this bit is set, Programmed I/O (PIO) mode is selected. When in the AT DMA mode (this bit is reset), by setting the AT HOST FIXED DISK REGISTER DMAENB bit (Register 52H, Bit 4) the PC can directly control the enabling of the DMA channel through Bit 0 of the AT HOST FIXED DISK Register (the local microcontroller can monitor this bit through the AT DMAEN bit — Bit 5 of Register 52H). Also, in the AT DMA mode (this bit is reset), the Host can respond to a DREQ (DMA REQUEST) with either DACK* (DMA ACKNOWLEDGE) or a Programmed I/O Host data access.
Bit 4	**ENABLE AUTO INTERRUPT:** (PC AT mode only) This bit is set when the RST* signal (Pin 36) is asserted low. When this bit is set, the CL–SH260 generates an interrupt to the Host when the local microcontroller initiates a Host data transfer. This is done by setting either the HOST WRITE ENABLE bit (Bit 2) or the HOST READ ENABLE bit (Bit 3) in the DMA CONTROL Register (53H), or if these bits are set, it is done by writing to Register 5FH.
Bit 5	**DISABLE AUTO COMMAND EXECUTION:** When this bit is set, it disables the automatic execution of Write, Write Long, Write Buffer, and Format commands. This bit is reset when the RST* signal (Pin 36) is asserted low.
Bit 6	**8/16 BIT DATA:** (PC AT mode only) When this bit is set, it selects 16-bit data transfer to/from the Host. This bit is set when the RST* signal (Pin 36) is asserted low.
Bit 7	**XT/AT SELECT:** This bit controls which Host interface is active, XT or AT. When this bit is set, the PC XT mode is selected. This bit is reset when the RST* signal (Pin 36) is asserted low.

8.7. 59H – BUFFER MANAGER/PC RESET CONTROL (Read/Write)

Any write to this register resets the READ ADDRESS POINTER (RAP) and the WRITE ADDRESS POINTER (WAP) Registers (5AH-5DH) and sets the PC STOP POINTER (Registers 5EH and 5FH) to a 01FFH. CAUTION: **Any write to this register also resets the PC interface operation. Bit 0 must be reset to execute PC AT Auto commands.**

Bit 0	**RESET:** When this bit is set, all registers associated with Buffer Manager and Host functions are held in the reset state until this bit is reset. This bit will also be set when the RST* signal (Pin 36) is asserted low.
Bits 1-7	**RESERVED.**

8.8. 5AH – READ ADDRESS POINTER [0:7] [RAPL] (Read/Write)

Bits 0-7	These bits are the low-order byte of the buffer memory address for read access. This register is reset when the RST* signal (Pin 36) is asserted low, when the microcontroller writes to the BUFFER MANAGER/PC RESET CONTROL Register (59H), or when the RESET bit (Register 59H, Bit 0) is set.

8.9. 5BH – READ ADDRESS POINTER [8:15] [RAPH] (Read/Write)

Bits 0-7	These bits are the high-order byte of the buffer memory address for read access. This register is reset when the RST* signal (Pin 36) is asserted low, when the microcontroller writes to the BUFFER MANAGER/PC RESET CONTROL Register (59H), or when the RESET bit (Register 59H, Bit 0) is set.

8.10. 5CH – WRITE ADDRESS POINTER [0:7] [WAPL] (Read/Write)

Bits 0-7	These bits are the low-order byte of the buffer memory address for write access. This register is reset when the RST* signal (Pin 36) is asserted low, when the microcontroller writes to the BUFFER MANAGER/PC RESET CONTROL Register (59H), or when the RESET bit (Register 59H, Bit 0) is set. This register is also reset when one of the Auto commands is issued.

8.11. 5DH – WRITE ADDRESS POINTER [8:15] [WAPH] (Read/Write)

Bits 0-7	These bits are the high-order byte of the buffer memory address for write access. This register is reset when the RST* signal (Pin 36) is asserted low, when the microcontroller writes to the BUFFER MANAGER/PC RESET CONTROL Register (59H), or when the RESET bit (Register 59H, Bit 0) is set. This register is also reset when one of the Auto commands is issued.

8.12. 5EH – PC STOP POINTER [0:7] [PC-SPL] (Read/Write)

Bits 0-7	These bits are the low-order byte of the PC Stop Pointer. It is used to detect the end of the Host data transfer. It is compared with the READ or WRITE ADDRESS POINTER (RAPL/WAPL) (Register 5AH or 5CH). This register is set when the RST* signal (Pin 36) is asserted low, when the microcontroller writes to the BUFFER MANAGER/PC RESET CONTROL Register (59H), or when the RESET bit (Register 59H, Bit 0) is set. This register is also set to FFH when one of the Auto commands is issued.

8.13. 5FH – PC STOP POINTER [8:15] [PC-SPH] (Read/Write)

Bits 0-7	These bits are the high-order byte of the PC Stop Pointer. It is used to detect the end of the Host data transfer. It is compared with the READ or WRITE ADDRESS POINTER (RAPH/WAPH) (Register 5BH or 5DH) masked by the contents of the BUFFER SIZE Register (54H). When they are equal, the HOST TRANSFER DONE bit (Register 53H, Bit 5) is set and the transfer is halted. If a new value is programmed in this register, a new transfer cycle will begin again if the appopriate HOST READ ENABLE bit (Register 53H, Bit 3) or HOST WRITE ENABLE bit (Register 53H, Bit 2) is still set. If the HOST READ ENABLE bit (Bit 3) or the HOST WRITE ENABLE bit (Bit 2) in Register 53H is set, a microcontroller write to this register restarts the PC data transfer. This register is set to 01H when the RST* signal (Pin 36) is asserted low, or when the microcontroller writes to the BUFFER MANAGER/PC RESET CONTROL Register (59H), or when the RESET bit (Register 59H, Bit 0) is set. This register is also set to 01H when one of the Auto commands is issued.

9. FORMATTER REGISTERS

9.1. 4EH – SECTOR SIZE (Read/Write)

Bits 0-7	Writing to this register sets the number of 256 byte data blocks to be transferred by the Disk Formatter, when the INHIBIT CARRY bit (Register 7AH, Bit 7) is used. The value programmed, should be one less than the number of underflows of the Current Sequencer Word [COUNT FIELD] that will be inhibited. With this register set to 00H and the INHIBIT CARRY bit (Register 7AH, Bit 7) set, only one underflow of the Current Sequencer Word will be inhibited. For a 532-byte Sector Data field, set the COUNT FIELD of the Writable Control Store (WCS) to 13H, set the SECTOR SIZE (Register 4EH) to 01H, and set the INHIBIT CARRY bit (Register 7AH, Bit 7). For a 4096-byte Sector Data field, set the COUNT FIELD of the Writable Control Store (WCS) to FFH, set the SECTOR SIZE (Register 4EH) to 0EH, and set the INHIBIT CARRY bit (Register 7AH, Bit 7). This register is reset when the RST* signal (Pin 36) is asserted low.

9.2. 71H – ECC CONTROL (Read/Write)

Bit 0	**ECC SYNDROME REVERSAL/CORRECTION CONTROL:** Setting this bit will select the correction operation. Resetting this bit will select the ECC Syndrome Reversal function. To start any of these functions the ECC SHIFT CONTROL bit (Bit 1) should be set.
Bit 1	**ECC SHIFT CONTROL:** Setting this bit starts the function selected in ECC SYNDROME REVERSAL/CORRECTION CONTROL (Bit 0).
	If the ECC SYNDROME REVERSAL/CORRECTION CONTROL bit (Bit 0) is reset, setting this bit will start shifting data from the ECC CORRECTION SHIFT-REGISTER/COUNTER (Register 72H) into the ECC circuit. This bit is cleared automatically after the shift is completed. If the ECC SYNDROME REVERSAL/CORRECTION CONTROL bit (Bit 0) is set, the correction function is selected and setting this bit will start the correction process. In this case, this bit is cleared if a correctable error is found, or the ECC circuit is shifted 256 bytes. ECC CORRECTION SHIFT REGISTER/COUNTER (Register 72H) is a byte counter and, in case of a correctable error, will provide the error offset. Note that all shifts are performed on byte boundaries. During normal Read/Write operations, this bit should be set to zero.
Bit 2	**DISABLE ECC FEEDBACK:** When this bit is set, the ECC circuit functions as a 56/32-bit shift register.
Bit 3	**CLEAR ECC:** ECC syndrome will be cleared when this bit is set and no Read or Write operation is in progress. If this bit is set during a Read or Write operation, the ECC syndrome will be cleared at the end of that operation.
Bit 4	**ENABLE SECTOR BRANCH:** When this bit is set, it enables the SECTOR signal (Pin 35) input as a condition for Sequencer branching, along with the INDEX signal (Pin 34) input so that Sequencer branches may begin at INDEX or SECTOR.
Bit 5	**FORMATTER RESET:** When the RST* signal (Pin 36) is asserted low, it sets this bit and generates a hardware Reset condition. When set by the microcontroller, a software Reset condition is generated. Either reset stops all operations in the Disk Formatter. The software Reset condition resets Registers 49H-4DH, 71H-76H, 78H-7AH, 7DH-7EH, deasserts the READ GATE signal (37), the WRITE GATE signal (Pin 38) and switches the NRZ signal (Pin 40), the WAM*/AMD*/SECTOR signal (Pin 35), and AD0-AD7 lines (Pins 24-31) to a high-impedance state. The Disk Formatter will remain in the Reset condition as long as this bit is set. The Reset condition can be removed by resetting this bit. Refer to the section on register initialization (Section 5.3). **Note:** This bit should be reset immediately after power-up because most register bit values and CL-SH260 functions are inhibited when this bit is set.
Bit 6	**32/56 BIT ECC SELECT:** When this bit is set, the 56-bit ECC polynomial is selected. When this bit is reset, the 32-bit ECC polynomial is selected.
Bit 7	**ECC POLYNOMIAL DIRECTION:** When this bit is reset, it selects the forward polynomial. When this bit is set, it selects the reverse polynomial for the correction process.

9.3. 72H – ECC CORRECTION SHIFT-REGISTER/COUNTER (Read/Write)

Bits 0-7	When the ECC SYNDROME REVERSAL/CORRECTION CONTROL bit (Register 71H, Bit 0) is set, this is an eight-bit counter. When the ECC SYNDROME REVERSAL/-CORRECTION CONTROL bit (Register 71H, Bit 0) is reset, this is a shift register.

9.4. 73H – ECC STATUS [31:24]/[7:0] (Read Only)

Bits 0-7	**ECC STATUS BITS [31:24]/[7:0]**: When 56-bit ECC is selected, these are ECC Bits 31:24 (Bit 0 = ECC Bit 31). When 32-bit ECC is selected, these are ECC Bits 7:0 (Bit 0 = ECC Bit 7). The status of the bits in this register will only be valid when ECC is not cycling. This register is set when the RST* signal (Pin 36) is asserted low or when the FORMATTER RESET bit (Register 71H Bit 5) is set.

9.5. 74H – ECC STATUS [39:32]/[15:8] (Read Only)

Bits 0-7	**ECC STATUS BITS [39:32]/[15:8]**: When 56-bit ECC is selected, these are ECC Bits 39:32 (Bit 0 = ECC Bit 39). When 32-bit ECC is selected, these are ECC Bits 15:8 (Bit 0 = ECC Bit 15). The status of the bits in this register will only be valid when ECC is not cycling. This register is set when the RST* signal (Pin 36) is asserted low or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.

9.6. 75H – ECC STATUS [47:40]/[23:16] (Read Only)

Bits 0-7	**ECC STATUS BITS [47:40]/[23:16]**: When 56-bit ECC is selected, these are ECC Bits 47:40 (Bit 0 = ECC Bit 47). When 32-bit ECC is selected, these are ECC Bits 23:16 (Bit 0 = ECC Bit 23). The status of the bits in this register will only be valid when ECC is not cycling. This register is set when the RST* signal (Pin 36) is asserted low or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.

9.7. 76H – ECC STATUS [55:48]/[31:24] (Read Only)

Bits 0-7	**ECC STATUS BITS [55:48]/[31:24]**: When 56-bit ECC is selected, these are ECC Bits 55:48 (Bit 0 = ECC Bit 55). When 32-bit ECC is selected, these are ECC Bits 31:24 (Bit 0 = ECC Bit 31). The status of the bits in this register will only be valid when ECC is not cycling. This register is set when the RST* signal (Pin 36) is asserted low or when the FORMATTER RESET bit (Register 71H Bit 5) is set.

9.8. 77H – FORMATTER MODE SELECTION (Read/Write)

This register is reset when the RST* signal (Pin 36) is asserted low.

Bit 0 — **HOST STATUS READ DETECTED**: When this bit is set, it indicates that the CL-SH260 has detected a read of the AT HOST CONTROLLER/DRIVE STATUS Register by the host since the last time this bit was polled. This bit is cleared by a read from the local microcontroller. This bit is reset only by a power-on Reset condition on the RST* signal (Pin 36).

Bit 1 — **HOST REGISTER FILE ACCESS ENABLE**: When this bit is set, it allows the Host Interface Registers to be accessed by the local microcontroller. The address space is specified by bit 2. When this bit is reset, addresses 40H - 47H and 60H - 67H are available for external system use.

Bit 2 — **HOST REGISTER FILE DECODE SELECT**: When this bit is set (and Bit 1 is set), the address space for the Host register file is 40H-47H (Addresses 60H - 67H are available for external system use). When this bit is reset (and Bit 1 is set), the address space for the Host register file is 60H-67H (Addresses 40H - 47H are available for external system use).

Microcontroller-Host Register File Decode Table

Reg. 77H Bit 1	Bit 2	CL–SH260 Decodes:	Available to MPU:
0	x	Neither	40H–47H and 60H–67H
1	1	Decodes 40H-47H	60H-67H
1	0	Decodes 60H–67H	40H-47H

Bit 3 — **LOCAL INT* ENABLE**: When this bit is set to logical 1, it enables local interrupt capability. The individual sources of interrupt can still be disabled by the Interrupt Enable Registers (Registers 51H and 7EH).

Bit 4 — **LOCAL INT* PIN PULLUP DISABLE**: When this bit is set to logical 1, it disables the pull-up on the INT* signal (Pin 19), leaving an open drain output. This is intended to support multiple interrupt sources.

Bit 5 — **PROGRAMMED CONTROL INDEX**: When this bit is set, it simulates an active index condition. This bit can be used in place of the INDEX signal (Pin 34).

Bit 6 — **SEQUENCER OUTPUT ENABLE**: When this bit is set, the INPUT/OUTPUT signal (Pin 33) is configured as an output. The value actually driven on the pin will be specified by the Current Sequencer Word CONTROL FIELD, Bit 2.

Bit 7 — **HARD/SOFT* SECTOR MODE CONTROL**: When this bit is set to logical 1, it selects the Hard Sector mode. In this mode, the WAM*/AMD*/SECTOR signal (Pin 35) functions as a SECTOR input signal. The SECTOR PAST bit (Register 7AH, Bit 1) and Branch on Sector circuit will be triggered by the rising (leading) edge of the SECTOR signal. When this bit is reset to logical 0, it selects the Soft Sector mode. In this mode, the WAM*/AMD*/SECTOR signal (Pin 35) functions as the WAM*/AMD* signal.

9.9. 78H – NEXT SEQUENCER ADDRESS (Read Only)

Bits 0-4	**NEXT ACTIVE SEQUENCER ADDRESS**: Bits 0-4 provide the next Writable Control Store (WCS) address to be executed by the Sequencer. This address could be the contents of the SEQUENCER START ADDRESS Register (79H), or the BRANCH ADDRESS Register (78H), or the CURRENT SEQUENCER WORD — NEXT ADDRESS Register (49H).
Bits 5-7	**RESERVED**.

9.10. 78H – BRANCH ADDRESS (Write Only)

Bits 0-4	The Sequencer will jump to the address specified in Bits 0-4 when a branch condition is programmed and met. This register is reset when the RST* signal (Pin 36) is asserted low, or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.
Bits 5-7	**RESERVED**.

9.11. 79H – SEQUENCER STATUS (Read Only)

Bit 0	**COMPARE EQUAL**: This bit is set when the result of the compare operation is equal. The comparison is done between the Read Data and either the Buffer Memory Data or the Writable Control Store (WCS) DATA FIELD (determined by the SEARCH OPERATION bit – Register 7AH, Bit 4), on all bytes where comparison was enabled in the COMPARE ENABLE bit (Bit 1) of the Writable Control Store (WCS) CONTROL FIELD. COMPARE EQUAL is not valid until the Sequencer is in the ECC FIELD.
Bit 1	**COMPARE LOW**: This bit is the same as Bit 0 above; however, this bit is set when the Read Data is lower.
Bit 2	**ECC ERROR**: This bit will be set after the last ECC data bit is read if there is a non-zero ECC syndrome indicating a data error.
Bit 3	**CORRECTABLE ERROR FOUND**: When this bit is set, it indicates that the interactive ECC correction circuit has found a correctable error and has shifted the error burst to a byte boundary. This bit is valid after the ECC SHIFT CONTROL bit (Register 71H, Bit 1) has gone from set to reset.
Bit 4	**SEQUENCER STOPPED**: When this bit is set, it indicates the Sequencer is stopped. The ECC contents have not been reset. The READ GATE signal (Pin 37) and the WRITE GATE signal (Pin 38) are reset.
Bit 5	**BRANCH ACTIVE**: This bit is set when a branch condition is met. Reading this register will reset this bit.
Bit 6	**DATA TRANSFER STATUS**: This bit indicates the status of the DATA TRANSFER bit (Writable Control Store (WCS) CONTROL FIELD, Bit 0). It is set during data transfer between the buffer memory and the disk.
Bit 7	**AM ACTIVE**: This bit is set when the DATA TRANSFER bit (Writable Control Store (WCS) CONTROL FIELD, Bit 0) is reset and the COUNT/AM bit (Writable Control Store (WCS) COUNT FIELD, Bit 7) is set. It is reset after reading or writing the ECC bytes. It is also reset when the Sequencer stops.

9.12. 79H – SEQUENCER START ADDRESS (Write Only)

The Sequencer can be stopped by writing 1FH to this register.

Bits 0-4	**START ADDRESS**: A write to this register will start the Sequencer at the latched address. This register is reset when the RST* signal (Pin 36) is asserted low, or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.
Bits 5-7	**RESERVED.**

9.13. 7AH – OPERATION/CONTROL STATUS (Read/Write)

Bit 0	**INDEX PAST**: This bit is set by the rising (leading) edge of the INDEX pulse from the disk drive. Reading this register will reset this bit. (Read only)
Bit 1	**SECTOR PAST**: This bit is valid in Hard Sector mode only. It is set by the rising (leading) edge of the pulse on the WAM*/AMD*/SECTOR signal (Pin 35). Reading this register will reset this bit. (Read only)
Bit 2	**NRZ DATA IN**: This bit is set when a rising (leading) edge is detected at the NRZ signal (Pin 40). Reading the register will reset this bit, but due to the asynchronous relationship between the NRZ signal and the microcontroller, race conditions may interfere with the reset. It is suggested that this bit be read until it reports as reset. (Read only)
Bit 3	**SYNC DETECT**: This bit is set during a Disk Read operation when the internal serializer/deserializer has been synchronized with the incoming NRZ data and matches the preprogrammed sync character in Register 7CH. This bit is cleared on the falling (trailing) edge of the READ GATE signal (Pin 37). (Read only)
Bit 4	**SEARCH OPERATION**: Setting this bit selects the source of the data for the compare operation. When this bit is set, Read Data is compared to Buffer Memory Data. When this bit is reset, Read Data is compared to the Writable Control Store (WCS) DATA FIELD.
Bit 5	**SUPPRESS TRANSFER**: When this bit is set, serialized or de-serialized data will not be read or written to the buffer memory (disabling the buffer memory access mechanism). During a Write operation, the NRZ data will be written with the contents of the Writable Control Store (WCS) DATA FIELD. During a Read operation, the incoming data will have the ECC verified but no data will be transferred to the buffer memory.
Bit 6	**RESERVED.**
Bit 7	**INHIBIT CARRY**: When this bit is set, the carry/load of the Writable Control Store (WCS) COUNT FIELD for the data transfer will be inhibited. This bit will be automatically reset whenever the Sector Size Counter is zero and there is an underflow from the current COUNT FIELD.

9.14. 7BH – WAM CONTROL (Read/Write)

Bits 0-7	**WRITE ADDRESS MARK CONTROL**: In Soft Sector mode, the WAM*/AMD*/SECTOR signal (Pin 35) will be asserted low for each bit cell time corresponding to the bits set in this register during a Write Address Mark operation. Output at the WAM*/AMD*/SECTOR signal (Pin 35) is shifted 3 bits toward the LSB at the output. In Hard Sector mode, the signal will not be asserted. This register is reset when the RST* signal (Pin 36) is asserted low.

9.15. 7CH – SYNC PATTERN (Read/Write)

Bits 0-7	**SYNC PATTERN**: This register is to be compared with NRZ read data when the READ GATE signal (Pin 37) and, if in Soft Sector mode, the WAM*/AMD*/SECTOR signal (Pin 35) are asserted. A match between this register and the serial NRZ read data input will set the SYNC DETECT bit (Register 7AH, Bit 3), and will cause NRZ read data to be gated into the ECC. Only those bits in this Register which are enabled by the CLOCK/SYNC CONTROL Register (7FH) will be used for comparison. In Soft Sector mode, the WAM*/AMD*/SECTOR signal (Pin 35) must also be asserted (for the SYNC DETECT bit (Register 7AH, Bit 3) to be set). This register is reset when the RST* signal (Pin 36) is asserted low.

9.16. 7DH – FORMATTER INTERRUPT STATUS (Read Only)

A microcontroller read of this register will reset any bits that were set except Bit 7. Bits 0-6 are also reset when the RST* signal (Pin 36) is asserted low, or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.

Bit 0	**INDEX PAST**: This bit is set by the rising (leading) edge of the INDEX pulse from the disk drive. Reading this register will reset this bit. This bit is the same as Register 7AH, Bit 0.
Bit 1	**SECTOR PAST**: This bit is valid in Hard Sector mode only. It is set by the rising (leading) edge of the pulse on the WAM*/AMD*/SECTOR signal (Pin 35). Reading this register will reset this bit. This bit is the same as Register 7AH, Bit 1.
Bit 2	**INPUT DETECTED**: This bit will be set by the rising (leading) edge of the INPUT signal (Pin 33). This bit will be cleared by a microcontroller read of this register.
Bit 3	**SEQUENCER STOPPED**: When this bit is set, it indicates that the Sequencer is stopped. The ECC contents have not been reset. The READ GATE signal (Pin 37) and the WRITE GATE signal (Pin 38) are deasserted. This bit is the same as Register 79H, Bit 4.
Bit 4	**ECC ERROR**: This bit is set after the last ECC data bit is read if there is a non-zero ECC syndrome indicating a data error. This bit is the same as Register 79H, Bit 2.
Bit 5	**DATA TRANSFER STATUS**: This bit will be set by the rising (leading) edge of the DATA TRANSFER STATUS bit (Register 79H, Bit 6). This bit will be cleared by a microcontroller read of this register.
Bit 6	**SEQUENCER OUTPUT DETECTED**: This bit will be set by the rising (leading) edge of the OUTPUT signal (Pin 33). This bit will be cleared by a microcontroller read of this register.
Bit 7	**HOST INTERRUPT ACTIVITY**: This bit is the logical-OR of Bits 0-2,4 of the HOST INTERRUPT STATUS Register (50H).

9.17. 7EH FORMATTER INTERRUPT ENABLE (Read/Write)

This register is reset when the RST* signal (Pin 36) is asserted low.

Bit 0	**INDEX ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the INDEX PAST bit (Register 7DH, Bit 0) is set.
Bit 1	**SECTOR ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the SECTOR PAST bit (Register 7DH, Bit 1) is set.
Bit 2	**INPUT DETECTED ENABLE**: When set this bit will cause the INT* signal (Pin 19) to be asserted low when the INPUT DETECTED bit (Register 7DH, Bit 2) is set.
Bit 3	**SEQUENCER STOPPED ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the SEQUENCER STOPPED bit (Register 7DH, Bit 3) is set.
Bit 4	**ECC ERROR ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the ECC ERROR bit (Register 7DH, Bit 4) is set.
Bit 5	**DATA TRANSFER DETECTED ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the DATA TRANSFER STATUS bit (Register 7DH, Bit 5) is set.
Bit 6	**SEQUENCER OUTPUT DETECTED ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the SEQUENCER OUTPUT DETECTED bit (Register 7DH, Bit 6) is set.
Bit 7	**RESERVED.**

9.18. 7FH – FORMATTER STACK READ (Read Only)

Bits 0-7	A read of this register reads the last byte that was enabled (by the STACK ENABLE bit (Bit 4 of the Writable Control Store (WCS) CONTROL FIELD)) on to the stack. The Address Pointer, in ring fashion, moves around the 8-byte circular stack. As the byte is read, the Address Pointer moves to the previous location. The data during a read is never 'popped' from the stack, it is not lost or removed, a continuous read of eight locations would bring one back around to the original location reading the same data. If 10 bytes in a field were enabled to the stack, the last eight bytes would be captured as the first two bytes would be overwritten. The first byte read would be the tenth byte enabled on to the stack. In reverse order all of the last eight bytes could then be read continuously in a circular manner.

9.19. 7FH – CLOCK/SYNC CONTROL (Write Only)

This register is reset when the RST* signal (Pin 36) is asserted low.

Bits 0-2	**SYNC COMPARE CONTROL:** These bits specify the number of bits to be used in the compare for the sync byte programmed in the SYNC PATTERN Register (7CH).

Bit 2	Bit 1	Bit 0	
0	0	0	= Only Bit 7 is compared.
0	0	1	= Only Bits 7:6 are compared.
0	1	0	= Only Bits 7:5 are compared.
0	1	1	= Only Bits 7:4 are compared.
1	0	0	= Only Bits 7:3 are compared
1	0	1	= Only Bits 7:2 are compared.
1	1	0	= Only Bits 7:1 are compared.
1	1	1	= All bits are compared.

Bit 3	**RESERVED.**
Bit 4	**RESERVED.**
Bit 5	**BCLK DISABLE**: The user **must** program this bit to be reset. When this bit is set, the internal clock will be disabled. It is used for testability purposes.
Bits 6-7	

Bit 7	Bit 6	
0	0	= Allows one buffer memory access cycle per four BCLK cycles.
0	1	= Allows one buffer memory access cycle per two BCLK cycles.
1	0	= Allows one buffer memory access cycle per BCLK cycle.
1	1	= Reserved.

10. EXTERNAL ACCESS REGISTERS

10.1. 4DH – SHADOW LATCH (Read Only)

Bits 0-7	**DATA:** When the microcontroller reads Register 70H, the content of the buffer memory data bus will be captured in this register. This register is reset when the RST* signal (Pin 36) is asserted low, or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.

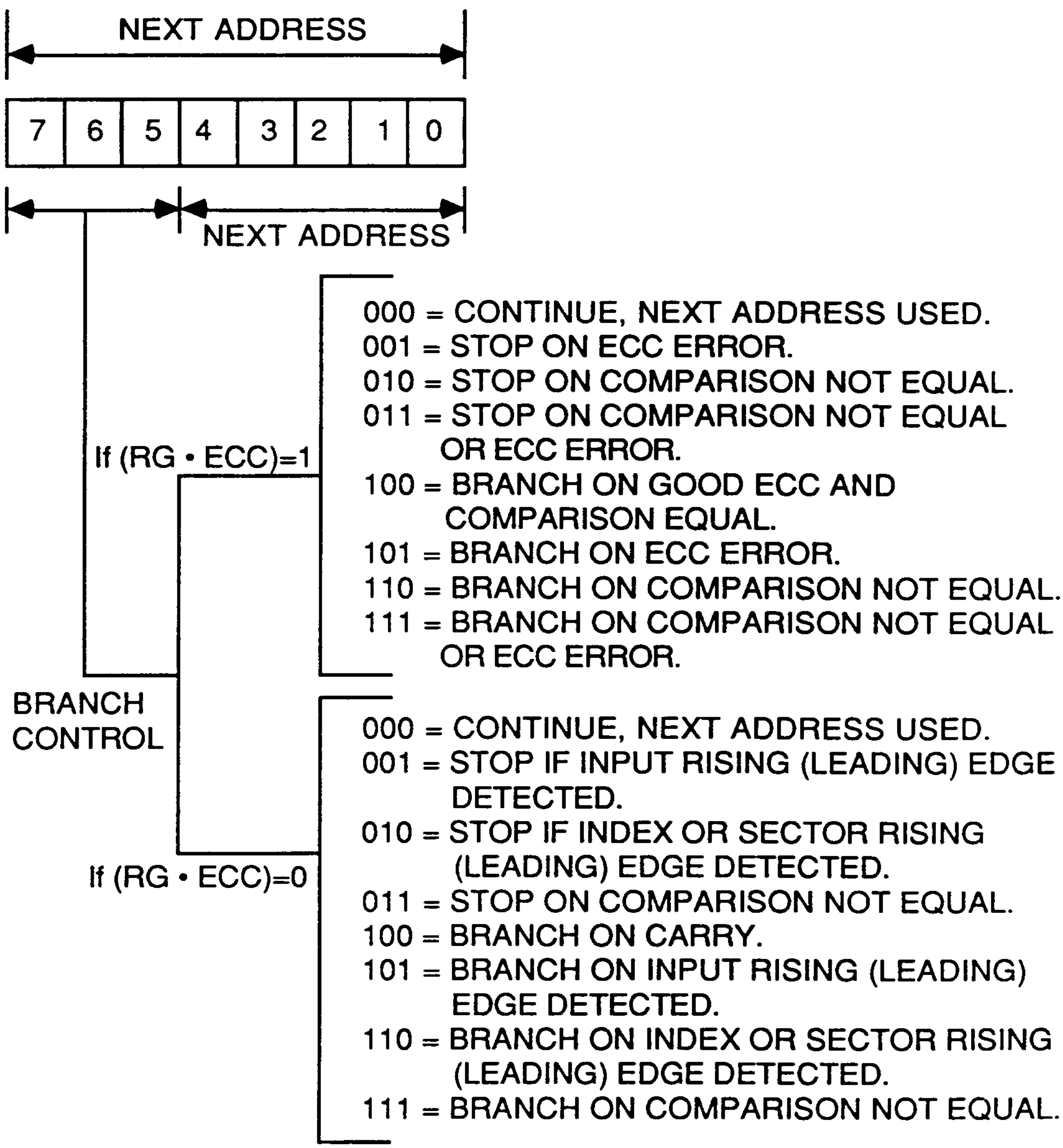
10.2. 70H – BUFFER MEMORY ACCESS (Read/Write)

Bits 0-7	**BUFFER MEMORY ACCESS:** Register 70H decode internally bridges the buffer memory data bus and the microcontroller bus (allowing the microcontroller to access the buffer memory) and causes the CL–SH260 to assert buffer memory address lines, the MOE* signal (Pin 17), and the WE* signal (Pin 18). Read data from the buffer memory will also be latched into the SHADOW LATCH Register (4DH). If the MOE* DISABLE bit (Register 52H, Bit 0) is set to logical 1, the MOE* signal (Pin 17) is not asserted so that the microcontroller can read external switch settings on the buffer memory data bus.

11. WRITABLE CONTROL STORE (WCS) FIELDS

The Writable Control Store (WCS) (addresses 80H-9EH, A0H-BEH, C0H-DEH, and E0H-FEH) may only be written to by the support microcontroller when there is no risk of the contents being accessed by the Sequencer. This is normally true only during long data transfers or when the Sequencer is stopped.

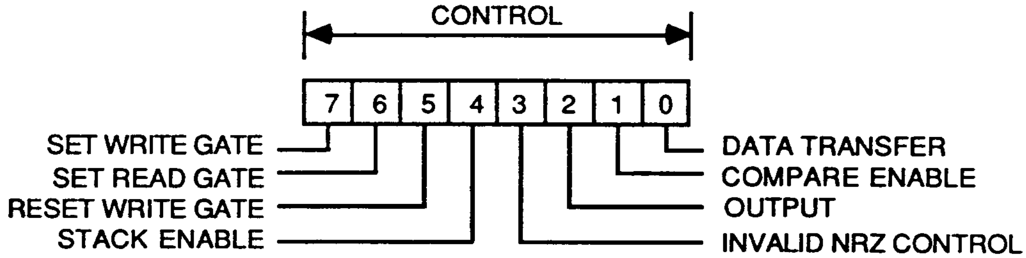
11.1. 80H-9EH – NEXT ADDRESS FIELD (Read/Write)



11.1. 80H-9EH – NEXT ADDRESS FIELD (Read/Write) *(cont.)*

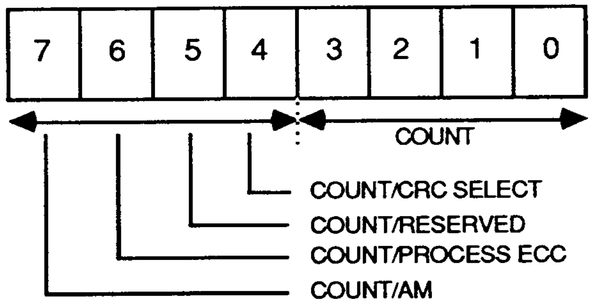
Bits 0-4	**NEXT ADDRESS**: This is the address the Sequencer will go to after the down counter has reached zero and a branch has not been taken. There are 31 possible next-address locations (00H-1EH). Address 1FH establishes the stopped condition.
Bits 5-7	**BRANCH CONDITION**: All branch conditions are evaluated during the last byte of execution of the Current Sequencer Word. Branch conditions when both the READ GATE signal (Pin 37) is asserted and the PROCESS ECC bit (Bit 6) of the Current Sequencer Word COUNT FIELD is set: 000 = Continue, next address used. 001 = Stop on ECC error. 010 = Stop on comparison not equal. 011 = Stop on comparison not equal or ECC error. 100 = Branch on good ECC and comparison equal. 101 = Branch on ECC error. 110 = Branch on comparison not equal. 111 = Branch on comparison not equal or ECC error. Branch conditions at all other times: 000 = Continue, next address used. 001 = Stop if INPUT rising (leading) edge detected. 010 = Stop if INDEX or SECTOR rising (leading) edge detected. 011 = Stop on comparison not equal. 100 = Branch on carry. 101 = Branch on INPUT rising (leading) edge detected. 110 = Branch on INDEX or SECTOR rising (leading) edge detected. 111 = Branch on comparison not equal.

11.2. A0H-BEH – CONTROL FIELD (Read/Write)



Bit 0	**DATA TRANSFER**: When this bit is set, the COUNT FIELD is used as an eight-bit counter. Each byte time that this bit is set, a byte of data will be accessed from buffer memory if the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is reset. If the WRITE GATE signal (Pin 38) is asserted, then a byte of data is read from the buffer memory (if the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is reset) or from the Writable Control Store (WCS) DATA FIELD (if the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is set), and is serialized and sent to the NRZ signal (Pin 40). If the READ GATE signal (Pin 37) is asserted, then a byte of data is de-serialized from the NRZ signal and is then written to the buffer memory if the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is reset. If the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is set, then no data is written to the buffer memory.
Bit 1	**COMPARE ENABLE**: When this bit is set and the READ GATE signal (Pin 37) is asserted, it will allow a comparison between Read Data and the Writable Control Store (WCS) DATA FIELD, or the buffer memory data (if the SEARCH OPERATION bit (Register 7AH, Bit 4) is set).
Bit 2	**OUTPUT**: This bit drives the OUTPUT signal (Pin 33) and is used to synchronize external logic functions to the state of the Writable Control Store (WCS).
Bit 3	**INVALID NRZ CONTROL**: When this bit is set with the READ GATE signal (Pin 37) asserted, it will block the NRZ data input from being processed.
Bit 4	**STACK ENABLE**: When this bit is set, Read Data is pushed on the eight-byte circular stack.
Bit 5	**RESET WRITE GATE**: This bit is used to deassert the WRITE GATE signal (Pin 38). The WRITE GATE signal (Pin 38) will be deasserted on the last count of the Sequencer word with this bit set. The WRITE GATE signal (Pin 38) is also deasserted when the Sequencer comes to the stopped state.
Bit 6	**SET READ GATE**: The READ GATE signal (Pin 37) will be asserted when the Sequencer word with this bit set is executed. The READ GATE signal (Pin 37) will be deasserted at the end of ECC or when the Sequencer goes to the stopped state. The READ GATE signal (Pin 37) will not be asserted if the WRITE GATE signal (Pin 38) is already asserted.
Bit 7	**SET WRITE GATE**: The WRITE GATE signal (Pin 38) will be asserted when the Sequencer word with this bit set is executed. After this bit is set, WRITE GATE control will be reset by executing a Sequencer word with the RESET WRITE GATE bit (Bit 5) set or when the Sequencer goes to the stopped state. The WRITE GATE signal (Pin 38) will not be asserted if the READ GATE signal (Pin 37) is already asserted.

11.3. C0H-DEH – COUNT FIELD (Read/Write)



COUNT FIELD FUNCTIONALITY

WG On	RG On	Data Transfer	Bit 7	Bit 6	Bit 5	Bit 4	Bits 3-0	Max Count
0	0	0	AM	PROCESS ECC	RESERVED	COUNT	COUNT	32
0	0	1	COUNT	COUNT	COUNT	COUNT	COUNT	256
0	1	0	AM	PROCESS ECC	RESERVED	CRC SEL	COUNT	16
0	1	1	ILLEGAL					
1	0	0	AM	PROCESS ECC	RESERVED	CRC SEL	COUNT	16
1	0	1	ILLEGAL					
1	1	0	ILLEGAL					
1	1	1	ILLEGAL					

11.3. C0H-DEH – COUNT FIELD (Read/Write) *(cont.)*

This sets the initial value of the Sequencer counter when a new state is entered.

Bits 0-3	**COUNT**: These bits are always used for the initial value of the Sequencer byte counter when a new state is entered. When it reaches zero, a new instruction word will be accessed from the Disk Formatter Writable Control Store (WCS).
Bit 4	**COUNT/CRC SELECT**: In the Current Sequencer Word, when the SET WRITE GATE and the SET READ GATE bits (CONTROL FIELD, Bits 7 and 6 respectively) are reset, or if the DATA TRANSFER bit (CONTROL FIELD, Bit 0) is set, this is a count bit (for a 5-bit, or an 8-bit count field). (Note that the DATA TRANSFER bit (CONTROL FIELD, Bit 0) set and the SET WRITE GATE or the SET READ GATE bit (CONTROL FIELD, Bits 7 and 6 respectively) set is an illegal selection.) If in the Current Sequencer Word, either the SET WRITE GATE or SET READ GATE bit (CONTROL FIELD, Bits 7 and 6 respectively) is set, and the DATA TRANSFER bit (CONTROL FIELD, Bit 0) is reset, then the CRC SELECT function is active. With this function active, this bit set initializes the ECC function to the CRC polynomial and when this bit is cleared, the ECC function is initialized to the 32/56-bit computer generated polynomial.
Bit 5	**COUNT/RESERVED**: When the DATA TRANSFER bit of the Current Sequencer Word (CONTROL FIELD, Bit 0) is set, this is a count bit (for an eight-bit count field). When the DATA TRANSFER bit (CONTROL FIELD, Bit 0) is reset, this bit is reserved.
Bit 6	**COUNT/PROCESS ECC**: When the DATA TRANSFER bit of the Current Sequencer Word (CONTROL FIELD, Bit 0) is set, this is a count bit (for an eight-bit count field). When the DATA TRANSFER bit (CONTROL FIELD, Bit 0) is reset, this bit treats the incoming NRZ data (if the READ GATE signal (Pin 37) is asserted), or the outgoing NRZ data (if the WRITE GATE signal (Pin 38) is asserted) as an ECC or CRC field.
Bit 7	**COUNT/AM**: When the DATA TRANSFER bit of the Current Sequencer Word (CONTROL FIELD, Bit 0) is set, this is a count bit (for an eight-bit count field). When the DATA TRANSFER bit (CONTROL FIELD, Bit 0) is reset, and the READ GATE signal (Pin 37) is asserted, this bit will set the AM ACTIVE bit (Register 79H, Bit 7). When the DATA TRANSFER bit (CONTROL FIELD, Bit 0) is reset, and the WRITE GATE signal (Pin 38) is asserted, this bit will set the AM ACTIVE bit (Register 79H, Bit 7), and will be used to initialize the CRC/ECC Registers. If in the Soft Sector mode (Register 77H, Bit 7 is reset), the WAM* output will be asserted low as programmed in the WAM CONTROL Register (7BH).

11.4. E0H-FEH – DATA FIELD (Read/Write)

DATA							
7	6	5	4	3	2	1	0

Bits 0-7	This register is the source for all overhead bytes of data used by the device during Write operations. During Read operations, it is one of the operands to the comparison logic. When the DATA TRANSFER bit in Current Sequencer Word (CONTROL FIELD, Bit 0) is set with the WRITE GATE signal (Pin 38) asserted, the source for write data will be the external buffer memory. When the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is set with the WRITE GATE signal (Pin 38) asserted, the source for write data will be the content of this register.

12. SEQUENCER REGISTERS

The Writable Control Store (WCS) word being executed is stored in these registers. These registers should only be written to by the microcontroller when the Sequencer is stopped. These registers can be read any time.

12.1. 49H – CURRENT SEQUENCER WORD - NEXT ADDRESS FIELD (Read/Write)

This register allows the microcontroller to access the NEXT ADDRESS FIELD of the Current Sequencer Word.

12.2. 4AH – CURRENT SEQUENCER WORD - COUNT FIELD (Read/Write)

This register allows the microcontroller to access the COUNT FIELD of the Current Sequencer Word.

12.3. 4BH – CURRENT SEQUENCER WORD - CONTROL FIELD (Read/Write)

This register allows the microcontroller to access the CONTROL FIELD of the Current Sequencer Word.

12.4. 4CH – CURRENT SEQUENCER WORD - DATA FIELD (Read/Write)

This register allows the microcontroller to access the DATA FIELD of the Current Sequencer Word.

13. MICROCONTROLLER-HOST INTERFACE

The local microcontroller interface to the Host is programmed through a set of command, status, and control registers. Many of these registers are shared for XT and AT applications. The registers are configured to operate in PC XT or PC AT mode by programming the XT/AT SELECT bit (Register 58H, Bit 7). This configuration has to be done on power-up or after any assertion low of the RST* signal (Pin 36). Host resets will not change this configuration. Eight of these registers can be mapped to locations 40H-47H or 60H-67H by programming the HOST REGISTER FILE DECODE SELECT bit (Register 77H, Bit 2). In general, these registers may be accessed at any time, except when noted.

13.1 XT MODE REGISTERS

These registers are configured for the XT Command Blocks, Status and Configuration information transfer when the XT/AT SELECT bit (Register 58H, Bit 7) is set. In this mode, the register file has eight Command/General Purpose Registers and three Control/Status Registers. The registers are as follows:

ADDRESS	READ	WRITE
40H or 60H	Command/General Byte 0	Command/General Byte 0
41H or 61H	Command/General Byte 1	Command/General Byte 1
42H or 62H	Command/General Byte 2	Command/General Byte 2
43H or 63H	Command/General Byte 3	Command/General Byte 3
44H or 64H	Command/General Byte 4	Command/General Byte 4
45H or 65H	Command/General Byte 5	Command/General Byte 5
46H or 66H	General Byte 6	General Byte 6
47H or 67H	General Byte 7	General Byte 7
55H	Mode/Status	Mode/Status
56H	Drive Type	Drive Type
57H	DMA/IRQ ENABLE Status	Reserved

13.1.1 40H-47H (60H-67H) – XT Command/General Purpose Registers (Read/Write)

Bits 0-7	The Command/General Purpose Registers allow the local microcontroller to transfer bytes between the Host and the disk controller without going through the buffer memory. These registers are used to receive the six command or configuration bytes and to send sense status or command completion status. The local microcontroller is locked out of these registers during transfers with the Host involving these registers. Host access to these registers are controlled by the local microcontroller through XT MODE/STATUS Register (55H). The microcontroller has read/write access to all the Command/General Purpose Registers. However, for the Host access, the read/write direction is controlled by the I/O* bit (Bit 5) in the XT MODE/STATUS Register (55H). These registers are not affected by any Reset condition.

13.1.2 55H – XT MODE/STATUS

This register contains control and status information for the XT interface. All transfers between the Host and the local register file are controlled by this register. This register is reset when the HOST RESET signal (HRESET—Pin 56) is asserted, or when the RST* signal (Pin 36) is asserted low, or by a Host Programmed Reset.

Bits 0-2	R/W **LRTC0:2**: These bits represent the number of bytes to be transferred between the Host and the Command/General Purpose Registers (40H-47H/60H-67H). Up to 8 bytes may be transferred each time. These bits contain the transfer length minus one (i.e., LRTC0:2=0 for a transfer of 1). The Transfer Address Pointer for the Command/General Purpose Registers always start with register 0 and is incremented on each byte transfer. A read of these bits represents the number of bytes minus one that is left to be transferred.
Bit 3	R/W **LRTNS**: When this bit is set, it initiates a transfer between the Host and the Command/General Purpose Registers (40H-47H/60H-67H). This bit will be reset when the Host transfer is completed. The local microcontroller should not access the Command/General Purpose Registers when this bit is set. This bit may be set by the local microcontroller only when there are no active transfers between the Host and buffer memory (i.e., when the BTRNS bit [Bit 4] is reset).
Bit 4	R BTRNS: This bit represents the state of Host-buffer memory access. When this bit is set, it indicates that transfers are active between the Host and the buffer memory. When this bit is set, the local microcontroller may not initiate a transfer between the Command/General Purpose Registers (40H-47H/60H-67H) and the Host.
Bit 5	R/W **I/O***: This bit determines the direction of Host data transfer when the BTRNS bit or the LRTNS bit (Bit 3 or 4 respectively) is asserted. See the following PC/XT I/O Bus Phase table.
Bit 6	R/W **C/D***: This bit determines the type of information being requested, Command, Status, or Data. See the following PC/XT I/O Bus Phase table.
Bit 7	R/W **BUSY**: This bit indicates that the disk controller is busy executing a command. This bit is set during the Selection phase by the Host by writing to the SELECT PORT (Port 2). The local microcontroller resets this bit at the end of the command.

BUSY	C/D*	I/O*	STATE OF CONTROLLER	DIRECTION OF TRANSFER
0	x	x	IDLE	
1	0	0	DATA PHASE	PC to Disk Controller
1	0	1	DATA PHASE	Disk Controller to PC
1	1	0	COMMAND PHASE	PC to Disk Controller
1	1	1	STATUS PHASE	Disk Controller to PC

PC/XT I/O Bus Phase Table

13.1.3 56H – XT DRIVE TYPE (Read/Write)

	This register may be accessed by the local microcontroller at any time. Generally, this register contains information required by the XT BIOS driver to configure the physical attributes of the drive (i.e., cylinders, heads, sectors/track). From the Host, this register appears as a read-only register which can be accessed by a Port 2 read. This register is not affected by any Reset condition.

13.1.4 57H – XT DMA/IRQ ENABLE (Read Only)

This register reflects the contents of the DMA/IRQ ENABLE Register (Port 3) which is written to by the Host. This register can be accessed at any time. This register is reset when the HOST RESET signal (HRESET—Pin 56) is asserted or under a Host Program Reset.

Bit 0	R	**DMAEN**: This bit is the same as Port 3, Bit 0. It allows driving the Host DREQ signal (Pin 51) during DATA phase transfers.
Bit 1	R	**IRQEN**: This bit controls the enable for the tri-stated Host Bus HINT signal (Pin 44). When this bit is reset, no interrupts will be issued to the Host microcontroller. When this bit is set, it allows the disk controller to interrupt the Host at the Command Completion phase.
Bits 2-7	-	**RESERVED.**

13.2 AT Mode Registers

These registers are configured for the PC AT Task File when the XT/AT SELECT bit (Register 58H, Bit 7) is reset. In this mode, the register file has eight Command/Parameter Registers and three Control/Status Registers. These registers are as follows:

ADDRESS	READ	WRITE
40H or 60H	Error Status	Error Status
41H or 61H	Write Precompensation	Write Precompensation
42H or 62H	Sector Count	Sector Count
43H or 63H	Sector Number	Sector Number
44H or 64H	Cylinder Low	Cylinder Low
45H or 65H	Cylinder High	Cylinder High
46H or 66H	Drive/Head Number	Drive/Head Number
47H or 67H	Command	Command
55H	Control/Status	Control/Status
56H	Drive 0 Status	Drive 0 Status
57H	Drive 1 Status	Drive 1 Status
73H	ECC Status [31:24]/[7:0]	Autocommand "LOCK" Release

These registers may be accessed by the local microcontroller after setting the XT/AT SELECT bit (Register 58H, Bit 7) to 0. (See the PC MODE CONTROL Register (58H), Section 8.6). The local microcontroller has write access to Registers 40H/60H - 47H/67H only when the BUSY bit (Register 55H, Bit 7) is set and the BTRANS bit (Register 55H, Bit 4) is reset. The registers, except the AT DRIVE/HEAD NUMBER Register (46H/66H), are not affected by any Reset condition.

NOTE: The local microcontroller always has read access.

13.2.1 40H (60H) – AT ERROR STATUS (Read/Write)

The local microcontroller can write detailed error status of the last command failure to this register. This register can also be used to set disk controller diagnostic errors during the Diagnostic command or on power-up. When an error occurs, this register can be loaded and the ERROR bit (Bit 0) set in the the AT CONTROL/STATUS Register (55H).

13.2.2 41H (61H) – AT WRITE PRECOMPENSATION (Read/Write)

This register sets the boundary at which the disk controller will start precompensating the data written to the disk drive. The value in this register is the cylinder address divided by four. This register may only be read by the Host when the BUSY bit (Bit 7) in the AT HOST CONTROLLER/DRIVE STATUS Register is not set.

13.2.3 42H (62H) – AT SECTOR COUNT (Read/Write)

This register is used to specify the number of sectors to be transferred during a Read/Write Sector command. This register is decremented by the local microcontroller as each sector is transferred. If this register is loaded with 0 then 256 sectors are transferred.

13.2.4 43H (63H) – AT SECTOR NUMBER (Read/Write)

This register is used to specify the starting sector number for the current Read/Write Sector command. This register is incremented by the local microcontroller as each sector is transferred between the Host and the disk controller.

13.2.5 44H (64H) – AT CYLINDER LOW (Read/Write)

This register is used to specify the lower eight bits of the disk cylinder address. This register, in conjunction with the AT CYLINDER HIGH Register (45H/65H), constitutes a 16-bit cylinder address. This register is incremented by the local microcontroller as each cylinder boundary is crossed.

13.2.6 45H (65H) – AT CYLINDER HIGH (Read/Write)

This register is used to specify the upper eight bits of the disk cylinder address. This register, in conjunction with the AT CYLINDER LOW Register (44H/64H), constitutes a 16-bit cylinder address. This register is incremented by the local microcontroller as each cylinder boundary is crossed if the lower cylinder value overflows.

13.2.7 46H (66H) – AT DRIVE / HEAD NUMBER (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXT	Sector Size		Drv #	Head Number			

This register is used to specify the sector size, drive and head number. The local microcontroller changes the head address as each track or cylinder boundary is crossed. This register is reset by assertion of the HOST RESET signal (HRESET—Pin 56), by assertion low of the RST* signal (Pin 36), by a Host Programmed Reset, or by a Diagnostic command (90H). The format of the register is shown above.

13.2.8 47H (67H) – AT COMMAND (Read/Write)

A new command issued by the Host to the disk controller is loaded in to this register.

13.2.9 55H – AT CONTROL / STATUS

This register is reset when the RST* signal (Pin 36) is asserted low, or when the HOST RESET signal (HRESET—Pin 56) is asserted, or under Host program reset. Bits 1,2, and 3 of this register, however, are only reset by the HOST RESET signal (HRESET—Pin 56).

Bit 0	R/W **ERROR**: This bit is set when an error occurred on the last command or power-up diagnostics. This bit is reflected in the ERROR bit (Bit 0) of the AT HOST CONTROLLER/DRIVE STATUS Register. This bit is automatically reset by any Host write to the command port 1F7H.
Bit 1	R **INTEN***: This bit reflects the status of the INTEN* bit (Bit 1) of the AT HOST FIXED DISK Register. The local microcontroller can only monitor this bit. When this bit is reset to logical 0, the tri-state interrupt line to the Host bus is enabled.
Bit 2	R **RESET**: This bit reflects the status of the RESET bit (Bit 2) of the AT HOST FIXED DISK Register. The local microcontroller can only monitor this bit. When this bit is set, the Host is issuing a programmed reset to the disk controller. This condition can be sensed by the local microcontroller through the PC RESET DETECTED bit (Bit 4) of the HOST INTERRUPT STATUS Register (50H).
Bit 3	R **HD3EN**: This bit reflects the HEAD SELECT 3 ENABLE bit (Bit 3) of the AT HOST FIXED DISK Register. The local microcontroller can only monitor this bit.
Bit 4	R/W **INT**: This bit allows the local microcontroller to set an interrupt to the Host by setting this bit. The read of this bit returns the status of the HINT signal (Pin 58).
Bit 5	R/W **CDATA**: This bit is set by the local microcontroller whenever, on the previous read sector transfer, a data error had been corrected. This bit is reflected in AT HOST CONTROLLER/DRIVE STATUS Register, Bit 2.
Bit 6	R **BTRNS**: This bit indicates the state of Host buffer memory access. When this bit is set, it indicates that transfers are active between the Host and the buffer memory. In a disk read, this bit is reset when the last data is transferred to the Host. In a disk write, this bit is reset when the last data is transferred to the buffer memory.
Bit 7	R/W **BUSY**: When this bit is set, it indicates that the disk controller is executing a command. This bit is set when the RST* signal (Pin 36) is asserted low, or when the HOST RESET signal (HRESET—Pin 56) is asserted, or when the RESET bit (Bit 2) of the AT HOST FIXED DISK Register is set. If the MASTER/SLAVE MODE ENABLE bit (Register 52H, Bit 1) is reset, this bit is also set when the Host writes to the AT HOST COMMAND Register. If the MASTER/SLAVE MODE ENABLE bit (Register 52H, Bit 1) is set, this bit is set when the Host writes to the AT HOST COMMAND Register only when the respective drive is selected. However, when the Host writes a Diagnostic command (90H) to the AT HOST COMMAND Register this bit will always be set. This bit is reset at the end of command execution by the local microcontroller.

13.2.10 56H – AT DRIVE 0 CONTROL / STATUS (Read/Write)

This register contains drive-related status information that is part of the AT HOST CONTROL/STATUS Register when Disk Drive 0 is selected in the DRIVE NUMBER field (Bit 4) of the AT HOST DRIVE/HEAD Register. This register may be accessed by the local microcontroller at any time. The XT/AT SELECT bit (Register 58H, Bit 7) must be reset for AT operation. This register is reset when the RST* signal (Pin 36) is asserted low.

Bit 0	**SKCMP0**: This bit reflects the state of the Seek Complete signal from Disk Drive 0. When the disk drive is not seeking, this bit is set.
Bit 1	**FAULT0**: This bit reflects the state of the Write Fault signal from Disk Drive 0. When this bit is set, it indicates that the disk drive is unsafe for access.
Bit 2	**READY0**: This bit reflects the state of the Ready signal from Disk Drive 0. When this bit is set, the disk drive is present but may not be ready for read/write transfers.
Bit 3	**RWC0**: This bit reflects the state of the Reduced Write Current signal from Disk Drive 0. When this bit is set, the current to the disk drive write heads has been reduced.
Bit 4	**OVERRIDE HD3EN0**: When this bit is set, the HD3EN Bit (Bit 3) of the AT HOST FIXED DISK Register for Disk Drive 0 is forced to logical 1.
Bits 5-7	**RESERVED.**

13.2.11 57H – AT DRIVE1 CONTROL / STATUS (Read/Write)

This register contains drive-related status information that is part of the AT HOST CONTROL/STATUS Register when Disk Drive 1 is selected in the DRIVE NUMBER field (Bit 4) of the AT HOST DRIVE/HEAD Register. This register may be accessed by the local microcontroller at any time. The XT/AT SELECT bit (Register 58H, Bit 7) must be reset for AT operation. This register is reset when the RST* signal (Pin 36) is asserted low.

Bit 0	**SKCMP1**: This bit reflects the state of the Seek Complete signal from Disk Drive 1. When the disk drive is not seeking, this bit is set.
Bit 1	**FAULT1**: This bit reflects the state of the Write Fault signal from Disk Drive 1. When this bit is set, it indicates that the disk drive is unsafe for access.
Bit 2	**READY1**: This bit reflects the state of the Ready signal from Disk Drive 1. When this bit is set, the disk drive is present but may not be ready for read/write transfers.
Bit 3	**RWC1**: This bit reflects the state of the Reduced Write Current signal from Disk Drive 1. When this bit is set, the current to the disk drive write heads has been reduced.
Bit 4	**OVERRIDE HD3EN1**: When this bit is set the HD3EN bit (Bit 3) of the AT HOST FIXED DISK Register for Disk Drive 1 is forced to logical 1.
Bits 5-7	**RESERVED.**

13.2.12 73H – AUTOCOMMAND "LOCK" RELEASE (Write Only)

A write to this register is the Autocommand LOCK Release mechanism. Releasing the Autocommand LOCK permits the local microcontroller write access to Registers 53H, 5CH, 5DH, and read/write access to Register 70H.

14. ELECTRICAL SPECIFICATIONS

14.1 Absolute Maximum Ratings

Ambient Temperature Under Bias .... 0° C to 70° C
Storage Temperature .... -65° C to 150° C
Voltage On Any Pin With Respect To Ground .... GND -0.5 to V_{CC} +0.5 Volts
Power Supply Voltage .... 7 Volts
Injection Current (Latch-up) at Room Temperature....... 50 mA

NOTE: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

14.2 DC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{CC}	Power Supply Voltage	4.75	5.25	Vdc	Operating
V_{IL}	Input Low Voltage	-0.5	0.8	Vdc	
V_{IH}	Input High Voltage	2.0	VCC+0.5	Vdc	
$V_{OL(1)}$†	Output Low Voltage		0.4	Vdc	I_{OL} = 2 mA
$V_{OL(2)}$	Output Low Voltage		0.5	Vdc	I_{OL} = 24 mA
V_{OH}	Output High Voltage		2.4	Vdc	I_{OH} = –400 µA
I_{CC}	Supply Current		50	mA	
$I_{OZ(1)}$	Tri-state Leakage	-10	10	µA	$0<V_{IN}<V_{CC}$
$I_{OZ(2)}$	Tri-state Leakage	-50	50	µA	$0<V_{IN}<V_{CC}$
I_L	Input Leakage Current	-10	10	µA	$0<V_{IN}<V_{CC}$
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	

NOTE: (1) All output pins except for the PC interface signals.
(2) PC interface outputs except HINT 10 mA.
(3) † I_{OL} = 4mA for RG and WG
(4) Unused inputs must be tied to their inactive state to V_{CC} or GND respectively.

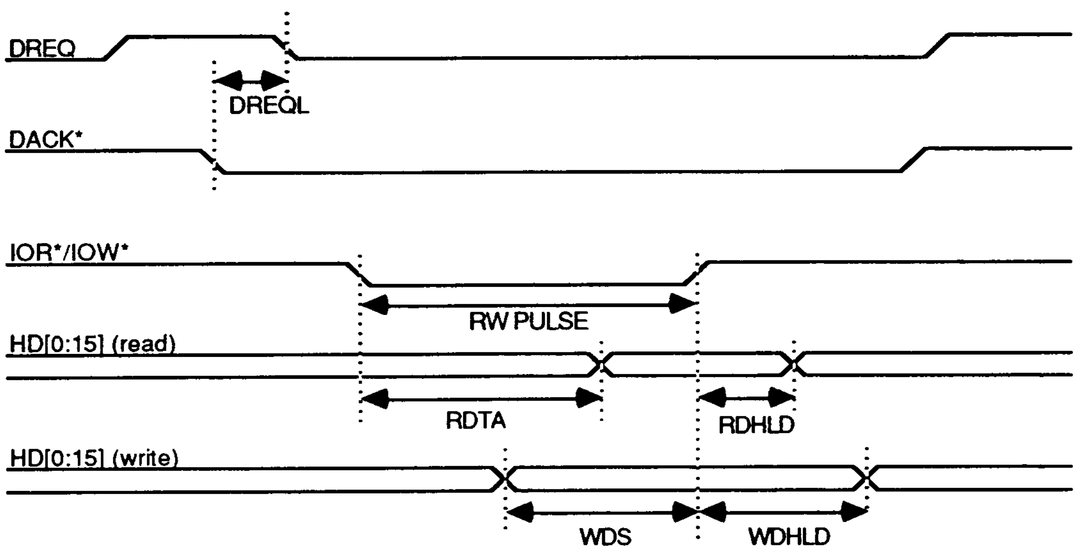
14.3 AC Characteristics

The following timings assume that all non-Host bus output pins will drive one Schottky TTL load in parallel with 50 pF, all Host bus output pins will drive a 300 pF load, and all inputs are at TTL levels. The MIN and MAX timings conform to the operating ranges of a power supply voltage of 5V ±5% and an ambient temperature of 0°C to 70°C.

Host DMA 8/16-Bit Interface Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
DREQL	DREQ low from DACK* low		80	ns
RDTA	IOR* low to HD[0:15] valid		50	ns
RDHLD	IOR* high to HD[0:15] tri-state	0	20	ns
WDS	HD[0:15] setup to IOW* high	40		ns
WDHLD	HD[0:15] hold from IOW* high	10		ns
RWPULSE	IOR*/IOW* pulse width	80		ns

Host DMA 8/16-Bit Interface Timing

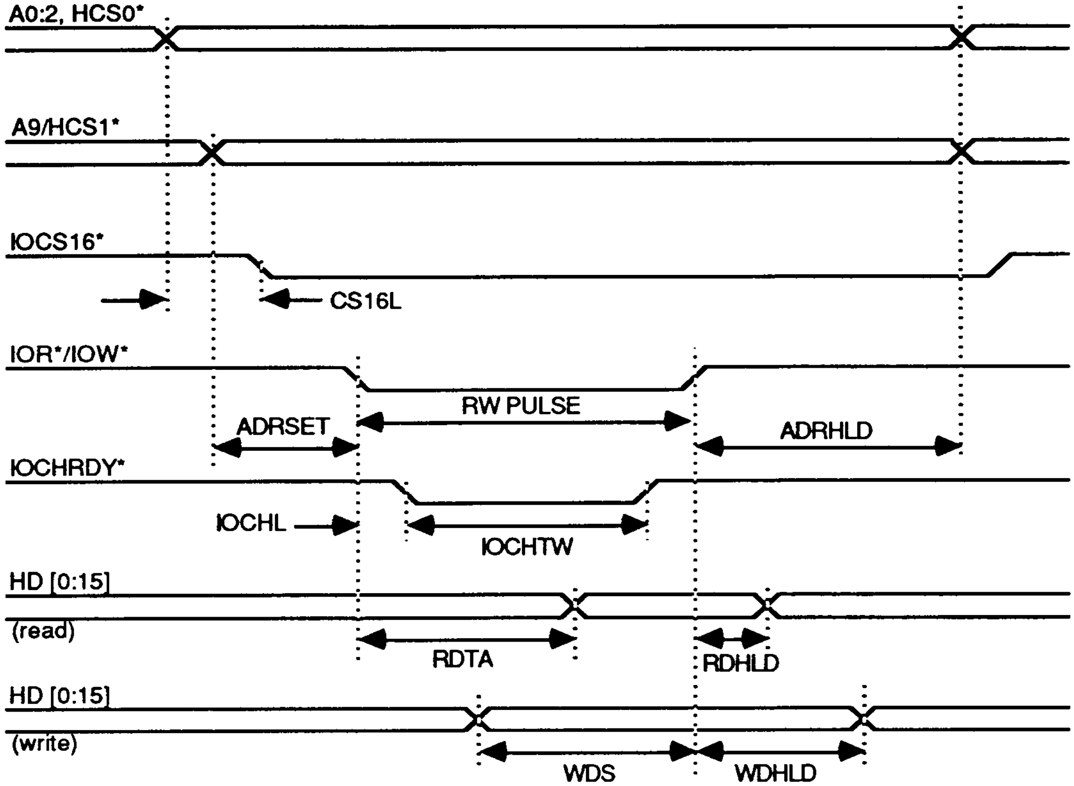


Host Programmed I/O 8/16-Bit Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
CS16L	HCS0* low, A0:2 low to IOCS16* low	0	20	ns
IOCHL	IOR*/IOW* low to IOCHRDY* low		25	ns
IOCHTW†	IOCHRDY* pulse width	0	5 x BUFCLK	ns
RDTA	IOR* low to HD[0:15] valid		60	ns
RDHLD	IOR* high to HD[0:15] tri-state	0	20	ns
WDS	HD[0:15] setup to IOW* high	40		ns
WDHLD	HD[0:15] hold from IOW* high	10		ns
RWPULSE	IOR*/IOW* pulse width	80		ns
ADRSET	HCS0*, A0:2, A9/HCS1*, setup to IOR*/IOW* low	25		ns
ADRHLD	HCS0*, A0:2, A9/HCS1* hold, from IOR*/IOW* high	10		ns

† Maximum specification applies when the Auto Wait State Generation is disabled (Register 58H, Bit 2 is reset).

Host Programmed I/O 8/16-Bit Timing



CIRRUS LOGIC

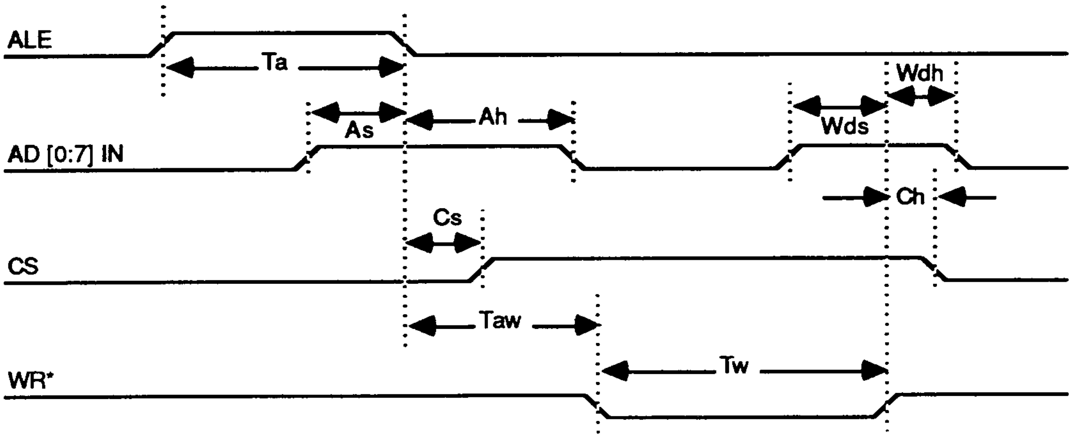
Microcontroller Interface Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
Ta	ALE Width	45		ns
Taw	ALE↓ to WRITE*↓	25		ns
Tar	ALE↓ to READ*↓	25		ns
Tw	WR* Width	140		ns
Tr	RD* Width	140		ns
As	Address AD [0:7] valid to ALE↓	5		ns
Ah	ALE↓ to Address AD [0:7] invalid	20		ns
Cs	ALE↓ to CS valid		5	ns
Ch	RD*↑ or WR*↑ to CS↓	0		ns
Wds	Write Data AD [0:7] valid to WR*↑	55		ns
Wdh	WR*+ to Write Data AD [0:7] invalid	10		ns
Tda	RD*↓ to Read Data AD [0:7] valid		100	ns
Tdh	RD*↑ to Read Data AD [0:7] float (undriven)		50	ns

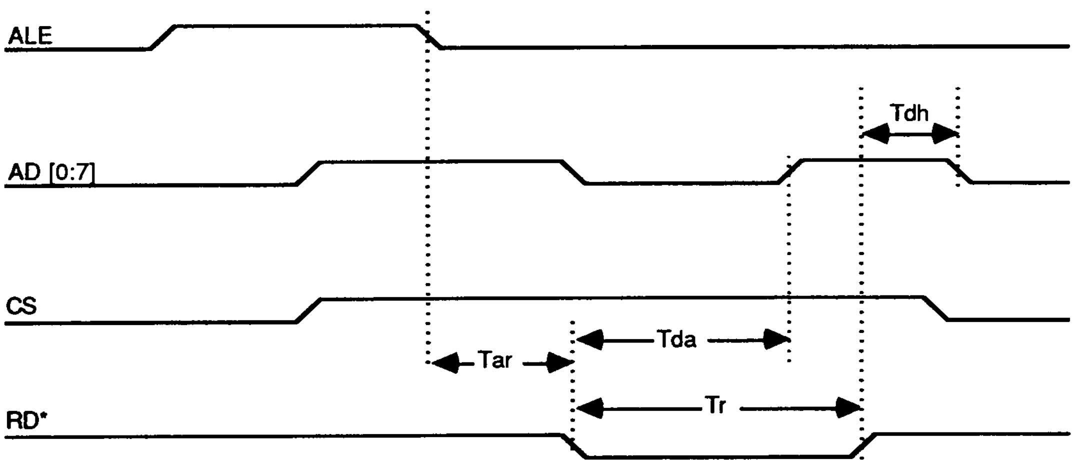
NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

Microcontroller Interface Timing

Register Write Timing



Register Read Timing



CIRRUS LOGIC

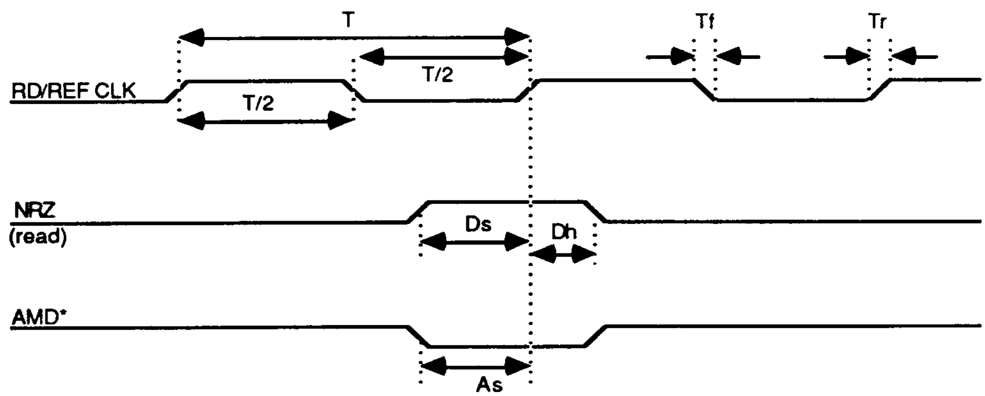
Disk Read/Write Timing Parameters

SYMBOL	PARAMETER	15 MHz MIN	15 MHz MAX	20 MHz MIN	20 MHz MAX	UNITS
T	RD/REF CLK Period	62.5		50		ns
T/2	RD/REF CLK High/Low Time	23		19		ns
Tr=Tf	RD/REF CLK Rise and Fall Time		5		5	ns
Ds	NRZ valid to RD/REF CLK↑	15		15		ns
Dh	RD/REF CLK↑ to NRZ invalid	7		7		ns
As †	AMD* valid to RD/REF CLK ↑	10		10		ns
Dv	RD/REF CLK↑ to NRZ valid	10	25	10	25	ns
WAv †	RD/REF CLK↑ to WAM* valid	10	25	10	25	ns

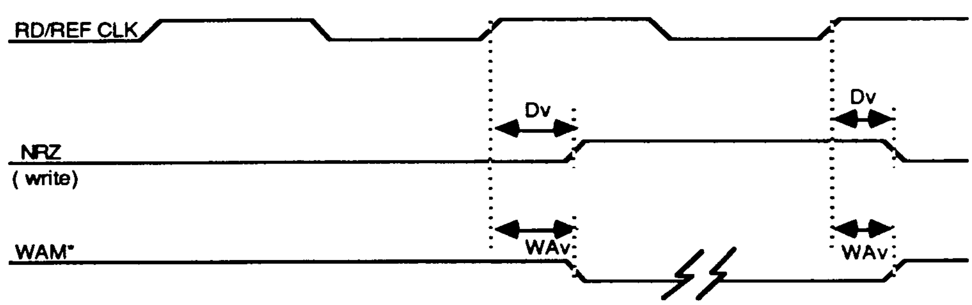
NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

† These specifications are only applicable in the Soft Sector mode.

Disk Read Timing



Disk Write Timing



NOTE: NRZ DATA changes after the rising (leading) edge of the RD/REF CLK (Pin 39).

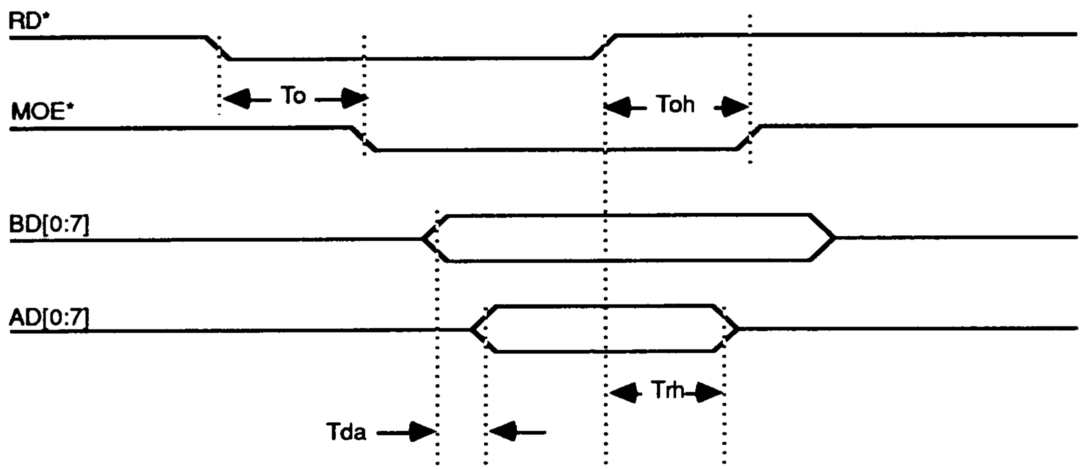
Register 70H Access Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
T_o	RD*↓ to MOE*↓		40	ns
Tda	BD[0:7] valid to AD[0:7] valid		55	ns
Trh	RD*↑ to AD[0:7] invalid		50	ns
Toh	RD*↑ or WR*↑ to MOE*↑		40	ns
Taw	AD [0:7] valid to WE*↓		55	ns
Tao	AD [0:7] valid to MOE*↓		55	ns
Tad	AD[0:7] valid to BD[0:7] valid		55	ns
Twwh	WR*↑ to WE*↑		40	ns
Twdh	WR*↑ to BD[0:7] invalid	50		ns

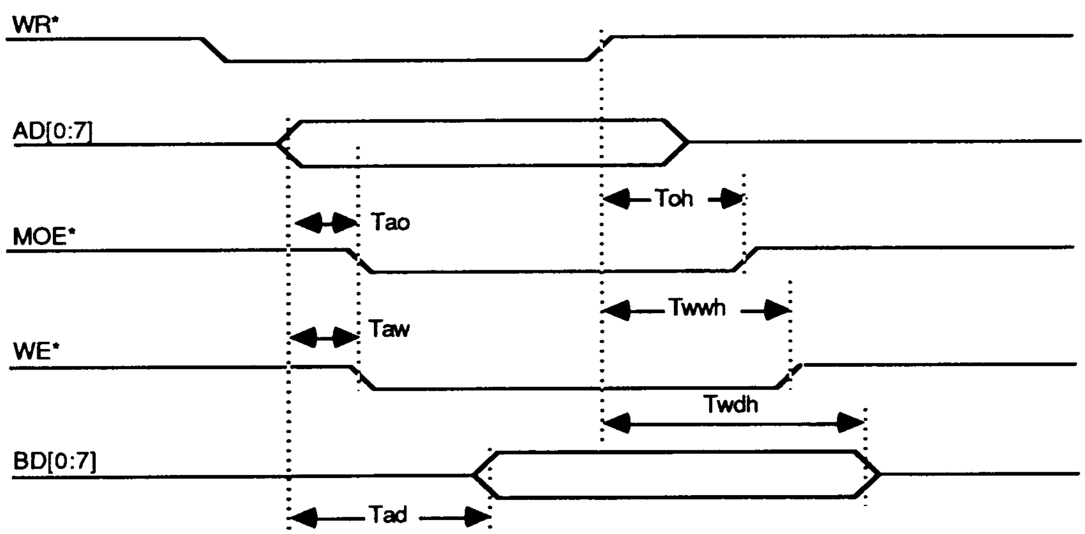
NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

BA [0:15] is valid from the previous cycles.

Register 70H Read Timing



Register 70H Write Timing



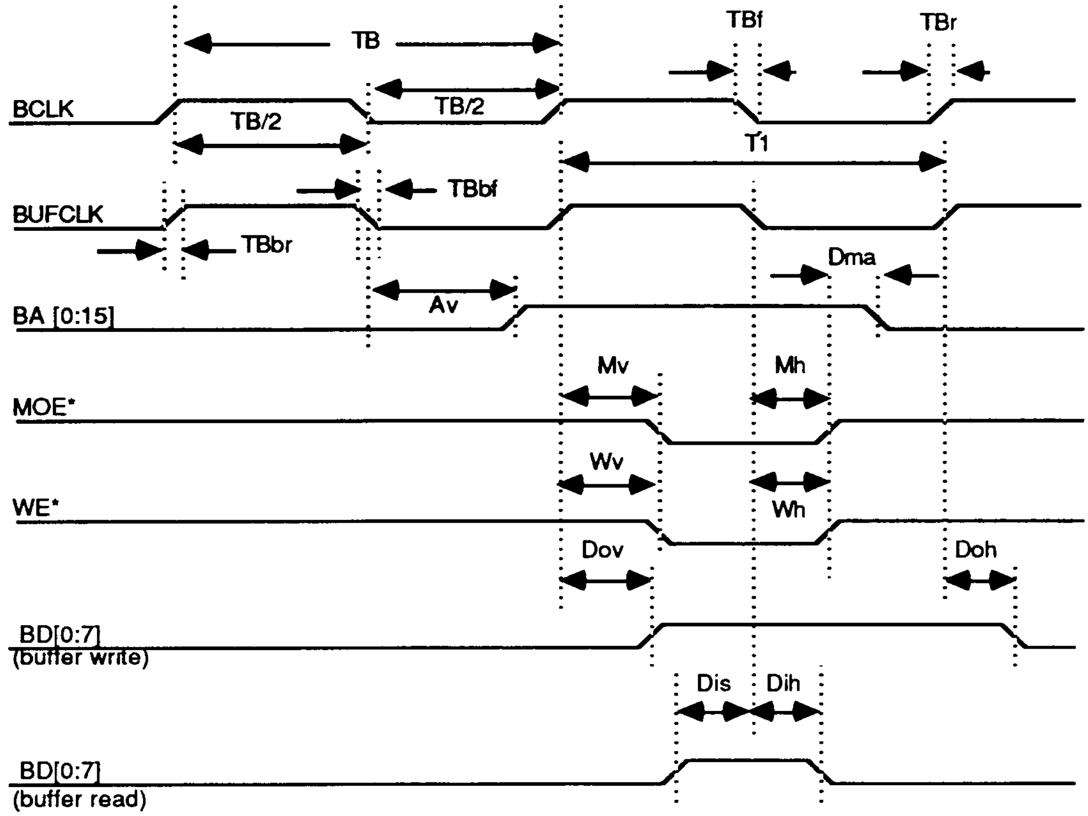
Buffer Memory Read/Write Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
T_B	BCLK Period	41		ns
$T_B/2$	BCLK High/Low Time	16		ns
$T_{Br}=T_{Bf}$	BCLK Rise and Fall Time		5	ns
T1	BUFCLK† Period	125		ns
Av	BUFCLK†↓ to BA [0:15] valid		50	ns
Dov	BUFCLK†↑ to BD [0:7] valid		50	ns
Doh	BUFCLK†↑ to BD [0:7] invalid	0		ns
Mv	BUFCLK†↑ to MOE*↓		30	ns
Mh	BUFCLK†↓ to MOE*↑	10	35	ns
Wv	BUFCLK†↑ to WE*↓		30	ns
Wh	BUFCLK†↓ to WE*↑	5	30	ns
Dma	MOE*↑ to BA [0:15] Hold	5	30	ns
Dis	BD [0:7] valid to BUFCLK†↓	0		ns
Dih	BUFCLK†↓ to BD [0:7] invalid	10		ns
TBbr	BCLK↑ to BUFCLK↑		24	ns
TBbf	BCLK↓ to BUFCLK↓		21	ns

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

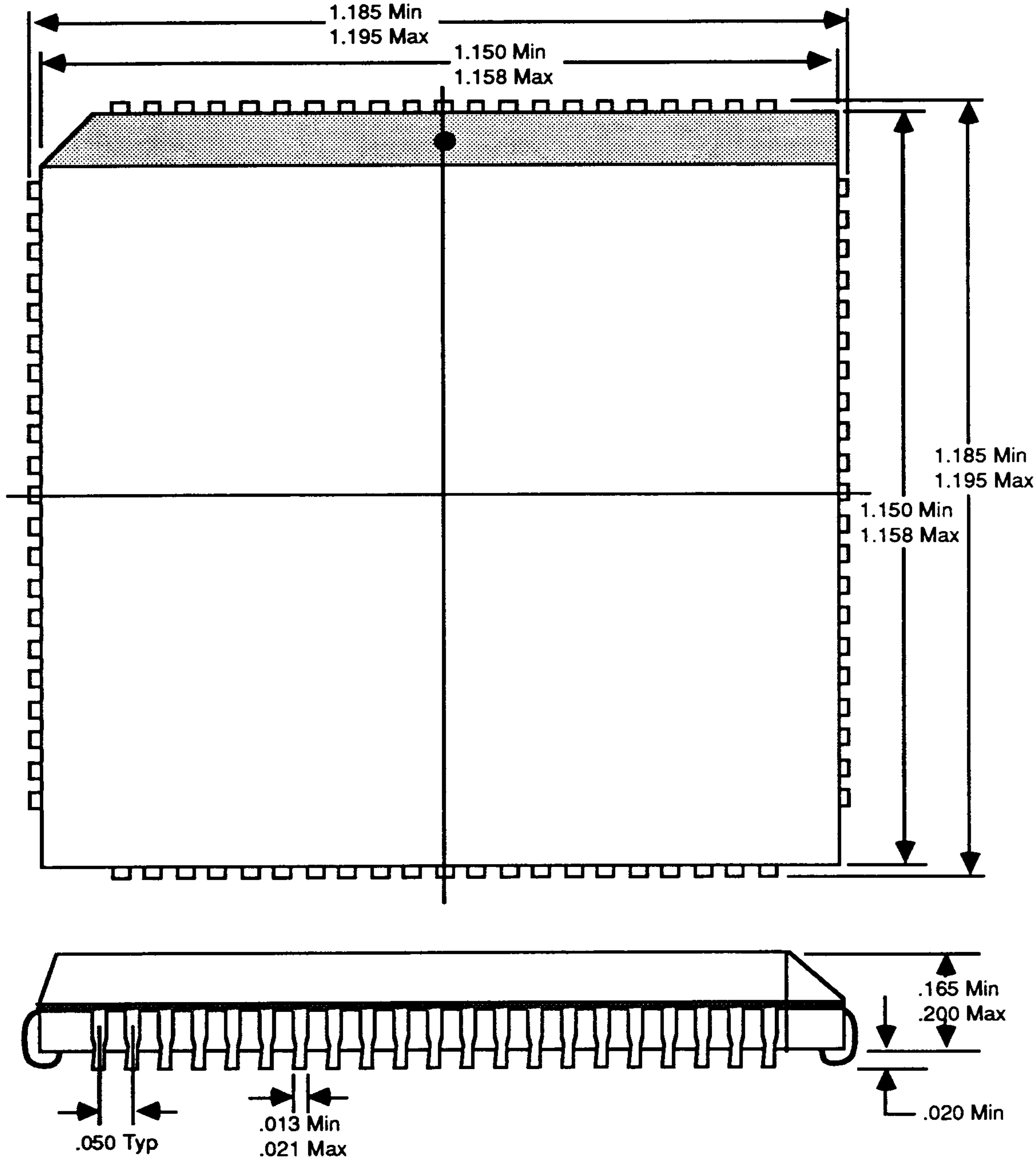
† BUFCLK is an internal signal which indicates the period of buffer memory access cycle. These specifications can be tested when the period of BCLK (Pin 41) is the same as the period of buffer memory access cycles (i.e., Register 7FH, Bits 6 and 7 are 1 and 0 respectively). If the buffer memory access cycle period is programmed to be a multiple of the period of BCLK, BUFCLK above refers to the buffer memory access cycles and the falling edge referred to above would be coinciding with the rising (leading) edge of the BCLK signal (Pin 41).

Buffer Memory Read/Write Timing



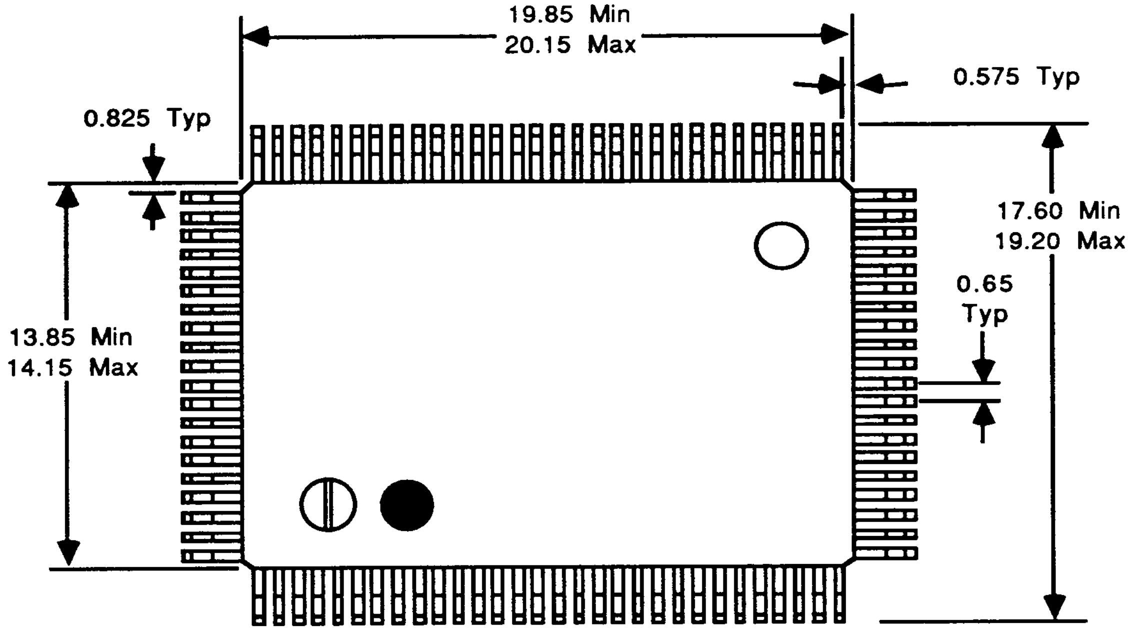
15. SAMPLE PACKAGE

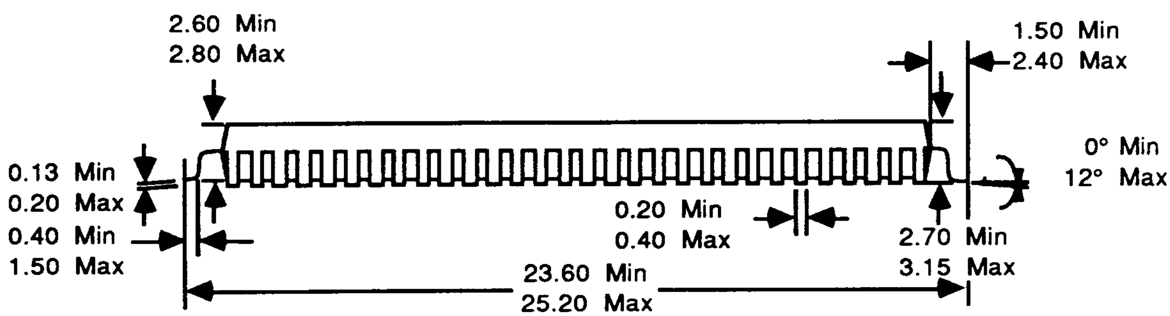
15.1 84-Pin Plastic Leaded Chip Carrier (PLCC) Sample Package



NOTE: Dimensions for the PLCC package are in inches.

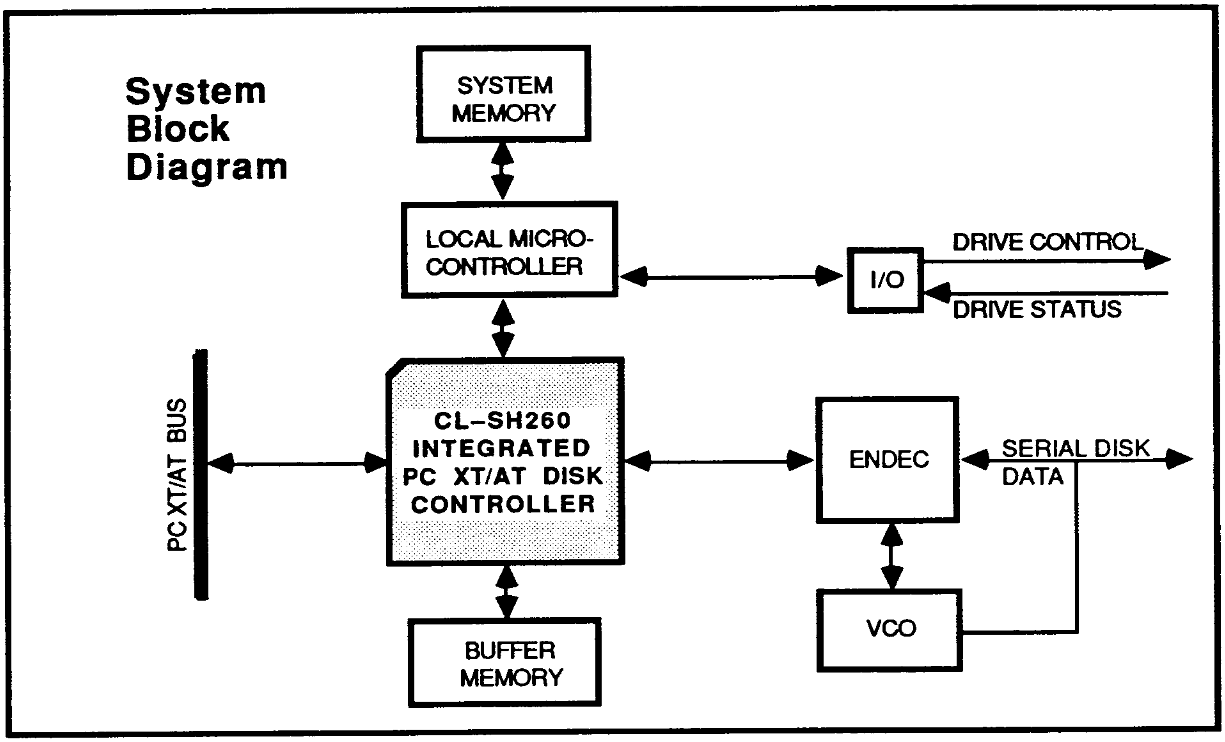
15.2 100-Pin Quad Flat Pack (QFP) Sample Package





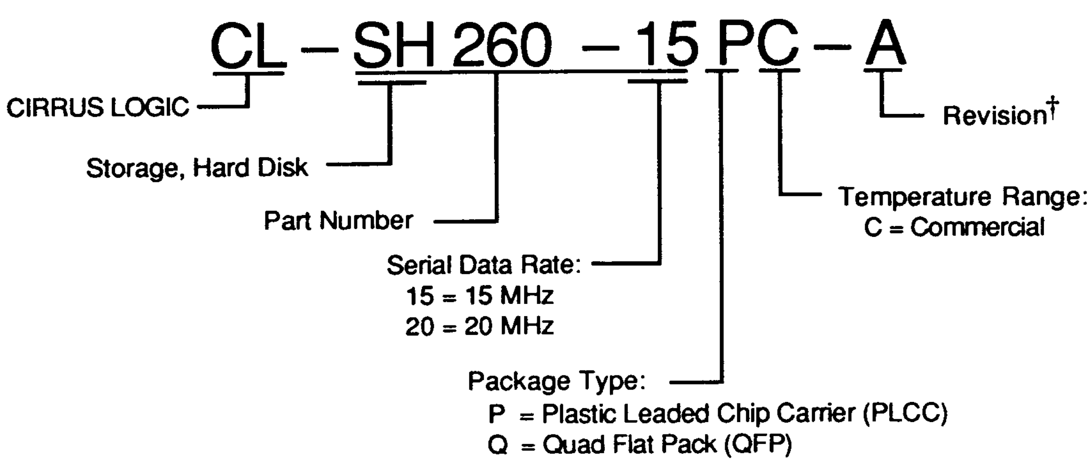
NOTE: Dimensions for the QFP package are in millimeters.

16. TYPICAL APPLICATION



17. ORDERING INFORMATION

CIRRUS LOGIC Numbering Guide



† Contact CIRRUS LOGIC for up-to-date information on revisions.

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The Company

Cirrus Logic, Inc., is a leading supplier of high-integration peripheral controller circuits for mass storage, graphics, and data communications. The company also produces state-of-the-art software and firmware to complement its product lines. Cirrus Logic technology is used in leading-edge personal computers, engineering workstations, and office automation.

The Cirrus Logic formula combines proprietary S/LA™† IC design automation with system design expertise. The S/LA design system is a proven tool for developing high-performance logic circuits in half the time of most semiconductor companies. The results are better VLSI products, on-time, that help you win in the marketplace.

Cirrus Logic's extensive quality assurance program — one of the industry's most stringent — ensures the utmost in product reliability. Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company — Cirrus Logic.

† U.S. Patent No. 4,293,783

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