APPLICATION NOTE USING ST6 ANALOG INPUTS FOR MULTIPLE KEY DECODING

## INTRODUCTION

The ST6 on-chip Analog to Digital Converter (ADC) is a useful peripheral integrated into the silicon of the ST6 family members. The flexibility of the I/O port structure allows the multiplexing of up to 13/8 Analog Inputs into the converter in a 28/20 pin device for the ST6210/15 2 k ROM and ST6220/25 4k ROM families, enabling full freedom in circuit layout. Many other members of the ST6 family also offer the Analog to Digital converter.
One of the more novel and practical applications of this converter, is to decode a number of keys. The technique is to connect the keys by resistive voltage dividers to the converter inputs. An example of key detection using 10 keys is illustrated in this note.
Using the Analog to Digital converter in this fashion does not require a static current and avoids false key detection.

## BASIC CIRCUIT

The basic circuit of the key decoder consists of a pull-up resistor connected to the ST6 Analog to Digital converter input with the first key directly switching to ground. The following keys are then connected in sequence to the ADC input through serial resistors. The number of keys which may be detected depends on the tolerance of the resistors used. It can be seen that if more than one key is pressed at the same time, the key detected will be the next key in the chain closest to the ADC input. This also allows the keys in the keyboard to be prioritized.

## PRINCIPLE OF OPERATION

The combination of the pull-up resistor, the serial resistors and the pressed key form a resistive voltage divider, generating a different voltage at the ADC input for each key pressed. The serial resistors are selected in order to give an equal distribution of voltage between VDD and Vss for each switch combination to give the best noise margin between keys.
When a key is pressed, the voltage at the ADC input is given by the activated voltage divider. This analog voltage is converted by the ADC and the digital value is used to determine which switch is closed. Two successive conversions may be made to avoid the influence of key bounce.

Figure 1. Analog Keyboard resistor key matrix


Figure 2. Multiple key press


Table 1. Key code ranges

| Key Nr | Valid Code <br> Range | Distance to <br> next key |
| :---: | :---: | :---: |
| 1 | 0 | 24 |
| 2 | $18-1 \mathrm{~A}$ | 22 |
| 3 | $30-33$ | 22 |
| 4 | $49-4 \mathrm{E}$ | 21 |
| 5 | $63-68$ | 20 |
| 6 | $7 C-81$ | 22 |
| 7 | $97-9 B$ | 21 |
| 8 | B0-B4 | 22 |
| 9 | CA-CD | 24 |
| 10 | E5-E6 | 25 |

If the top key is pressed, the voltage measured is always zero. For nkeys, the resistor values should be selected such that the voltage for the second key from top is $V_{D D} / n$, for the $3 r d-2 x V_{D D} / n$, for the 4th $3 x V_{D D} / n$ and for the $n$th - $(n-1) \times V_{D D} / n$. Resistor values from the tolerance set used must be selected to meet this requirement.
The recommended resistor values for a 10-key keyboard with $2 \%$ resistors from the E24 series, used with a $10 \mathrm{k} \Omega$ pull-up resistor, are shown in table 2. If more current can be allowed, then a $1 \mathrm{k} \Omega$ resistor can be used in which case the serial resistor values should be divided by 10 .

Table 2. Used resistors and Tolerance

| Resistor | Value ( $\Omega \mathbf{)}$ | $\mathbf{- 2 \%}(\Omega)$ | $\mathbf{+ 2 \%}(\Omega)$ |
| :---: | :---: | :---: | :---: |
| Rp | 10000 | 9800 | 10200 |
| R1 | 1100 | 1078 | 1122 |
| R2 | 1300 | 1274 | 1326 |
| R3 | 1800 | 1764 | 1836 |
| R4 | 2400 | 2352 | 2448 |
| R5 | 3300 | 3234 | 3366 |
| R6 | 5100 | 4998 | 5202 |
| R7 | 8200 | 8036 | 8364 |
| R9 | 16000 | 15680 | 16320 |

## PRACTICAL LIMITATIONS

Theoretically, for an ideal power supply, ADC and resistors, 255 keys could be detected. Practically however, it is necessary to take into account potential errors coming from:

- the power supply - the key resistivity - the resistor tolerance - the ADC error

The power supply tolerance can normally be neglected providing noise is not present at a frequency within or above the frequency range of the RC delay of the resistive divider, as the ADC reference is normally provided by the power supply of the ST6. For ST6 family members with external ADC reference voltage inputs, AVDD and AVss may be used instead of VDD and Vss.
The sensitivity of the key can normally be neglected, as the resistance of the divider is high in comparison to it. If the key resistivity is significant, it should be added to the "serial" pull-down resistance of the different dividers. The key resistivity variation must also be added to the tolerance of the serial pull-down resistor (see resistor tolerance following).
The resistor tolerance affects the tolerance of the dividers. Two situations must be taken into account:
a) minimum value of pull-up combined with maximum values of pull-down = maximum voltage of the divider at the ADC input.
b) maximum value of the pull-up combined with the minimum values of pull-down $=$ minimum voltage at the ADC input. These two cases give the maximum voltage variation of each divider (see Table 3). The voltage variation ranges of two dividers must not overlap otherwise the key cannot be decoded, even with an ideal converter.

Table 3. Effective Divider Resistors

| Active <br> Key | $\mathbf{R - 2 \%}(\Omega)$ | $\mathbf{R + 2 \%}(\Omega)$ |
| :---: | ---: | ---: |
| S0 | 0 | 0 |
| S1 | 1078 | 1122 |
| S2 | 2352 | 2448 |
| S3 | 4116 | 4284 |
| S4 | 6468 | 6732 |
| S5 | 9702 | 10098 |
| S6 | 14700 | 15300 |
| S7 | 22736 | 23664 |
| S8 | 38416 | 39984 |
| S9 | 88396 | 92004 |

Realistic converters require a margin between the range of variation. In the case of a significant variation in the key resistivity, the maximum resistivity of the key has to be added to the value of the pulldown resistor in case a). For case b) no error needs to be added as the resistivity cannot be less than $0 \Omega$.

The linearity of the ADC converter of the ST6 is normally specified for $\pm 2$ LSB, therefore a minimum distance of 4 LSB is needed between the edges of the resistance tolerance ranges. For the best results, a minimum of 8 LSB should be used (see Table 4).

Table 4. Voltage at the ADC-Input,Converter Results (5V supply)

| Active Key | V (Rxmin-Rpmax) |  |  | V (Rxmax-Rpmin) |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $V$ | hex. | dec. | $V$ | hex. | dec. |
| S0 | 0.00 | 00 | 0 | 0.00 | 00 | 0 |
| S1 | 0.48 | 18 | 24 | 0.51 | $1 A$ | 26 |
| S2 | 0.94 | 30 | 48 | 1.00 | 33 | 51 |
| S3 | 1.44 | 49 | 73 | 1.52 | $4 E$ | 78 |
| S4 | 1.94 | 63 | 99 | 2.04 | 68 | 104 |
| S5 | 2.44 | $7 C$ | 124 | 2.54 | 81 | 129 |
| S6 | 2.95 | 97 | 151 | 3.05 | $9 B$ | 155 |
| S7 | 3.45 | B0 | 176 | 3.54 | B4 | 180 |
| S8 | 3.95 | C9 | 201 | 4.02 | CD | 205 |
| S9 | 4.48 | E5 | 229 | 4.52 | E6 | 230 |

Table 5. AD-Converter Results

| Active Key | R Error Range <br> (LSB) | Distance to next <br> Key | Valid Key Range |
| :---: | :---: | :---: | :---: |
| S0 | 0 | 24 | $0-0$ |
| S1 | 2 | 22 | $18-1 \mathrm{~A}$ |
| S2 | 3 | 22 | $30-33$ |
| S3 | 4 | 21 | $49-4 \mathrm{E}$ |
| S4 | 5 | 20 | $63-68$ |
| S5 | 5 | 22 | $7 \mathrm{C}-81$ |
| S7 | 5 | 21 | $97-9 B$ |
| S8 | 4 | 22 | B0-B4 |
| 24 | 25 | E5-E6 |  |

## EXTENSION FOR WAKE UP

ST6 family members with the Analog input capacity can also generate a wakeup operation (from WAIT or STOP modes) on the pressing of a key. This can be achieved by a modification of the circuit shown in figure 1. The pull-up resistor is not connected to $V_{D D}$ but to an additional I/O port bit. During key polling, this additional port bit is set to output mode active high, thus effectively switching $V_{D D}$ to the pull-up resistor. The resistance of the pull-up resistor must be high enough to give no significant voltage drop, or the resulting error must be calculated and taken into account. The other I/O bit is used as the Analog input to the ADC as in the original circuit.
During the wait for the key press, the first I/O pin, used to pull the pull-up resistor high to $V_{D D}$ while polling, is switched into a high impedance state (e.g. open drain output mode). The second I/O pin, used as the ADC input while polling, is switched to the interrupt input with pullup mode. The internal pull-up is in the range of 100 k , in comparison to the 1 k 10k of the external resistor used during polling. If any key is now pressed an interrupt will be generated if the voltage at the second I/O pin is below the Schmitt trigger low level threshold. The serial resistors in the keyboard chain must not be too high in this case, therefore the maximum number of keys is reduced in comparison to the normal mode.

Figure 3. Keyboard wake-up circuit


Figure 4. Keyboard reading


Figure 5. Interrupt configuration


## APPENDIX A: Key Input by Polling





## APPENDIX B: Key Input by Interrupt



```
en_kint:
            ldi ddrpb,inpall ; sets all port B pins low - all input
            ldi orpb,02h ;option register:
                            ; sets bit b1 high, the rest low
    ldi drpb,01h ;data register:
    ; sets bit b0 high, the rest low
    ;- pb0 becomes input, no pull-up, no int
    ; pb1 becomes input with pull-up and int.
    ; pb2-7 become input with pull-up, but
    ; are not used here
    ldi ior,10h ;interrupt option register:
    ;- set D4: enable all interrupts
    ; reset D5: falling edge on int.input(#2)
    ret ;return to the calling address
;*** hd_kint (handle key interrupt) interrupt service routine
;*** evaluates the data resulting in pushing a key.
;*** Interrupt vector #2 (0ff4h and 0ff5h) must point (jump) to hd_kint.
hd_kint: ldi drpb,03h ;data register:
    ; 0000 0011
    ldi ddrpb,01h ;data direction register:
    ; 0000 0001
    ; - pb0 becomes output
    ldi orpb,03h ;option register:
        ; 0000 0011
        ; - pbO: push-pull output
        ; - pb1: ADC-input
        ; pb2-7 become input with pull-up, but
        ; are not used here
    ldi adcr,30h ;A/D control register:
        ; 0011 0000 - -activate A/D converter
        ; -start conversion
        -disable A/D interrupt
loop: jrr 6,adcr,loop ;waits until the End Of Conversion
    ; bit is set (indicator that a conversion
    ; has been completed)
    ld a,adr ;load acc with the result of the A/D
        ; conversion
        ;now the result is compared with the
        ; values which represent the different
        ; switches
```

| sw1: | cpi | a,peg1_2 | ; compare with peg1_2 |
| :--- | :--- | :--- | :--- |
| jrnz | sw2 | ;A/D result was smaller than peg1_2 |  |
| jp | s1 | $;-$ switch1 was pressed: jump to s1 |  |


| sw2: | cpi | a,peg2_3 | ; compare with peg2_3 |
| :--- | :--- | :--- | :--- |
|  | jrnz | sw3 | ;A/D result was smaller than peg2_3 |
|  | jp | s2 | ; - switch2 was pressed: jump to s2 |


| sw3: | cpi | a,peg3_4 | ; compare with peg3_4 |
| :--- | :--- | :--- | :--- |
|  | jrnz | sw4 | ;A/D result was smaller than peg3_4 |
| $j p$ | s3 | $;-$ switch3 was pressed: jump to s3 |  |

sw4: cpi a,peg4_5 ;compare with peg4_5
jrnz sw5
jp s
sw5: cpi a,peg5_6 ;compare with peg5_6
jrnz sw6 ;A/D result was smaller than peg5_6
jp s5 ; - switch5 was pressed: jump to s5
sw6: cpi a,peg6_7 ;compare with peg6_7
jrnz sw7 ;A/D result was smaller than peg6_7
jp s6 ; - switch6 was pressed: jump to s6
sw7: cpi a,peg7_8 ;compare with peg7_8
jrnz sw8 ;A/D result was smaller than peg7_8
jp s7
; - switch7 was pressed: jump to s7

| sw8: | cpi | a,peg8_9 | ; compare with peg8_9 |
| :---: | :---: | :---: | :---: |
|  | jrnz | sw9 | ;A/D result was smaller than peg8_9 |
|  | jp | s8 | ; - switch8 was pressed: jump to s8 |
| sw9: | jp | s9 | ;A/D result was bigger than peg8_9 |
|  |  |  | ; - switch9 was pressed: jump to s9 |
|  |  |  | ; |

;*** The routines handling the reaction to the individual key presses ;*** are to be included here

```
s1:
s2:
s3:
s4:
s5:
s6:
s7:
s8:
s9:
;*** Each routine must end with the following lines in order to enable
;*** another interrupt when the next key is pressed.
    call en_kint ; enable another interrupt
return: reti
```


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