T-46-19-11

# ACT™ 2 Field Programmable Gate Arrays

## Features

- Up to 8000 Gate Array Gates (20,000 PLD/LCA™ equivalent gates)
- Replaces up to 210 TTL Packages
- Replaces up to 69 20-Pin PAL Packages
- Design Library with over 250 Macros
- Single-Module Sequential Functions
- Wide-Input Combinatorial Functions
- Up to 1232 Programmable Logic Modules
- Up to 998 Flip-Flops
- 16-Bit Counter Performance to 85 MHz
- 16-Bit Accumulator Performance to 33 MHz
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Two High-Speed, Low-Skew Clock Networks
- I/O Drive to 10 mA
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment

## Product Family Profile

| Device | A1280 | A1240 | A1225 |
|---|---|---|---|
| Capacity | | | |
| Gate Array Equivalent Gates | 8,000 | 4,000 | 2,500 |
| PLD/LCA Equivalent Gates | 20,000 | 10,000 | 6,250 |
| TTL Equivalent Packages | 210 | 105 | 70 |
| 20-Pin PAL Equivalent Packages | 69 | 34 | 23 |
| Logic Modules | 1,232 | 684 | 451 |
| S-Modules | 624 | 348 | 231 |
| C-Modules | 608 | 336 | 220 |
| Flip-Flops (maximum) | 998 | 565 | 382 |
| Routing Resources | | | |
| Horizontal Tracks/Channel | 36 | 36 | 36 |
| Vertical Tracks/Column | 15 | 15 | 15 |
| PLICE® Antifuse Elements | 750,000 | 400,000 | 250,000 |
| User I/Os (maximum) | 140 | 104 | 83 |
| Packages[1] | 176 CPGA<br>160 PQFP<br>172 CQFP | 132 CPGA<br>144 PQFP<br>84 PLCC | 100 CPGA<br>100 PQFP<br>84 PLCC |
| Performance[2] | | | |
| 16-Bit Counters | 55 MHz | 75 MHz | 85 MHz |
| 16-Bit Accumulators | 30 MHz | 33 MHz | 33 MHz |
| CMOS Process | 1.2 µm | 1.2 µm | 1.2 µm |

**Note:**

1. See product plan for package availability.
2. Performance is based on a –1 speed graded device at commercial worst-case operating conditions.


**Figure 1. A1280 176-Pin CPGA**

## Description

The ACT™ 2 family represents Actel's second generation of field programmable gate arrays (FPGAs). The ACT 2 family presents a two-module architecture, consisting of C-Modules and S-Modules. These modules are optimized for both combinatorial and sequential designs. Based on Actel's patented channeled array architecture, the ACT 2 family provides significant enhancements to gate density and performance while maintaining upward compatibility with the ACT 1 design environment. The devices are implemented in silicon gate, 1.2-µm, two-level metal CMOS, and employ Actel's PLICE antifuse technology. This revolutionary architecture offers gate array design flexibility, high performance and fast time-to-production through user programming. The ACT 2 family is supported by the Action Logic™ System (ALS), which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and debug and diagnostic probe capabilities. The Action Logic System is supported on the following platforms: 386/486 PC and Sun®, HP® and Apollo® workstations. It provides CAE interfaces to the following design environments: Valid™, Viewlogic®, Mentor Graphics®, HP DCS and OrCAD™.

1

## ACT 2 Architecture

This section of the datasheet is meant to familiarize the user with the architecture of ACT 2 family devices. A generic description of the family will be presented first, followed by a detailed description of the logic blocks, the routing structure, the antifuses, and the special function circuits. Diagrams for the A1280, A1240, and A1225 are provided at the end of the datasheet. The additional circuitry required to program and test the devices will not be covered.

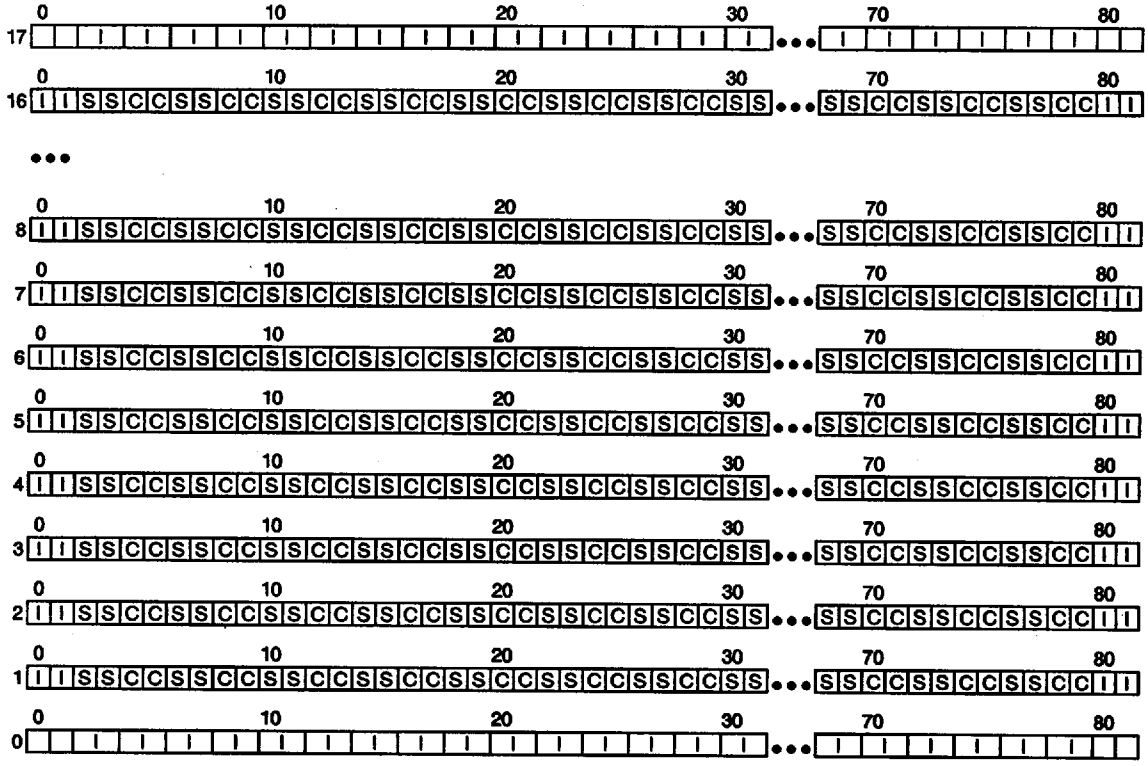
### Array Topology

The ACT 2 family architecture is composed of five key elements or building blocks: Logic modules, I/O modules, Routing Tracks, Global Clock Networks, and Probe Circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, and I/Os.

**Table 1. Array Sizes**

| Device | Rows | Columns | Logic | I/O |
|---|---|---|---|---|
| A1280 | 18 | 82 | 1232 | 140 |
| A1240 | 14 | 62 | 684 | 104 |
| A1225 | 13 | 46 | 451 | 83 |

The Logic and I/O modules are arranged in a two-dimensional array (Figure 2). There are three types of modules: Logic, I/O, and Bin. Logic and I/O modules are available as user resources. Bin modules are used during testing and are not available to users.




S = Sequential Module, C = Combinatorial Module, I = I/O Module

**Figure 2. A1280 Simplified Floor Plan**

## Logic Modules

Logic modules are classified into two types: combinatorial C-modules and sequential S-modules (see Figures 3 and 4). The C-module is an enhanced version of the Act 1 family logic module optimized to implement high fan-in combinatorial macros, such as 5-input AND, 5-input OR, etc. The S-module is designed to implement high speed flip-flop functions within a single module. S-modules also include combinatorial logic, which allows an additional level of logic to be implemented without additional propagation delay. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating pairs (shown in Figure 2) and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). I/O-modules are arranged around the periphery of the array.

The combinatorial module (shown in Figure 2) implements the following function:

$$Z = !S1 * (D00 * !S0 + D01 * S0) + S1 * (D10 * !S0 + D11 * S0)$$

where:

$$S0 = A0 * B0$$
$$S1 = A1 + B1$$

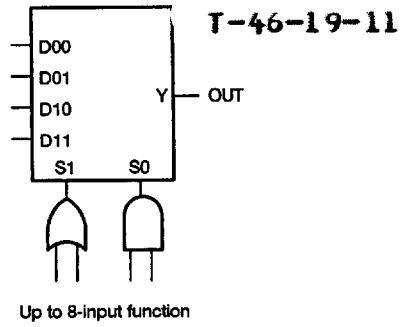



**Figure 3. C-Module Implementation**

The sequential module implements this same function Z, followed by a sequential block. The sequential block can be configured to implement either a D-type flip-flop or transparent latch. It can also be fully transparent so that S-modules can be used to implement purely combinatorial functions. The function of the sequential module is determined by the macro selection from the design library of hard macros. Allowable S-module implementations are shown in Figure 4.



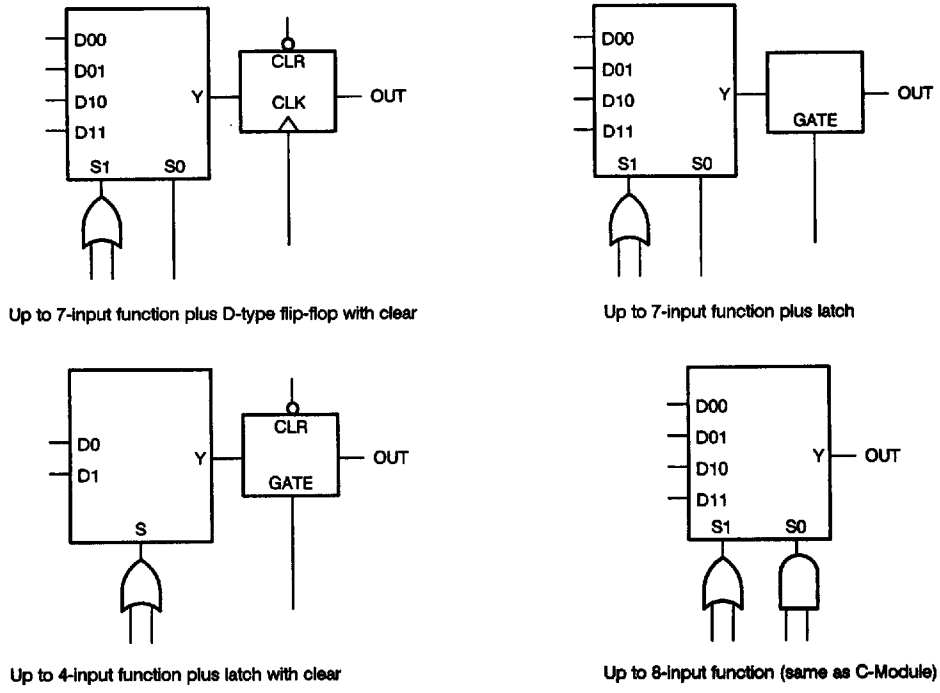



**Figure 4. S-Module Implementations**

### I/Os

The I/O architecture consists of pad drivers located near the bonding pads and I/O modules located in the array. Top/bottom I/O modules are located in the top and bottom rows respectively. Side I/O modules occupy the leftmost two columns and the rightmost two columns of the array. The function of all I/O modules is identical, but the top/bottom I/O modules have a different routing interface to the array than the side I/O modules. I/Os implement a variety of user functions determined by library macro selection.

### Special Purpose I/Os

Certain I/O pads are temporarily used for programming and testing the device. During normal user operation, these special I/O pads are identical to other I/O pads. The following special I/O pads and their functions, are shown in Table 2.

**Table 2. Special I/O Pads**

| | |
|---|---|
| SDI | Serial Data In |
| SDIO | Serial Data Out |
| BININ | Binning Circuit In |
| BINOUT | Binning Circuit Out |
| DCLK | Serial Data Clock In |
| PRA | Probe A Output |
| PRB | Probe B Output |

Two other pads, CLKA and CLKB, also differ from normal I/Os in that they can be used to drive the global clock networks. Power, Ground, and Programming pads are not considered I/O functions. Their function is summarized as follows:

| | |
|---|---|
| VCCA, VCCQ, VCCI | Power |
| GNDA, GNDQ, GNDI | Circuit Ground |
| VSV, VKS | Programming Pads |
| MODE | Program/Debug Control |

### I/O Pads

I/O pads are located on the periphery of the die and consist of the bonding pad, the high-drive CMOS drivers, and the TTL level-shifter inputs. Each I/O pad is associated with a specific I/O module. Connections form the I/O pad to the I/O module are made using the signals DATAOUT, DATAIN and EN (shown in Figure 5).

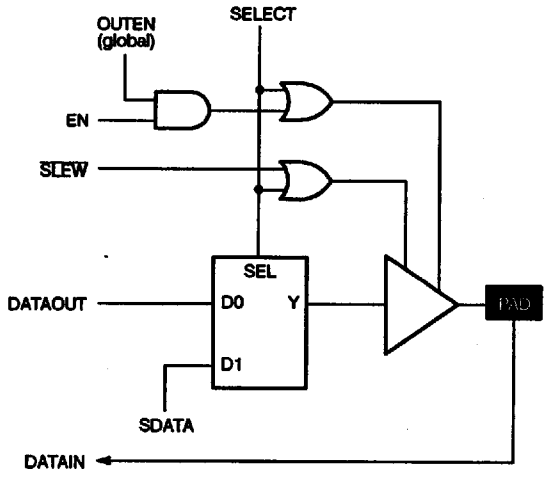



**Figure 5. I/O Pad Signals**

### I/O Modules

There are two types of I/O modules: side and top/bottom. The I/O module schematic is shown in Figure 6. In the side I/O modules, there are two inputs supplying the data to be output from the chip: UO1 and UO2. (UO stands for user output). Two are used so that the router can choose to take the signal from either the routing channel above or the routing channel below the I/O module. The top/bottom I/O modules interact with only one channel and therefore have only one UO input.

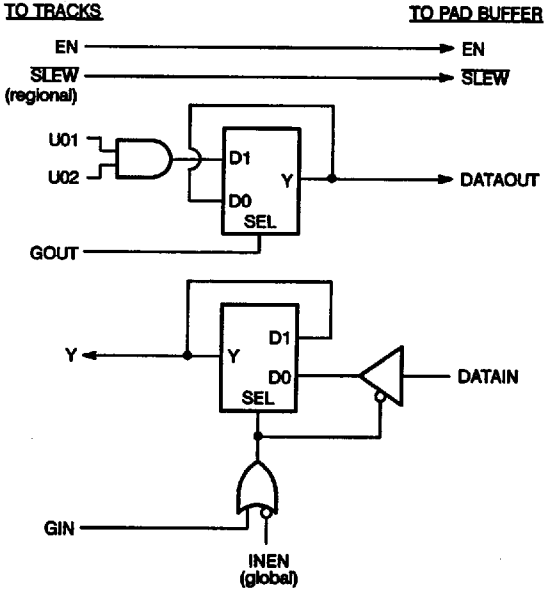



**Figure 6. I/O Module**

The EN input enables the tristate output buffer. The global signals INEN and OUTEN (Figure 5) are used to disable the inputs and outputs during certain test modes. Latches are provided in the input and output path. When GOUT is low, the output signal on UO1/UO2 is latched. When it is high, the latch is transparent. The latch can be used as the second stage of a rising-edge flip-flop as described in the Applications note accompanying this data sheet. GIN is the reverse of GOUT. When GIN is high, the input data is latched; when it is low, the input latch becomes transparent.

The output of the module, Y, is used for data being input to the chip. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below it (similar to logic modules). Side I/O modules may also connect to the array through nondedicated Long Vertical Tracks (LVTs). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom must be routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section). As a result, I/O signals connected to I/O modules on either the top or bottom of the array may incur a slight delay penalty (~1nS) over signals connected to I/O modules on the sides.

## Hard Macros

Designing within the Actel design environment is accomplished using a building block approach. Over 250 logic function macros are provided in the ACT 2 design library. Hard macro logic functions range from simple SSI gates such as AND, NOR, and Exclusive OR to more complex functions such as flip-flops with 4:1 Multiplexed Data inputs. Hard macros are implemented in the ACT 2 architecture by using one or more C-modules or S-modules. Over 150 of the macros are implemented in a single module, while several two-module macros are also available. Two-module hard macros always utilize a module-pair, either SS, CC, CS, or SC. Because one- and two-module macros have small propagation delay variances, their performances can be predicted very accurately. Hard macro propagation delays are specified in the datasheet. Soft macros are comprised of multiple hard macros connected together to form complex functions. These functions range from MSI functions to 16-bit counters and accumulators. A large number of TTL equivalent hard and soft macros are also provided. Soft macro delays are not specified in the datasheet.

## Routing Structure

The ACT 2 architecture uses Vertical and Horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into pieces called segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

## Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 7. Nondedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

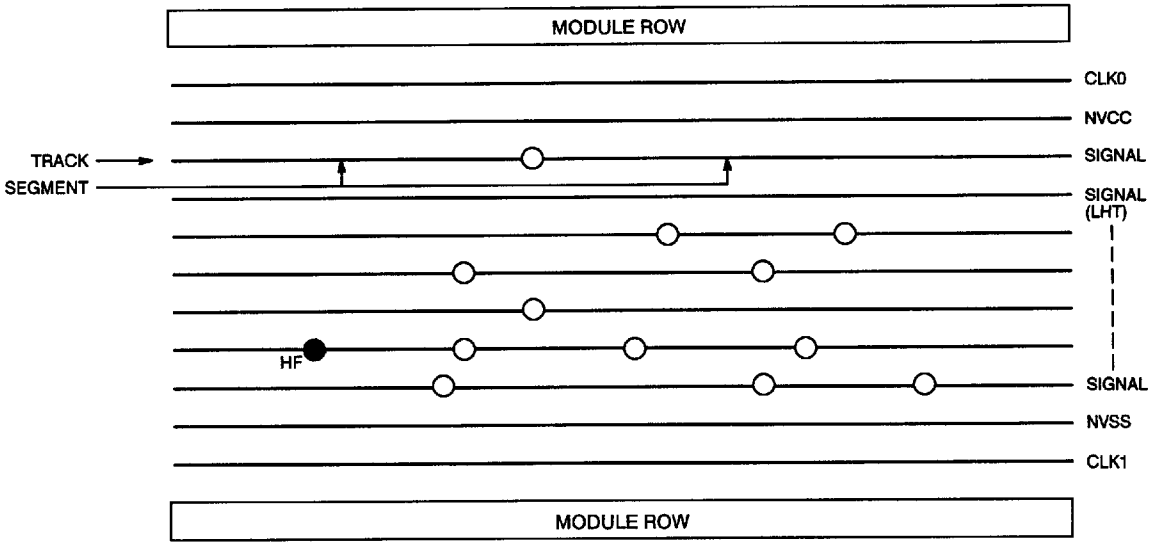



**Figure 7. Horizontal Routing Tracks and Segments**

## Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 8.

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PAL®s. The use of antifuses to implement a Programmable Logic Device results in highly testable structures as well as efficient programming algorithms. The structure is highly testable because there are no pre-existing connections, therefore temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

## Antifuse Structures

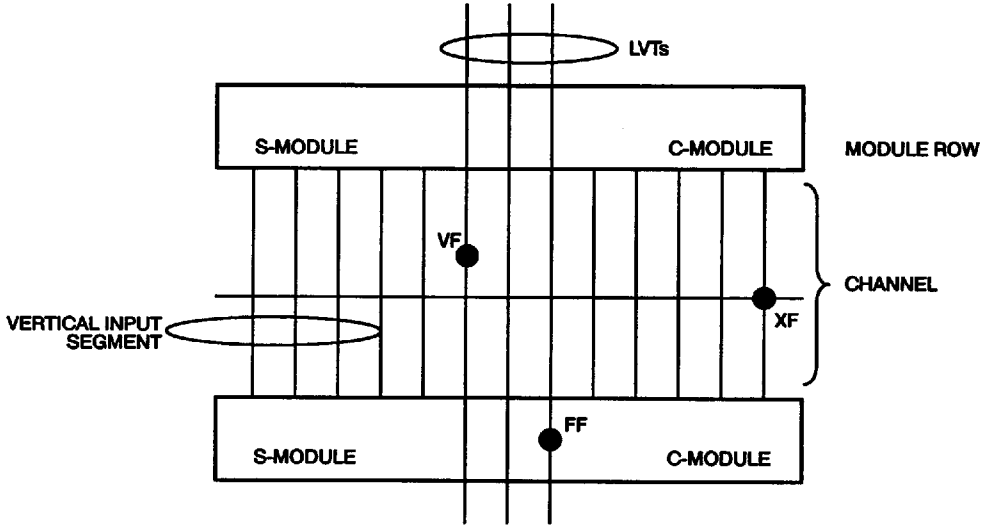



**Figure 8. Vertical Routing Tracks and Segments**

## Antifuse Connections

Four types of antifuse connections are used in the routing structure of the Act 2 array. (The physical structure of the antifuse is identical in each case, only the usage differs.) The four types are:

| | | |
|---|---|---|
| XF | Cross connected antifuse | Most intersections of horizontal and vertical tracks have an XF that connects the perpendicular tracks. |
| HF | Horizontally connected antifuse | Adjacent segments in the same horizontal track are connected end-to-end by an HF. |
| VF | Vertically connected antifuse | Some long vertical tracks are divided into two segments. Adjacent long segments are connected end-to-end by a VF. |
| FF | "Fast-Fuse" antifuse | The FF connects a module output directly to a long vertical track. |

Examples of all four antifuse connections are shown in Figures 7 and 8.

### Antifuse Programming

The ACT 2 family uses the PLICE™ antifuse developed by Actel. The PLICE element is programmed by placing a high voltage (~20 V) across the element and supplying current (~5 mA) for a short duration (< 1ms). In the ACT 2 architecture, most antifuses are programmed to ~500 ohms resistance, except for the F-fuses which are programmed to ~250 ohms. The programming circuits are transparent to the user.

### Clock Networks

Two low-skew, high fan-out clock distribution networks are provided in the ACT 2 architecture (Figure 9). These networks are referred to as CLK0 and CLK1. Each network has a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows:

1. externally from the CLKA pad
2. externally from the CLKB pad
3. internally from the CLKINA input
4. internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

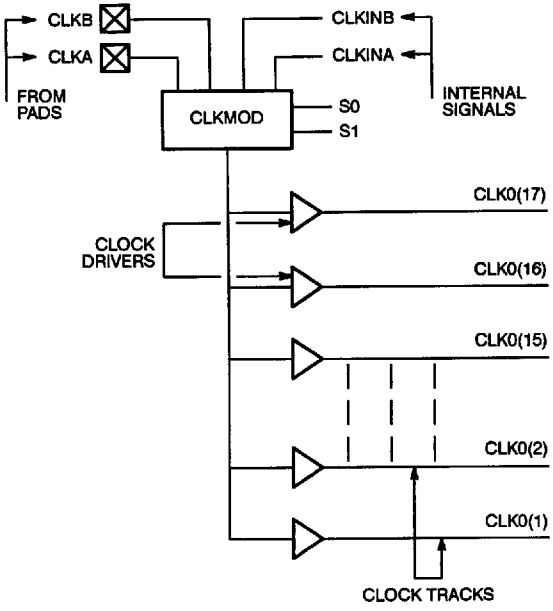



**Figure 9. Clock Networks**

The user configures the clock module by selecting one of two clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used.

The clock input pads may also be used as normal I/Os, by-passing the clock networks.

### Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

### Module Input Connections

Vertical tracks span the vertical height of the array. The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive (off), which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active (on) to verify the continuity of the metal tracks. Vertical input segments span only one channel. Inputs to the array modules come either from the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below (Figure 10).

### Module Output Connections

Module outputs have dedicated output segments. Output segments extend vertically two channels above and two channels below, except at the top or bottom of the array. Output segments twist, as shown in Figure 10, so that only four vertical tracks are required.

### LVT Connections

Outputs may also connect to non-dedicated segments (LVTs). Each module pair in the array shares three LVTs that span the length of column as shown in Figure 9. Any module in the column pair can connect to one of the LVTs in the column using an FF connection. The FF connection uses antifuses connected directly to the driver stage of the module output, by-passing the isolation transistor. FF antifuses are programmed at a higher current level than HF, VF, or XF antifuses to produce a lower resistance value.

### Antifuse Connections

In general every intersection of a vertical segment and a horizontal segment contains an unprogrammed antifuse (XF-type). One exception is in the case of the clock networks.

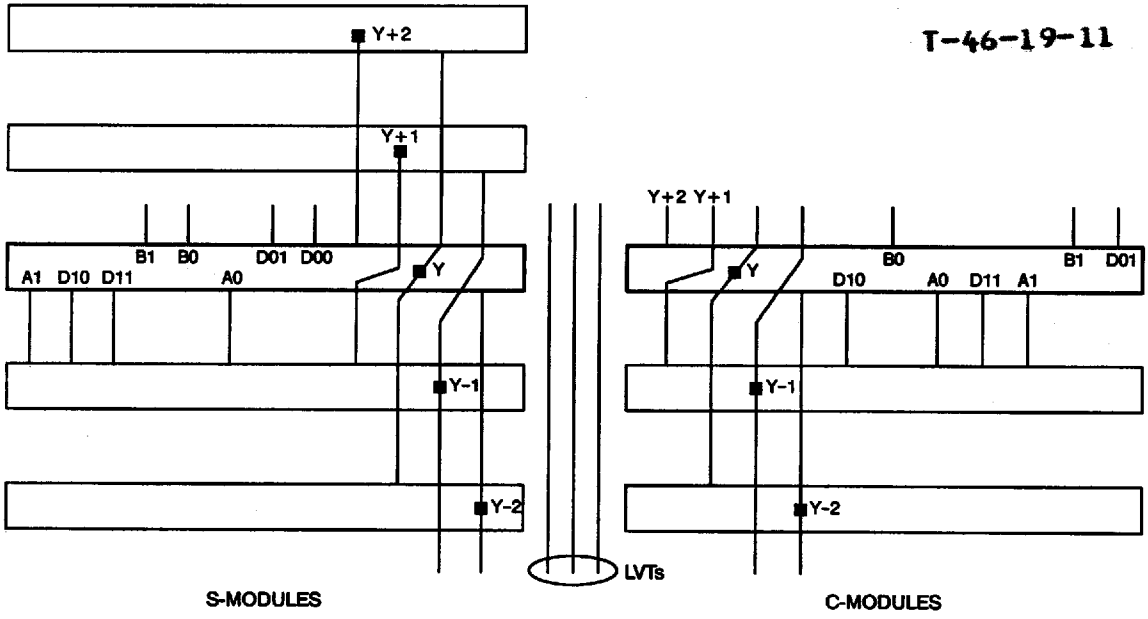



**Figure 10. Logic Module Routing Interface**

## Clock Connections

To minimize loading on the clock networks, only a subset of inputs has fuses on the clock tracks. Only a few of the C-module and S-module inputs can be connected to the clock networks. To further reduce loading on the clock network, only a subset of the horizontal routing tracks can connect to the clock inputs of the S-Module. Both of these are illustrated in Figure 11.

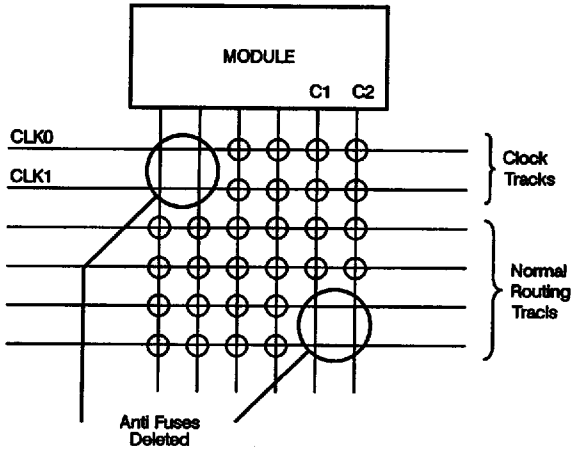



**Figure 11. Fuse Deletion on Clock Networks**

## Programming and Test Circuits

The array of logic and I/O modules is surrounded by test and programming circuits controlled by the external pins: MODE, SDI, DCLK. The function of these pins is summarized below. When MODE is low (GND), the device is in normal or user mode. When MODE is high (VCC), the device is placed into one of several programming or test states. The SDI pin (when MODE is high) is used to input serial data to the Mode register and various address registers surrounding the array. Data is clocked into these registers using the DCLK pin. The registers are connected as a long series of shift registers as shown in Figure 12. The Mode register determines the test or programming state of the device. Many of the test modes are used during wafer sort and final test at the factory. Other test modes are used during programming in the Activator® 2, and some of the modes are available only after programming. The Actionprobe® function is one such function available to users.

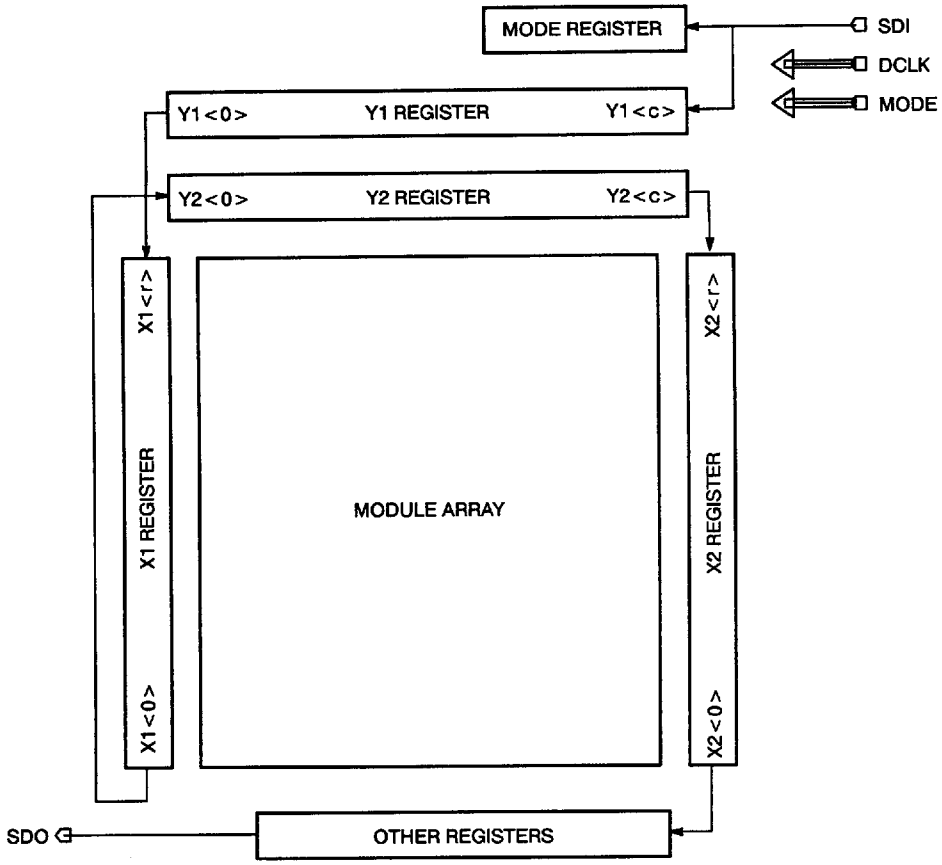



**Figure 12. ACT 2 Shift Register**

## Actionprobe

If a device has been successfully programmed and the security fuse has not been programmed, any internal logic or I/O module output can be observed using the Actionprobe circuitry and the PRA and/or PRB pins. The Actionprobe Diagnostic system provides the software and hardware required to perform real-time debugging. The software automatically performs the following functions.

A pattern of "1s" and "0s" is shifted into the device from the SDI pin at each positive edge transition of DCLK. The complete sequence contains 10 bits of counter, 21 bits of Mode Register, n bits of zeros (filler of unused fields, where n depends on the particular device type), R bits of X2, C bits of Y2, R bits of X1, C bits of Y1, and a stop bit ("0" or "1"). After the stop bit has been shifted in, DCLK is left high (see definitions below). X1 and Y1 represent the (X,Y) location in the array for the Actionprobe output, PRA.

X2 and Y2 represent the (X,Y) location in the array for the Actionprobe output, PRB. R and C are the row and column size as defined in Table 1. The filler bits, counter pattern, and Mode register pattern are shown in Table 3. Addressing for rows and columns is active high, i.e. unselected rows and columns are "zeros" and the selected row and column is "high." The timing sequence is shown in Figure 13. The recommended frequency is 10 MHz with 10 nS setup and hold times allowing for SDI and DCLK transitions. The selected module output will be present at the PRA or PRB output approximately 20 nS after the stop-bit transition.

**Table 3. Bit Stream Definitions for Actionprobe Diagnostics**

| Device | Probe_Mode | Filler (n) | Counter_Pattern | Mode_Register_Pattern | # of clocks |
|---|---|---|---|---|---|
| A1280 | Probe A only | 443 | 0011011111 | 00000011000111100000 | 675 |
| A1280 | Probe B only | 443 | 0011011111 | 00000010100111100000 | 675 |
| A1280 | Probe A and B | 443 | 0011011111 | 00000011100111100000 | 675 |
| A1240 | Probe A only | 361 | 1111000001 | 00000011000111100000 | 541 |
| A1240 | Probe B only | 361 | 1111000001 | 00000010100111100000 | 541 |
| A1240 | Probe A and B | 361 | 1111000001 | 00000011100111100000 | 541 |
| A1225 | Probe A only | 308 | 1101011010 | 00000011000111100000 | 458 |
| A1225 | Probe B only | 308 | 1101011010 | 00000010100111100000 | 458 |
| A1225 | Probe A and B | 308 | 1101011010 | 00000011100111100000 | 458 |

For Example: Selecting PRA for A1280 results in the following bit stream:

0011011111_00000011000111100000_
(443 zeros)_X2<0>...X2<17>_Y2<81>...Y2<0>_X1<0>...X1<0>...X1<17>_Y1<0>...Y1<81>_0,

where "_" is used for clarity only.

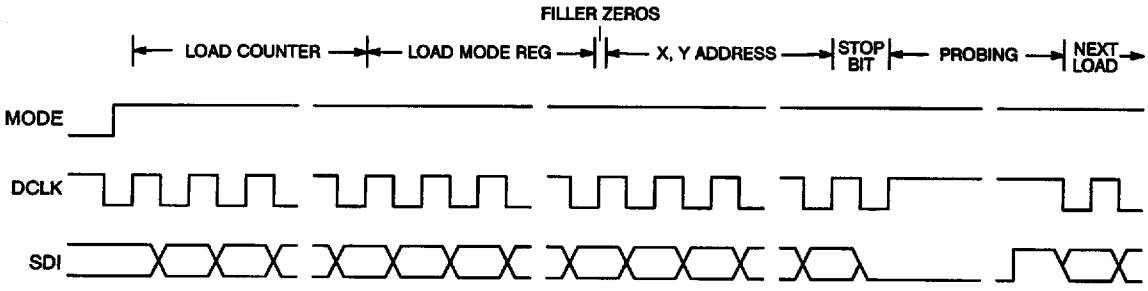
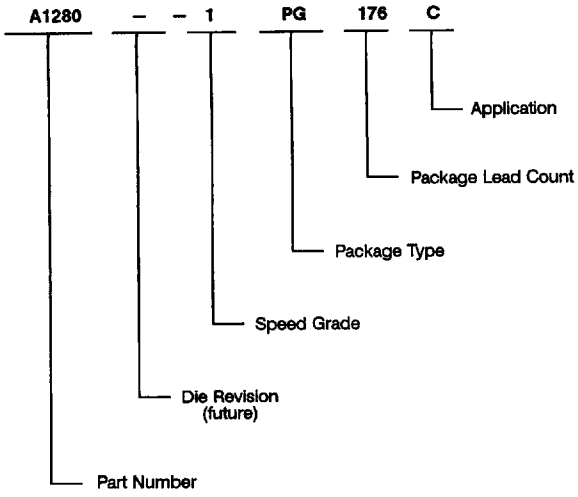



**Figure 13. Timing Waveforms**

## Ordering Information

T-46-19-11




## Product Plan

| | Speed Grade | | Application | | | | |
|---|---|---|---|---|---|---|---|
| | Std | –1* | C | I | M | B | E |
| **A1280 Device** | | | | | | | |
| 176-pin Ceramic Pin Grid Array (PG) | ✓ | ✓ | ✓ | – | ✓ | ✓ | – |
| 160-pin Plastic Quad Flatpack (PQ) | ✓ | ✓ | ✓ | ✓ | – | – | – |
| 172-pin Ceramic Quad Flatpack (CQ) | ✓ | P | ✓ | – | ✓ | ✓ | ✓ |
| **A1240 Device** | | | | | | | |
| 132-pin Ceramic Pin Grid Array (PG) | ✓ | ✓ | ✓ | – | ✓ | ✓ | – |
| 144-pin Plastic Quad Flatpack (PQ) | ✓ | ✓ | ✓ | ✓ | – | – | – |
| 84-pin Plastic Leaded Chip Carrier (PL) | ✓ | ✓ | ✓ | ✓ | – | – | – |
| **A1225 Device** | | | | | | | |
| 100-pin Ceramic Pin Grid Array (PG) | ✓ | ✓ | ✓ | – | – | – | – |
| 100-pin Plastic Quad Flatpack (PQ) | ✓ | ✓ | ✓ | ✓ | – | – | – |
| 84-pin Plastic Leaded Chip Carrier (PL) | ✓ | ✓ | ✓ | ✓ | – | – | – |

Applications: C = Commercial
I = Industrial
M = Military
B = 883B
E = Extended Flow

Availability: ✓ = Available
P = Planned
– = Not Planned

* Speed Grade: –1 = 15% faster than Standard

## Device Resources

| Device Series | Logic Modules | Gates | User I/Os | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | CPGA | | | PQFP | | | PLCC | CQFP |
| | | | 176-pin | 132-pin | 100-pin | 160-pin | 144-pin | 100-pin | 84-pin | 172-pin |
| A1280 | 1232 | 8000 | 140 | – | – | 125 | – | – | – | 140 |
| A1240 | 684 | 4000 | – | 104 | – | – | 104 | – | 72 | – |
| A1225 | 451 | 2500 | – | – | 83 | – | – | – | 72 | – |

## Pin Description

### CLKA Clock A (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

### CLKB Clock B (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

### DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### GND Ground (Input)

Input LOW supply voltage.

### I/O Input/Output (Input, Output)

I/O pins function as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

### MODE Mode (Input)

The MODE pin controls the use of multi-function pins (DCLK, PRA, PRB, SDI, SDO). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os.

### NC No Connection

This pin is not connected to circuitry within the device.

### PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### SDO Serial Data Output (Output)

Serial data output for diagnostic probe. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### $V_{CC}$ Supply Voltage (Input)

Input HIGH supply voltage.

### $V_{KS}$ Programming Voltage (Input)

Input supply voltage used for device programming. This pin must be connected to GND during normal operation.

### $V_{PP}$ Programming Voltage (Input)

Input supply voltage used for device programming. This pin must be connected to $V_{CC}$ during normal operation.

### $V_{SV}$ Programming Voltage (Input)

Input supply voltage used for device programming. This pin must be connected to $V_{CC}$ during normal operation.

## Absolute Maximum Ratings

Free air temperature range

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage[1,2,3] | -0.5 to +7.0 | Volts |
| $V_I$ | Input Voltage | -0.5 to $V_{CC}$ +0.5 | Volts |
| $V_O$ | Output Voltage | -0.5 to $V_{CC}$ +0.5 | Volts |
| $I_{IK}$ | Input Clamp Current | ±20 | mA |
| $I_{OK}$ | Output Clamp Current | ±20 | mA |
| $I_{OK}$ | Continuous Output Current | ±25 | mA |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |

Stresses beyond those listed above may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.

**Notes:**

1. $V_{PP} = V_{CC}$, except during device programming.
2. $V_{SV} = V_{CC}$, except during device programming.
3. $V_{KS}$ = GND, except during device programming.

## Recommended Operating Conditions

| Parameter | Commercial | Industrial | Military | Units |
|---|---|---|---|---|
| Temperature Range[1] | 0 to +70 | -40 to +85 | -55 to +125 | °C |
| Power Supply Tolerance | ±5 | ±10 | ±10 | %$V_{CC}$ |

**Note:**

1. Ambient temperature ($T_A$) used for commercial and industrial. Case temperature ($T_C$) used for military.

## Electrical Specifications

| Parameter | | Commercial | | Industrial | | Military | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $V_{OH}$[1] | ($I_{OH}$ = -10 mA)[2] | 2.4 | | | | | | V |
| | ($I_{OH}$ = -6 mA) | 3.84 | | | | | | V |
| | ($I_{OH}$ = -4 mA) | | | 3.7 | | 3.7 | | V |
| $V_{OL}$[1] | ($I_{OL}$ = 10 mA)[2] | | 0.5 | | | | | V |
| | ($I_{OL}$ = 6 mA) | | 0.33 | | 0.40 | | 0.40 | V |
| $V_{IL}$ | | -0.3 | 0.8 | -0.3 | 0.8 | -0.3 | 0.8 | V |
| $V_{IH}$ | | 2.0 | $V_{CC}$ + 0.3 | 2.0 | $V_{CC}$ + 0.3 | 2.0 | $V_{CC}$ + 0.3 | V |
| Input Transition Time $t_R$, $t_F$[2] | | | 500 | | 500 | | 500 | ns |
| $C_{IO}$ I/O Capacitance[2, 3] | | | 10 | | 10 | | 10 | pF |
| Standby Current, $I_{CC}$[4] | | | 10 | | 20 | | 25 | mA |
| Leakage Current[5] | | -10 | 10 | -10 | 10 | -10 | 10 | µA |

**Notes:**

1. Only one output tested at a time. $V_{CC}$ = min.
2. Not tested, for information only.
3. Includes worst-case 176 CPGA package capacitance. $V_{OUT}$ = 0 V, f = 1 MHz.
4. All outputs unloaded. All inputs = $V_{CC}$ or GND, typical $I_{CC}$ = 1 mA.
5. $V_O$, $V_{IN}$ = $V_{CC}$ or GND.

T-46-19-11

## Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the maximum power dissipation for a CPGA 176-pin package at commercial temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. military temp. (°C)}}{\theta ja\ (°C/W)} = \frac{150°C - 70°C}{20°C/W} = 4.0\ W$$

| Package Type | Pin Count | θjc | θja Still air | θja 300 ft/min. | Units |
|---|---|---|---|---|---|
| CPGA | 100 | 5 | 35 | 17 | °C/W |
| | 132 | 5 | 30 | 15 | °C/W |
| | 176 | 2 | 20 | 8 | °C/W |
| PQFP[1] | 100 | 13 | 55 | 47 | °C/W |
| | 144 | 15 | 35 | 26 | °C/W |
| | 160 | 15 | 33 | 24 | °C/W |
| PLCC | 84 | 12 | 44 | 33 | °C/W |

Note:
1. Maximum Power Dissipation for PQFP Package = 2.0 Watts

## Power Dissipation

$P = [I_{CC} + I_{active}] \cdot V_{CC} + I_{OL} \cdot V_{OL} \cdot N + I_{OH} \cdot (V_{CC} - V_{OH}) \cdot M$

Where:

$I_{CC}$ is the current flowing when no inputs or outputs are changing.

$I_{active}$ is the current flowing due to CMOS switching.

$I_{OL}$, $I_{OH}$ are TTL sink/source currents.

$V_{OL}$, $V_{OH}$ are TTL level output voltages.

N equals the number of outputs driving TTL loads to $V_{OL}$.

M equals the number of outputs driving TTL loads to $V_{OH}$.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

### Static Power

Static power dissipation is typically a small component of the overall power. From the values provided in the Electrical Specifications, the maximum static power (commercial) dissipation is:

10 mA x 5.25 V = 52.5 mW

The static power dissipated by TTL loads depends on the number of outputs that drive high or low and the DC lead current flowing. Again, this number is typically small. For instance, a 32-bit bus driving TTL loads will generate 42 mW ATT with all outputs driving low or 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

### Active Power

The active power component in CMOS devices is frequency dependent and depends on the user's logic and the external I/O. Active power dissipation results from charging internal chip capacitance such as that associated with the interconnect, unprogrammed antifuses, module inputs, and module outputs plus external capacitance due to PC board traces and load device inputs. An additional component of active power dissipation is due to totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

### Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1.

$$\text{Power}\ (\mu W) = C_{EQ} \cdot V_{CC}^2 \cdot f \qquad (1)$$

Where:

$C_{EQ}$ is the equivalent capacitance expressed in pF.

$V_{CC}$ is power supply in volts.

f is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring $I_{active}$ at a specified frequency and voltage for each circuit component of interest. The results for ACT 2 devices are:

| | $C_{EQ}$ (pF) |
|---|---|
| Modules | 7.7 |
| Input Buffers | 18.0 |
| Output Buffers | 25.0 |
| Clock Buffer Loads | 2.5 |

To calculate the active power that is dissipated from the complete design, you must solve Equation 1 for each component. In order to do this, you must know the switching frequency of each part of the logic. The exact equation is a piece-wise linear summation over all components, as shown in Equation 2.

$$\text{Power} = [(m \cdot 7.7 \cdot f_1) + (n \cdot 18.0 \cdot f_2) + (p \cdot (25.0 + C_L) \cdot f_3) + (q \cdot 2.5 \cdot f)] \cdot V_{CC}^2 \qquad (2)$$

Where:

n = Number of logic modules switching at frequency $f_1$

m = Number of input buffers switching at frequency $f_2$

p = Number of output buffers switching at frequency $f_3$

q = Number of clock loads on the global clock network

f = Frequency of global clock

$f_1$ = Average logic module switching rate in MHz

$f_2$ = Average input buffer switching rate in MHz

$f_3$ = Average output buffer switching rate in MHz

$C_L$ = Output load capacitance

### Determining Average Switching Frequency

In order to determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following rules will help you to determine average switching frequency in logic circuits. These rules are meant to represent worst-case scenarios so that they can be generally used for predicting the upper limits of power dissipation. These rules are as follows:

Module Utilization = 80% of combinatorial modules

Average Module Frequency = F/10

Inputs = 1/3 of I/O

Average Input Frequency = F/5

Outputs = 2/3 of I/Os

Average Output Frequency = F/10

Clock Net 1 Loading = 40% of sequential modules

Clock Net 1 Frequency = F

Clock Net 2 Loading = 40% of sequential modules

Clock Net 2 Frequency = F/2

### Estimated Power

T-46-19-11

The results of estimating active power are displayed in Figure 14. The graphs provide a simple guideline for estimating power. The tables may be interpolated when your application has different resource utilizations or frequencies.

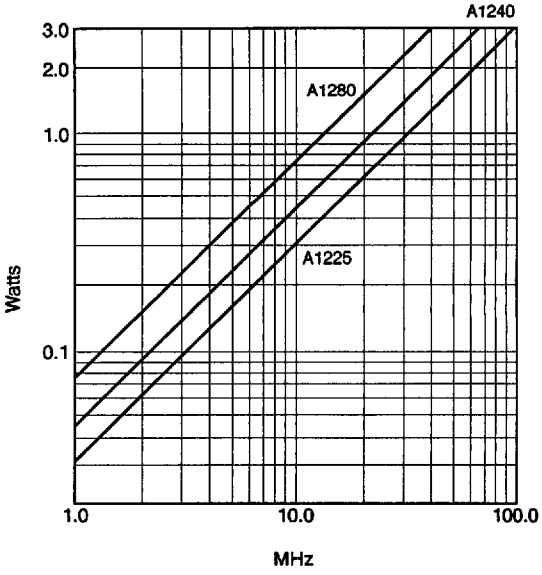



**Figure 14. ACT 2 Power Estimates**

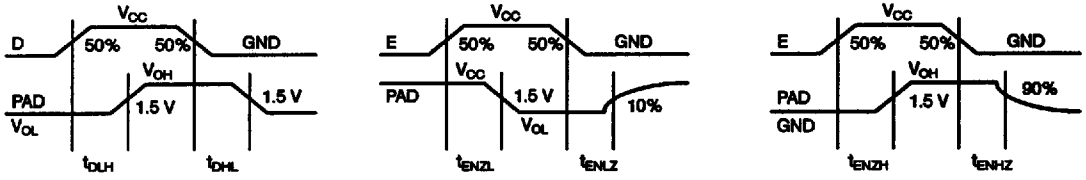
1

Actel

## Parameter Measurement

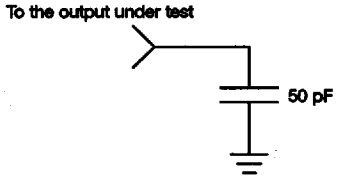
T-46-19-11

### Output Buffer Delays

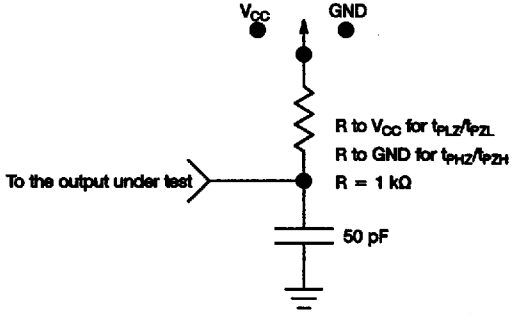




### AC Test Loads

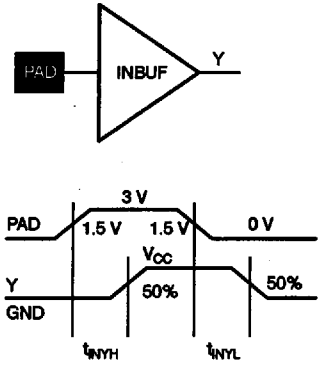
**Load 1**
**(Used to measure propagation delay)**



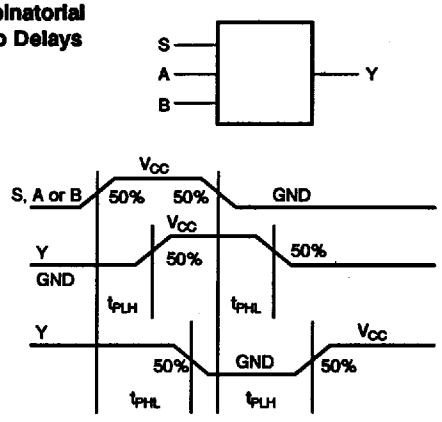

**Load 2**
**(Used to measure rising/falling edges)**




### Input Buffer Delays



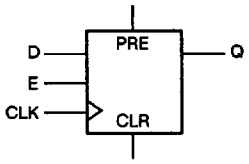

### Combinatorial Macro Delays



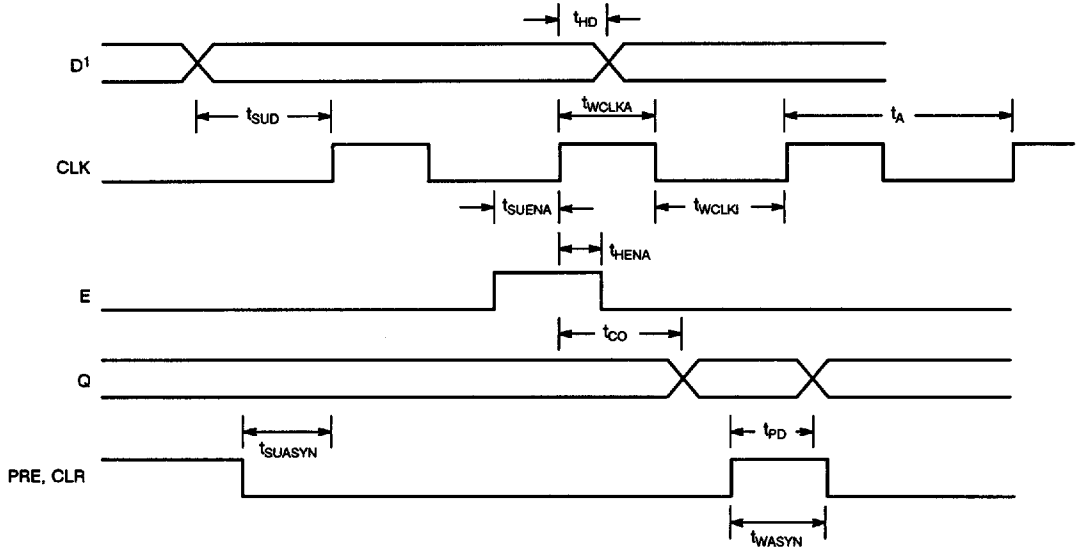
## Sequential Timing Characteristics

T-46-19-11

### Flip-Flops and Latches




(Positive edge triggered)



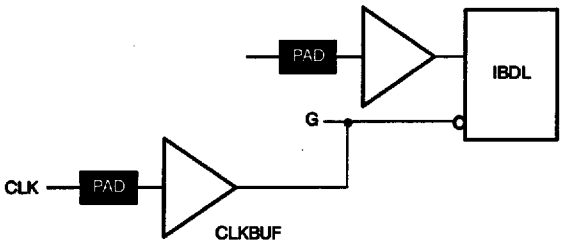

**Notes:**

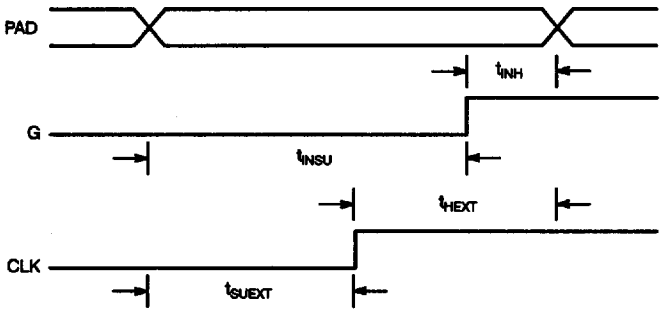
1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

## Sequential Timing Characteristics (continued)

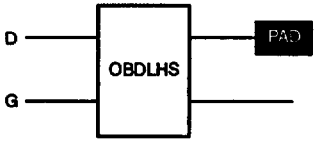
T-46-19-11

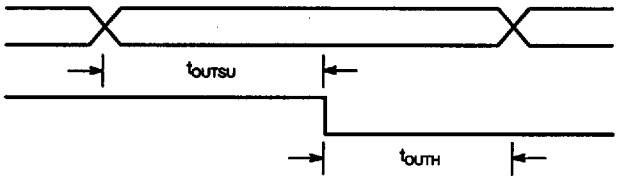
### Input Buffer Latches




### Output Buffer Latches



## Timing Characteristics

Timing characteristics for ACT arrays fall into three categories: family dependent, device dependent, and design dependent. The output buffer characteristics are common to all ACT 2 family members. Internal module delays are device dependent. Internal wiring delays between modules are design dependent. Design dependency means actual delays are not determined until after placement and routing of the users design is complete. Delay values may then be determined by using the ALS Timer utility or performing simulation with post-layout delays.

The macro propagation delays shown in the Timing Characteristics tables include the module delay plus estimates derived from statistical analysis for wiring delay. This statistical estimate is based on fully utilized devices (90% module utilization).

### Critical Nets and Typical Nets

Propagation delays are expressed for two types of nets: critical and typical. Critical nets are determined by net property assignment before placement and routing. Up to 6% of the nets in a design may be designated as *critical*, while 90% of the nets in a design are *typical*.

### Fan-Out Dependency

Propagation delays depend on the fan-out (number of loads) driven by a macro. Delay time increases when fan-out increases due to the capacitive loading of the macro's inputs, as well as the interconnect's resistance and capacitance.

### Long Tracks

T-46-19-11

Some nets in the design use *long tracks*. Long tracks are special routing resources that span multiple rows or columns or modules, and are used frequently in large fan-out ( > 10) situations. Long tracks employ three and sometimes four antifuse connections. This increased capacitance and resistance results in longer net delays for macros connected to long tracks. Typically up to 6% of the nets in a fully utilized device require long tracks. Long tracks contribute an additional 10 ns to 15 ns delay.

## Timing Derating

Operating temperature, operating voltage, and device processing conditions, along with device die size and speed grade, account for variations in array timing characteristics. These variations are summarized into a derating factor for ACT 2 array typical timing specifications. The derating factors shown in the table below are based on the recommended operating conditions for ACT 2 applications. The derating curves in Figure 15 show worst-to-best case operating voltage range and best-to-worst case operating temperature range. The temperature derating curve is based on device junction temperature. Actual junction temperature is determined from Ambient Temperature, Power Dissipation, and Package Thermal characteristics.

1

**Timing Derating Factor** (x typical)

| Commercial | | Industrial | | Military | |
|---|---|---|---|---|---|
| **Best-Case** | **Worst-Case** | **Best-Case** | **Worst-Case** | **Best-Case** | **Worst-Case** |
| 0.40 | 1.40 | 0.37 | 1.50 | 0.35 | 1.6 |

**Note:**
"Best-case" reflects maximum operating voltage, minimum operating temperature, and best-case processing. "Worst-case" reflects minimum operating voltage, maximum operating temperature, and worst-case processing. Best-case derating is based on sample data only and is not guaranteed.

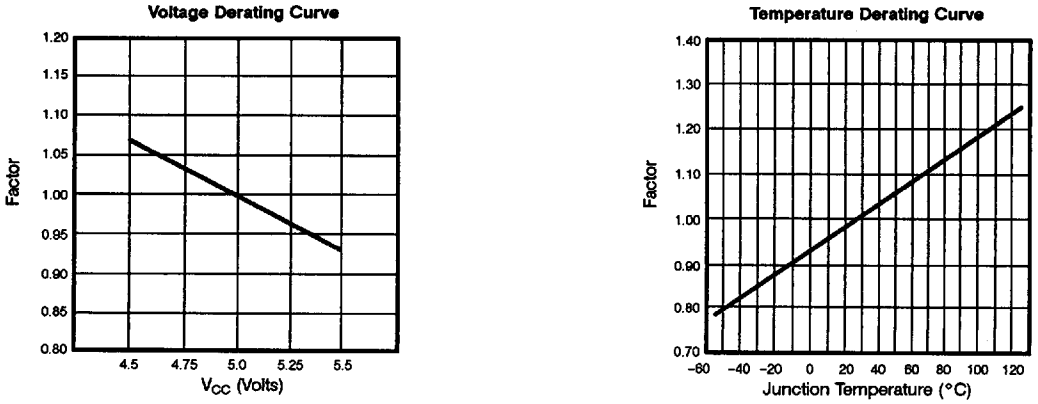



**Figure 15. Operating Curves**

## A1280 Timing Characteristics

T-46-19-11

**Propagation Delays** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | Output Net | FO = 1 | FO = 2 | FO = 3 | FO = 4 | FO = 8 | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PD1}$ | Single Module | Critical | 4.5 | 5.0 | 5.5 | 6.0 | – | ns |
| $t_{PD1}$ | Single Module | Typical | 5.7 | 6.2 | 6.7 | 8.2 | 11.7 | ns |
| $t_{PD2}$ | Dual Module | Critical | 7.5 | 8.0 | 8.5 | 9.0 | – | ns |
| $t_{PD2}$ | Dual Module | Typical | 8.7 | 9.2 | 9.7 | 11.2 | 14.7 | ns |
| $t_{CO}$ | Sequential Clk to Q | Critical | 4.5 | 5.0 | 5.5 | 6.0 | – | ns |
| $t_{CO}$ | Sequential Clk to Q | Typical | 5.7 | 6.2 | 6.7 | 8.2 | 11.7 | ns |
| $t_{GO}$ | Latch G to Q | Critical | 4.5 | 5.0 | 5.5 | 6.0 | – | ns |
| $t_{GO}$ | Latch G to Q | Typical | 5.7 | 6.2 | 6.7 | 8.2 | 11.7 | ns |
| $t_{PD}$ | Asynchronous to Q | Critical | 4.5 | 5.0 | 5.5 | 6.0 | – | ns |
| $t_{PD}$ | Asynchronous to Q | Typical | 5.7 | 6.2 | 6.7 | 8.2 | 11.7 | ns |

**Sequential Timing Characteristics** (Over Worst-Case Recommended Operating Conditions; No Further Derating Required)

| | | Commercial | | Industrial | | Military | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.5 | | 1.0 | | ns |
| $t_{SUASYN}$ | Flip-Flop (Latch) Asynchronous Input Setup | 1.0 | | 1.5 | | 2.0 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Setup | 1.0 | | 1.5 | | 2.0 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.0 | | 4.5 | | 5.0 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.0 | | 4.5 | | 5.0 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 18.0 | | 20.0 | | 22.0 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | | 2.0 | | 2.5 | | 2.5 | ns |
| $t_{INSU}$ | Input Buffer Latch Setup | -2.5 | | -3.0 | | -3.5 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{OUTSU}$ | Output Buffer Latch Setup | 0.4 | | 0.5 | | 1.0 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 48.0 | | 43.0 | | 39.0 | MHz |

**Notes:**

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## A1280 Timing Characteristics (continued)

T-46-19-11

**I/O Buffer Timing** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | FO = 1 | FO = 2 | FO = 3 | FO = 4 | FO = 8 | Units |
|---|---|---|---|---|---|---|---|
| $t_{INYH}$ | Pad to Y High | 6.7 | 7.2 | 7.7 | 8.2 | 11.7 | ns |
| $t_{INYL}$ | Pad to Y Low | 6.6 | 7.1 | 7.6 | 8.1 | 11.5 | ns |
| $t_{INGH}$ | G to Y High | 6.6 | 7.2 | 7.7 | 8.2 | 11.7 | ns |
| $t_{INGL}$ | G to Y Low | 6.4 | 6.9 | 7.5 | 8.0 | 11.4 | ns |

**Global Clock Network** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | FO = 32 | FO = 128 | FO =384 | Units |
|---|---|---|---|---|---|
| $t_{CKH}$ | Input Low to High | 9.1 | 10.1 | 12.3 | ns |
| $t_{CKL}$ | Input High to Low | 9.1 | 10.2 | 12.5 | ns |
| $t_{PWH}$ | Minimum Pulse Width High | 4.0 | 4.5 | 5.0 | ns |
| $t_{PWL}$ | Minimum Pulse Width Low | 4.0 | 4.5 | 5.0 | ns |
| $t_{CKSW}$ | Maximum Skew | 0.5 | 1.0 | 2.5 | ns |
| $t_{SUEXT}$ | Input Latch External Setup[1] | 0.0 | 0.0 | 0.0 | ns |
| $t_{HEXT}$ | Input Latch External Hold[1] | 7.0 | 8.0 | 11.2 | ns |
| $t_P$ | Minimum Period | 13.3 | 14.3 | 15.3 | ns |
| $f_{MAX}$ | Maximum Frequency | 75.0 | 70.0 | 65.0 | MHz |

**Note:**
1. Derating does not apply to this parameter.

**Output Buffer Timing** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | TTL | CMOS | Units |
|---|---|---|---|---|
| $t_{DLH}$ | Data to Pad High | 4.6 | 6.7 | ns |
| $t_{DHL}$ | Data to Pad Low | 6.5 | 4.9 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | 8.3 | 8.3 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | 5.5 | 5.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | 4.5 | 4.5 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | 6.0 | 6.0 | ns |
| $t_{GLH}$ | G to Pad High | 4.6 | 4.6 | ns |
| $t_{GHL}$ | G to Pad Low | 6.5 | 6.5 | ns |
| $d_{TLH}$ | Delta Low to High | 0.06 | 0.11 | ns/pF |
| $d_{THL}$ | Delta High to Low | 0.11 | 0.08 | ns/pF |

1

## A1280-1 Timing Characteristics

T-46-19-11

**Propagation Delays** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | Output Net | FO = 1 | FO = 2 | FO = 3 | FO = 4 | FO = 8 | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PD1}$ | Single Module | Critical Net | 3.9 | 4.3 | 4.8 | 5.3 | – | ns |
| $t_{PD1}$ | Single Module | Typical Net | 4.9 | 5.3 | 5.7 | 7.0 | 10.0 | ns |
| $t_{PD2}$ | Dual Module | Critical Net | 7.5 | 8.0 | 8.5 | 9.0 | – | ns |
| $t_{PD2}$ | Dual Module | Typical Net | 7.9 | 8.3 | 8.7 | 10.0 | 13.0 | ns |
| $t_{CO}$ | Sequential Clk to Q | Critical Net | 3.9 | 4.3 | 4.8 | 5.3 | – | ns |
| $t_{CO}$ | Sequential Clk to Q | Typical Net | 4.9 | 5.3 | 5.7 | 7.0 | 10.0 | ns |
| $t_{GO}$ | Latch G to Q | Critical Net | 3.9 | 4.3 | 4.8 | 5.3 | – | ns |
| $t_{GO}$ | Latch G to Q | Typical Net | 4.9 | 5.3 | 5.7 | 7.0 | 10.0 | ns |
| $t_{PD}$ | Asynchronous to Q | Critical | 3.9 | 4.3 | 4.8 | 5.3 | – | ns |
| $t_{PD}$ | Asynchronous to Q | Typical | 4.9 | 5.3 | 5.7 | 7.0 | 10.0 | ns |

**Sequential Timing Characteristics** (Over Worst-Case Recommended Operating Conditions; No Further Derating Required)

| | | Commercial | | Industrial | | Military | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.5 | | 1.0 | | ns |
| $t_{SUASYN}$ | Flip-Flop (Latch) Asynchronous Input Setup | 1.0 | | 1.5 | | 2.0 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Setup | 1.0 | | 1.5 | | 2.0 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.0 | | 4.5 | | 5.0 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.0 | | 4.5 | | 5.0 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 15.0 | | 18.0 | | 20.0 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | | 2.0 | | 2.5 | | 2.5 | ns |
| $t_{INSU}$ | Input Buffer Latch Setup | -2.5 | | -3.0 | | -3.5 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{OUTSU}$ | Output Buffer Latch Setup | 0.4 | | 0.5 | | 1.0 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 65.0 | | 60.0 | | 50.0 | MHz |

Notes:

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## A1280-1 Timing Characteristics (continued)

T-46-19-11

**I/O Buffer Timing** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | FO = 1 | FO = 2 | FO = 3 | FO = 4 | FO = 8 | Units |
|---|---|---|---|---|---|---|---|
| $t_{INYH}$ | Pad to Y High | 6.1 | 6.5 | 5.9 | 7.4 | 10.5 | ns |
| $t_{INYL}$ | Pad to Y Low | 5.9 | 6.4 | 6.8 | 7.3 | 10.4 | ns |
| $t_{INGH}$ | G to Y High | 6.1 | 6.5 | 5.9 | 7.4 | 10.5 | ns |
| $t_{INGL}$ | G to Y Low | 5.9 | 6.4 | 6.8 | 7.3 | 10.4 | ns |

**Global Clock Network** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | FO = 32 | FO = 128 | FO = 384 | Units |
|---|---|---|---|---|---|
| $t_{CKH}$ | Input Low to High | 7.8 | 8.7 | 10.4 | ns |
| $t_{CKL}$ | Input High to Low | 7.8 | 8.8 | 10.6 | ns |
| $t_{PWH}$ | Minimum Pulse Width High | 4.0 | 4.5 | 5.0 | ns |
| $t_{PWL}$ | Minimum Pulse Width Low | 4.0 | 4.5 | 5.0 | ns |
| $t_{CKSW}$ | Maximum Skew | 0.5 | 1.0 | 2.5 | ns |
| $t_{SUEXT}$ | Input Latch External Setup[1] | 0.0 | 0.0 | 0.0 | ns |
| $t_{HEXT}$ | Input Latch External Hold[1] | 7.0 | 8.0 | 11.2 | ns |
| $t_P$ | Minimum Period | 11.4 | 12.0 | 13.0 | ns |
| $f_{MAX}$ | Maximum Frequency | 89.0 | 83.0 | 77.0 | MHz |

**Note:**
1. Derating does not apply to this parameter.

1

**Output Buffer Timing** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | TTL | CMOS | Units |
|---|---|---|---|---|
| $t_{DLH}$ | Data to Pad High | 4.6 | 6.7 | ns |
| $t_{DHL}$ | Data to Pad Low | 6.5 | 4.9 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | 8.3 | 8.3 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | 5.5 | 5.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | 4.5 | 4.5 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | 6.0 | 6.0 | ns |
| $t_{GLH}$ | G to Pad High | 4.6 | 4.6 | ns |
| $t_{GHL}$ | G to Pad Low | 6.5 | 6.5 | ns |
| $d_{TLH}$ | Delta Low to High | 0.06 | 0.11 | ns/pF |
| $d_{THL}$ | Delta High to Low | 0.11 | 0.08 | ns/pF |

## A1240 Timing Characteristics

**PRELIMINARY DATA**

**Propagation Delays** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | Output Net | FO = 1 | FO = 2 | FO = 3 | FO = 4 | FO = 8 | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PD1}$ | Single Module | Critical Net | 3.9 | 4.3 | 4.8 | 5.3 | – | ns |
| $t_{PD1}$ | Single Module | Typical Net | 4.9 | 5.3 | 5.7 | 7.0 | 10.0 | ns |
| $t_{PD2}$ | Dual Module | Critical Net | 7.5 | 8.0 | 8.5 | 9.0 | – | ns |
| $t_{PD2}$ | Dual Module | Typical Net | 7.9 | 8.3 | 8.7 | 10.0 | 13.0 | ns |
| $t_{CO}$ | Sequential Clk to Q | Critical Net | 3.9 | 4.3 | 4.8 | 5.3 | – | ns |
| $t_{CO}$ | Sequential Clk to Q | Typical Net | 4.9 | 5.3 | 5.7 | 7.0 | 10.0 | ns |
| $t_{GO}$ | Latch G to Q | Critical Net | 3.9 | 4.3 | 4.8 | 5.3 | – | ns |
| $t_{GO}$ | Latch G to Q | Typical Net | 4.9 | 5.3 | 5.7 | 7.0 | 10.0 | ns |
| $t_{PD}$ | Asynchronous to Q | Critical | 3.9 | 4.3 | 4.8 | 5.3 | – | ns |
| $t_{PD}$ | Asynchronous to Q | Typical | 4.9 | 5.3 | 5.7 | 7.0 | 10.0 | ns |

**Sequential Timing Characteristics** (Over Worst-Case Recommended Operating Conditions; No Further Derating Required)

| | | Commercial | | Industrial | | Military | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.5 | | 1.0 | | ns |
| $t_{SUASYN}$ | Flip-Flop (Latch) Asynchronous Input Setup | 1.0 | | 1.5 | | 2.0 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Setup | 1.0 | | 1.5 | | 2.0 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.0 | | 4.5 | | 5.0 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.0 | | 4.5 | | 5.0 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 15.0 | | 18.0 | | 20.0 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | | 2.0 | | 2.5 | | 2.5 | ns |
| $t_{INSU}$ | Input Buffer Latch Setup | -2.5 | | -3.0 | | -3.5 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{OUTSU}$ | Output Buffer Latch Setup | 0.4 | | 0.5 | | 1.0 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 66.0 | | 55.0 | | 50.0 | MHz |

Notes:

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## A1240 Timing Characteristics (continued)

PRELIMINARY DATA

**I/O Buffer Timing** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | FO = 1 | FO = 2 | FO = 3 | FO = 4 | FO = 8 | Units |
|---|---|---|---|---|---|---|---|
| $t_{INYH}$ | Pad to Y High | 6.1 | 6.5 | 5.9 | 7.4 | 10.5 | ns |
| $t_{INYL}$ | Pad to Y Low | 5.9 | 6.4 | 6.8 | 7.3 | 10.4 | ns |
| $t_{INGH}$ | G to Y High | 6.1 | 6.5 | 5.9 | 7.4 | 10.5 | ns |
| $t_{INGL}$ | G to Y Low | 5.9 | 6.4 | 6.8 | 7.3 | 10.4 | ns |

**Global Clock Network** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | FO = 32 | FO = 128 | FO =256 | Units |
|---|---|---|---|---|---|
| $t_{CKH}$ | Input Low to High | 9.1 | 10.1 | 11.2 | ns |
| $t_{CKL}$ | Input High to Low | 9.1 | 10.2 | 11.3 | ns |
| $t_{PWH}$ | Minimum Pulse Width High | 4.0 | 4.5 | 5.0 | ns |
| $t_{PWL}$ | Minimum Pulse Width Low | 4.0 | 4.5 | 5.0 | ns |
| $t_{CKSW}$ | Maximum Skew | 0.5 | 1.0 | 2.5 | ns |
| $t_{SUEXT}$ | Input Latch External Setup[1] | 0.0 | 0.0 | 0.0 | ns |
| $t_{HEXT}$ | Input Latch External Hold[1] | 7.0 | 8.0 | 11.2 | ns |
| $t_P$ | Minimum Period | 11.1 | 11.5 | 11.8 | ns |
| $f_{MAX}$ | Maximum Frequency | 90.0 | 87.0 | 85.0 | MHz |

Note:
1. Derating does not apply to this parameter.

**Output Buffer Timing** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | TTL | CMOS | Units |
|---|---|---|---|---|
| $t_{DLH}$ | Data to Pad High | 4.6 | 6.7 | ns |
| $t_{DHL}$ | Data to Pad Low | 6.5 | 4.9 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | 8.3 | 8.3 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | 5.5 | 5.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | 4.5 | 4.5 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | 6.0 | 6.0 | ns |
| $t_{GLH}$ | G to Pad High | 4.6 | 4.6 | ns |
| $t_{GHL}$ | G to Pad Low | 6.5 | 6.5 | ns |
| $d_{TLH}$ | Delta Low to High | 0.06 | 0.11 | ns/pF |
| $d_{THL}$ | Delta High to Low | 0.11 | 0.08 | ns/pF |

## A1240-1 Timing Characteristics

**PRELIMINARY DATA**

**Propagation Delays** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | Output Net | FO = 1 | FO = 2 | FO = 3 | FO = 4 | FO = 8 | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PD1}$ | Single Module | Critical Net | 3.5 | 3.9 | 4.3 | 4.8 | – | ns |
| $t_{PD1}$ | Single Module | Typical Net | 4.4 | 4.8 | 5.1 | 6.3 | 9.0 | ns |
| $t_{PD2}$ | Dual Module | Critical Net | 7.5 | 8.0 | 8.5 | 9.0 | – | ns |
| $t_{PD2}$ | Dual Module | Typical Net | 7.4 | 7.8 | 8.1 | 9.3 | 12.0 | ns |
| $t_{CO}$ | Sequential Clk to Q | Critical Net | 3.5 | 3.9 | 4.3 | 4.8 | – | ns |
| $t_{CO}$ | Sequential Clk to Q | Typical Net | 4.4 | 4.8 | 5.1 | 6.3 | 9.0 | ns |
| $t_{GO}$ | Latch G to Q | Critical Net | 3.5 | 3.9 | 4.3 | 4.8 | – | ns |
| $t_{GO}$ | Latch G to Q | Typical Net | 4.4 | 4.8 | 5.1 | 6.3 | 9.0 | ns |
| $t_{PD}$ | Asynchronous to Q | Critical | 3.5 | 3.9 | 4.3 | 4.8 | – | ns |
| $t_{PD}$ | Asynchronous to Q | Typical | 4.4 | 4.8 | 5.1 | 6.3 | 9.0 | ns |

**Sequential Timing Characteristics** (Over Worst-Case Recommended Operating Conditions; No Further Derating Required)

| | | Commercial | | Industrial | | Military | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.5 | | 1.0 | | ns |
| $t_{SUASYN}$ | Flip-Flop (Latch) Asynchronous Input Setup | 1.0 | | 1.5 | | 2.0 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Setup | 1.0 | | 1.5 | | 2.0 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.0 | | 4.5 | | 5.0 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.0 | | 4.5 | | 5.0 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 13.0 | | 15.0 | | 18.0 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | | 2.0 | | 2.5 | | 2.5 | ns |
| $t_{INSU}$ | Input Buffer Latch Setup | -2.5 | | -3.0 | | -3.5 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{OUTSU}$ | Output Buffer Latch Setup | 0.4 | | 0.5 | | 1.0 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 75.0 | | 66.0 | | 55.0 | MHz |

**Notes:**

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## A1240-1 Timing Characteristics (continued)

PRELIMINARY DATA

**I/O Buffer Timing** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | FO = 1 | FO = 2 | FO = 3 | FO = 4 | FO = 8 | Units |
|---|---|---|---|---|---|---|---|
| $t_{INYH}$ | Pad to Y High | 5.5 | 5.9 | 5.3 | 6.7 | 9.5 | ns |
| $t_{INYL}$ | Pad to Y Low | 5.3 | 5.8 | 6.1 | 6.6 | 9.4 | ns |
| $t_{INGH}$ | G to Y High | 5.5 | 5.9 | 5.3 | 6.7 | 9.5 | ns |
| $t_{INGL}$ | G to Y Low | 5.3 | 5.8 | 6.1 | 6.6 | 9.4 | ns |

**Global Clock Network** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | FO = 32 | FO = 128 | FO =256 | Units |
|---|---|---|---|---|---|
| $t_{CKH}$ | Input Low to High | 7.8 | 8.7 | 9.3 | ns |
| $t_{CKL}$ | Input High to Low | 7.8 | 8.8 | 9.4 | ns |
| $t_{PWH}$ | Minimum Pulse Width High | 4.0 | 4.5 | 5.0 | ns |
| $t_{PWL}$ | Minimum Pulse Width Low | 4.0 | 4.5 | 5.0 | ns |
| $t_{CKSW}$ | Maximum Skew | 0.5 | 1.0 | 2.5 | ns |
| $t_{SUEXT}$ | Input Latch External Setup[1] | 0.0 | 0.0 | 0.0 | ns |
| $t_{HEXT}$ | Input Latch External Hold[1] | 7.0 | 8.0 | 11.2 | ns |
| $t_P$ | Minimum Period | 9.1 | 19.5 | 10.0 | ns |
| $f_{MAX}$ | Maximum Frequency | 110.0 | 105.0 | 100.0 | MHz |

Note:
1. Derating does not apply to this parameter.

**Output Buffer Timing** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | TTL | CMOS | Units |
|---|---|---|---|---|
| $t_{DLH}$ | Data to Pad High | 4.6 | 6.7 | ns |
| $t_{DHL}$ | Data to Pad Low | 6.5 | 4.9 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | 8.3 | 8.3 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | 5.5 | 5.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | 4.5 | 4.5 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | 6.0 | 6.0 | ns |
| $t_{GLH}$ | G to Pad High | 4.6 | 4.6 | ns |
| $t_{GHL}$ | G to Pad Low | 6.5 | 6.5 | ns |
| $d_{TLH}$ | Delta Low to High | 0.06 | 0.11 | ns/pF |
| $d_{THL}$ | Delta High to Low | 0.11 | 0.08 | ns/pF |

Actel

T-46-19-11

## A1225 Timing Characteristics

**PRELIMINARY DATA**

**Propagation Delays** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | Output Net | FO = 1 | FO = 2 | FO = 3 | FO = 4 | FO = 8 | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PD1}$ | Single Module | Critical Net | 3.9 | 4.3 | 4.8 | 5.3 | – | ns |
| $t_{PD1}$ | Single Module | Typical Net | 4.9 | 5.3 | 5.7 | 7.0 | 10.0 | ns |
| $t_{PD2}$ | Dual Module | Critical Net | 7.5 | 8.0 | 8.5 | 9.0 | – | ns |
| $t_{PD2}$ | Dual Module | Typical Net | 7.9 | 8.3 | 8.7 | 10.0 | 13.0 | ns |
| $t_{CO}$ | Sequential Clk to Q | Critical Net | 3.9 | 4.3 | 4.8 | 5.3 | – | ns |
| $t_{CO}$ | Sequential Clk to Q | Typical Net | 4.9 | 5.3 | 5.7 | 7.0 | 10.0 | ns |
| $t_{GO}$ | Latch G to Q | Critical Net | 3.9 | 4.3 | 4.8 | 5.3 | – | ns |
| $t_{GO}$ | Latch G to Q | Typical Net | 4.9 | 5.3 | 5.7 | 7.0 | 10.0 | ns |
| $t_{PD}$ | Asynchronous to Q | Critical | 3.9 | 4.3 | 4.8 | 5.3 | – | ns |
| $t_{PD}$ | Asynchronous to Q | Typical | 4.9 | 5.3 | 5.7 | 7.0 | 10.0 | ns |

**Sequential Timing Characteristics** (Over Worst-Case Recommended Operating Conditions; No Further Derating Required)

| | | Commercial | | Industrial | | |
|---|---|---|---|---|---|---|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.5 | | ns |
| $t_{SUASYN}$ | Flip-Flop (Latch) Asynchronous Input Setup | 1.0 | | 1.5 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | | 0.0 | | 0.0 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Setup | 1.0 | | 1.5 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | | 0.0 | | 0.0 | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.0 | | 4.5 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.0 | | 4.5 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 13.0 | | 15.0 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | | 2.0 | | 2.5 | ns |
| $t_{INSU}$ | Input Buffer Latch Setup | -2.5 | | -3.0 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | | 0.0 | | 0.0 | ns |
| $t_{OUTSU}$ | Output Buffer Latch Setup | 0.4 | | 0.5 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 75.0 | | 66.0 | MHz |

Notes:

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## A1225 Timing Characteristics (continued)

**I/O Buffer Timing** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | FO = 1 | FO = 2 | FO = 3 | FO = 4 | FO = 8 | Units |
|---|---|---|---|---|---|---|---|
| $t_{INYH}$ | Pad to Y High | 6.1 | 6.5 | 5.9 | 7.4 | 10.5 | ns |
| $t_{INYL}$ | Pad to Y Low | 5.9 | 6.4 | 6.8 | 7.3 | 10.4 | ns |
| $t_{INGH}$ | G to Y High | 6.1 | 6.5 | 5.9 | 7.4 | 10.5 | ns |
| $t_{INGL}$ | G to Y Low | 5.9 | 6.4 | 6.8 | 7.3 | 10.4 | ns |

**Global Clock Network** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | FO = 32 | FO = 128 | FO = 256 | Units |
|---|---|---|---|---|---|
| $t_{CKH}$ | Input Low to High | 7.8 | 8.7 | 9.3 | ns |
| $t_{CKL}$ | Input High to Low | 7.8 | 8.8 | 9.4 | ns |
| $t_{PWH}$ | Minimum Pulse Width High | 4.5 | 5.1 | 5.5 | ns |
| $t_{PWL}$ | Minimum Pulse Width Low | 4.5 | 5.1 | 5.5 | ns |
| $t_{CKSW}$ | Maximum Skew | 0.5 | 1.0 | 2.5 | ns |
| $t_{SUEXT}$ | Input Latch External Setup[1] | 0.0 | 0.0 | 0.0 | ns |
| $t_{HEXT}$ | Input Latch External Hold[1] | 7.0 | 8.0 | 11.2 | ns |
| $t_P$ | Minimum Period | 9.1 | 9.5 | 10.0 | ns |
| $f_{MAX}$ | Maximum Frequency | 110.0 | 105.0 | 100.0 | MHz |

Note:
1. Derating does not apply to this parameter.

**Output Buffer Timing** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | TTL | CMOS | Units |
|---|---|---|---|---|
| $t_{DLH}$ | Data to Pad High | 4.6 | 6.7 | ns |
| $t_{DHL}$ | Data to Pad Low | 6.5 | 4.9 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | 8.3 | 8.3 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | 5.5 | 5.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | 4.5 | 4.5 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | 6.0 | 6.0 | ns |
| $t_{GLH}$ | G to Pad High | 4.6 | 4.6 | ns |
| $t_{GHL}$ | G to Pad Low | 6.5 | 6.5 | ns |
| $d_{TLH}$ | Delta Low to High | 0.06 | 0.11 | ns/pF |
| $d_{THL}$ | Delta High to Low | 0.11 | 0.08 | ns/pF |

## A1225-1 Timing Characteristics

**PRELIMINARY DATA**

**Propagation Delays** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | Output Net | FO = 1 | FO = 2 | FO = 3 | FO = 4 | FO = 8 | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PD1}$ | Single Module | Critical Net | 3.5 | 3.9 | 4.3 | 4.8 | – | ns |
| $t_{PD1}$ | Single Module | Typical Net | 4.4 | 4.8 | 5.1 | 6.3 | 9.0 | ns |
| $t_{PD2}$ | Dual Module | Critical Net | 7.5 | 8.0 | 8.5 | 9.0 | – | ns |
| $t_{PD2}$ | Dual Module | Typical Net | 7.4 | 7.8 | 8.1 | 9.3 | 12.0 | ns |
| $t_{CO}$ | Sequential Clk to Q | Critical Net | 3.5 | 3.9 | 4.3 | 4.8 | – | ns |
| $t_{CO}$ | Sequential Clk to Q | Typical Net | 4.4 | 4.8 | 5.1 | 6.3 | 9.0 | ns |
| $t_{GO}$ | Latch G to Q | Critical Net | 3.5 | 3.9 | 4.3 | 4.8 | – | ns |
| $t_{GO}$ | Latch G to Q | Typical Net | 4.4 | 4.8 | 5.1 | 6.3 | 9.0 | ns |
| $t_{PD}$ | Asynchronous to Q | Critical | 3.5 | 3.9 | 4.3 | 4.8 | – | ns |
| $t_{PD}$ | Asynchronous to Q | Typical | 4.4 | 4.8 | 5.1 | 6.3 | 9.0 | ns |

**Sequential Timing Characteristics** (Over Worst-Case Recommended Operating Conditions; No Further Derating Required)

| | | Commercial | | Industrial | | |
|---|---|---|---|---|---|---|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.5 | | ns |
| $t_{SUASYN}$ | Flip-Flop (Latch) Asynchronous Input Setup | 1.0 | | 1.5 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | | 0.0 | | 0.0 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Setup | 1.0 | | 1.5 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | | 0.0 | | 0.0 | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.0 | | 4.5 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.0 | | 4.5 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 11.7 | | 13.3 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | | 2.0 | | 2.5 | ns |
| $t_{INSU}$ | Input Buffer Latch Setup | -2.5 | | -3.0 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | | 0.0 | | 0.0 | ns |
| $t_{OUTSU}$ | Output Buffer Latch Setup | 0.4 | | 0.5 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 85.0 | | 75.0 | MHz |

Notes:

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## A1225-1 Timing Characteristics (continued)

PRELIMINARY DATA

**I/O Buffer Timing** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | FO = 1 | FO = 2 | FO = 3 | FO = 4 | FO = 8 | Units |
|---|---|---|---|---|---|---|---|
| $t_{INYH}$ | Pad to Y High | 5.5 | 5.9 | 5.3 | 6.7 | 9.5 | ns |
| $t_{INYL}$ | Pad to Y Low | 5.3 | 5.8 | 6.1 | 6.6 | 9.4 | ns |
| $t_{INGH}$ | G to Y High | 5.5 | 5.9 | 5.3 | 6.7 | 9.5 | ns |
| $t_{INGL}$ | G to Y Low | 5.3 | 5.8 | 6.1 | 6.6 | 9.4 | ns |

**Global Clock Network** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | FO = 32 | FO = 128 | FO =256 | Units |
|---|---|---|---|---|---|
| $t_{CKH}$ | Input Low to High | 7.0 | 7.8 | 8.6 | ns |
| $t_{CKL}$ | Input High to Low | 7.0 | 7.8 | 8.6 | ns |
| $t_{PWH}$ | Minimum Pulse Width High | 4.2 | 4.5 | 5.0 | ns |
| $t_{PWL}$ | Minimum Pulse Width Low | 4.2 | 4.5 | 5.0 | ns |
| $t_{CKSW}$ | Maximum Skew | 0.5 | 1.0 | 2.5 | ns |
| $t_{SUEXT}$ | Input Latch External Setup[1] | 0.0 | 0.0 | 0.0 | ns |
| $t_{HEXT}$ | Input Latch External Hold[1] | 7.0 | 8.0 | 11.2 | ns |
| $t_P$ | Minimum Period | 8.3 | 8.7 | 9.1 | ns |
| $f_{MAX}$ | Maximum Frequency | 120.0 | 115.0 | 110.0 | MHz |

**Note:**
1. Derating does not apply to this parameter.

**Output Buffer Timing** ($V_{CC}$ = 5.0 V; $T_J$ = 25°C; Process = Typical; Derating Required)

| Parameter | Description | TTL | CMOS | Units |
|---|---|---|---|---|
| $t_{DLH}$ | Data to Pad High | 4.6 | 6.7 | ns |
| $t_{DHL}$ | Data to Pad Low | 6.5 | 4.9 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | 8.3 | 8.3 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | 5.5 | 5.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | 4.5 | 4.5 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | 6.0 | 6.0 | ns |
| $t_{GLH}$ | G to Pad High | 4.6 | 4.6 | ns |
| $t_{GHL}$ | G to Pad Low | 6.5 | 6.5 | ns |
| $d_{TLH}$ | Delta Low to High | 0.06 | 0.11 | ns/pF |
| $d_{THL}$ | Delta High to Low | 0.11 | 0.08 | ns/pF |

T-46-19-11

## Macro Library

### Overview

The following tables describe ACT 2 macros, which are building blocks for designing FPGAs with the ALS and your CAE interface.

The macros are divided into four categories: I/O Macros, Hard Macros (Combinable and Non-Combinable), Soft Macros, and TTL Macros.

### Equation Statement Elements

#### Combinatorial Elements

All equations for combinatorial logic elements use the following operators:

| Operator | Symbol |
|---|---|
| AND | See Note 1 |
| NOT | ! |
| OR | + |
| XOR | ^ |

Notes:
1. A space between the 'A' and 'B' in the equation Y = A B means A AND B.
2. Order of operators in decreasing precedence is: NOT, AND, XOR, and OR.
3. Signals expressed in bold have a dual module delay.

#### Sequential Elements

All equations for sequential logic elements use the following formula:

**Q = <!> (<!> CLK or G, <data equation>, <!> CLR, <!> PRE)**

| | |
|---|---|
| <!> | Optional Inversion |
| CLK | Flip-Flop Clock Pin |
| G | Latch Gate Pin |
| CLR | Asynchronous Clear Pin |
| PRE | Asynchronous Preset Pin |

## ACT 2 Macro Selections

### I/O Macros

| Macro Name | No. of Modules | | Description |
|---|---|---|---|
| | I/O | Clock | |
| INBUF | 1 | | Input |
| IBDL | 1 | | Input with Input Latch |
| BBDLHS | 1 | | Bidirectional with Input Latch and Output Latch |
| BBHS | 1 | | Bidirectional |
| BIBUF | 1 | | Bidirectional |
| CLKBIBUF | 1 | 1 | Bidirectional with Input Dedicated to Clock Network |
| CLKBUF | 1 | 1 | Input for Dedicated Clock Network |
| OBDLHS | 1 | | Output with Output Latch |
| OBHS | 1 | | Output |
| OUTBUF | 1 | | Output |
| TBDLHS | 1 | | Three State Output with Latch |
| TBHS | 1 | | Three State Output |
| TRIBUFF | 1 | | Three State Output |

Note:
The following are functionally identical:
OBHS and OUTBUF; TRIBUFF and TBHS; BBHS and BIBUF.

T-46-19-11

## TTL Macros

| Macro Name | Description | Logic Levels | No. of Modules | |
|---|---|---|---|---|
| | | | Seq. | Comb. |
| TA00 | 2-input NAND | 1 | | 1 |
| TA02 | 2-input NOR | 1 | | 1 |
| TA04 | Inverter | 1 | | 1 |
| TA07 | Buffer | 1 | | 1 |
| TA08 | 2-input AND | 1 | | 1 |
| TA10 | 3-input NAND | 1 | | 1 |
| TA11 | 3-input AND | 1 | | 1 |
| TA20 | 4-input NAND | 1 | | 2 |
| TA21 | 4-input AND | 1 | | 1 |
| TA27 | 3-input NOR | 1 | | 1 |
| TA32 | 2-input OR | 1 | | 1 |
| TA40 | 4-input NAND | 1 | | 2 |
| TA42 | 4 to 10 decoder | 1 | | 10 |
| TA51 | AND-OR-Invert | 1 | | 2 |
| TA54 | 4-wide AND-OR-Invert | 2 | | 5 |
| TA55 | 2-wide 4-input AND-OR-Invert | 2 | | 3 |
| TA86 | 2-Input exclusive OR | 1 | | 1 |
| TA138 | 3 to 8 decoder with enable and active low outputs | 2 | | 12 |
| TA139 | 2 to 4 decoder with enable and active low outputs | 1 | | 4 |
| TA150 | 16 to 1 multiplexor | 3 | | 6 |
| TA151 | 8 to 1 multiplexor with enable and active low outputs | 3 | | 5 |
| TA153 | 4 to 1 multiplexor | 2 | | 2 |
| TA154 | 4 to 16 decoder | 2 | | 22 |
| TA157 | 2 to 1 multiplexor | 1 | | 1 |
| TA160 | 4-bit decode counter with clear | 4 | 4 | 12 |
| TA161 | 4-bit binary counter with clear | 3 | 4 | 10 |
| TA164 | 8-bit serial in, parallel out shift register | 1 | 8 | |
| TA169 | 4-bit up/down counter | 6 | 4 | 14 |
| TA174 | Hex D-type flip-flop with clear | 1 | 6 | |
| TA175 | Quadruple D-type flip-flop with clear | 1 | 4 | |
| TA190 | 4-bit up/down decode counter with up/down mode | 7 | 4 | 31 |
| TA191 | 4-bit up/down binary counter with up/down mode | 7 | 4 | 30 |
| TA194 | 4-bit shift register | 1 | 4 | 4 |
| TA195 | 4-bit shift register | 1 | 4 | 1 |
| TA269 | 8-bit up/down binary counter | 8 | 8 | 28 |
| TA273 | Octal register with clear | 1 | 8 | |
| TA280 | Parity generator and checker | 4 | | 9 |
| TA377 | Octel register with active low enable | 1 | 8 | |
| TA688 | 8-bit identity comparator | 3 | | 9 |

1

## Soft Macros

T-46-19-11

| Function | Description | Macro Name | Logic Levels | No. of Modules | |
|---|---|---|---|---|---|
| | | | | Seq. | Comb. |
| Counters | 4-bit binary counter with load, clear | CNT4A | 4 | 4 | 8 |
| | 4-bit binary counter with load, clear, carry in, carry out | CNT4B | 4 | 4 | 7 |
| | 4-bit up/down counter with load, carry in, and carry out | UDCNT4A | 5 | 4 | 13 |
| | very fast 16-bit down counter | VCNT16C | 1 | 34 | 31 |
| | 2-bit down counter, prescaler | VCNT2CP | 1 | 5 | 2 |
| | 2-bit down counter, most significant bit | VCNT2CU | 1 | 2 | 3 |
| | 4-bit down counter, middle bits | VCNT4C | 1 | 4 | 8 |
| | 4-bit down counter, low order bits | VCNT4CL | 1 | 4 | 7 |
| Decoders | 2 to 4 decoder | DEC2X4 | 1 | | 4 |
| | 2 to 4 decoder with active low outputs | DEC2X4A | 1 | | 4 |
| | 3 to 8 decoder | DEC3X8 | 1 | | 8 |
| | 3 to 8 decoder with active low outputs | DEC3X8A | 1 | | 8 |
| | 4 to 16 decoder with active low outputs | DEC4X16A | 2 | | 20 |
| | 2 to 4 decoder with enable | DECE2X4 | 1 | | 4 |
| | 2 to 4 decoder with enable and active low outputs | DECE2X4A | 1 | | 4 |
| | 3 to 8 decoder with enable | DECE3X8 | 2 | | 11 |
| | 3 to 8 decoder with enable and active low outputs | DECE3X8A | 2 | | 11 |
| Registers | octal latch with clear | DLC8A | 1 | 8 | |
| | octal latch with enable | DLE8 | 1 | 8 | |
| | octal latch with multiplexed data | DLM8 | 1 | 8 | |
| | 4-bit shift register with clear | SREG4A | 1 | 4 | |
| | 8-bit shift register with clear | SREG8A | 1 | 8 | |
| Adders | 8-bit adder | FADD8 | 3 | | 44 |
| | 9-bit adder | FADD9 | 3 | | 49 |
| | 10-bit adder | FADD10 | 3 | | 56 |
| | 12-bit adder | FADD12 | 4 | | 69 |
| | 16-bit adder | FADD16 | 5 | | 97 |
| | 2-bit sum generator | SUMX1A | 2 | | 5 |
| | very fast 16-bit adder | VADD16C | 3 | | 97 |
| Comparators | 4-bit identity comparator | ICMP4 | 2 | | 5 |
| | 8-bit identity comparator | ICMP8 | 3 | | 5 |
| | 2-bit magnitude comparator with enable | MCMPC2 | 3 | | 9 |
| | 4-bit magnitude comparator with enable | MCMPC4 | 4 | | 18 |
| | 8-bit magnitude comparator with enable | MCMPC8 | 6 | | 36 |
| Multiplexors | 8 to 1 multiplexor | MX8 | 2 | | 3 |
| | 8 to 1 multiplexor with active low outputs | MX8A | 2 | | 3 |
| | 16 to 1 multiplexor | MX16 | 2 | | 5 |

T-46-19-11

## Combinable Hard Macros 1 (for DF1, DF1B, DFC1B, DFC1D, DL1, DL1B, DLC, and DLCA)

| Function | Description | Macro Name | Equation(s) | No. of Modules | |
|---|---|---|---|---|---|
| | | | | Seq. | Comb. |
| AND | 2-input | AND2 | Y = A B | | 1 |
| | | AND2A | Y = !A B | | 1 |
| | | AND2B | Y = !A !B | | 1 |
| | | AND3B | Y = !A !B C | | 1 |
| AND-OR | | AO1A | Y = ((!A) B) + C | | 1 |
| | | AO1D | Y = (!A !B) + C | | 1 |
| AND-OR Invert | | AOI1D | Y = !((!A !B) + !C) | | 1 |
| Buffers and Inverters | | BUF | Y = A | | 1 |
| | | BUFA | Y = !(!A) | | 1 |
| | | INV | Y = !A | | 1 |
| | | INVA | Y = !A | | 1 |
| Clock Net Interface | | GAND2 | Y = A G | | 1 |
| | | GNOR2 | Y = !(A + G) | | 1 |
| | | GOR2 | Y = A + G | | 1 |
| Multiplexor | 2:1 | MX2 | Y = (A !S) + (B S) | | 1 |
| NAND | 2-input | NAND2A | Y = !(!A B) | | 1 |
| | | NAND2B | Y = !(!A !B) | | 1 |
| | 3-input | NAND3C | Y = !(!A !B !C) | | 1 |
| NOR | 2-input | NOR2 | Y = !(A + B) | | 1 |
| | | NOR2A | Y = !(!A + B) | | 1 |
| | | NOR2B | Y = !(!A + !B) | | 1 |
| | 3-input | NOR3A | Y = !(!A + B + C) | | 1 |
| OR-AND | | OA1 | Y = (A + B) C | | 1 |
| OR | 2-input | OR2 | Y = A + B | | 1 |
| | | OR2A | Y = !A + B | | 1 |
| | 3-input | OR3 | Y = A + B + C | | 1 |

Actel

## Combinable Hard Macros 2 (for DF1, DF1B, DFC1B, DFC1D, DL1, and DL1B)

T-46-19-11

| Function | Description | Macro Name | Equation(s) | No. of Modules | |
|---|---|---|---|---|---|
| | | | | Seq. | Comb. |
| AND | 3-input | AND3 | Y = A B C | | 1 |
| | | AND3A | Y = !A B C | | 1 |
| | | AND3C | Y = !A !B !C | | 1 |
| | 4-input | AND4B | Y = !A !B C D | | 1 |
| | | AND4C | Y = !A !B !C D | | 1 |
| AND-OR | | AO1 | Y = (A B) + C | | 1 |
| | | AO1B | Y = (A B) + (!C) | | 1 |
| | | AO1C | Y = ((!A) B) + (!C) | | 1 |
| | | AO1E | Y = (!A !B) + !C | | 1 |
| | | AO11 | Y = A B + ((A + B) C) | | 1 |
| | | AO2 | Y = ((A B) + C + D) | | 1 |
| | | AO2A | Y = ((!A B) + C + D) | | 1 |
| | | AO2B | Y = (!A !B) + C + D | | 1 |
| | | AO2C | Y = (!A B) + !C + D | | 1 |
| | | AO2D | Y = (!A !B) + !C + D | | 1 |
| | | AO3 | Y = (!A B C) + D | | 1 |
| | | AO3B | Y = (!A !B C) + D | | 1 |
| | | AO3C | Y = (!A !B !C) + D | | 1 |
| | | A04A | Y = (!A B C) + (A C D) | | 1 |
| | | AO5A | Y = (!A B) + (A C) + D | | 1 |
| AND-OR Invert | | AOI1A | Y = !((!A B) + C) | | 1 |
| | | AOI1B | Y = !((A B) + !C) | | 1 |
| | | AOI1C | Y = !((!A !B) + C) | | 1 |
| | | AOI2A | Y = !((!A B) + C + D) | | 1 |
| | | AOI3A | Y = !((!A !B !C)+(!A !D) | | 1 |
| Exclusive OR | XNOR, AND-XOR | AX1B | Y = (!A !B) ^ C | | 1 |
| Boolean | | CS2 | Y = !((A + S) B) C + ((A + S) B) D | | 1 |
| | | CY2B | Y = A1 B1 + (A0+B0) A1 + (A0+B0) B1 | | 1 |
| Clock Net Interface | | GMX4 | Y = (D0 !S0 !G) + (D1 !G S0) + (D2 G !S0) + (D3 S0 G) | | 1 |
| | | GNAND2 | Y = !(A G) | | 1 |
| | | GXOR2 | Y = A ^ G | | 1 |
| AND-OR | | MAJ3 | Y = (A B) + (B C) + (A C) | | 1 |
| Multiplexor | | MX2A | Y = (!A !S) + (B S) | | 1 |
| | | MX2C | Y = (!A !S) + (!B S) | | 1 |
| | 4:1 | MX4 | Y = (D0 !S0 !S1) + (D1 S0 !S1) + (D2 !S0 S1) + (D3 S0 S1) | | 1 |
| NAND | 2-input | NAND2 | Y = !(A B) | | 1 |
| | 3-input | NAND3A | Y = !(!A B C) | | 1 |
| | | NAND3B | Y = !(!A !B C) | | 1 |
| | 4-input | NAND4C | Y = !(!A !B !C D) | | 1 |
| | | NAND4D | Y = !(!A !B !C !D) | | 1 |
| NOR | 3-input | NOR3 | Y = !(A + B + C) | | 1 |
| | | NOR3B | Y = !(!A + !B + C) | | 1 |
| | | NOR3C | Y = !(!A + !B + !C) | | 1 |
| | 4-input | NOR4A | Y = !(!A + B + C + D) | | 1 |
| | | NOR4B | Y = !(!A + !B + C + D) | | 1 |

**Combinable Hard Macros 2** (continued) (for DF1, DF1B, DFC1B, DFC1D, DL1, and DL1B) T-46-19-11

| Function | Description | Macro Name | Equation(s) | No. of Modules | |
|---|---|---|---|---|---|
| | | | | Seq. | Comb. |
| OR-AND | | OA1A | Y = (!A + B) C | | 1 |
| | | OA1B | Y = (A + B) (!C) | | 1 |
| | | OA1C | Y = (!A + B) (!C) | | 1 |
| | | OA2 | Y = (A + B) (C + D) | | 1 |
| | | OA2A | Y = (!A + B) (C+ D) | | 1 |
| | | OA3 | Y = ((A + B) C D) | | 1 |
| | | OA3A | Y = ((A + B) !C D) | | 1 |
| | | OA4 | Y = (A + B + C) D | | 1 |
| | | OA4A | Y = ((A + B + !C) D) | | 1 |
| | | OA5 | Y = (A+B+C)(A+D) | | 1 |
| OR-AND Invert | | OAI1 | Y = !((A + B) C) | | 1 |
| | | OAI2A | Y = !((A + B + C) !D) | | 1 |
| | | OAI3A | Y = !((A + B) !C !D ) | | 1 |
| OR | 3-Input | OR3A | Y = !A + B + C | | 1 |
| | | OR3B | Y = !A + !B + C | | 1 |
| | 4-Input | OR4 | Y = A + B + C + D | | 1 |
| | | OR4A | Y = !A + B + C + D | | 1 |
| Exclusive OR | XOR | XOR | Y = A ^ B | | 1 |
| | | XO1 | Y = (A ^ B) + C | | 1 |
| | | XO1A | Y = !(A ^ B) + C | | 1 |
| | XNOR, AND-XOR | XNOR | Y = !(A ^ B) | | 1 |
| | | XA1 | Y = (A ^ B) C | | 1 |
| | | XA1A | Y = !(A ^ B) C | | 1 |

1

## Non-Combinable Hard Macros

T-46-19-11

| Function | Description | Macro Name | Equation(s) | No. of Modules | |
|---|---|---|---|---|---|
| | | | | Seq. | Comb. |
| AND | 4-input | AND4 | Y = A B C D | | 1 |
| | | AND4A | Y = (!A B C D) | | 1 |
| | | AND4D | Y = !A !B !C !D | | 2 |
| | 5-input | AND5B | Y = !A !B C D E | | 1 |
| OR | 2-input | OR2B | Y = !A + !B | | 1 |
| | 3-input | OR3C | Y = !A + !B + !C | | 1 |
| | 4-input | OR4B | Y = !A + !B + C + D | | 1 |
| | | OR4C | Y = !A + !B + !C + D | | 1 |
| | | OR4D | Y = !A + !B + !C + !D | | 2 |
| | 5-input | OR5B | Y = !A + !B + C + D + E | | 1 |
| NAND | 3-input | NAND3 | Y = !(A B C) | | 1 |
| | 4-input | NAND4 | Y = !(A B C D) | | 2 |
| | | NAND4A | Y = !(!A B C D ) | | 1 |
| | | NAND4B | Y = !(!A !B C D) | | 1 |
| | 5-input | NAND5C | Y = !(!A !B !C D E) | | 1 |
| NOR | 4-input | NOR4 | X = !(A + B + C + D) | | 2 |
| | | NOR4C | Y = !(!A + !B + !C + D) | | 1 |
| | | NOR4D | Y = !(!A + !B + !C + !D) | | 1 |
| | 5-input | NOR5C | Y = !(!A + !B + !C + D +E) | | 1 |
| Exclusive OR | XNOR, AND-XOR | AX1 | Y = (!A B) ^ C | | 1 |
| | | AX1A | Y = !(!A B) ^ C | | 2 |
| | | AX1C | Y = (A B) ^ C | | 1 |
| AND-OR | | A02E | Y = (!A !B) + !C + !D | | 1 |
| | | AO3A | Y = (A B C) + D | | 1 |
| | | AO6 | Y = A B + C D | | 1 |
| | | AO6A | Y = A B + C !D | | 1 |
| | | AO7 | Y = A B C + D + E | | 1 |
| | | AO8 | Y = (A B) + (!C !D) + E | | 1 |
| | | AO9 | Y = (A B) + C + D + E | | 1 |
| | | AO10 | Y = (A B + C) (D + E) | | 1 |
| AND-OR Invert | | AOI1 | Y = !(A B + C) | | 1 |
| | | AOI2B | Y = !((!A B) + !C + D) | | 1 |
| | | AOI4 | Y=!((A B) + (C D)) | | 2 |
| | | AOI4A | Y = !(A B + !C D) | | 1 |
| OR-AND | | OA3B | Y = ((!A + B) !C D) | | 1 |
| OR-AND Invert | | OAI3 | Y = !((A + B) C D) | | 1 |
| Multiplexor | 2:1 | MX2B | Y = (A !S) + (!B S) | | 1 |

T-46-19-11

## Non-Combinable Hard Macros (continued)

| Function | Description | Macro Name | Equation(s) | No. of Modules Seq. | No. of Modules Comb. |
|---|---|---|---|---|---|
| Adders | half | HA1 | CO = A B<br>S = A ^ B | | 2 |
| | | HA1A | CO = !A B<br>S = !(A ^ B) | | 2 |
| | | HA1B | CO = !(A B)<br>S = !(A ^ B) | | 2 |
| | | HA1C | CO = !(A B)<br>S = (A ^ B) | | 2 |
| | full | FA1A | CO = (CI !B !A) + (A !B ) + (B CI A)<br>S = (B !A !CI) + (CO !A CI) + (CO A !CI)<br>+ (B A CI) | | 2 |
| | | FA1B | CO = !A(!B + B CI) + A(!B CI)<br>S = !A(!CI CO + CI B) + A(!CI B + CI CO) | | 2 |
| | | FA2A | CO = (CI !B !(A0+A1)) + (!B (A0+A1))<br>+ (B CI (A0+A1))<br>S = (B !(A0+A1) !CI) + (CO !(A0+A1) CI)<br>+ (CO(A0+A1) !CI) + (B(A0+A1)CI) | | 2 |
| Boolean | | CS1 | Y = !(A + S B) C + D (A + S B) | | 1 |
| | | CY2A | Y = A1 B1 + A0 B0 A1 + A0 B0 B1 | | 1 |
| | | MXT | Y = (!S1 (!S0A D0) + (S0A D1))<br>+ (S1 (!S0B D2 + S0B D3)) | | 2 |
| | | MXC1 | Y = !(!S A + S B) C + (!S A + S B) D | | 2 |
| D-type Flip-Flops | | DF1 | Q = (CLK, D, -, -) | 1 | |
| | | DF1A | QN = !(CLK, D, -, -) | 1 | |
| | | DF1B | Q = (!CLK, D, -, -) | 1 | |
| | | DF1C | QN = !(!CLK, D,- ,-) | 1 | |
| | with clear | DFC1 | Q = (CLK, D, CLR, -) | 1 | 1 |
| | | DFC1A | Q = (!CLK, D, CLR, -) | 1 | 1 |
| | | DFC1B | Q = (CLK, D, !CLR, -) | 1 | |
| | | DFC1D | Q = (!CLK, D, !CLR, -) | 1 | |
| | | DFC1E | QN = !(CLK, D, !CLR, -) | 1 | 1 |
| | | DFC1G | QN = !(!CLK, D, !CLR, -) | 1 | 1 |
| | with enable | DFE | Q = (CLK, !E Q + E D, -, -) | 1 | |
| | | DFE1B | Q = (CLK, !E D + E Q, -, -) | 1 | |
| | | DFE1C | Q = (!CLK, D !E + Q E, -, -) | 1 | |
| | | DFE3A | Q = (CLK, D E + Q !E, !CLR, -) | 1 | |
| | | DFE3B | Q = (!CLK, D E + Q !E, !CLR, -) | 1 | |
| | | DFE3C | Q = (CLK, D !E + Q E, !CLR, -) | 1 | |
| | | DFE3D | Q = (!CLK, D !E + Q E, !CLR, -) | 1 | |
| | | DFEA | Q = (!CLK, !E Q + E D, -, -) | 1 | 1 |

1

T-46-19-11

## Non-Combinable Hard Macros (continued)

| Function | Description | Macro Name | Equation(s) | No. of Modules | |
|---|---|---|---|---|---|
| | | | | Seq. | Comb. |
| D-type Flip-Flops (continued) | | DFM | Q = (CLK, A !S + B S, –, –) | 1 | |
| | | DFM1B | QN = !(CLK, A !S + B S, –, –) | 1 | |
| | | DFM1C | QN = !(!CLK, A !S + B S, –, –) | 1 | |
| | | DFM3 | Q = (CLK, A !S + B S, CLR, –) | 1 | 1 |
| | | DFM3B | Q = (!CLK, A !S + B S, !CLR, –) | 1 | |
| | | DFM3E | Q = (!CLK, A !S + B S, CLR, –) | 1 | 1 |
| | | DFM4C | QN = !(CLK, !A !S + !B S, –, !PRE) | 1 | |
| | with multiplexed data | DFM4D | QN = !(!CLK, A !S + B S, –, !PRE) | 1 | |
| | | DFM6A | Q = (CLK, (D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1), !CLR, –) | 1 | |
| | | DFM6B | Q = (!CLK, (D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1), !CLR, –) | 1 | |
| | | DFM7A | Q = (CLK, !CLR, (D0 !S0 + D1 S0) !(S10 + S11) + (D2 !S0 + D3 S0) (S10 + S11)) | 1 | |
| | | DFM7B | Q = (!CLK, !CLR, (D0 !S0 + D1 S0) !(S10 + S11) + (D2 !S0 + D3 S0) (S10 + S11)) | 1 | |
| | | DFMA | Q = (!CLK, A !S + B S, –, –) | 1 | |
| | | DFMB | Q = (CLK, A !S + B S, !CLR, –) | 1 | |
| | | DFME1A | Q = (CLK, !E A !S + !E B S + E Q, –, –) | 1 | |
| | with preset | DFP1 | Q = (CLK, D, –, PRE) | | 2 |
| | | DFP1A | Q = (!CLK, D, –, PRE) | | 2 |
| | | DFP1B | Q = (CLK, D, –, !PRE) | | 2 |
| | | DFP1C | QN = !(CLK, D, –, PRE) | 1 | 1 |
| | | DFP1D | Q = (!CLK, D, –, !PRE) | 2 | |
| | | DFP1E | QN = !(CLK, D, –, !PRE) | 1 | |
| | | DFP1F | Q = (!CLK, D, –, PRE) | 1 | 1 |
| | | DFP1G | QN = !(!CLK, D, –, !PRE) | | 1 |
| | with clear and preset | DFPC | Q = (CLK, D, CLR, PRE) | | 2 |
| | | DFPCA | Q = (!CLK, D, !CLR, PRE) | | 2 |
| JK Flip-Flops | | JKF | Q = (CLK, !Q J + Q K, –, –) | 1 | |
| | | JKF1B | Q = (!CLK, !Q J + Q K, –, –) | 1 | |
| | | JKF2A | Q = (CLK, !Q J + Q K, !CLR, –) | 1 | |
| | | JKF2B | Q = (!CLK, !Q J + Q K, !CLR, –) | 1 | |
| | | JKF2C | Q = (CLK, !Q J + Q K, CLR, –) | 1 | 1 |
| | | JKF2D | Q = (!CLK, !Q J + Q K, CLR, –) | 1 | 1 |
| T-type Flip-Flops | | TF1A | Q = (CLK, T !Q + !T Q, !CLR, –) | 1 | |
| | | TF1B | Q = (!CLK, T !Q + !T Q, !CLR, –) | 1 | |
| Data Latch | | DL1 | Q = (G, D, –, –) | 1 | |
| | | DL1A | QN = !(G, D, –, –) | 1 | |
| | | DL1B | Q = (!G, D, –, –) | 1 | |
| | | DL1C | QN = !(!G, D, –, –) | 1 | |
| | | DL2A | Q = (G, D, !CLR, PRE) | | 2 |
| | | DL2B | QN = !(!G, D, CLR, PRE) | | 2 |
| | | DL2C | Q = (!G, D, !CLR, PRE) | | 2 |
| | | DL2D | QN = !(G, D, CLR, !PRE) | | 2 |

T-46-19-11

## Non-Combinable Hard Macros (continued)

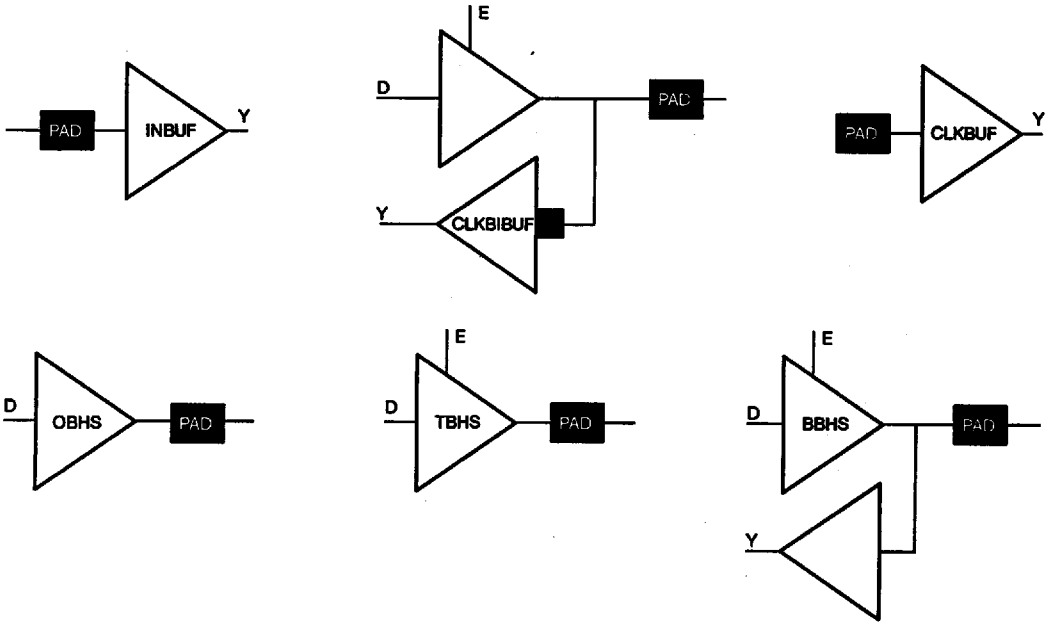
| Function | Description | Macro Name | Equation(s) | No. of Modules Seq. | No. of Modules Comb. |
|---|---|---|---|---|---|
| Data latch (continued) | with clear | DLC | Q = (G, D, !CLR, -) | 1 | |
| | | DLC1 | Q = (G, D, CLR, -) | | 1 |
| | | DLC1A | Q = (!G, D, CLR, -) | | 1 |
| | | DLC1F | QN = !(G, D, CLR, -) | | 1 |
| | | DLC1G | QN = !(!G, D, CLR, -) | | 1 |
| | | DLCA | Q = (!G, D, !CLR, -) | 1 | |
| | with enable | DLE | Q = (G, Q !E + D E, -, -) | 1 | |
| | | DLE1D | QN = !(!G, !E !D + E QN, -, -) | 1 | |
| | | DLE2A | Q = (!G, Q !E + D E, CLR, -) | 1 | 1 |
| | | DLE2B | Q = (!G, D !E + Q E, !CLR, -) | 1 | |
| | | DLE2C | Q = (!G, !E D + Q E, CLR, -) | | 1 |
| | | DLE3A | Q = (!G, E D + Q !E, -, PRE) | | 2 |
| | | DLE3B | Q = (!G, !E D + Q E, -, PRE) | | 1 |
| | | DLE3C | Q = (!G, !E D + Q E, -, !PRE) | | 1 |
| | | DLEA | Q = (G, Q E + D !E, -, -) | 1 | |
| | | DLEB | Q = (!G, Q !E + D E, -, -) | 1 | |
| | | DLEC | Q = (!G, Q E + D !E, -, -) | 1 | |
| | with multiplexed data | DLM | Q = (G, A !S + B S, -, -) | 1 | |
| | | DLM2A | Q = (!G, A !S + B S, CLR, -) | 1 | 1 |
| | | DLM3 | Q = (G, D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1, -, -) | 1 | |
| | | DLM3A | Q = (!G, D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1, -, -) | 1 | |
| | | DLMA | Q = (!G, A !S + B S, -, -) | 1 | |
| | with multiplexed data and enable | DLME1A | Q = (!G, A !S !E + B S !E + E Q, -, -) | 1 | |
| | with preset | DLP1 | Q = (G, D, -, PRE) | | 1 |
| | | DLP1A | Q = (!G, D, -, PRE) | | 1 |
| | | DLP1B | Q = (G, D, -, !PRE) | | 1 |
| | | DLP1C | Q = (!G, D, -, PRE) | | 1 |
| | | DLP1D | QN = !(G, D, -, !PRE) | 1 | |
| | | DLP1E | QN = !(!G, D, -, !PRE) | 1 | |
| Clock Net Interface | | CLKINT | | clock modules = 1 | |
| Tie-Off | | VCC | | modules = 0 | |
| | | GND | | modules = 0 | |

1

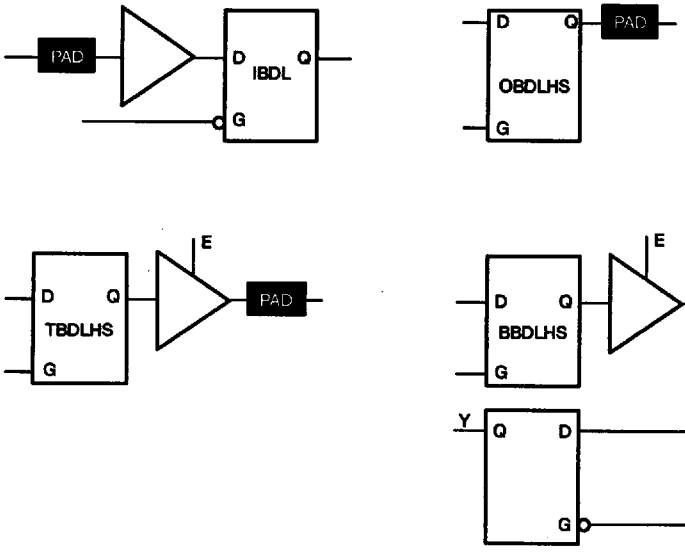
## Hard Macro Symbols

T-46-19-11

### I/O Buffers
(I/O Module Count = 1)

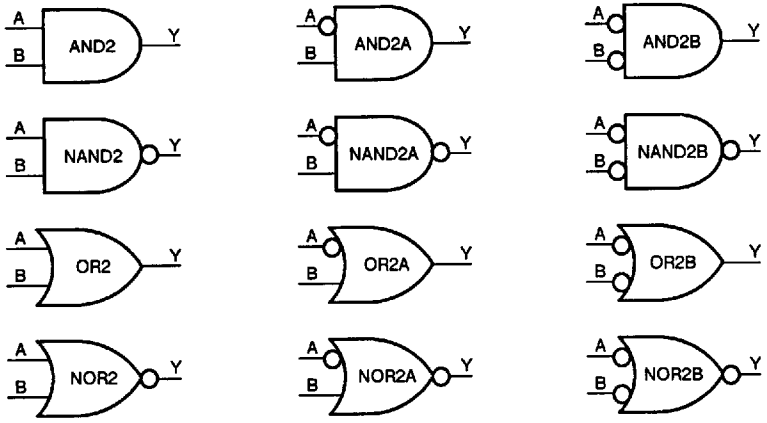



### I/O Buffers with Latches



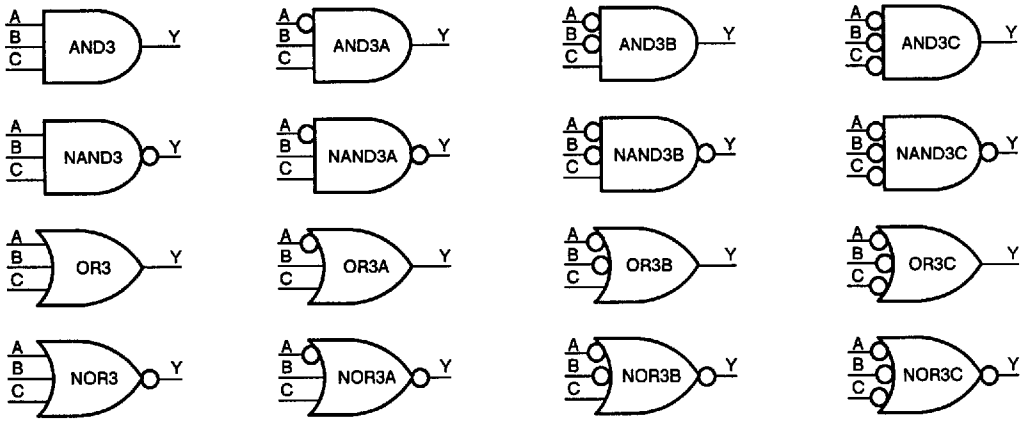
T-46-19-11

### 2-Input Gates
(Module Count = 1)



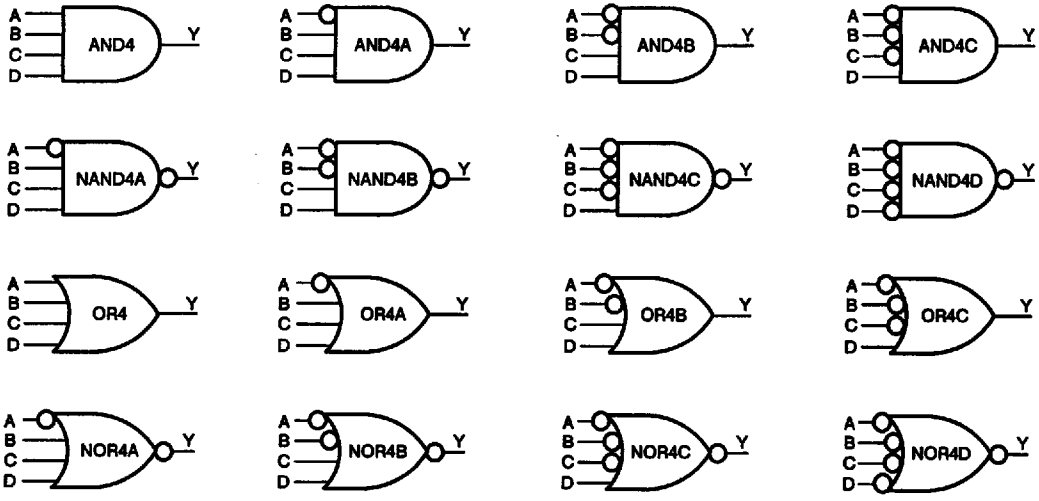

1

### 3-Input Gates
(Module Count = 1)

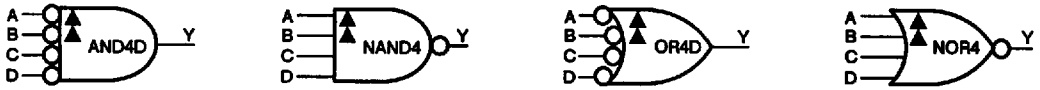


T-46-19-11

### 4-Input Gates
(Module Count = 1)



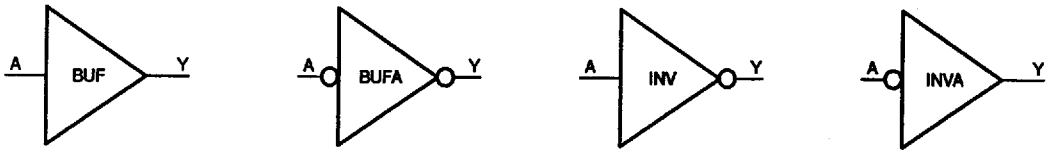

(Module Count = 2)



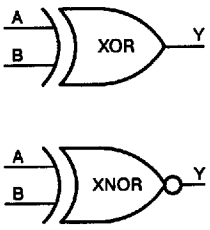

▲ Indicates extra delay input

### 5-Input Gates
(Module Count = 1)

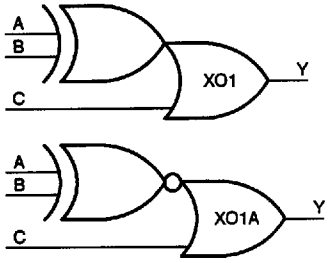

### Buffers
(Module Count = 1)



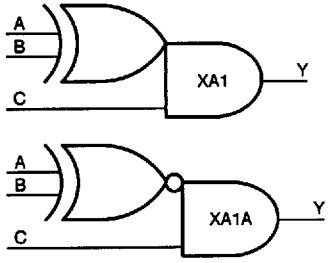
**XOR Gates** (Module Count = 1)



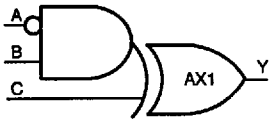

**XOR-OR Gates** (Module Count = 1)

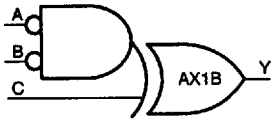


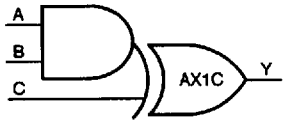

**XOR-AND Gates** (Module Count = 1)



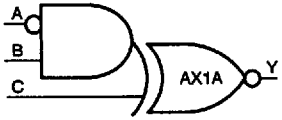

**AND-XOR Gates**
(Module Count = 1)




(Module Count = 2)

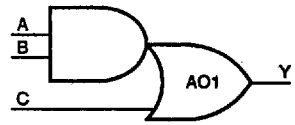


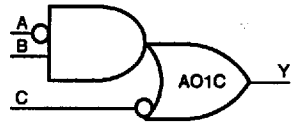

1

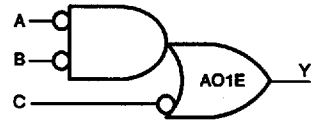
T-46-19-11

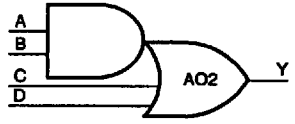
## AND-OR Gates

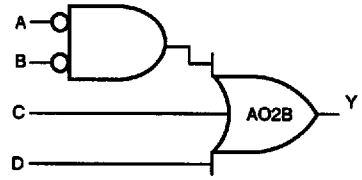
(Module Count = 1)

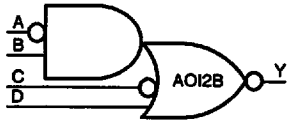


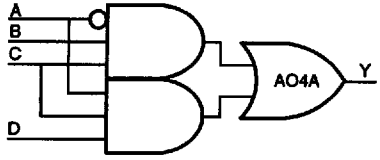



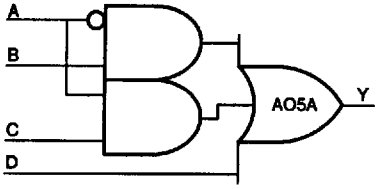



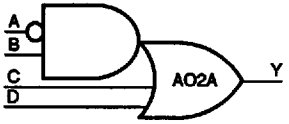



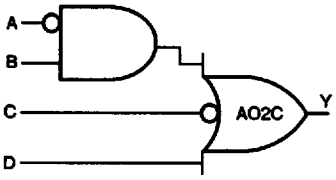



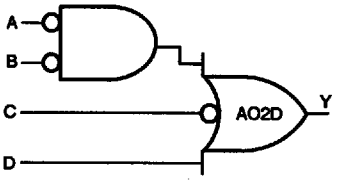



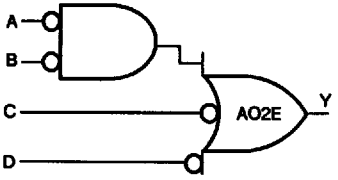



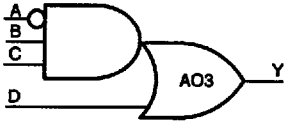


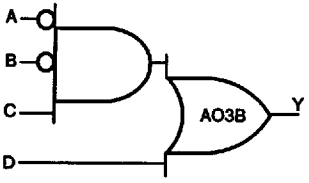


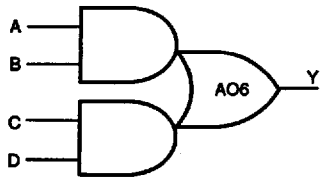



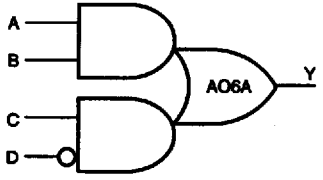



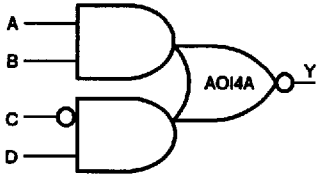



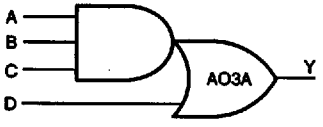



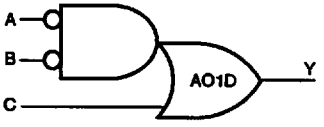



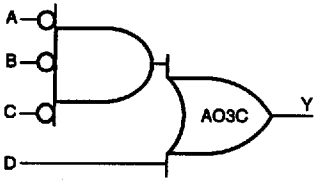



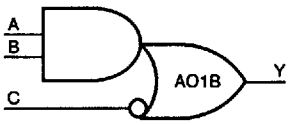



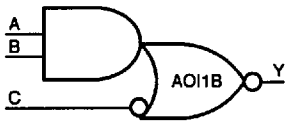



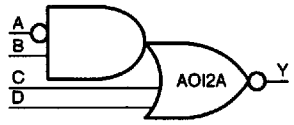



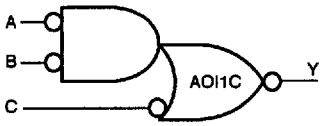
**AND-OR Gates,** continued
(Module Count = 1)

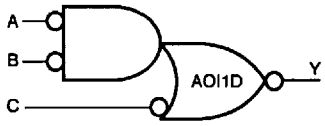
T-46-19-11

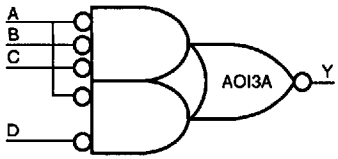


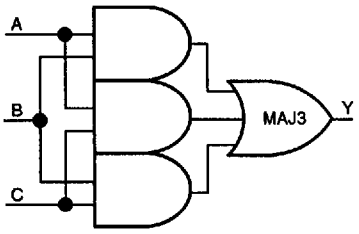



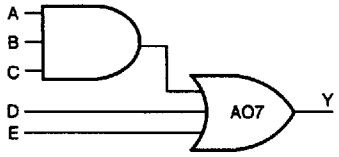



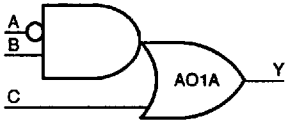



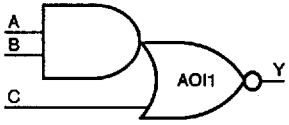



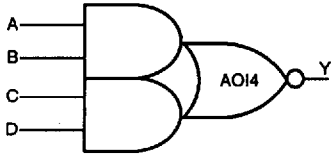



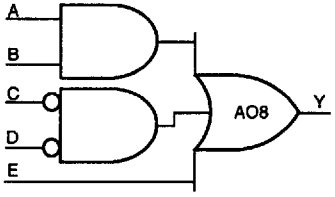



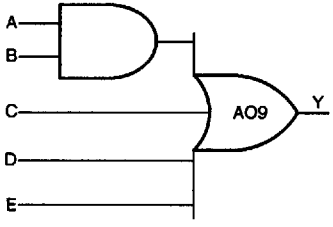



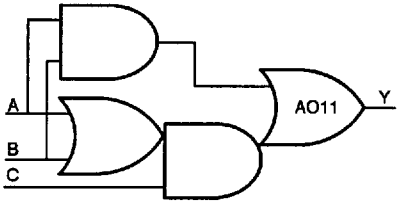




(Module Count = 2)



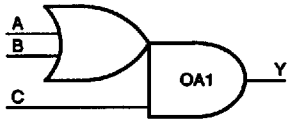



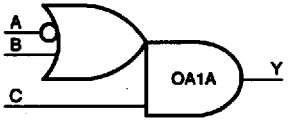



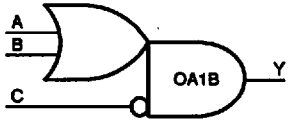



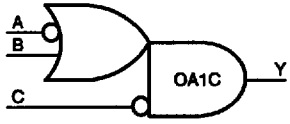
T-46-19-11

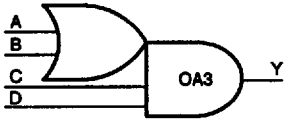
## OR-AND Gates
(Module Count = 1)

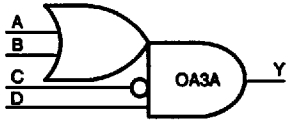


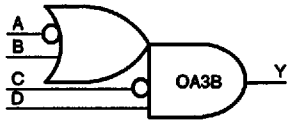



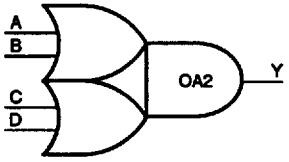



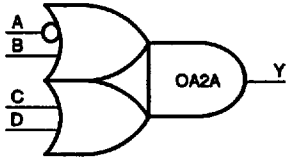



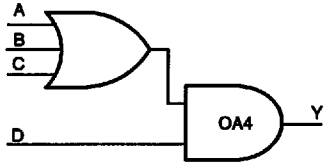



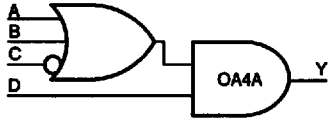



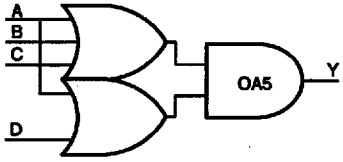



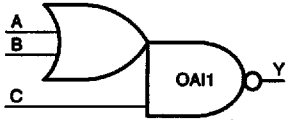



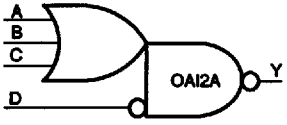



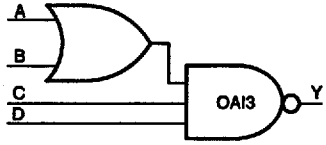



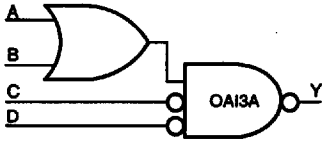



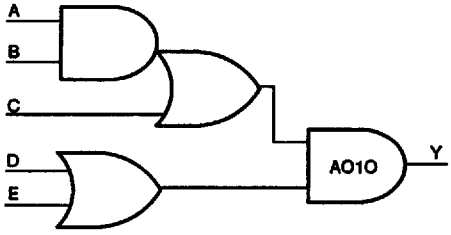



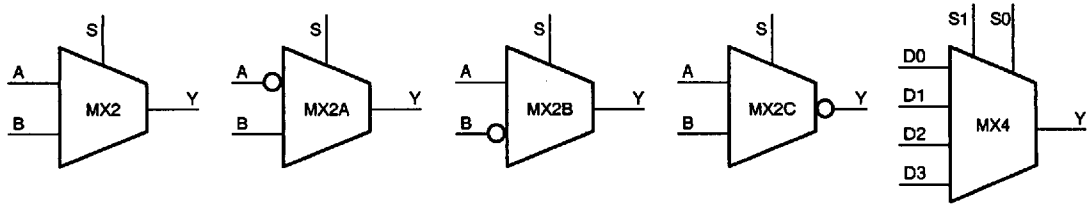



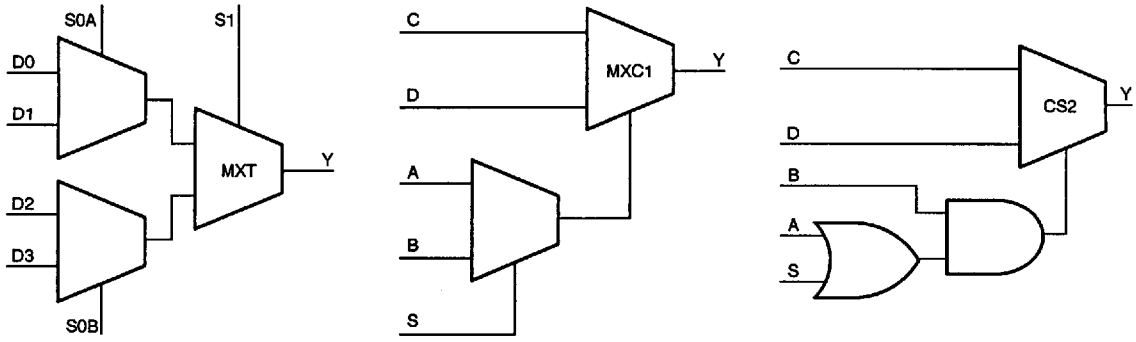
T-46-19-11

## Multiplexors

(Module Count = 1)

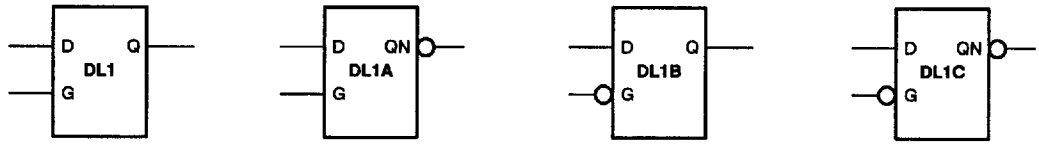



(Module Count = 2)




## Latches

(Module Count = 1)

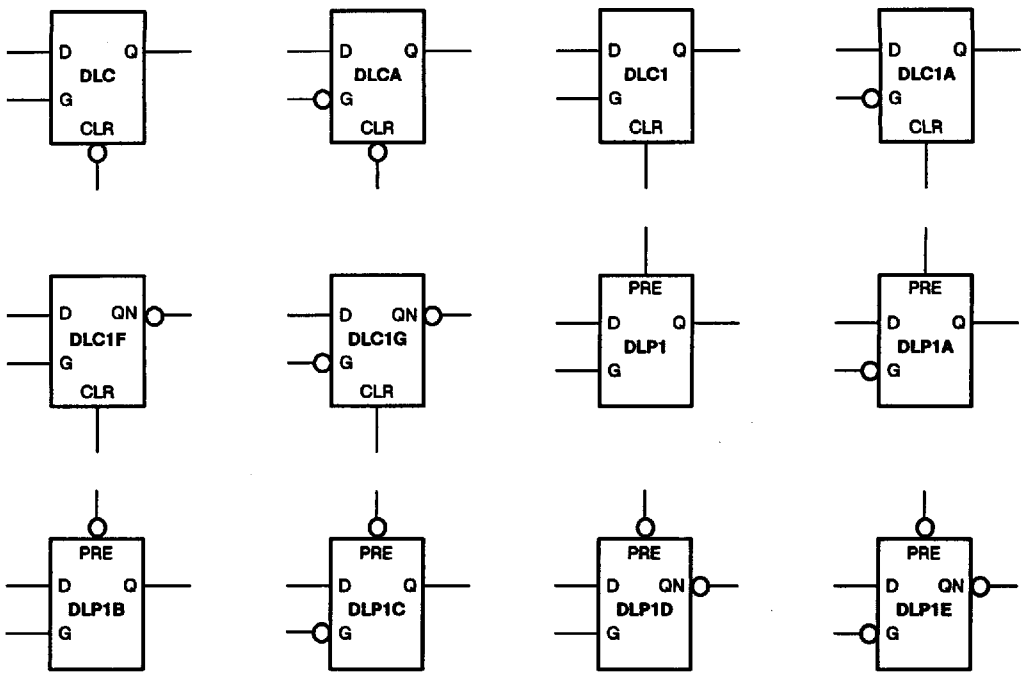


Actel

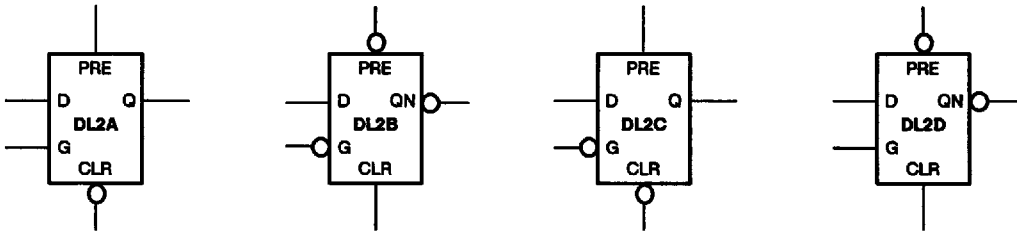
T-46-19-11

## D-Latches with Clear

(Module Count = 1)



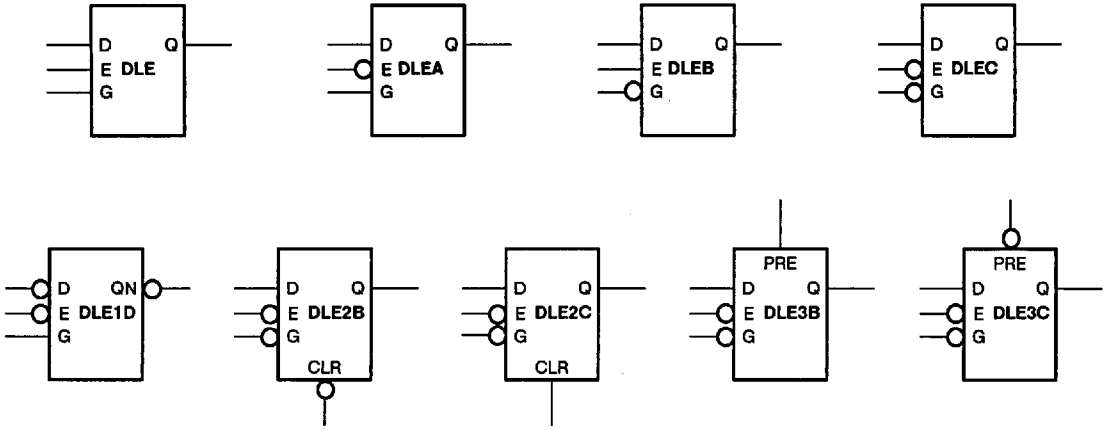

(Module Count = 2)



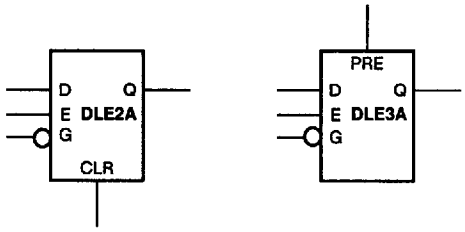
### D-Latches with Enable

(Module Count = 1)

T-46-19-11



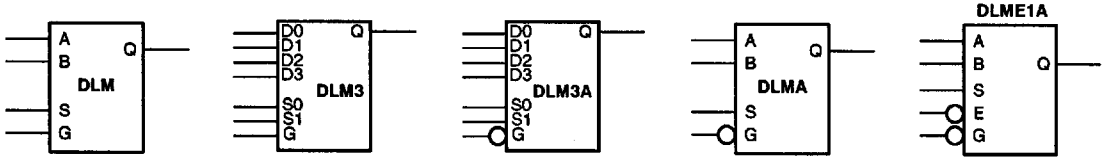

(Module Count = 2)



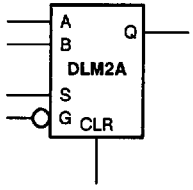

1

### Mux Latches

(Module Count = 1)



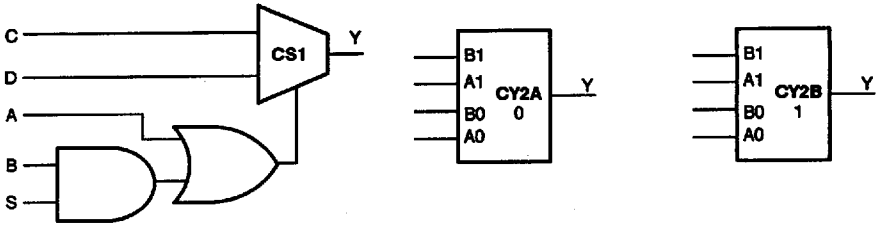

(Module Count = 2)



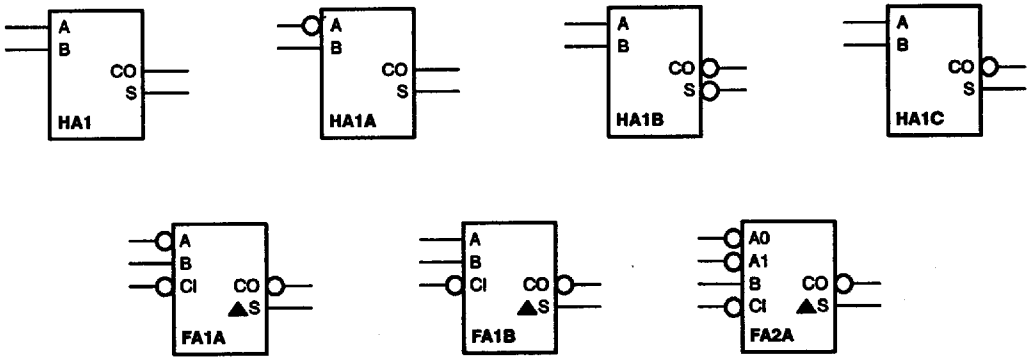
## Adders

(Module Count = 1)

T-46-19-11



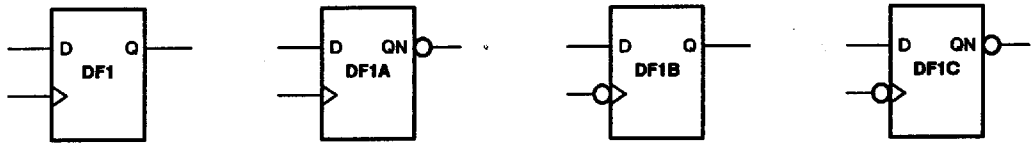

(Module Count = 2)




Macros FA1A, FA1B, and FA2A have two level delays from the inputs to the S outputs, as indicated by the▲

## D-Type Flip-Flops

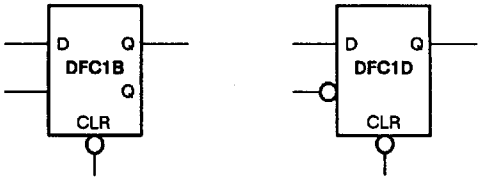
(Module Count = 1)



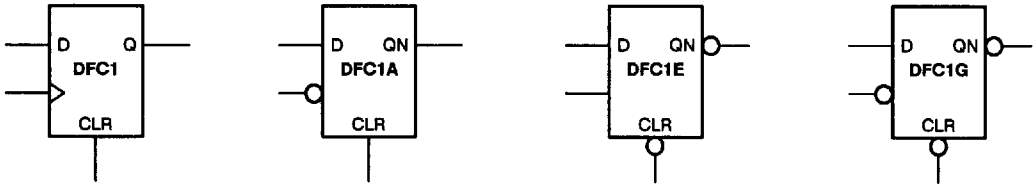
T-46-19-11

### D-Type Flip-Flops with Clear

(Module Count = 1)

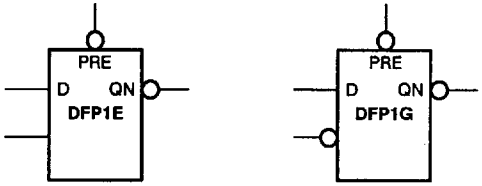



(Module Count = 2)

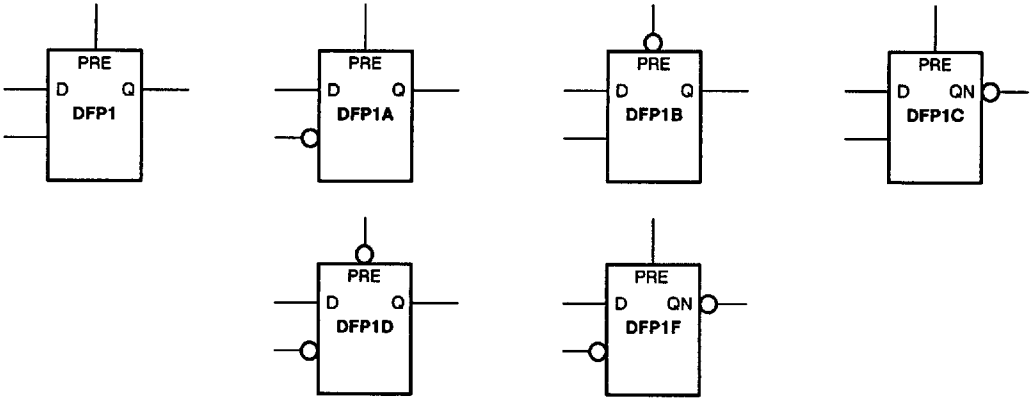



### D-Type Flip-Flops with Preset

(Module Count = 1)

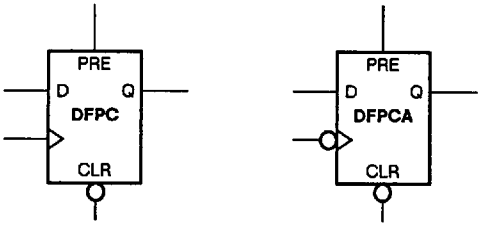



(Module Count = 2)




### D-Type Flip-Flops with Preset and Clear

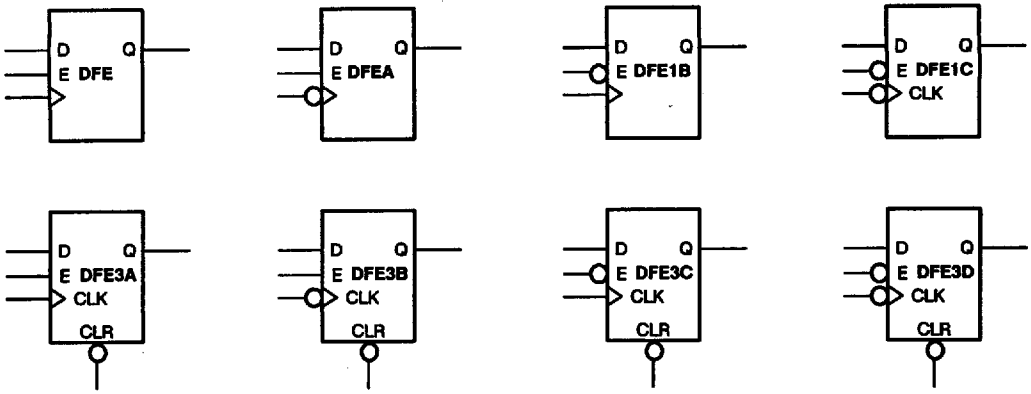
(Module Count = 2)



T-46-19-11

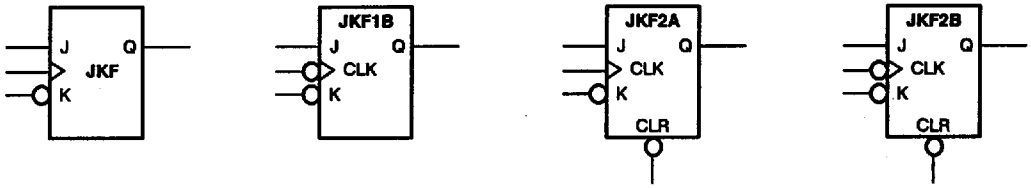
### D-Type Flip-Flops with Enable

(Module Count = 1)

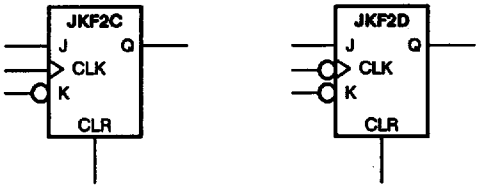



### JK Flip-Flops

(Module Count = 1)

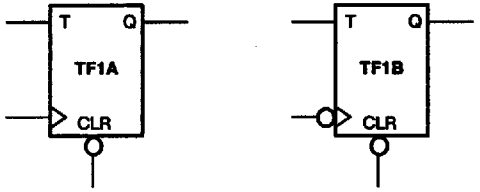



(Module Count = 2)




### Toggle Flip-Flops

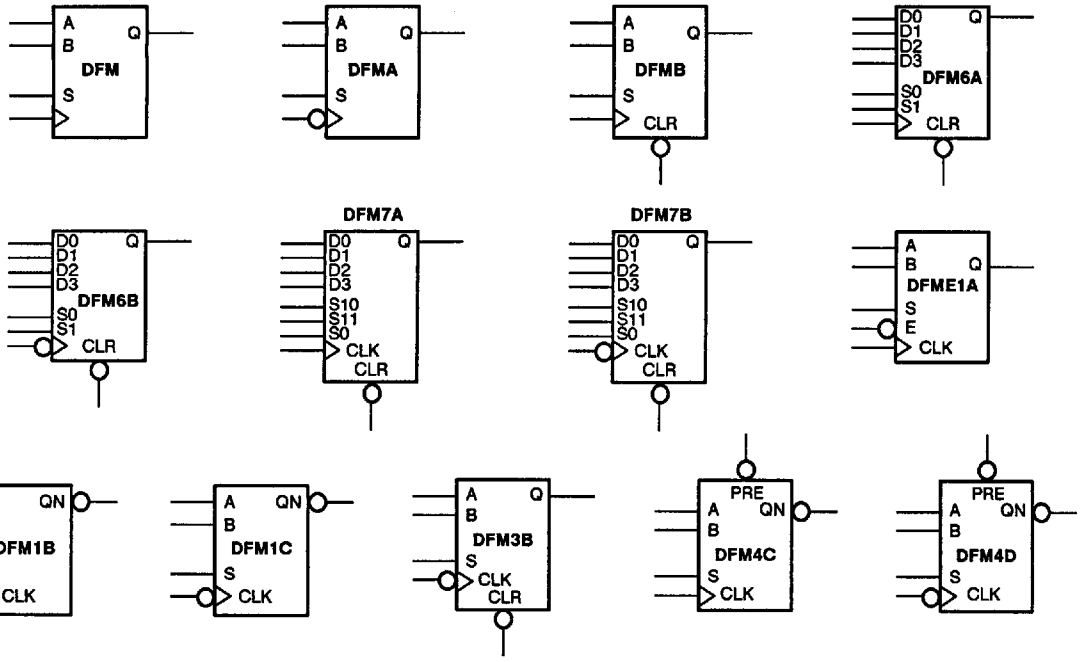
(Module Count = 1)



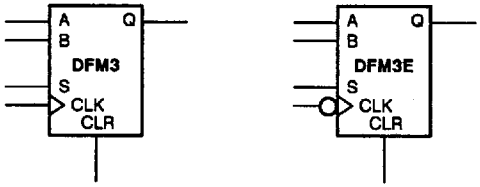
T-46-19-11

### Mux Flip-Flops

(Module Count = 1)

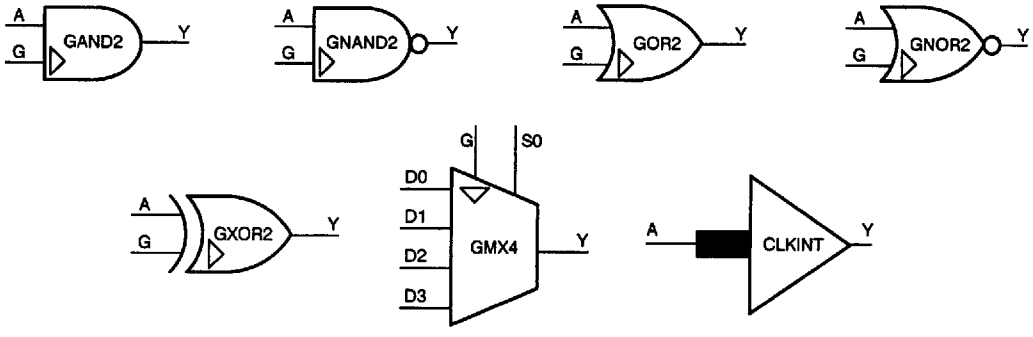



(Module Count = 2)




### CLKBUF Interface Macros

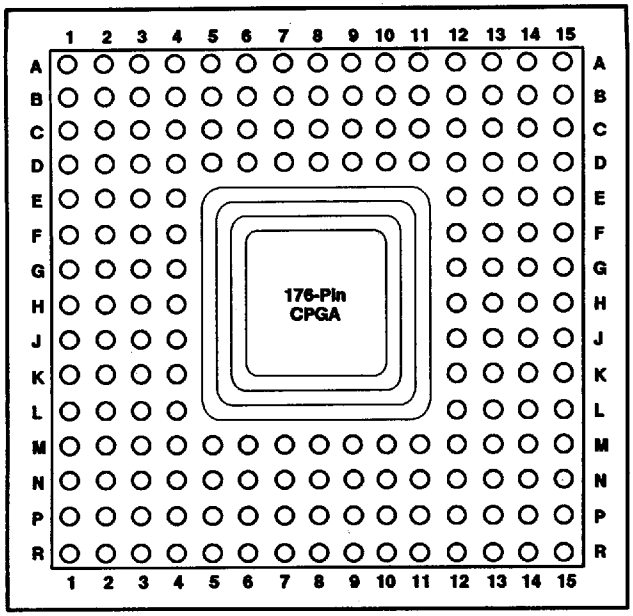
(Module Count = 1)




▷ Indicates clock input for connection to the global clock networks.

## Package Pin Assignments: 176-Pin CPGA
(Top View)

T-46-19-11

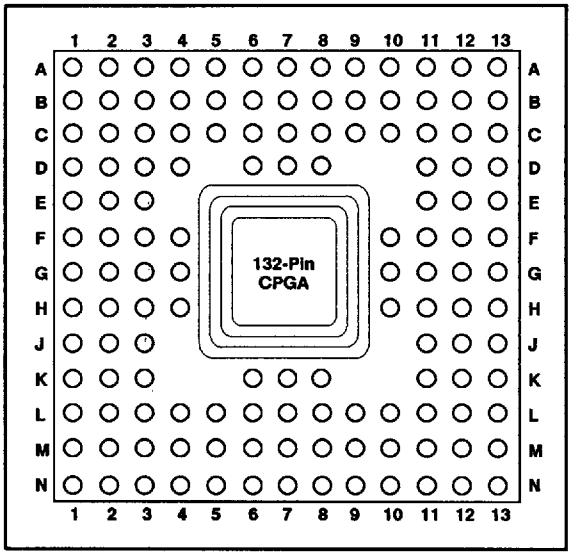



| Signal | Pin No. | Location |
|---|---|---|
| PRA or I/O | 152 | C9 |
| PRB or I/O | 160 | D7 |
| MODE | 2 | C3 |
| SDI or I/O | 135 | B14 |
| SDO or I/O | 87 | P13 |
| DCLK or I/O | 175 | B3 |
| CLKA or I/O | 154 | A9 |
| CLKB or I/O | 158 | B8 |
| GND | 1, 8, 18, 23, 33, 38, 45, 57, 67, 77, 89, 101, 106, 111, 121, 126, 133, 145, 156, 165 | D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12, K12, J12, H12, F12, E12, D12, D10, C8, D6 |
| $V_{CC}$ | 13, 24, 28, 52, 68, 82, 112, 116, 140, 155, 170 | F4, H3, J4, M5, N8, M11, H13, G12, D11, D8, D5 |
| $V_{PP}$ | 110 | J14 |
| $V_{SV}$ | 25, 113 | H2, H14 |
| $V_{KS}$ | 109 | J13 |

Notes:
1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP}$ = $V_{CC}$, except during device programming.
5. $V_{SV}$ = $V_{CC}$, except during device programming.
6. $V_{KS}$ = GND, except during device programming.

## Package Pin Assignments: 132-Pin CPGA (Top View)

T-46-19-11

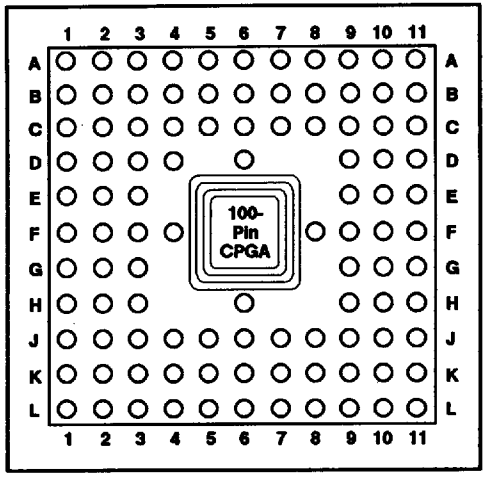



| Signal | Pin No. | Location |
|---|---|---|
| PRA or I/O | 113 | B8 |
| PRB or I/O | 121 | C6 |
| MODE | 2 | A1 |
| SDI or I/O | 101 | B12 |
| SDO or I/O | 65 | N12 |
| DCLK or I/O | 132 | C3 |
| CLKA or I/O | 115 | B7 |
| CLKB or I/O | 119 | B6 |
| GND | 9, 10, 26, 27, 41, 58, 59, 73, 74, 92, 93, 107, 108, 125, 126 | E3, F4, J2, J3, L5, M9, L9, K12, J11, E12, E11, C9, B9, B5, C5 |
| $V_{CC}$ | 18, 19, 49, 50, 83, 84, 116, 117 | G3, G2, L7, K7, G10, G11, D7, C7 |
| $V_{PP}$ | 82 | G13 |
| $V_{SV}$ | 17, 85 | G4, G12 |
| $V_{KS}$ | 81 | H13 |

Notes:
1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP}$ = $V_{CC}$, except during device programming.
5. $V_{SV}$ = $V_{CC}$, except during device programming.
6. $V_{KS}$ = GND, except during device programming.

## Package Pin Assignments: 100-Pin CPGA (Top View)

T-46-19-11

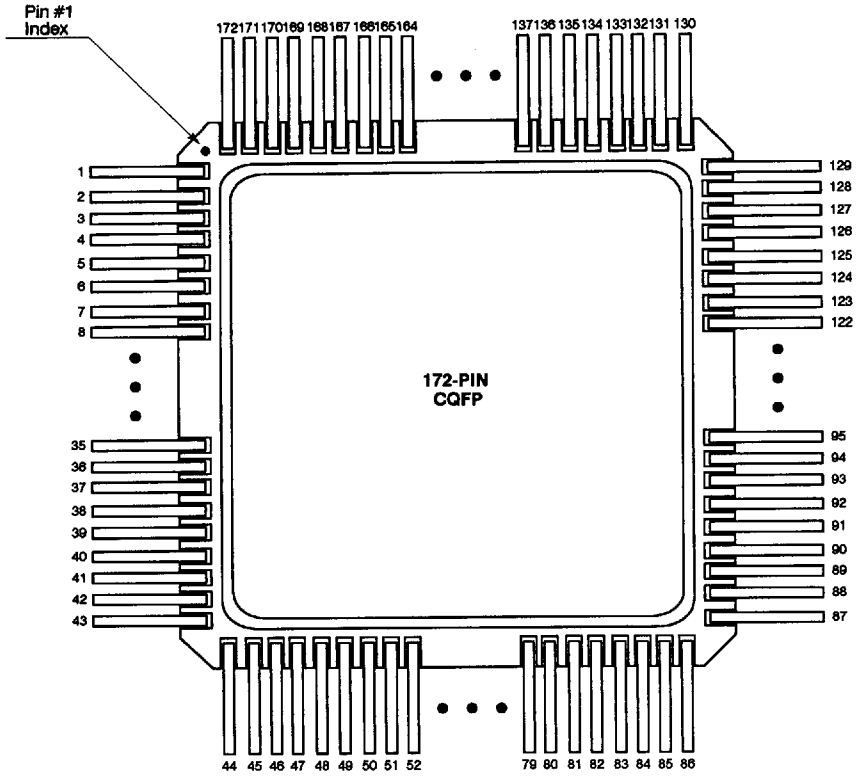



| Signal | Pin No. | Location |
|---|---|---|
| PRA or I/O | 85 | A7 |
| PRB or I/O | 92 | A4 |
| MODE | 2 | C2 |
| SDI or I/O | 77 | C8 |
| SDO or I/O | 50 | J9 |
| DCLK or I/O | 100 | C3 |
| CLKA or I/O | 87 | C6 |
| CLKB or I/O | 90 | D6 |
| GND | 7, 20, 32, 44, 55, 70, 82, 94 | E3, G3, J5, J7, G9, D10, C7, C5 |
| $V_{CC}$ | 15, 38, 64, 88 | F3, K6, F9, B6 |
| $V_{PP}$ | 63 | F10 |
| $V_{SV}$ | 14, 65 | G1, E11 |
| $V_{KS}$ | 62 | F11 |

Notes:
1. All unassigned pins are available for use as I/Os.
2. Unused I/O pins are designated as outputs by ALS and driven low.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP}$ = $V_{CC}$, except during device programming.
5. $V_{SV}$ = $V_{CC}$, except during device programming.
6. $V_{KS}$ = GND, except during device programming.

## Package Pin Assignments: 172-Pin CQFP (Top View)

T-46-19-11



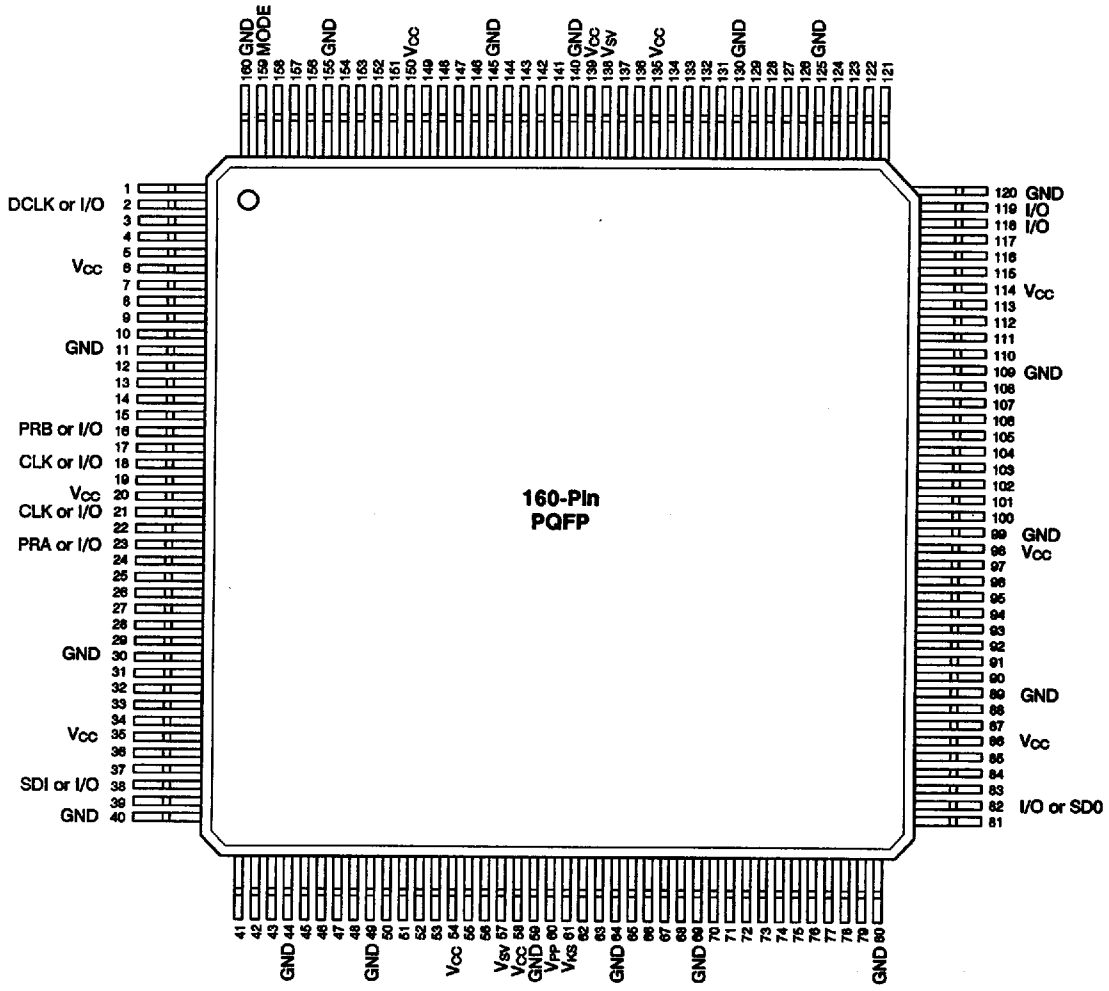

| Signal | Pin Number |
|---|---|
| MODE | 1 |
| GND | 7, 17, 22, 32, 37, 55, 65, 75, 98, 103, 108, 118, 123, 141, 152, 161 |
| $V_{CC}$ | 12, 23 ,27, 50, 66, 80, 109, 113, 136, 151, 166 |
| $V_{SV}$ | 24, 110 |
| $V_{KS}$ | 106 |
| $V_{PP}$ | 107 |
| SDO or I/O | 85 |
| SDI or I/O | 131 |
| PRA or I/O | 148 |
| PRB or I/O | 156 |
| CLKA or I/O | 150 |
| CLKB or I/O | 154 |
| DCLK or I/O | 171 |

**Notes:**

1. $V_{PP}$ must be terminated to $V_{CC}$, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

## Package Pin Assignments: 160-Pin PQFP (Top View)

T-46-19-11

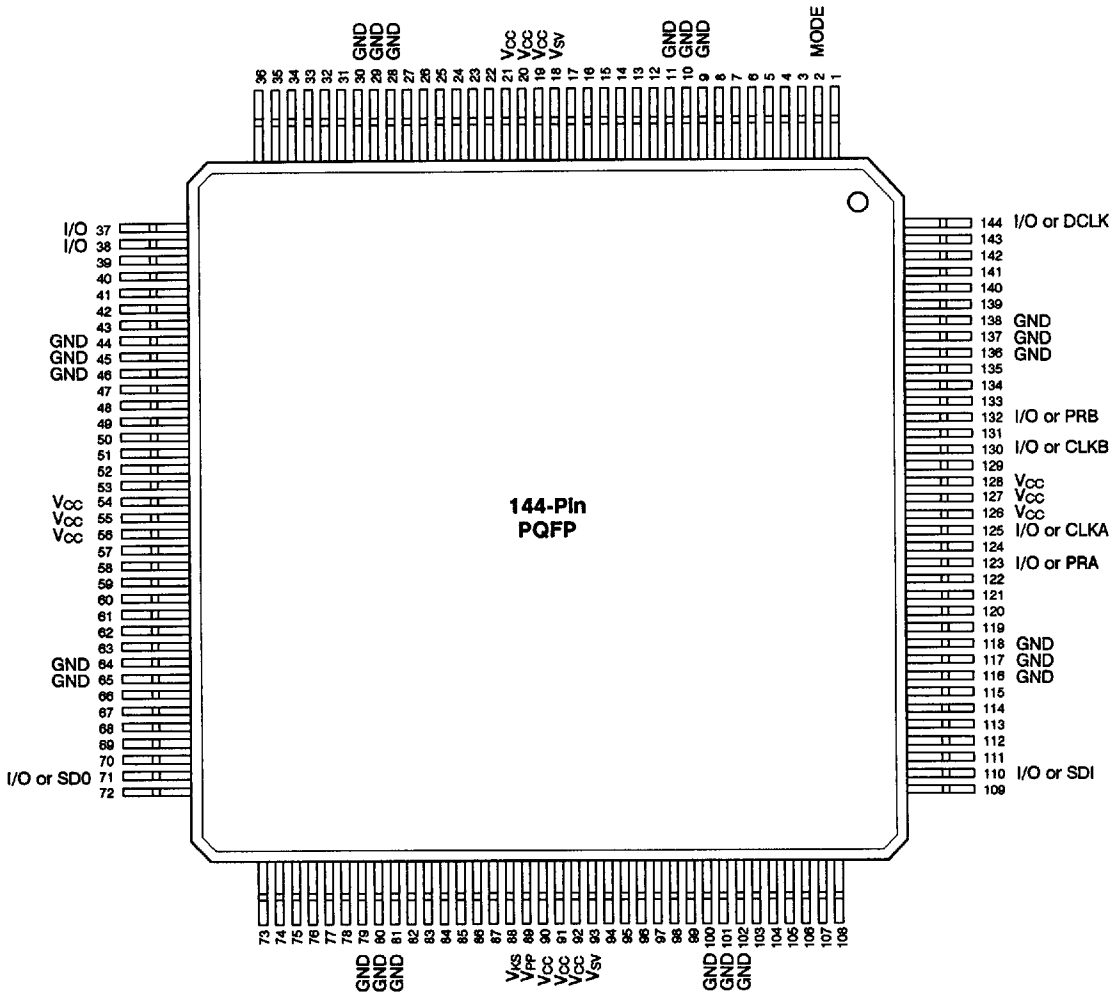



Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. $V_{KS} = GND$, except during device programming.

## Package Pin Assignments: 144-Pin PQFP (Top View)

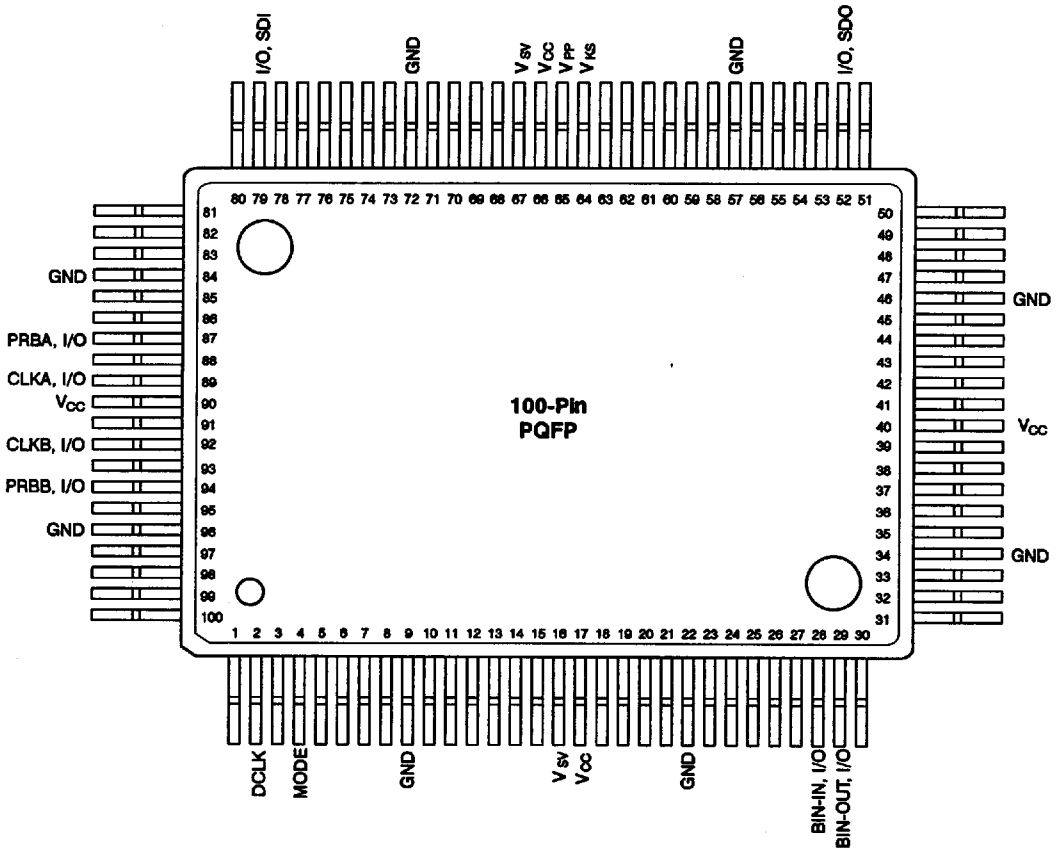
T-46-19-11




Notes:
1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP}$ = $V_{CC}$, except during device programming.
5. $V_{SV}$ = $V_{CC}$, except during device programming.
6. $V_{KS}$ = GND, except during device programming.

## Package Pin Assignments: 100-Pin PQFP (Top View)

T-46-19-11

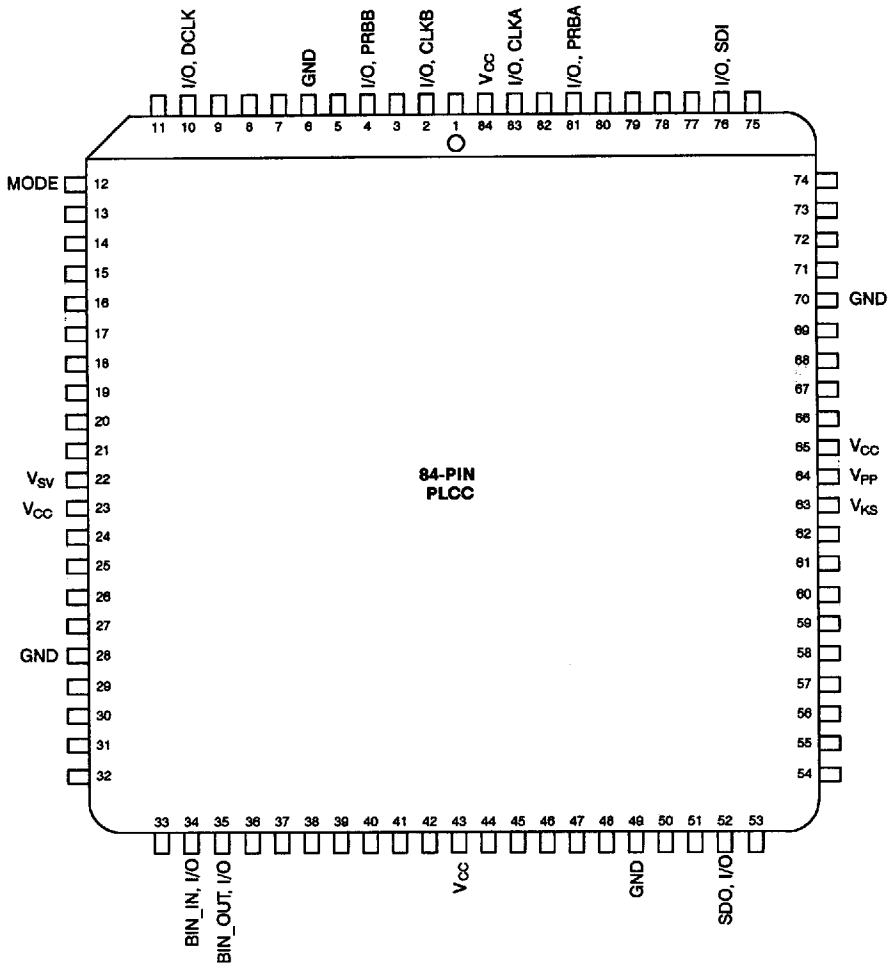



Notes:

1. $V_{PP}$ must be terminated to $V_{CC}$, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

## Package Pin Assignments: 84-Pin PLCC (Top View)

T-46-19-11

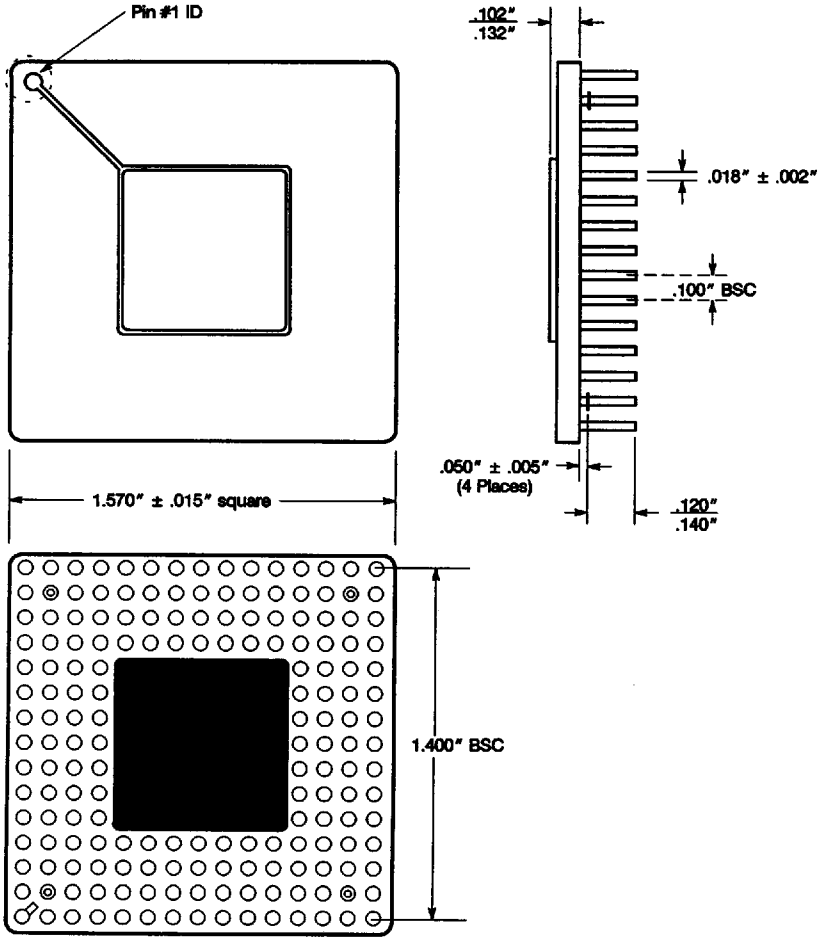



Notes:

1. $V_{PP}$ must be terminated to $V_{CC}$, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

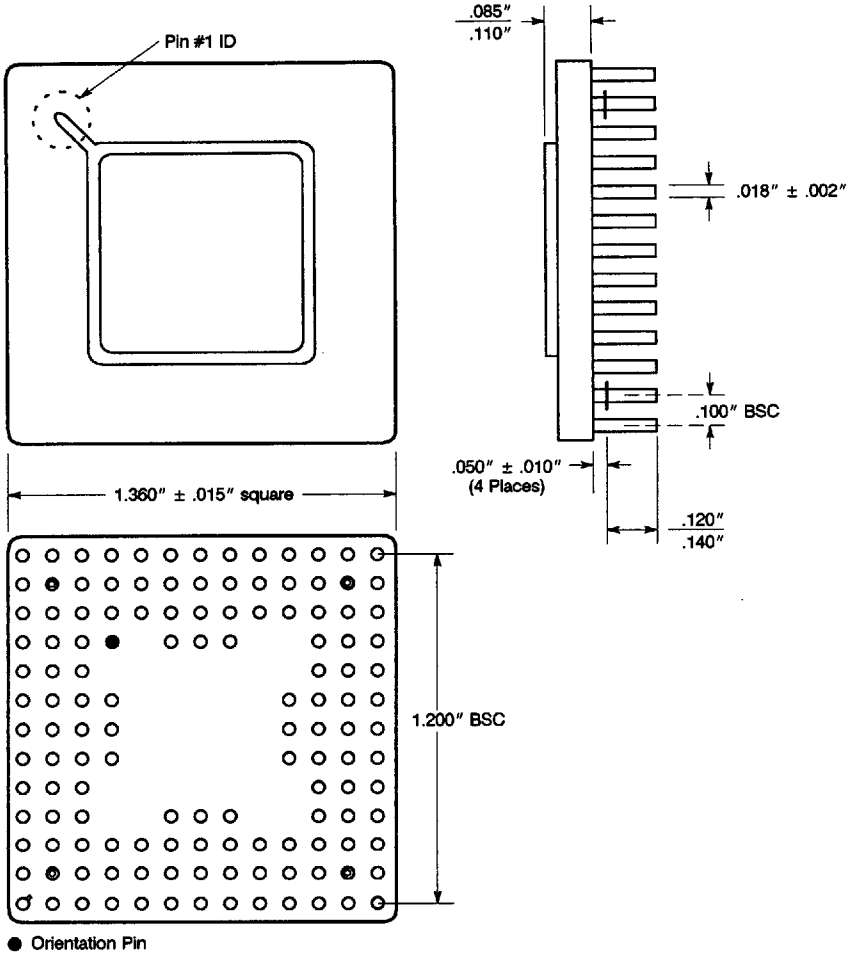
## Package Mechanical Details: 176-Pin CPGA

T-46-19-11



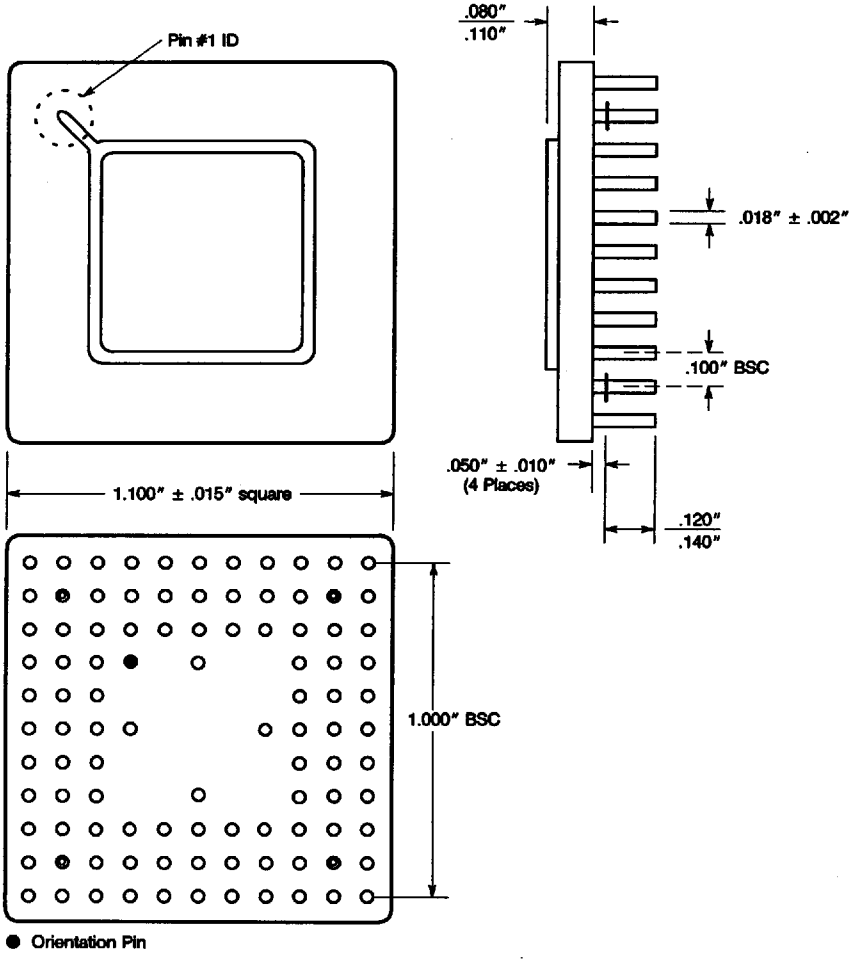
## Package Mechanical Details: 132-Pin CPGA

T-46-19-11



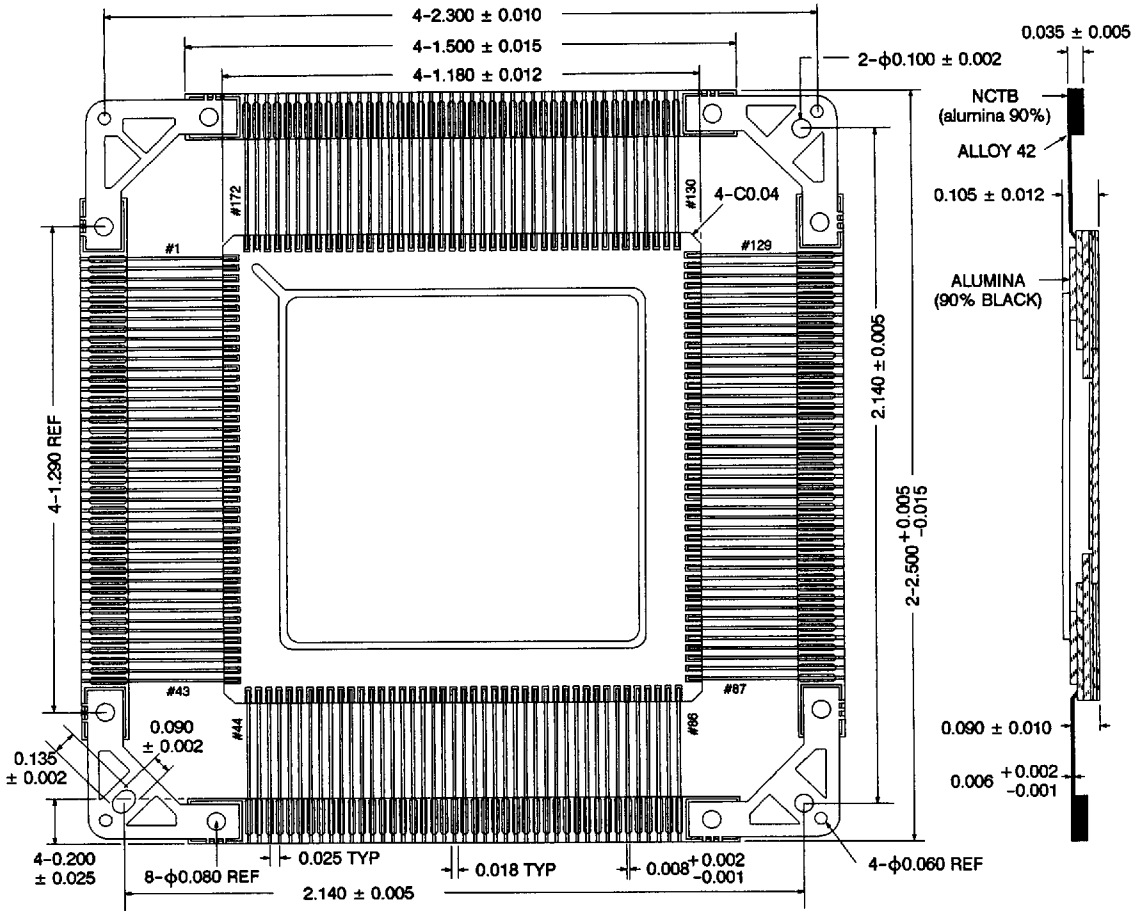
## Package Mechanical Details: 100-Pin CPGA

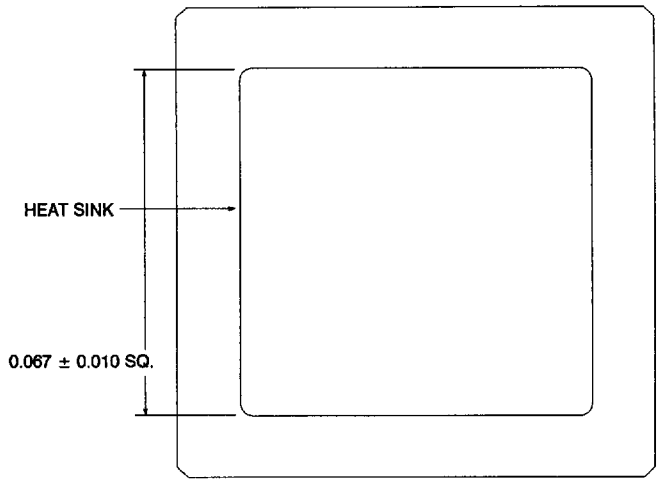
T-46-19-11



## Package Mechanical Details: 172-Pin CQFP

T-46-19-11



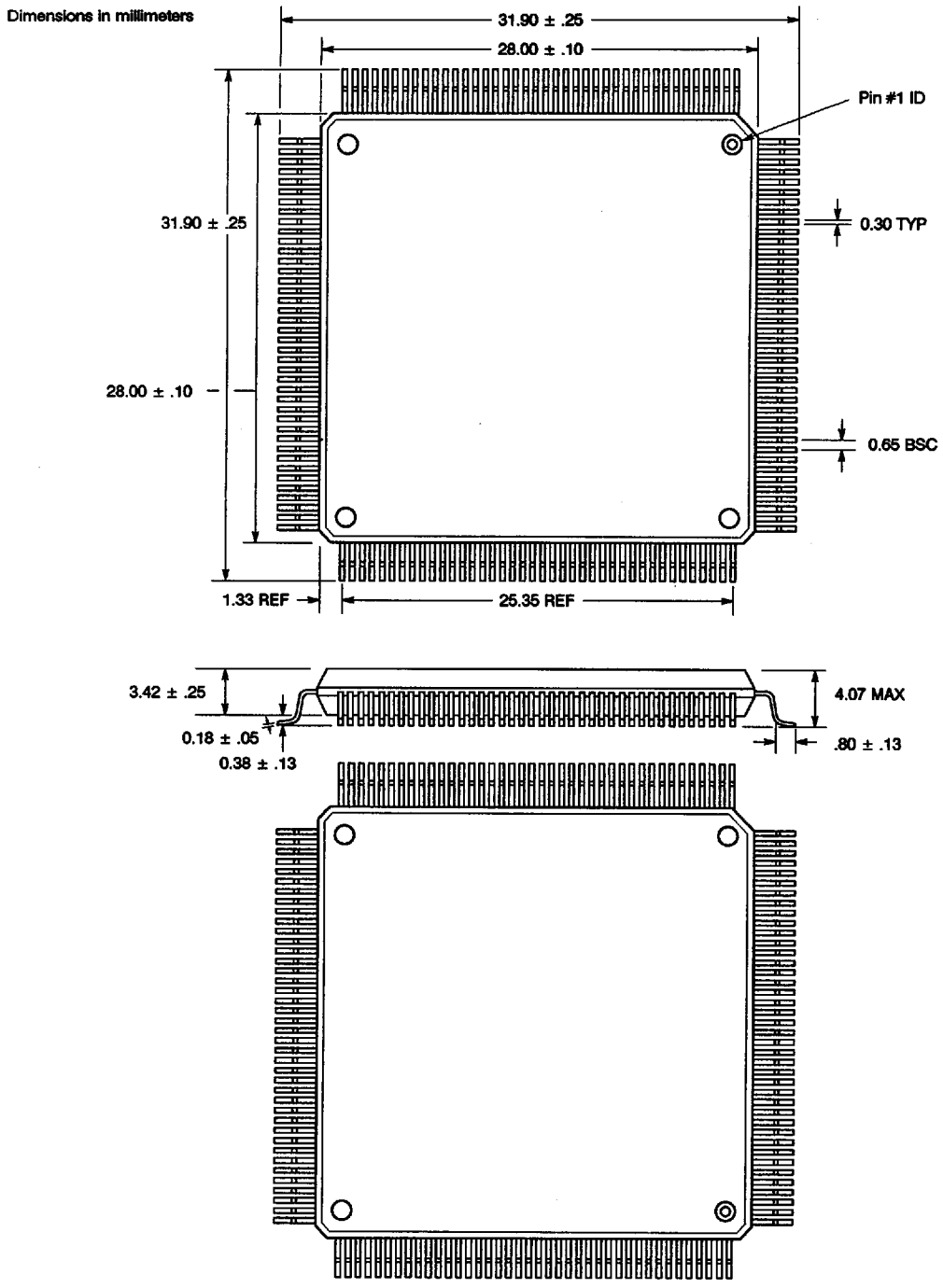

BOTTOM VIEW

**Notes:**

1. All exposed metalized areas and leads are gold plated 100 microinches (2.5 μ mm) min. thickness over 80 to 350 microinches 2.0 to 8.9 μ mm) thickness of nickel.
2. Seal ring area is connected to GNDA.
3. Die attach pad is connected to GNDA.
4. GNDQ (4 PLS) is connected to GNDA.
5. Tolerances unless otherwise specified: ±1% N.L.T. ±0.005.

## Package Mechanical Details: 160-Pin PQFP

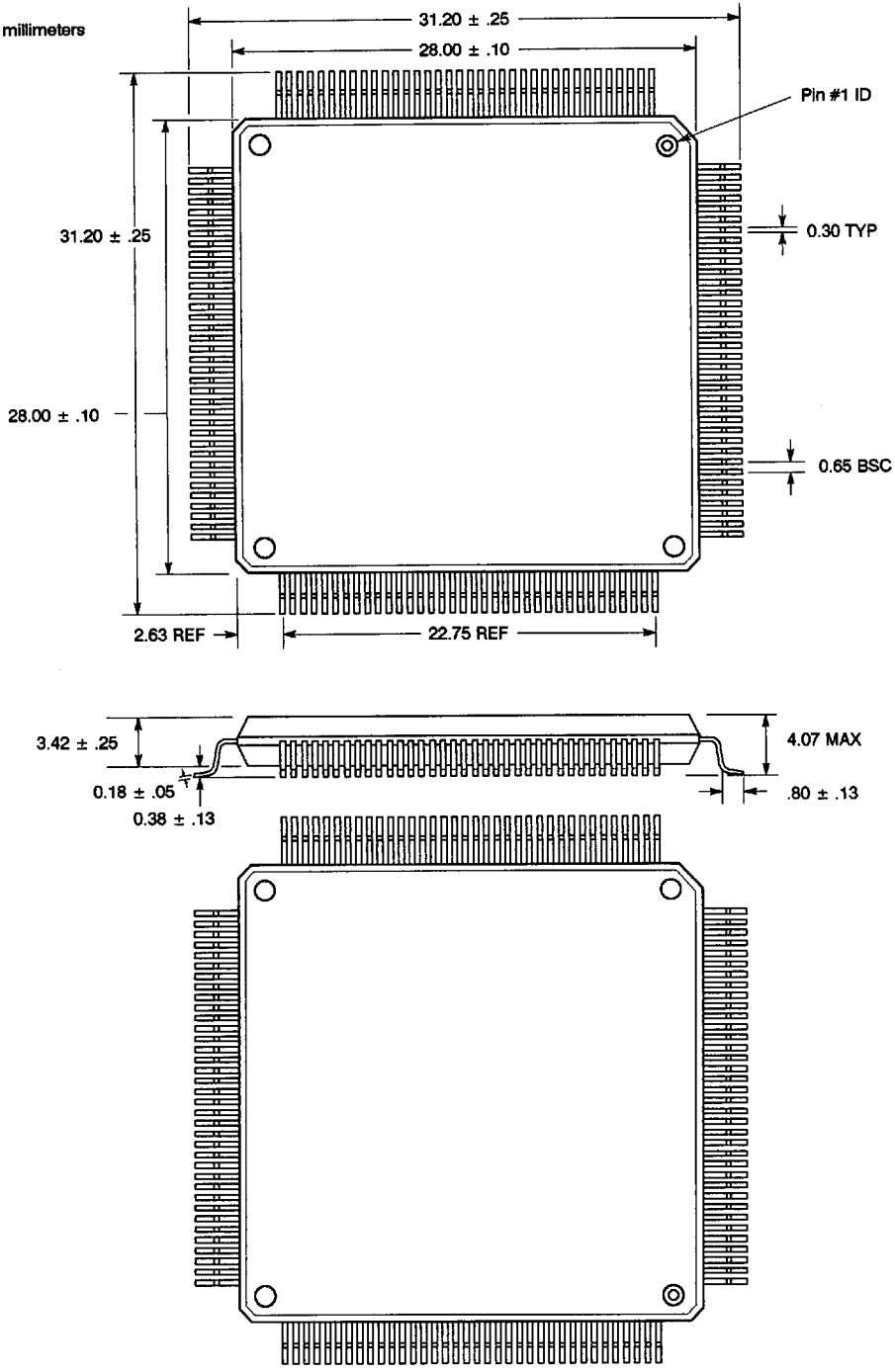
T-46-19-11



## Package Mechanical Details: 144-Pin PQFP

T-46-19-11

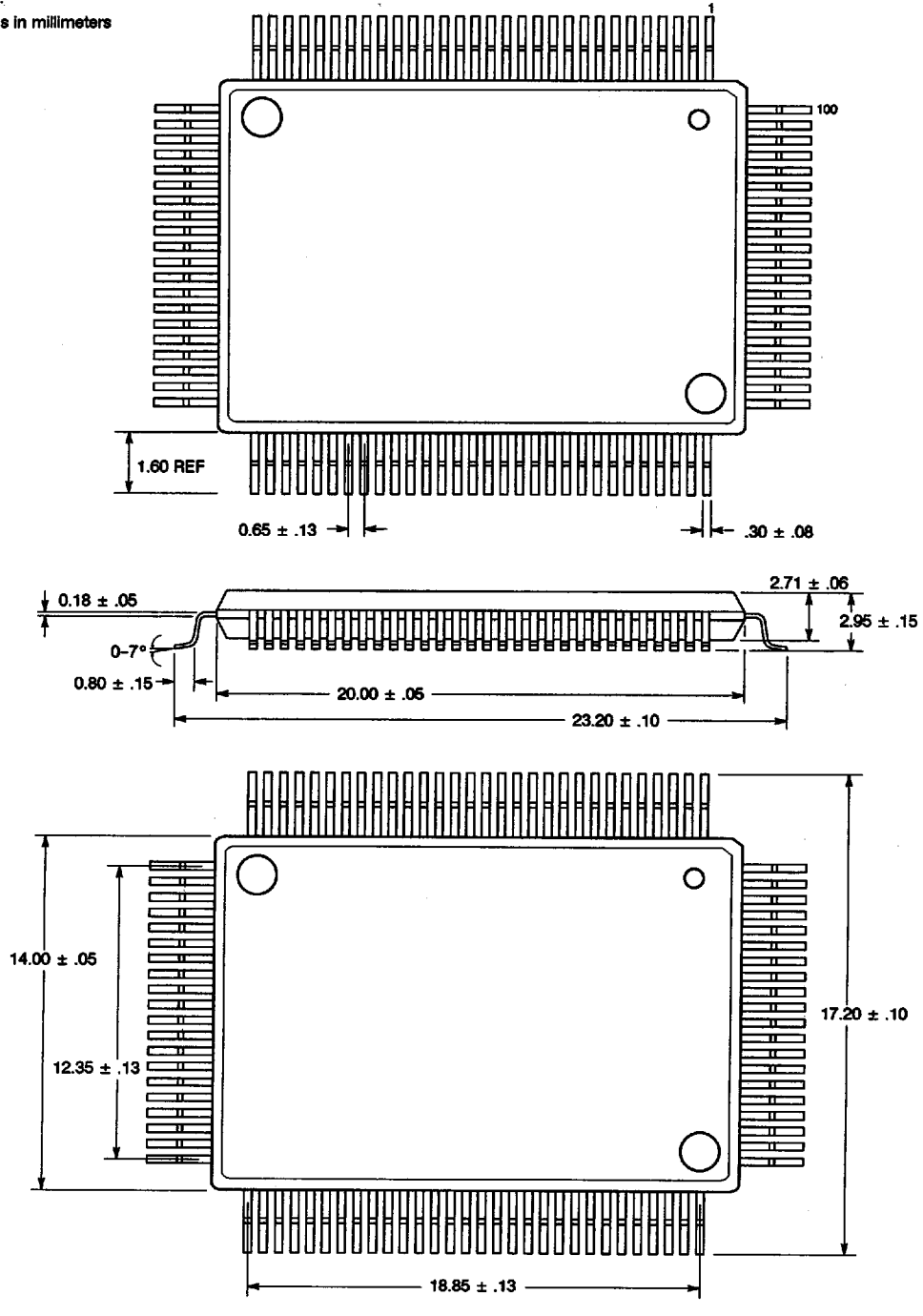
Dimensions in millimeters



## Package Mechanical Details: 100-Pin PQFP

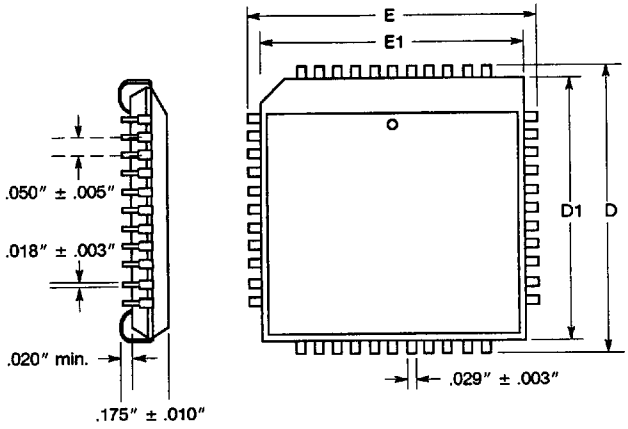
T-46-19-11

Dimensions in millimeters



## Package Mechanical Details: 84-Pin PLCC

T-46-19-11




| Lead Count | D, E | D1, E1 |
|---|---|---|
| 44 | .690" ± .005" | .655" ± .005" |
| 68 | .990" ± .005" | .955" ± .005" |
| 84 | 1.190" ± .005" | 1.155" ± .005" |

1