SEEQ

64K Electrically Erasable PROM

October 1989

Features

- **Full Military and Extended Temperature Range**
  - M52B33/M52B33H: –55° to 125° C
  - E52B33/E52B33H: – 40° to 85° C
- **10,000 Write Cycles/Byte Over Temperature**
- **Input Latches**
- **5 V ± 10% Vcc**
- **1 ms (52B33H) or 9 ms (52B33) TTL Byte Erase/Byte Write**
- **Power Up/Down Protection**
- **DiTrace®**
- **Fast Read Access Time—250 ns**
- **Infinite Number of Read Cycles**
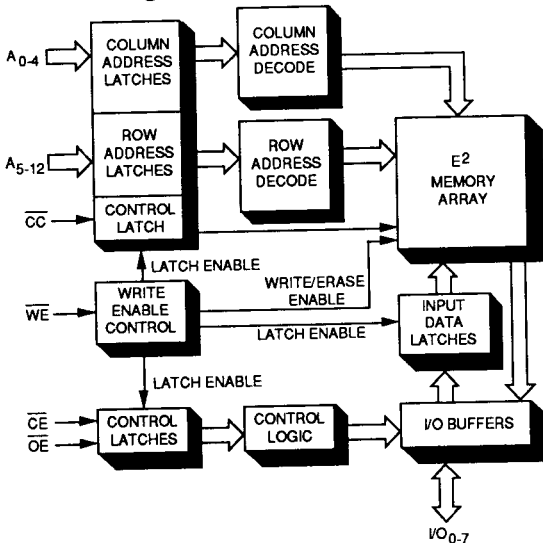- **JEDEC Approved Byte-Wide Memory Pinout**

Description

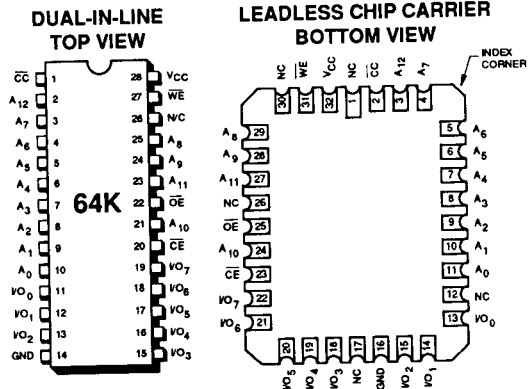SEEQ's M52B33 and E52B33 are 8192 x 8 bit, 5V electrically erasable programmable read only memories (EEPROMs) which are specified over the military and extended temperature range respectively. They have input latches on all addresses, data, and control (chip and output) lines. In addition, for applications requiring fast byte write time (1 ms), an E52B33H and M52B33H are available. Data is latched and electrically written by a TTL pulse on the Write Enable pin. Once written, there is no limit to the number of times data may be read. The erasure time is under 10 ms, and each byte may be erased and written a minimum of 10,000 times.

The E/M52B33 is available in a 28 pin cerdip or 32 pad leadless chip carrier. The pin configuration is to the JEDEC approved byte wide memory pinout for these two types of packages. These EEPROMs are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic configuration (the al-

Block Diagram

DiTrace is a registered trademark of SEEQ Technology Inc.

Pin Configuration

DUAL-IN-LINE TOP VIEW

LEADLESS CHIP CARRIER BOTTOM VIEW

Pin Names

A_0-A_4	ADDRESSES – COLUMN (LOWER ORDER BITS)
A_5 -A_{12}	ADDRESSES – ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O$_{0-7}$	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
$\overline{CC}$	CHIP CLEAR
N/C	NO CONNECT

SEEQ *Technology, Incorporated*

MD400009/C

6-15

teration of opening software in real-time) is made possible by this device. Applications will be found in military avionics systems, programmable character generators, self-calibrating instrument/machines, programmable industrial controllers, and an assortment of other systems. Designing the EEPROMs into eight and sixteen bit microprocessor system is also simplified by utilizing the fast access time zero wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance.

Device Operation

SEEQ E/M52B33 and E/M52B33H have six modes of operation (see Table 1) and require only TTL inputs to operate these modes.

To write into a particular location, that byte must first be erased. A memory location is erased by having valid addresses, Chip Enable at a TTL low, Output Enable at TTL high, and TTL highs (logical 1's) presented to all the I/O lines. Write Enable is then brought to a TTL low level to latch all the inputs. The erase operation requires under 10 ms. A write operation is the same as an erase except true data is presented to the I/O lines. The 52B33H performs the same as the E/M52B33 except that the byte erase/byte write time has been enhanced to 1 ms.

A characteristic of all EEPROMs is that the total number of write and erase cycles is not unlimited. The E/M52B33 is designed for applications requiring up to 10,000 write and erase cycles per byte over the temperature range. The write and erase cycling characteristics are completely byte independent. Adjacent bytes are not affected during write/erase cycling.

After the device is written, data is read by applying a TTL high to $\overline{WE}$, enabling the chip, and enabling the outputs.

Data is available, t_{CE} time after Chip Enable is applied or t_{AA} time from the addresses. System power may be reduced by placing the device into a standby mode. Raising Chip Enable to a TTL high will reduce the power consumption by over 60%.

DiTrace

SEEQ's family of EEPROMs incorporate a DiTrace field. The DiTrace feature is a method for storing production flow information in an extra row of EEPROM cells. As each major manufacturing operation is performed the DiTrace field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

Chip Clear

Certain applications may require all bytes to be erased simultaneously. See A.C. Operating Characteristics for TTL chip erase timing specifications.

Power Up/Down Considerations

SEEQ's "52B" E² family has internal circuitry to minimize false erase or write during system V_{cc} power up or down. This circuitry prevents writing or erasing under any one of the following conditions:

1. V_{cc} is less than 3 V.[1]
2. A negative Write Enable transition has not occurred when V_{cc} is between 3 V and 5 V.

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the Mode Selection table.

Mode Selection (Table 1)

Mode	Function (Pin)	$\overline{CE}$ (20)	$\overline{CC}$ (1)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13,15-19)
Read		V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}
Standby		V_{IH}	Don't Care	Don't Care	Don't Care	High Z
Byte Erase		V_{IL}	V_{IH}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write		V_{IL}	V_{IH}	V_{IH}	V_{IL}	D_{IN}
Chip Clear		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL} or V_{IH}
Write/Erase Inhibit		V_{IH}	Don't Care	Don't Care	Don't Care	High Z

NOTE:
1. Characterized. Not tested.

SeeQ Technology, Incorporated

Absolute Maximum Stress Ratings*

Temperature
  Storage .... −65°C to +150°C
  Under Bias .... −65°C to +135°C
D.C. Voltage applied to all Inputs or Outputs
  with respect to ground .... +6.0 V to −0.5 V
Undershoot/Overshoot pulse of less then 10 ns
(measured at 50% point) applied to all inputs or
  outputs with respect to ground .... (undershoot) −1.0 V
                                        (overshoot) + 7.0 V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

V_{CC} Supply Voltage	5 V ± 10%
Temperature Range: M52B33/M52B33H (Case)	−55°C to +125°C
E52B33/E52B33H (Ambient)	−40° C to +85° C

Endurance and Data Retention

| Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

D.C. Operating Characteristics During Read or Erase/Write

(Over the operating V_{CC} and temperature range)

Symbol	Parameter	Min.	Nom.	Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max.
I_{WE}	Write Enable Leakage Read Mode W/E Mode			10 10	μA μA	$\overline{WE} = V_{IH}$ $\overline{WE} = V_{IL}$
I_{CC1}	V_{CC} Standby Current		15	50	mA	$\overline{CE} = V_{IH}$
I_{CC2}	V_{CC} Active Current		50	120	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

NOTE: See next page for notes.

MILITARY

A.C. Operating Characteristics During Read (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Device Number Extension	M52B33 M52B33H Min.	Max.	E52B33 E52B33H Min.	Max.	Units	Test Conditions
t_{AA}	Address Access Time	−250		250		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
		−300		300		300	ns	
t_{CE}	Chip Enable to Data Valid	−250		250		250	ns	$\overline{OE} = V_{IL}$
		−300		300		300	ns	
t_{OE}[2]	Output Enable to Data Valid	−250		90		90	ns	$\overline{CE} = V_{IL}$
		−300		90		90	ns	
t_{DF}[3]	Output Enable to High Impedance	−250	0	70	0	70	ns	$\overline{CE} = V_{IL}$
		−300	0	70	0	70	ns	
t_{OH}	Output Hold	All	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$
C_{IN}/C_{OUT}[4]	Input/Output Capacitance	All		10		10	pF	$V_{IN} = 0$ V for C_{IN}, $V_{OUT} = 0$ V for C_{OUT}, $T_A = 25°C$

Read Cycle Timing
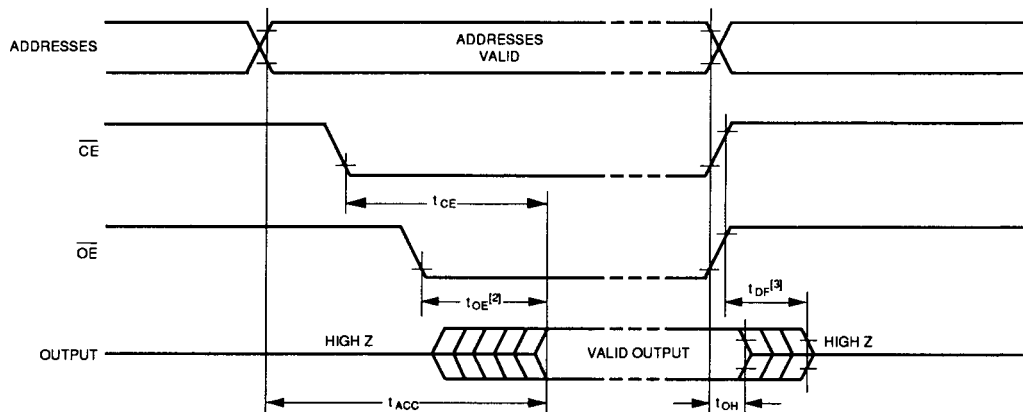
NOTES:

1. Nominal values are for $T_A = 25°$ C and $V_{CC} = 5.0$V.
2. $\overline{OE}$ may be delayed to $t_{AA} − t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{AA}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
4. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
5. After t_H, hold time, from $\overline{WE}$, the inputs $\overline{CE}$, $\overline{OE}$, CC, Address and Data are latched and are "Don't Cares" until t_{WR}, Write Recovery Time, after the trailing edge of $\overline{WE}$.
6. The Write Recovery Time, t_{WR}, is the time after the trailing edge of $\overline{WE}$ that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.
7. These are equivalent test conditions and actual test conditions are dependent on the tester.

seeq *Technology, Incorporated*

Equivalent A.C. Test Conditions[7]

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
  Inputs 1 V and 2 V
  Outputs 0.8 V and 2 V

A.C. Operating Characteristics During Write/Erase

(Over the operating V_{CC} and temperature range)

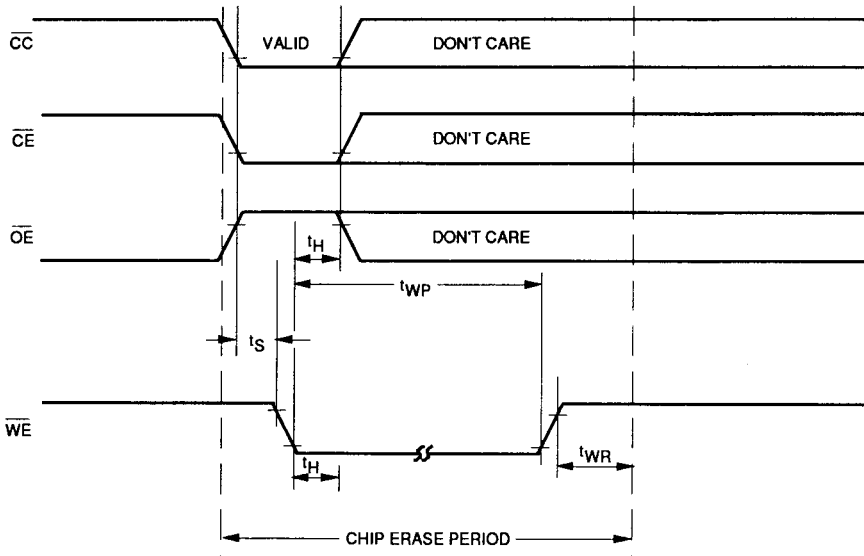| Symbol	Parameter	Min.	Max.	Units
t_S	$\overline{CE}$, $\overline{OE}$ or Address Setup to $\overline{WE}$	50		ns
t_{DS}	Data Setup to $\overline{WE}$	15		ns
t_H [5]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, Address or Data Change	50		ns
t_{WP}	Write Enable, ($\overline{WE}$) Pulse Width			
	Byte Modes — M52B33/E52B33	9		ms
	Byte Modes — M52B33H	1		ms
t_{WR} [6]	$\overline{WE}$ to Mode Change			
	$\overline{WE}$ to Next Byte Write/Erase Cycle	50		ns
	$\overline{WE}$ to Start of a Read Cycle	1		µs

Byte Erase or Byte Write Cycle Timing
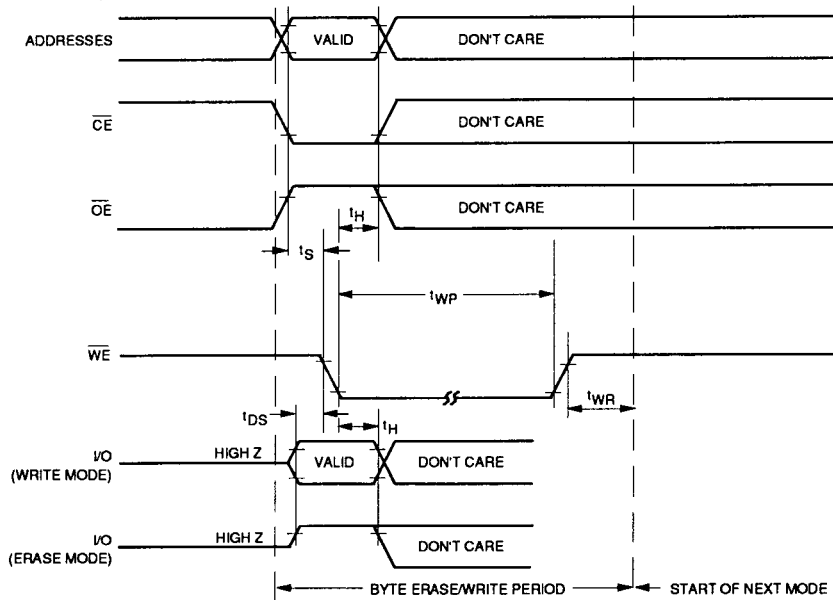
NOTES
See previous page for notes.

MILITARY

A.C. Operating Characteristics During Chip Erase.

(Over the operating V_{CC} and temperature range)

Symbol	Parameter	Min.	Max.	Units
t_S	$\overline{CC}$, $\overline{CE}$, $\overline{OE}$ Setup to $\overline{WE}$	50		ns
t_H [4]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, $\overline{CC}$ change	50		ns
t_{WP}	Write Enable ($\overline{WE}$) Pulse Width Chip Erase —M52B33/M52B33H Chip Erase — E52B33H/E52B33H	10		ms
t_{WR} [5]	$\overline{WE}$ to Mode change $\overline{WE}$ to Start of Next Byte Write Cycle	50		ns
	$\overline{WE}$ to Start of Read Cycle		1	µs

TTL Chip Erase Timing

NOTE: Address, Data are don't care during Chip Clear.

Ordering Information

D M 52B33 H – 250 /B

PACKAGE TYPE	OPERATING TEMPERATURE RANGE	PART TYPE	EEPROM BYTE WRITE TIME	ACCESS TIME	SCREENING OPTION
D – CERAMIC DIP L – LEADLESS CHIP CARRIER	E – –40° C to +85°C M – –55° C to +125° C	8K x 8 EEPROM	(BLANK) = STANDARD WRITE TIME H = FAST WRITE TIME	250 = 250 ns 300 = 300 ns	/B – MIL 883 CLASS B SCREENED

seeq Technology, Incorporated