Dual-Channel, 12-Bit 125 MSPS IF Sampling A/D Converter

AD10226

FEATURES

Two Independent 12-Bit, 125 MSPS ADCs
Channel-to-Channel Isolation, > 80 dB
AC-Coupled Signal Conditioning Included
Gain Flatness up to Nyquist, < 0.1 dB
Input VSWR 1.1:1 to Nyquist
80 dB Spurious-Free Dynamic Range
Two's Complement Output Format
3.3 V or 5 V CMOS-Compatible Output Levels
1.5 W Per Channel
Single-Ended or Differential Input
350 MHz Input Bandwidth

APPLICATIONS

Wireless and Wired Broadband Communications
Base Stations and "Zero-IF" or Direct IF Sampling Subsystems
Wireless Local Loop (WLL)
Local Multipoint Distribution Service (LMDS)
Radar and Satellite Subsystems

PRODUCT DESCRIPTION

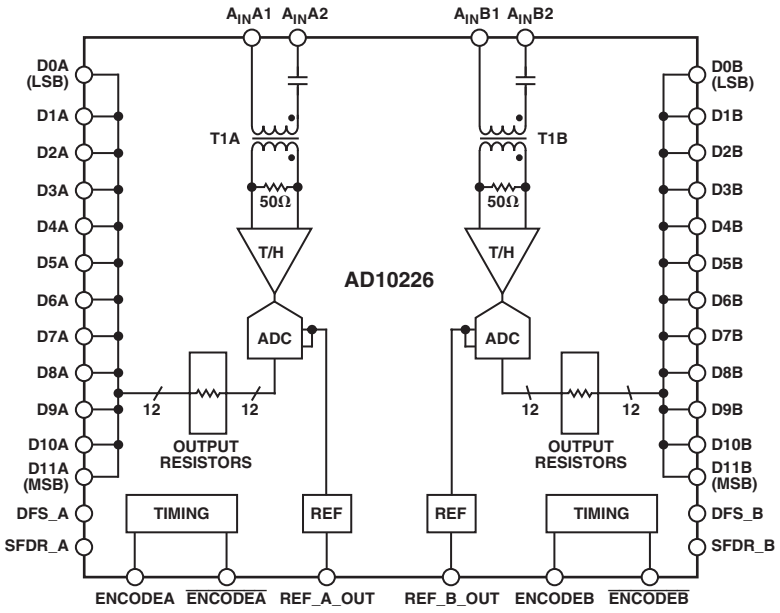
The AD10226 offers two complete ADC channels with on-module signal conditioning for improved dynamic performance. Each wide dynamic range ADC has a transformer coupled front end optimized for direct-IF sampling. The AD10226 has on-chip track-and-hold circuitry and utilizes an innovative architecture to achieve 12-bit, 125 MSPS performance. The AD10226 uses innovative high density circuit design to achieve exceptional performance, while still maintaining excellent isolation and providing for board area savings.

The AD10226 operates with 5.0 V analog supply and 3.3 V digital supply. Each channel is completely independent, allowing operation with independent ENCODE and analog inputs. The AD10226 is available in a 35 mm square 385-lead BGA package.

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate of 125 MSPS
2. Input signal conditioning included with full-power bandwidth to 350 MHz
3. Industry-leading IF sampling performance

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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AD10226–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS[1] (V_{DD} = 3.3 V, V_{CC} = 5.0 V; ENCODE = 125 MSPS, unless otherwise noted.)

Parameter	Temp	Test Level	Min	Typ	Max	Unit
RESOLUTION				12		Bits
DC ACCURACY						
Differential Nonlinearity[2]	Full	IV	–0.99	±0.3	+0.99	LSB
Integral Nonlinearity[2]	Full	IV	–1.3	±0.75	+1.3	LSB
No Missing Codes	Full	IV		Guaranteed		
Gain Error[3]	25°C	I	–9	±1	+9	% FS
Output Offset	25°C	I	–12	+2	+12	LSB
Gain Tempco	Full	V		100		ppm/°C
Offset Tempco	Full	V		–50		ppm/°C
ANALOG INPUT						
Input Voltage Range	25°C	V		1.84		V p-p
Input Impedance	25°C	V		50		Ω
Input VSWR[4]	Full	V		1.1:1	1.25:1	Ratio
Analog Input Bandwidth, High	Full	IV	300	350		MHz
Analog Input Bandwidth, Low	Full	IV	1			MHz
ANALOG REFERENCE						
Output Voltage	25°C	V		2.5		V
Load Current	25°C	V		5		mA
Tempco	Full	V		±80		ppm/°C
SWITCHING PERFORMANCE[5]						
Maximum Conversion Rate	Full	VI	125			MSPS
Minimum Conversion Rate	Full	IV			10	MSPS
Duty Cycle	Full	IV	45	50	55	%
Aperture Delay (t_A)	25°C	V		2.1		ns
Aperture Uncertainty (Jitter)	25°C	V		0.25		ps rms
Output Valid Time (t_V)[6]	Full	IV	3.0	4.5		ns
Output Propagation Delay (t_{PD})[6]	Full	IV		4.5	6.0	ns
Output Rise Time (t_R)	25°C	V		3.5		ns
Output Fall Time (t_F)	25°C	V		3.3		ns
DIGITAL INPUTS						
ENCODE Input Common-Mode	Full	IV		3.75		V
Differential Input (ENC, $\overline{\text{ENC}}$)	Full	IV		500		mV
Logic "1" Voltage	Full	IV	2.0			V
Logic "0" Voltage	Full	IV			0.8	V
Input Resistance	Full	IV	3	6		kΩ
Input Capacitance	25°C	V		3		pF
DIGITAL OUTPUTS						
Logic "1" Voltage[6]	Full	IV	3.1	3.3		V
Logic "0" Voltage[6]	Full	IV		0	0.2	V
Output Coding				Two's Complement		
POWER SUPPLY[7]						
Power Dissipation[8]	Full	VI		3040	3300	mW
Power Supply Rejection Ratio	Full	IV		±0.5	±5.0	mV/V
Total I (DV_{DD}) Current	Full	VI		40	60	mA
Total I (AV_{CC}) Current	Full	VI		540	650	mA

Parameter	Temp	Test Level	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio (SNR)[9] (Without Harmonics)						
f_{IN} = 10.3 MHz	25°C	I	66.5	68.5		dBFS
f_{IN} = 49 MHz	25°C	V		67		dBFS
f_{IN} = 71 MHz	25°C	I	63	66		dBFS
f_{IN} = 121 MHz	25°C	V		64		dBFS
f_{IN} = 250 MHz	25°C	V		60		dBFS
Signal-to-Noise Ratio (SINAD)[10] (With Harmonics)						
f_{IN} = 10.3 MHz	25°C	I	65.5	68		dBFS
f_{IN} = 49 MHz	25°C	V		66.5		dBFS
f_{IN} = 71 MHz	25°C	I	62.5	65		dBFS
f_{IN} = 121 MHz	25°C	V		62.5		dBFS
f_{IN} = 250 MHz	25°C	V		59.5		dBFS
Spurious-Free Dynamic Range[11]						
f_{IN} = 10 MHz	25°C	I	76.5	82		dBFS
f_{IN} = 41 MHz	25°C	V		77		dBFS
f_{IN} = 71 MHz	25°C	I	66	72		dBFS
f_{IN} = 121 MHz	25°C	V		71		dBFS
f_{IN} = 250 MHz	25°C	V		70		dBFS
Two-Tone Intermodulation Distortion[12] (IMD)						
f_{IN} = 29.3 MHz; f_{IN} = 30.3 MHz	25°C	V		78		dBc
f_{IN} = 150 MHz; f_{IN} = 151 MHz	25°C	V		70		dBc
Channel-to-Channel Isolation[13]						
f_{IN} = 121 MHz	Full	IV		85		dB

NOTES

[1]All ac specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially, with the analog input applied to $A_{IN}X1$ and $A_{IN}X2$ tied to ground.

[2]SFDR enabled (SFDR = 1) for DNL and INL specifications.

[3]Gain error measured at 10.3 MHz.

[4]Input VSWR, see TPC 14.

[5]See Figure 1, Timing Diagram.

[6]t_V and t_{PD} are measured from the transition points of the ENCODE input to the 50%/50% levels of the digital outputs swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of ±40 μA.

[7]Supply voltages should remain stable within ±5% for normal operation.

[8]Power dissipation measures with encode at rated speed.

[9]Analog input signal power at –1 dBFS; signal-to-noise (SNR) is the ratio of signal level to total noise (first six harmonics removed). ENCODE = 125 MSPS, SFDR mode = 1. SNR is reported in dBFS, related back to converter full-scale.

[10]Analog input signal power at –1 dBFS; signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise + harmonics. ENCODE = 125 MSPS. SINAD is reported in dBFS, related back to converter full-scale.

[11]Analog input signal equals –1 dBFS; SFDR is ratio of converter full-scale to worst spur.

[12]Both input tones at –7 dBFS; two-tone intermodulation distortion (IMD) rejection is the ratio of either tone to the worst third order intermod product.

[13]Channel-to-channel isolation tested with A channel/50 Ω terminated (A_{IN}A2) grounded and a full-scale signal applied to B channel (A_{IN}B2).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} . . . . . 6 V
V_{CC} . . . . . 6 V
Analog Inputs . . . . . 5 V p-p (18 dBm)
Digital Inputs . . . . . –0.5 V to V_{DD} + 0.5 V
Digital Output Current . . . . . 20 mA
Operating Temperature (Ambient) . . . . . –55°C to +125°C
Storage Temperature (Ambient) . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . 150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

385-Lead BGA Package:
The typical θ_{JA} of the module as determined by an IR scan is 26.25°C/W.

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested
II 100% production tested at 25°C and sample tested at specific temperatures
III Sample tested only
IV Parameter is guaranteed by design and characterization testing
V Parameter is a typical value only
VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range

Table I. Output Coding (V_{REF} = 2.5 V) (Two's Complement)

Code	A_{IN} (V)	Digital Output
+2047	+0.875	0111 1111 1111
.	.	.
.	.	.
0	0	0000 0000 0000
–1	–0.000427	1111 1111 1111
.	.	.
.	.	.
–2048	–0.875	1000 0000 0000

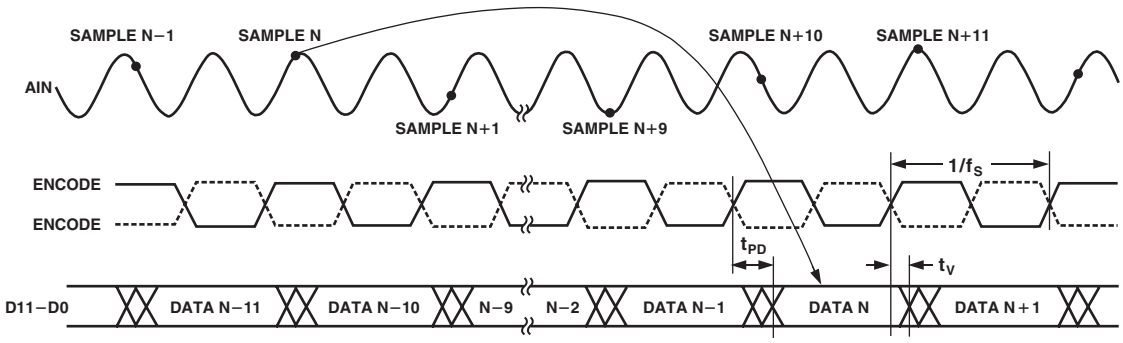


Figure 1. Timing Diagram

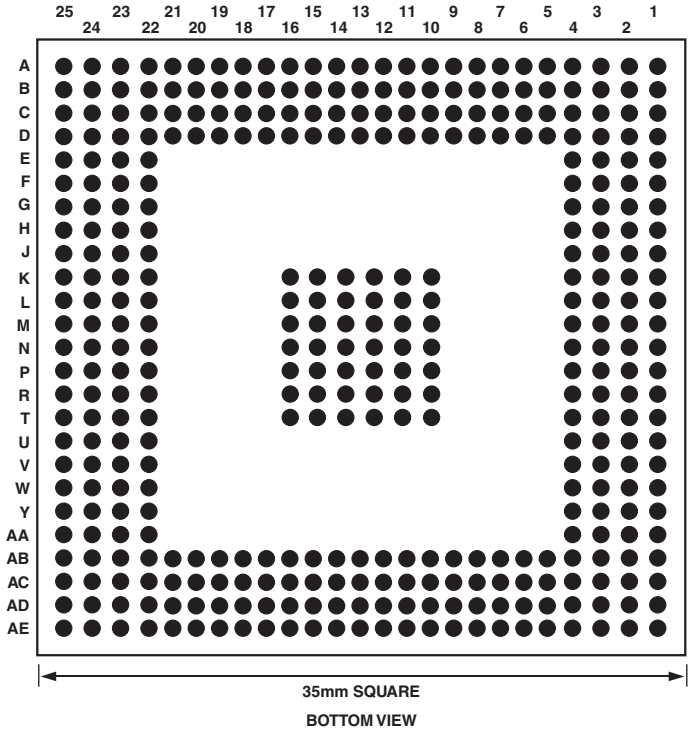
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD10226AB	–25°C to +85°C (Ambient)	385-Lead BGA (35 mm × 35 mm)	B-385
AD10226/PCB	25°C	Evaluation Board with AD10226AB	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD10226 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Mnemonic	Function
AGNDA	A Channel Analog Ground. A and B grounds should be connected as close to the device as possible.
REF_A_OUT	A Channel Internal Voltage Reference
NC	No connection
A_{IN}A1	Analog Input for A side ADC (– input)
A_{IN}A2	Analog Input for A side ADC (+ input)
AV_{CC}A	Analog Positive Supply Voltage (nominally 5.0 V)
DGNDA	A Channel Digital Ground
D11A–D0A	Digital Outputs for ADC A. D0 (LSB)
$\overline{\text{ENCODEA}}$	Complement of ENCODE
ENCODEA	Data conversion initiated on the rising edge of ENCODE input.
DV_{CC}A	Digital Positive Supply Voltage (nominally 3.3 V)
DGNDB	B Channel Digital Ground
D11B–D0B	Digital Outputs for ADC B. D0 (LSB)
AGNDB	B Channel Analog Ground. A and B grounds should be connected as close to the device as possible.
DV_{CC}B	Digital Positive Supply Voltage (nominally 3.3 V)
$\overline{\text{ENCODEB}}$	Complement of ENCODE
ENCODEB	Data conversion initiated on rising edge of ENCODE input.
REF_B_OUT	B Channel Internal Voltage Reference
A_{IN}B1	Analog Input for B side ADC (– input)
A_{IN}B2	Analog Input for B side ADC (+ input)
AV_{CC}B	Analog Positive Supply Voltage (nominally 5.0 V)
DFS	Data format select. Low = Two's Complement, High = Binary.
SFDR Mode	CMOS control pin that enables (SFDR MODE = 1) a proprietary circuit that may improve the spurious free dynamic range (SFDR) performance. It is useful in applications where the dynamic range of the system is limited by discrete spurious frequency content caused by nonlinearities in the ADC transfer function. SFDR Mode = 0 for normal operation.

385-LEAD BGA PINOUT

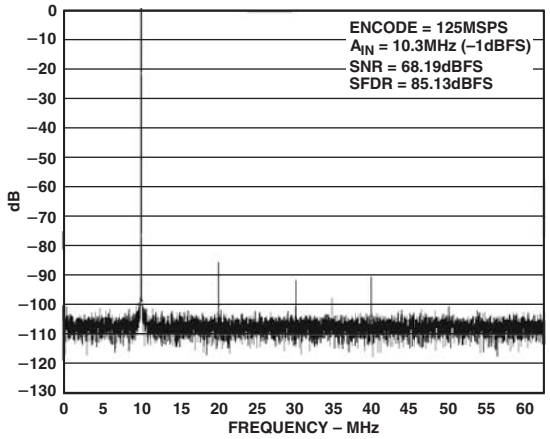
Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A1	AGNDA	C16	$AV_{CC}B$	H24	AGNDB	N16	AGNDB	V24	DB3	AC13	DGNDA
A2	AGNDA	C17	AGNDB	H25	AGNDB	N22	AGNDB	V25	DB3	AC14	DGNDB
A3	AGNDA	C18	$AV_{CC}B$	J1	$AV_{CC}A$	N23	AGNDB	W1	DA8	AC15	DB11
A4	AGNDA	C19	DNC	J2	$AV_{CC}A$	N24	AGNDB	W2	DA8	AC16	DB10
A5	AGNDA	C20	DNC	J3	$AV_{CC}A$	N25	AGNDB	W3	DA8	AC17	DB9
A6	AGNDA	C21	AGNDB	J4	$AV_{CC}A$	P1	AGNDA	W4	DA8	AC18	DB8
A7	DNC	C22	AGNDB	J22	REF_B_OUT	P2	AGNDA	W22	DB4	AC19	DB7
A8	DNC	C23	AGNDB	J23	REF_B_OUT	P3	AGNDA	W23	DB4	AC20	DB6
A9	AGNDA	C24	AGNDB	J24	REF_B_OUT	P4	AGNDA	W24	DB4	AC21	DGNDB
A10	$AV_{CC}A$	C25	AGNDB	J25	REF_B_OUT	P10	AGNDA	W25	DB4	AC22	DGNDB
A11	REF_A_OUT	D1	AGNDA	K1	AGNDA	P11	AGNDA	Y1	DA7	AC23	DGNDB
A12	AGNDA	D2	AGNDA	K2	AGNDA	P12	AGNDA	Y2	DA7	AC24	DGNDB
A13	DNC	D3	AGNDA	K3	AGNDA	P13	DNC	Y3	DA7	AC25	DGNDB
A14	AGNDB	D4	AGNDA	K4	AGNDA	P14	AGNDB	Y4	DA7	AD1	DGNDA
A15	AGNDB	D5	AGNDA	K10	SFDR_MODE_A	P15	AGNDB	Y22	DB5	AD2	DGNDA
A16	$AV_{CC}B$	D6	AGNDA	K11	AGNDA	P16	AGNDB	Y23	DB5	AD3	DGNDA
A17	AGNDB	D7	$A_{IN}A2$	K12	AGNDA	P22	$DV_{CC}B$	Y24	DB5	AD4	DGNDA
A18	$AV_{CC}B$	D8	$A_{IN}A1$	K13	DNC	P23	$DV_{CC}B$	Y25	DB5	AD5	DGNDA
A19	DNC	D9	AGNDA	K14	AGNDB	P24	$DV_{CC}B$	AA1	DGNDA	AD6	DA6
A20	DNC	D10	$AV_{CC}A$	K15	AGNDB	P25	$DV_{CC}B$	AA2	DGNDA	AD7	DA5
A21	AGNDB	D11	REF_A_OUT	K16	SFDR_MODE_B	P25	$DV_{CC}B$	AA3	DGNDA	AD8	DA4
A22	AGNDB	D12	AGNDA	K22	AGNDB	R1	$DV_{CC}A$	AA4	DGNDA	AD9	DA3
A23	AGNDB	D13	DNC	K23	AGNDB	R2	$DV_{CC}A$	AA22	DGNDB	AD10	DA2
A24	AGNDB	D14	AGNDB	K24	AGNDB	R3	$DV_{CC}A$	AA23	DGNDB	AD11	DA1
A25	AGNDB	D15	AGNDB	K25	AGNDB	R4	$DV_{CC}A$	AA24	DGNDB	AD12	DA0
B1	AGNDA	D16	$AV_{CC}B$	L1	AGNDA	R10	AGNDA	AA25	DGNDB	AD13	DGNDA
B2	AGNDA	D17	AGNDB	L2	AGNDA	R11	AGNDA	AB1	OVRA	AD14	DGNDB
B3	AGNDA	D18	$AV_{CC}B$	L3	AGNDA	R12	AGNDA	AB2	OVRA	AD15	DB11
B4	AGNDA	D19	$A_{IN}B2$	L4	AGNDA	R13	DNC	AB3	OVRA	AD16	DB10
B5	AGNDA	D20	$A_{IN}B1$	L10	DFS_A	R14	AGNDB	AB4	OVRA	AD17	DB9
B6	AGNDA	D21	AGNDB	L11	AGNDA	R15	AGNDB	AB5	DGNDA	AD18	DB8
B7	DNC	D22	AGNDB	L12	AGNDA	R16	AGNDB	AB6	DA6	AD19	DB7
B8	DNC	D23	AGNDB	L13	DNC	R22	DB0	AB7	DA5	AD20	DB6
B9	AGNDA	D24	AGNDB	L14	AGNDB	R23	DB0	AB8	DA4	AD21	DGNDB
B10	$AV_{CC}A$	D25	AGNDB	L15	AGNDB	R24	DB0	AB9	DA3	AD22	DGNDB
B11	REF_A_OUT	E1	AGNDA	L16	DFS_B	R25	DB0	AB10	DA2	AD23	DGNDB
B12	AGNDA	E2	AGNDA	L22	ENCBB	T1	DA11	AB11	DA1	AD24	DGNDB
B13	DNC	E3	AGNDA	L23	ENCBB	T2	DA11	AB12	DA0	AD25	DGNDB
B14	AGNDB	E4	AGNDA	L24	ENCBB	T3	DA11	AB13	DGNDA	AE1	DGNDA
B15	AGNDB	E22	AGNDB	L25	ENCBB	T4	DA11	AB14	DGNDB	AE2	DGNDA
B16	$AV_{CC}B$	E23	AGNDB	M1	ENCAB	T10	$AV_{CC}A$	AB15	DB11	AE3	DGNDA
B17	AGNDB	E24	AGNDB	M2	ENCAB	T11	AGNDA	AB16	DB10	AE4	DGNDA
B18	$AV_{CC}B$	E25	AGNDB	M3	ENCAB	T12	AGNDA	AB17	DB9	AE5	DGNDA
B19	DNC	F1	AGNDA	M4	ENCAB	T13	DNC	AB18	DB8	AE6	DA6
B20	DNC	F2	AGNDA	M10	AGNDA	T14	$AV_{CC}B$	AB19	DB7	AE7	DA5
B21	AGNDB	F3	AGNDA	M11	AGNDA	T15	GAIN_B	AB20	DB6	AE8	DA4
B22	AGNDB	F4	AGNDA	M12	AGNDA	T16	AGNDB	AB21	DGNDB	AE9	DA3
B23	AGNDB	F22	AGNDB	M13	DNC	T22	DB1	AB22	OVRB	AE10	DA2
B24	AGNDB	F23	AGNDB	M14	AGNDB	T23	DB1	AB23	OVRB	AE11	DA1
B25	AGNDB	F24	AGNDB	M15	AGNDB	T24	DB1	AB24	OVRB	AE12	DA0
C1	AGNDA	F25	AGNDB	M16	AGNDB	T25	DB1	AB25	OVRB	AE13	DGNDA
C2	AGNDA	G1	AGNDA	M22	ENCB	U1	DA10	AC1	DGNDA	AE14	DGNDB
C3	AGNDA	G2	AGNDA	M23	ENCB	U2	DA10	AC2	DGNDA	AE15	DB11
C4	AGNDA	G3	AGNDA	M24	ENCB	U3	DA10	AC3	DGNDA	AE16	DB10
C5	AGNDA	G4	AGNDA	M25	ENCB	U4	DA10	AC4	DGNDA	AE17	DB9
C6	AGNDA	G22	AGNDB	N1	ENCA	U22	DB2	AC5	DGNDA	AE18	DB8
C7	DNC	G23	AGNDB	N2	ENCA	U23	DB2	AC6	DA6	AE19	DB7
C8	DNC	G24	AGNDB	N3	ENCA	U24	DB2	AC7	DA5	AE20	DB6
C9	AGNDA	G25	AGNDB	N4	ENCA	U25	DB2	AC8	DA4	AE21	DGNDB
C10	$AV_{CC}A$	H1	AGNDA	N10	GAIN_A	V1	DA9	AC9	DA3	AE22	DGNDB
C11	REF_A_OUT	H2	AGNDA	N11	AGNDA	V2	DA9	AC10	DA2	AE23	DGNDB
C12	AGNDA	H3	AGNDA	N12	AGNDA	V3	DA9	AC11	DA1	AE24	DGNDB
C13	DNC	H4	AGNDA	N13	DNC	V4	DA9	AC12	DA0	AE25	DGNDB
C14	AGNDB	H22	AGNDB	N14	AGNDB	V22	DB3				
C15	AGNDB	H23	AGNDB	N15	AGNDB	V23	DB3				

385-LEAD BGA PINOUT (Top View, PCB Footprint)

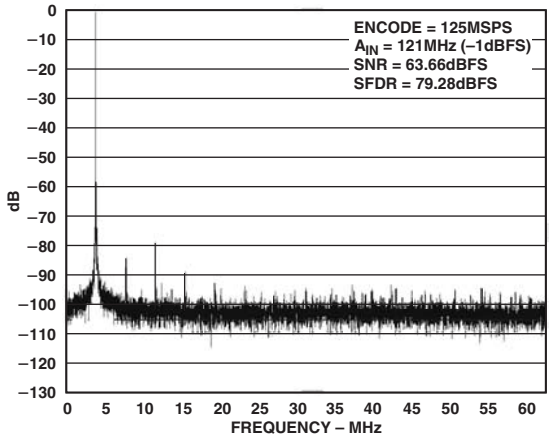
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	AGNDA	AGNDA	AGNDA	AGNDA	AGNDA	AGNDA	DNC	DNC	AGNDA	$AV_{CC}A$	REF_A_OUT	AGNDA	DNC	AGNDB	AGNDB	$AV_{CC}B$	AGNDB	$AV_{CC}B$	DNC	DNC	AGNDB	AGNDB	AGNDB	AGNDB	AGNDB
B	AGNDA	AGNDA	AGNDA	AGNDA	AGNDA	AGNDA	DNC	DNC	AGNDA	$AV_{CC}A$	REF_A_OUT	AGNDA	DNC	AGNDB	AGNDB	$AV_{CC}B$	AGNDB	$AV_{CC}B$	DNC	DNC	AGNDB	AGNDB	AGNDB	AGNDB	AGNDB
C	AGNDA	AGNDA	AGNDA	AGNDA	AGNDA	AGNDA	DNC	DNC	AGNDA	$AV_{CC}A$	REF_A_OUT	AGNDA	DNC	AGNDB	AGNDB	$AV_{CC}B$	AGNDB	$AV_{CC}B$	DNC	DNC	AGNDB	AGNDB	AGNDB	AGNDB	AGNDB
D	AGNDA	AGNDA	AGNDA	AGNDA	AGNDA	AGNDA	$A_{IN}A2$	$A_{IN}A1$	AGNDA	$AV_{CC}A$	REF_A_OUT	AGNDA	DNC	AGNCB	AGNCB	$AV_{CC}B$	AGNCB	$AV_{CC}B$	$A_{IN}B2$	$A_{IN}B1$	AGNDB	AGNDB	AGNDB	AGNDB	AGNDB
E	AGNDA	AGNDA	AGNDA	AGNDA																		AGNDB	AGNDB	AGNDB	AGNDB
F	AGNDA	AGNDA	AGNDA	AGNDA																		AGNDB	AGNDB	AGNDB	AGNDB
G	AGNDA	AGNDA	AGNDA	AGNDA																		AGNDB	AGNDB	AGNDB	AGNDB
H	AGNDA	AGNDA	AGNDA	AGNDA																		AGNDB	AGNDB	AGNDB	AGNDB
J	$AV_{CC}A$	$AV_{CC}A$	$AV_{CC}A$	$AV_{CC}A$																		REF_B_OUT	REF_B_OUT	REF_B_OUT	REF_B_OUT
K	AGNDA	AGNDA	AGNDA	AGNDA						SFDR Mode A	AGNDA	AGNDA	DNC	AGNDB	AGNDB	SFDR Mode B						AGNDB	AGNDB	AGNDB	AGNDB
L	AGNDA	AGNDA	AGNDA	AGNDA						DFS_A	AGNDA	AGNDA	DNC	AGNDB	AGNDB	DFS_B						ENCBB	ENCBB	ENCBB	ENCBB
M	ENCAB	ENCAB	ENCAB	ENCAB						AGNDA	AGNDA	AGNDA	DNC	AGNDB	AGNDB	AGNDB						ENCB	ENCB	ENCB	ENCB
N	ENCA	ENCA	ENCA	ENCA						AGNDA	AGNDA	AGNDA	DNC	AGNDB	AGNDB	AGNDB						AGNDB	AGNDB	AGNDB	AGNDB
P	AGNDA	AGNDA	AGNDA	AGNDA						AGNDA	AGNDA	AGNDA	DNC	AGNDB	AGNDB	AGNDB						$DV_{CC}B$	$DV_{CC}B$	$DV_{CC}B$	$DV_{CC}B$
R	$DV_{CC}A$	$DV_{CC}A$	$DV_{CC}A$	$DV_{CC}A$						AGNDA	AGNDA	AGNDA	DNC	AGNDB	AGNDB	AGNDB						DB0	DB0	DB0	DB0
T	DA11	DA11	DA11	DA11						$AV_{CC}B$	AGNDA	AGNDA	DNC	$AV_{CC}B$	AGNDB	AGNDB						DB1	DB1	DB1	DB1
U	DA10	DA10	DA10	DA10																		DB2	DB2	DB2	DB2
V	DA9	DA9	DA9	DA9																		DB3	DB3	DB3	DB3
W	DA8	DA8	DA8	DA8																		DB4	DB4	DB4	DB4
Y	DA7	DA7	DA7	DA7																		DB5	DB5	DB5	DB5
AA	DGNDA	DGNDA	DGNDA	DGNDA																		DGNDB	DGNDB	DGNDB	DGNDB
AB	OVRA	OVRA	OVRA	OVRA	DGNDA	DA6	DA5	DA4	DA3	DA2	DA1	DA0	DGNDA	DGNDB	DB11	DB10	DB9	DB8	DB7	DB6	DGNDB	OVRB	OVRB	OVRB	OVRB
AC	DGNDA	DGNDA	DGNDA	DGNDA	DGNDA	DA6	DA5	DA4	DA3	DA2	DA1	DA0	DGNDA	DGNDB	DB11	DB10	DB9	DB8	DB7	DB6	DGNDB	DGNDB	DGNDB	DGNDB	DGNDB
AD	DGNDA	DGNDA	DGNDA	DGNDA	DGNDA	DA6	DA5	DA4	DA3	DA2	DA1	DA0	DGNDA	DGNDB	DB11	DB10	DB9	DB8	DB7	DB6	DGNDB	DGNDB	DGNDB	DGNDB	DGNDB
AE	DGNDA	DGNDA	DGNDA	DGNDA	DGNDA	DA6	DA5	DA4	DA3	DA2	DA1	DA0	DGNDA	DGNDB	DB11	DB10	DB9	DB8	DB7	DB6	DGNDB	DGNDB	DGNDB	DGNDB	DGNDB

DNC = DO NOT CONNECT

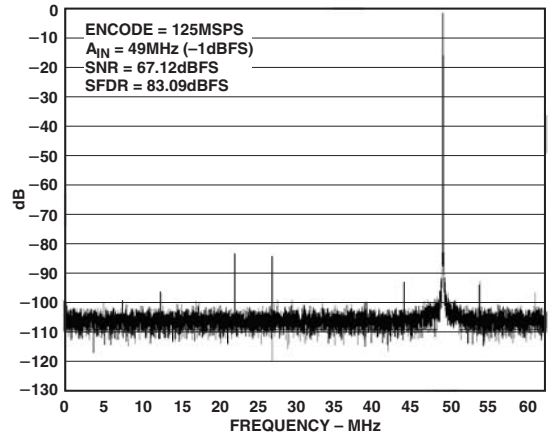
AD10226 – Typical Performance Characteristics



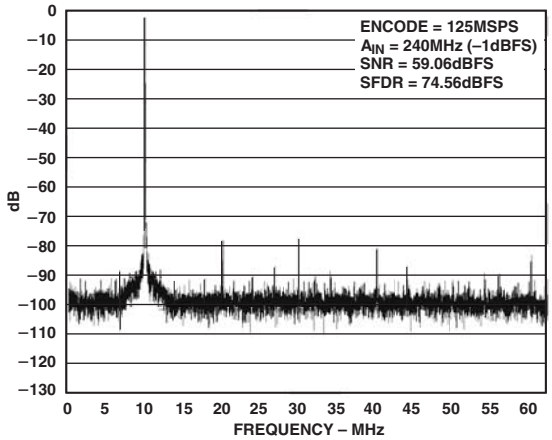
TPC 1. Single Tone @ 10.3 MHz



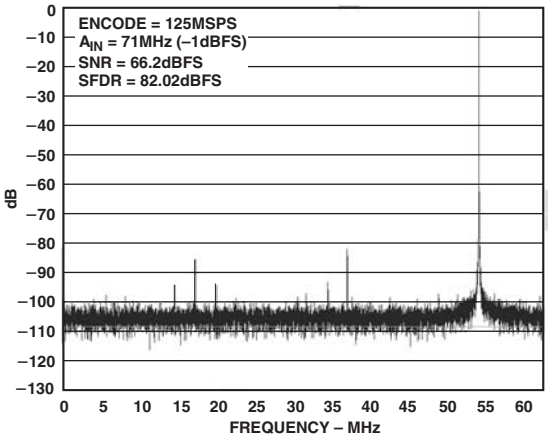
TPC 4. Single Tone @ 121 MHz



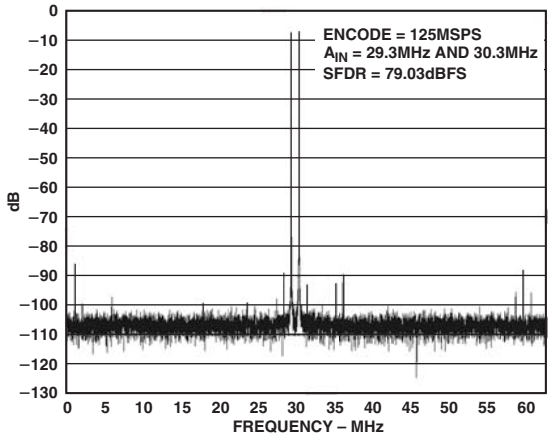
TPC 2. Single Tone @ 49 MHz



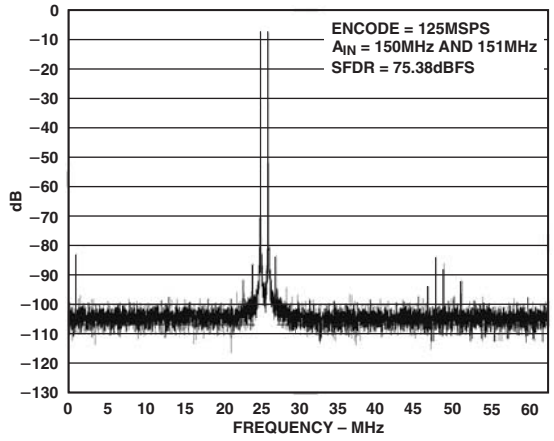
TPC 5. Single Tone @ 240 MHz



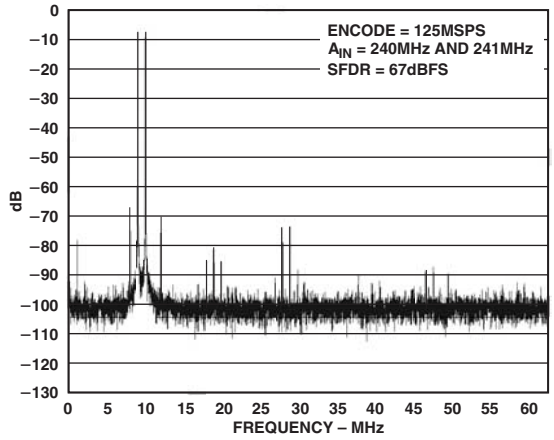
TPC 3. Single Tone @ 71 MHz



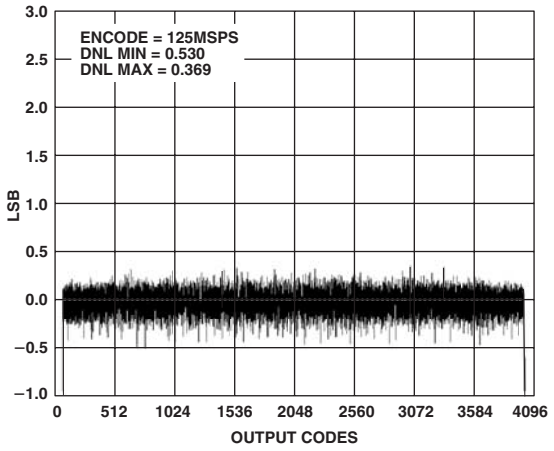
TPC 6. Two Tone @ 29/30 MHz



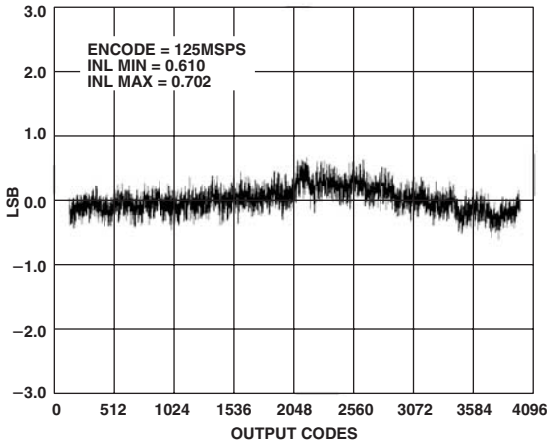
TPC 7. Two Tone @ 150/151 MHz



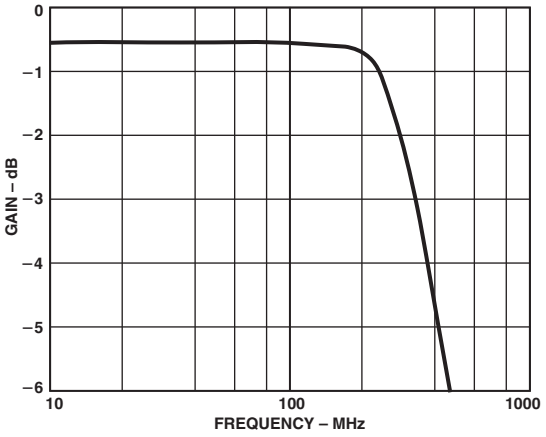
TPC 8. Two Tone @ 240/241 MHz



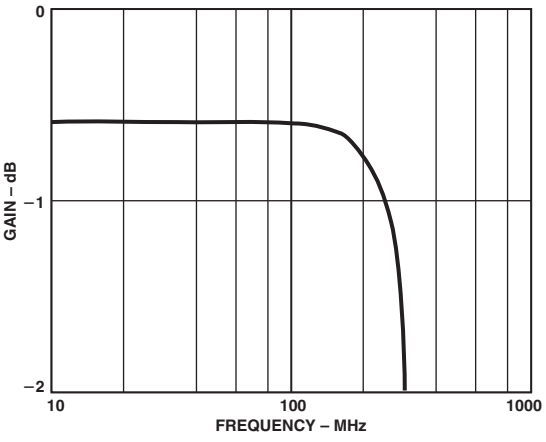
TPC 9. Differential Nonlinearity



TPC 10. Integral Nonlinearity

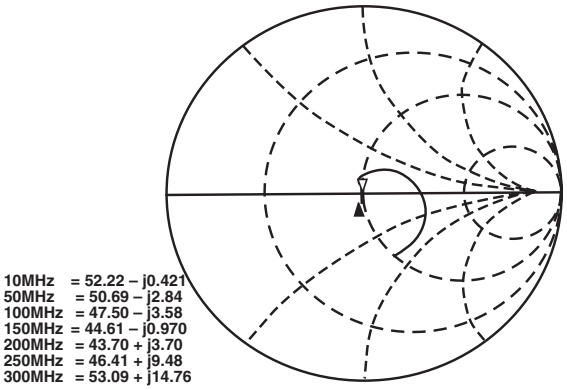


TPC 11. Frequency Response

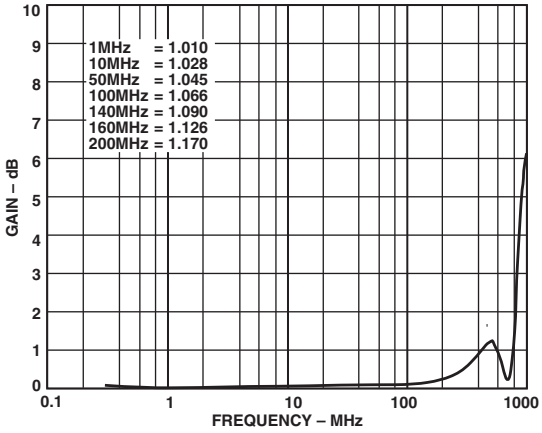


TPC 12. Gain Flatness*

*Gain flatness measurement is performed by applying a constant voltage at the device input.

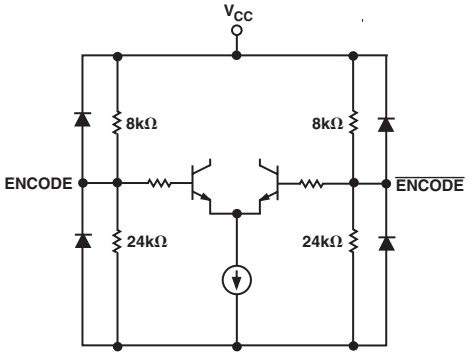


TPC 13. Input Impedance S11

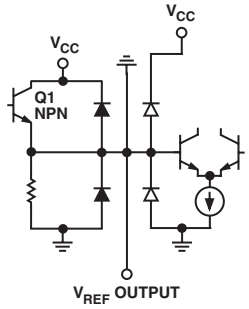


TPC 14. Voltage Standing Wave Ratio (VSWR)

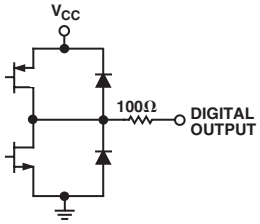
Equivalent Circuits



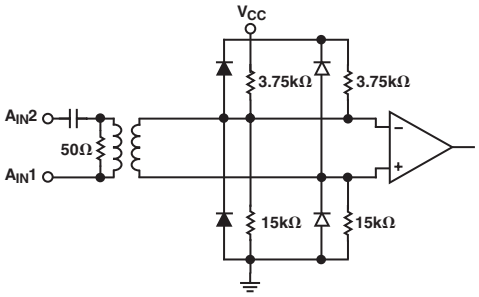
Test Circuit 1. Equivalent ENCODE Input



Test Circuit 3. Equivalent Voltage Reference Output



Test Circuit 2. Equivalent Digital Output



Test Circuit 4. Equivalent Analog Input

DEFINITION OF TERMS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point on the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

ENCODE Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in logic "1" state to achieve rated performance; pulsewidth low is the minimum time ENCODE pulse should be left in low state. At a given clock rate, these specs define an acceptable ENCODE duty cycle.

Harmonic Distortion
The ratio of the rms signal amplitude to the rms value of the worst harmonic component.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The ENCODE rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The ENCODE rate at which parametric testing is performed.

Output Propagation Delay
The delay between the 50% point of the rising edge of ENCODE command and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio
The ratio of a change in output offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full-scale) to the rms value of the sum of all other spectral components, excluding the first six harmonics and dc. [May be reported in dBc (i.e., degrades as signal levels are lowered) or in dBFS (always related back to converter full-scale).]

Signal-to-Noise Ratio (without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full-scale) to the rms value of the sum of all other spectral components, excluding the first six harmonics and dc. [May be reported in dBc (i.e., degrades as signal levels are lowered) or in dBFS (always related back to converter full-scale).]

Spurious-Free Dynamic Range
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. [May be reported in dBc (i.e., degrades as signal levels is lowered) or in dBFS (always related back to converter full-scale).]

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Voltage Standing Wave Ratio (VSWR)
The ratio of the amplitude of the electric field at a voltage maximum to that at an adjacent voltage minimum.

APPLICATION NOTES

Theory of Operation

The AD10226 is a high-dynamic-range dual 12-bit, 125 MHz subrange pipeline converter that uses switched capacitor architecture. The analog input section uses A_{IN}A2/B2 at 1.84 V p-p with an input impedance of 50 Ω. The analog input includes an ac-coupled wideband 1:1 transformer, which provides high dynamic range and SNR while maintaining VSWR and gain flatness. The ADC includes a high bandwidth linear track/hold that gives excellent spurious performance up to and beyond the Nyquist rate. The high bandwidth track/hold has a low jitter of 0.25 ps rms, leading to excellent SNR and SFDR performance. AC-coupled differential PECL/ECL encode inputs are recommended for optimum performance.

USING THE AD10226

ENCODE Input

Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A track/hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD10226, and the user is advised to give commensurate thought to the clock source.

The monolithic converter has an internal clock duty cycle stabilization circuit that locks to the rising edge of ENCODE (falling edge of $\overline{\text{ENCODE}}$ if driven differentially), and optimizes timing internally. This allows for a wide range of input duty cycles at the input without degrading performance. Jitter in the rising edge of the input is still of paramount concern and is not reduced by the internal stabilization circuit. This circuit is always on and cannot be disabled by the user.

The ENCODE and $\overline{\text{ENCODE}}$ inputs are internally biased to 3.75 V (nominal) and support either differential or single-ended signals. For best dynamic performance, a differential signal is recommended. Good performance is obtained using an MC10EL16 in the circuit to directly drive the encode inputs, as illustrated in Figure 2.

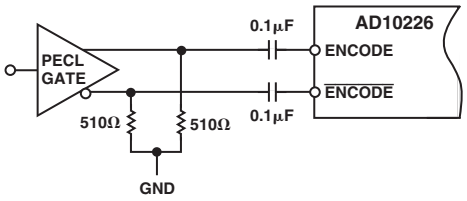


Figure 2. Using PECL to Drive ENCODE Inputs

Often, the cleanest clock source is a crystal oscillator producing a pure, single-ended sine wave. In this configuration, or with any roughly symmetrical, single-ended clock source, the signal can be ac-coupled to the ENCODE input. To minimize jitter, the signal amplitude should be maximized within the input range described in the Table II.

Table II. ENCODE Inputs

Description	Min	Nom	Max
Differential Signal Amplitude (V_{ID})	200 mV	750 mV	5.5 V
Input Voltage Range (V_{HID}, V_{ILD}, V_{HIS})	–5 V		V_{CC} + 0.5 V
Internal Common-Mode Voltage (V_{ICM})		3.75 V	
External Common-Mode Bias (V_{ECM})	2.0 V		4.25 V

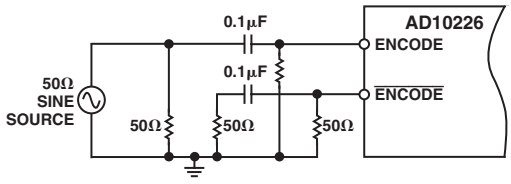


Figure 3. Single-Ended 50 Sine Encode Circuit

The 10 kΩ resistors to ground at each of the inputs, in parallel with the internal bias resistors, set the common-mode voltage to ~ 2.5 V,

allowing the maximum swing at the input. The ENCODE input should be bypassed with a capacitor to ground to reduce noise. This ensures that the internal bias voltage is centered on the encode signal (Figure 3). For best dynamic performance, impedances at ENCODE and $\overline{\text{ENCODE}}$ should match.

Figure 4 shows another preferred method for clocking the AD10226. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD10226 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to the other portions of the AD9433, and limits the noise presented to the ENCODE inputs. A crystal clock oscillator can also be used to drive the RF transformer if an appropriate limiting resistor (typically 100 Ω) is placed in the series with the primary.

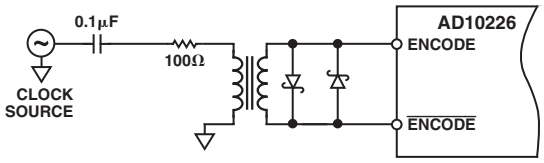


Figure 4. Double-Ended 50 Sine Encode Circuit

ENCODE Voltage Level Definition

The voltage level definitions for driving ENCODE and $\overline{\text{ENCODE}}$ in differential mode is shown in Figure 6.

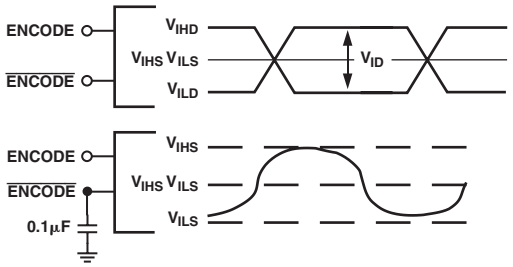


Figure 5. Differential Input Levels

Analog Input

The analog input is a single-ended ac-coupled high performance 1:1 transformer with an input impedance of 50 Ω to 350 MHz. The nominal full scale input is 1.87 V p-p.

Special care was taken in the design of the analog input section of the AD10226 to prevent damage and corruption of data when the input is overdriven.

SFDR Optimization

The SFDR MODE pin enables (SFDR MODE = 1) a proprietary circuit that may improve the spurious-free dynamic range (SFDR) performance of the AD10226. It is useful in applications where the dynamic range of the system is limited by discrete spurious frequency content caused by nonlinearities in the ADC transfer function.

Enabling this circuit will give the circuit a dynamic transfer function, meaning that the voltage threshold between two adjacent output codes may change from clock cycle to clock cycle. While improving spurious frequency content, this dynamic aspect of the transfer function may be inappropriate for some time domain applications of the converter. Connecting the SFDR Mode pin to ground will disable this function. The Typical Performance Characteristics section of the data sheet illustrates the improvement in the linearity of the converter and its effect on spurious-free dynamic range.

Digital Outputs

The digital outputs are 3.3 V (2.7 V to 3.6 V) TTL/CMOS-compatible for lower power consumption. The output data format is selectable through the data format select (DFS) CMOS input. DFS = 1 selects offset binary coding (Table III); DFS = 0 selects Two's Complement coding (Table IV).

Table III. Offset Binary Output Coding (DFS = 1, V_{REF} = 2.5 V)

Code	$A_{IN} - \overline{A_{IN}}$ (V) Range = 2 V p-p	Digital Output
4095	+0.92	1111 1111 1111
•	•	•
•	•	•
2048	0	1000 0000 0000
2047	–0.00045	0111 1111 1111
•	•	•
•	•	•
0	–0.92	0000 0000 0000

Table IV. Two's Complement Output Coding (DFS = 0, V_{REF} = 2.5 V)

Code	$A_{IN} - \overline{A_{IN}}$ (V) Range = 2 V p-p	Digital Output
+2047	+0.92	0111 1111 1111
•	•	•
•	•	•
0	0	0000 0000 0000
–1	–0.00045	1111 1111 1111
•	•	•
•	•	•
–2048	–0.92	1000 0000 0000

Voltage Reference

A stable and accurate 2.5 V voltage reference is designed into the AD10226 (V_{REFOUT}). An external voltage reference is not required.

Timing

The AD10226 provides latched data outputs, with 10 pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the ENCODE command (see Figure 1). The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD10226; these transients can detract from the converter's dynamic performance.

The minimum guaranteed conversion rate of the AD10226 is 10 MSPS. At internal clock rates below 10 MSPS, dynamic performance may degrade. Therefore, input clock rates below 10 MHz should be avoided.

GROUNDING AND DECOUPLING

Analog and Digital Grounding

Proper grounding is essential in any high-speed, high resolution system. Multilayer printed circuit boards (PCBs) are recommended to provide optimal grounding and power schemes. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the powerplane, PCB insulation, and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout that prevents noise from coupling to the input signal. Digital signals should not be run in parallel with input signal traces and should be routed away from the input circuitry. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path and manage the power and ground currents. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

Solder Reflow Profile

The Solder Reflow Profile for the AD10226 is shown in Figure 6.

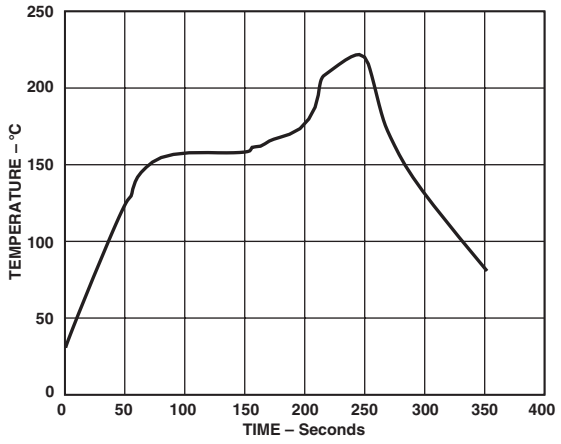


Figure 6. Typical Solder Reflow Profile

LAYOUT INFORMATION

The schematic of the evaluation board (Figures 7a–7d) represents a typical implementation of the AD10226. The pinout of the AD10226 is very straightforward and facilitates ease of use and the implementation of high-frequency/high resolution design practices. It is recommended that high quality ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. All capacitors can be standard high quality ceramic chip capacitors.

Care should be taken when placing the digital output runs. Because the digital outputs have such a high slew rate, the capacitive loading on the digital outputs should be minimized. Circuit traces for the digital outputs should be kept short and connect directly to the receiving gate. Internal circuitry buffers the outputs of the AD9433 ADC through a resistor network to eliminate the need to externally isolate the device from the receiving gate.

EVALUATION BOARD

The AD10226 evaluation board (Figures 7a–7d) is designed to provide optimal performance for evaluation of the AD10226 analog-to-digital converter. The board encompasses everything needed to ensure the highest level of performance for evaluating the AD10226. The board requires an analog input signal, an ENCODE clock and power supply inputs. The clock is buffered on-board to provide clocks for the latches. The digital outputs and out clocks are available at the standard 40-pin connectors J1 and J2. Power to the analog supply pins is connected via banana jacks. The analog supply powers the associated components and analog section of the AD10226. The digital outputs of the AD10226 are also powered via banana jacks with 3.3 V. Contact the factory if additional layout or application assistance is required.

BILL OF MATERIALS LIST FOR AD10226 EVALUATION BOARD

Quantity	Reference Designator	Value	Description	Part Number
2	U16, U17		IC, Low Voltage 16-Bit D-Type Flip-Flop with 5 V Tolerant Inputs and Outputs	74LCX16374MTD (Fairchild)
1	U1		IC, BGA 35 × 35 385	AD10226AB
2	U14, U15		IC, Precision Low Dropout any CAP Voltage Regulator	ADP3330ART-3.3-RL7 (Analog)
4	R38, R39, R56, R58	33 kΩ	RES 33 kΩ 1/10W 0.1% 0805 SMD	ERA-6YEB333V (Panasonic)
8	R1, R7, R8, R41, R60, R61, R71, R72	51 Ω	RES 51 Ω 1/10W 5% 0805 SMD	ERJ-6GEYJ510V (Panasonic)
32	R3, R4, R9–R18, R23–R30, R35, R36, R40, R42–R46, R63–R66	100 Ω	RES 100 Ω 1/10W 1% 0805 SMD	ERJ-6ENF1000V (Panasonic)
23	C1, C2, C5–C10, C12, C16–C18, C20–C26, C28, C33–C35	0.1 µF	CAP 0.1 µF 50 V Ceramic Y5V 0805	ECJ-2VF1H104Z (Panasonic)
2	C13, C27	0.47 µF	CAP 0.47 µF 25 V Ceramic Y5V 0805	ECJ-2YF1E474Z (Panasonic)
2	J1, J2		2 × 20 Male Connector Strip, 100 Centers	TSW-120-08G-D (Samtec)
4	L1, L2, L3, L4	47 Ω	SMT Ferrite Bead	2743019447 (Fair Rite)
4	U2, U3, U9, U11		IC, 3.3 V/5 V ECL Differential Receiver/Driver	MC10EP16D (Motorola)
8	E3–E6, E25, E26, E33, E34		Power Jack, Banana Plug	108-0740-001 (Johnson Company)
2	U4, U10		3.3 V Dual Differential LVPECL-to-LVTTL Translator	SY100ELT23L (Micrel-Synergy)
10	C3, C4, C11, C14, C15, C19, C29, C30–C32	10 µF	Solid Tantalum Chip Capacitor, 10 µF, 16 V, 20%	T491C106M016AS (KEMET)
8	J3–J7, J10–J12		SMA PLUG 200Mil STR GOLD	142-0801-201 (Johnson Components Inc.)
4			Spacer Aluminum, Hex M–F (Standoff)	
4			Nut Hex Stl #4-40 UNC-2B	
1	AD10201/AD10226 Evaluation Board		GS03983 Rev. A (PCB)	
2	C36, C37		CAP 0.047 µF 25 V Ceramic Y5V 0603	ECJ-1VB1C473K
6	JP3, JP4, JP6, JP8, JP9, JP12	0 Ω	RES 0 Ω 1/16 W 5% 0402	ER J-2GEOR00

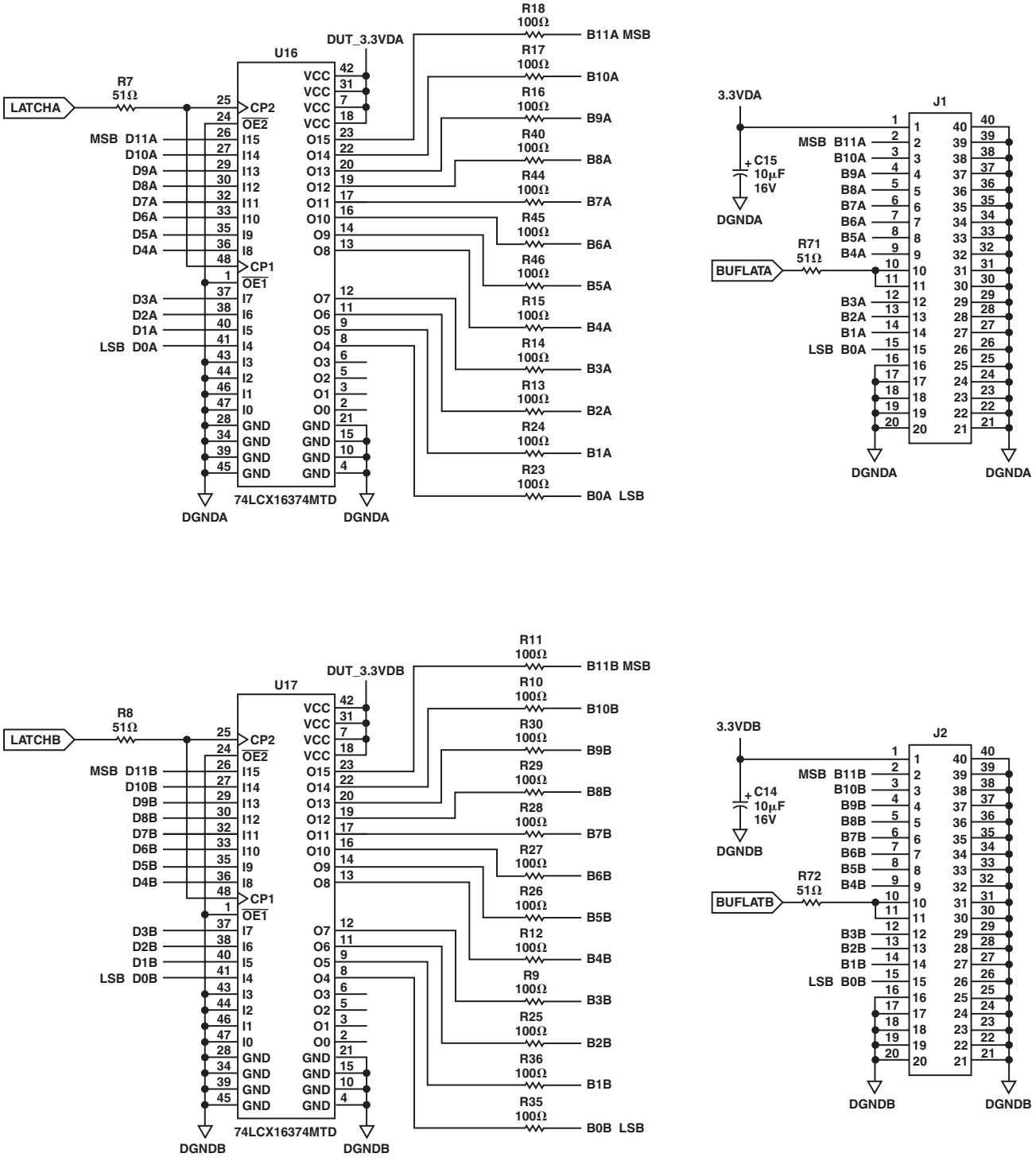


Figure 7a. Evaluation Board Schematic

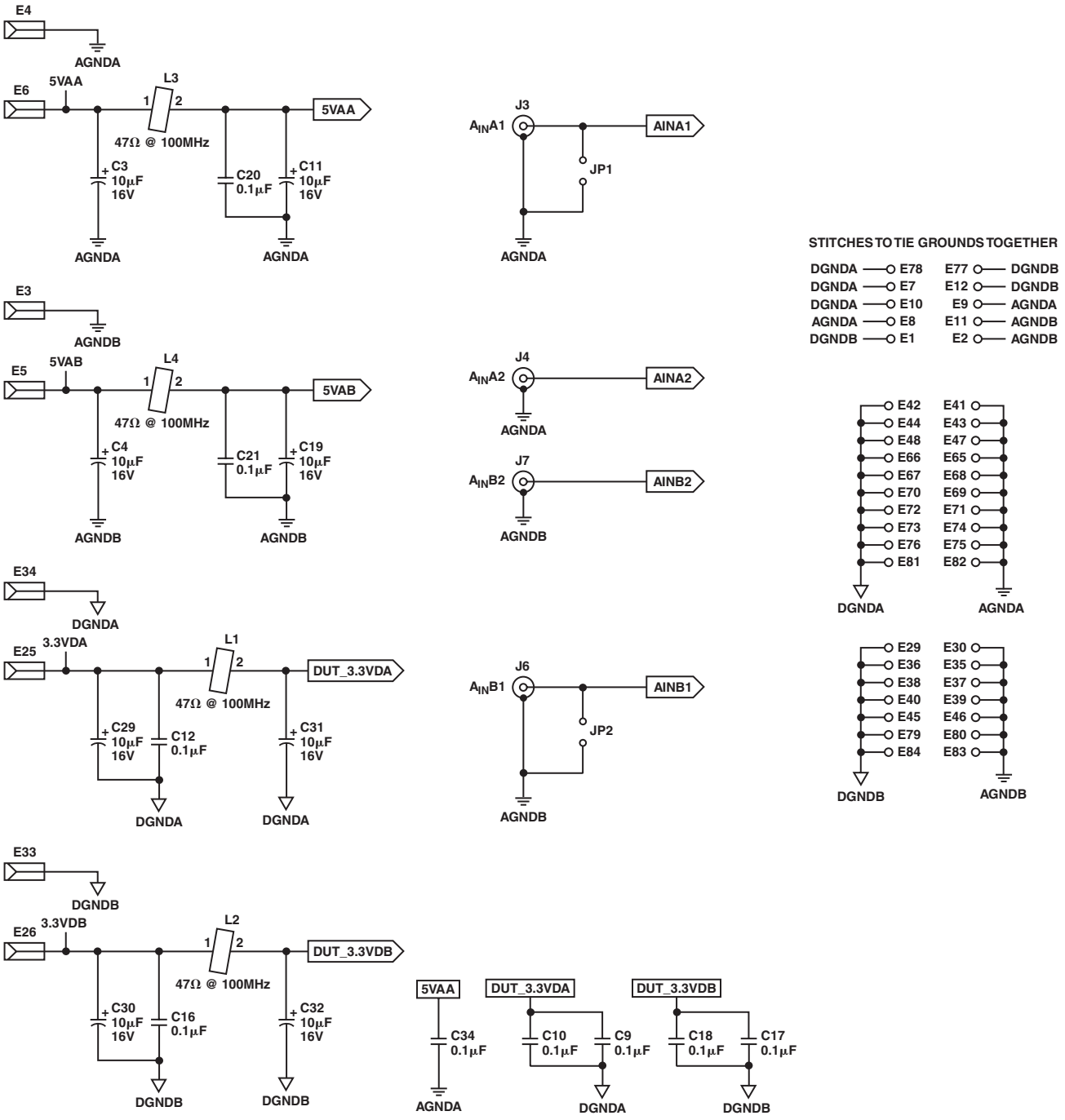


Figure 7b. Evaluation Board Schematic

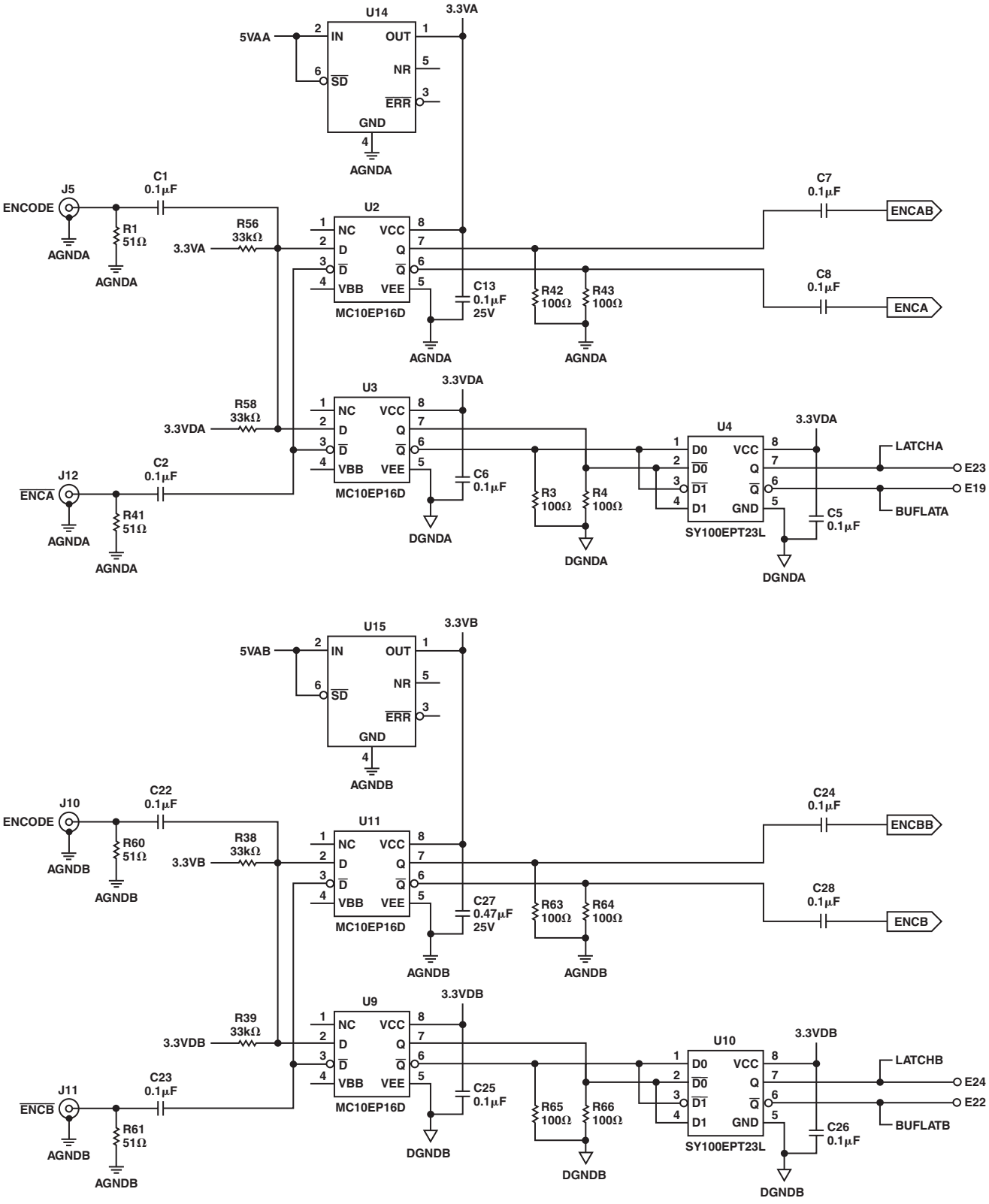


Figure 7c. Evaluation Board Schematic

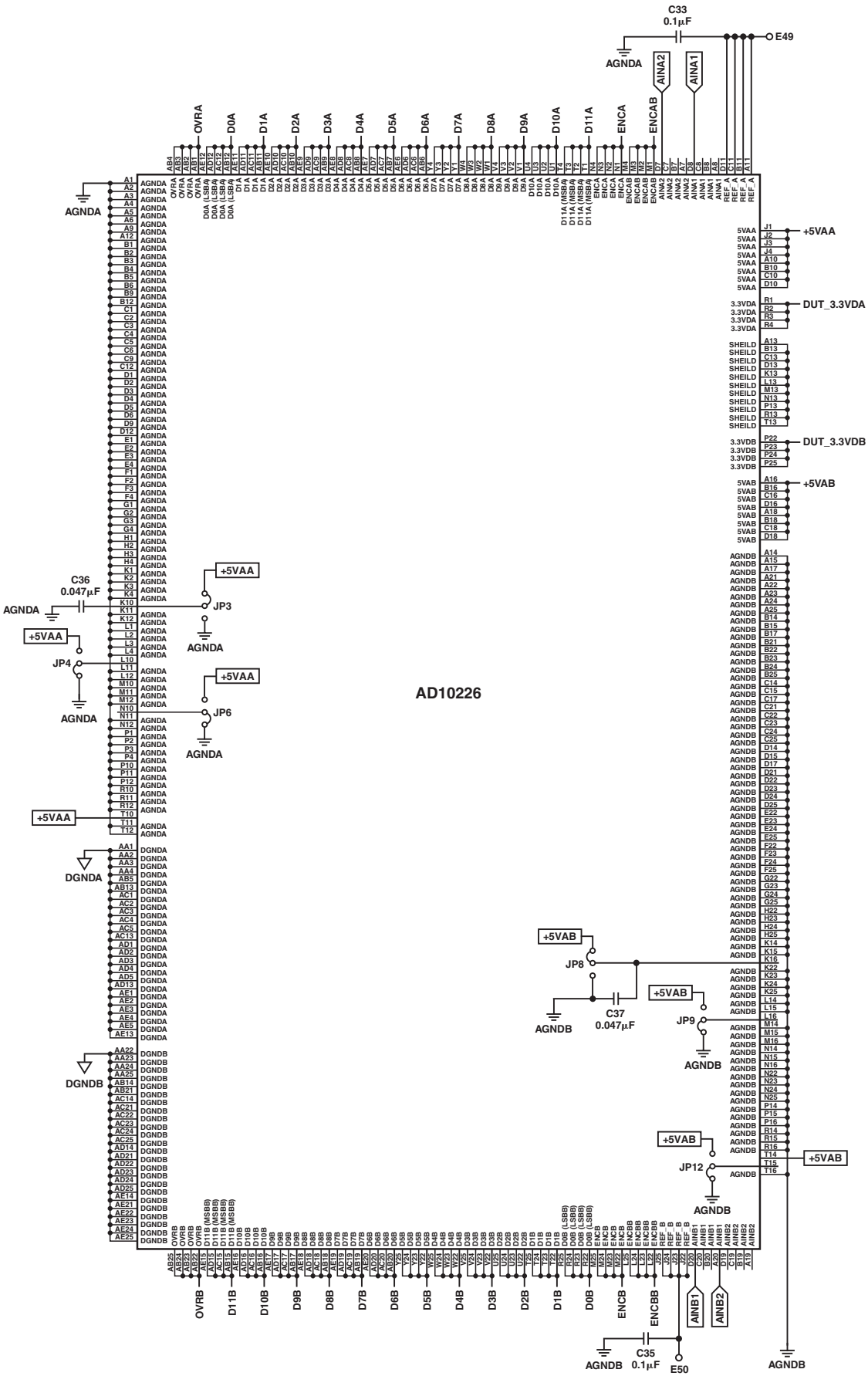


Figure 7d. Evaluation Board Schematic

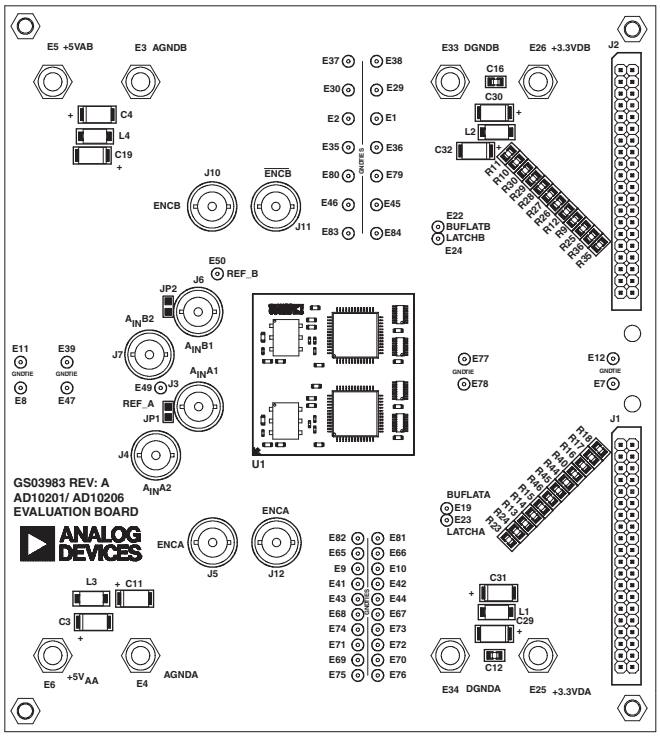


Figure 8a. Mechanical Layout Top View

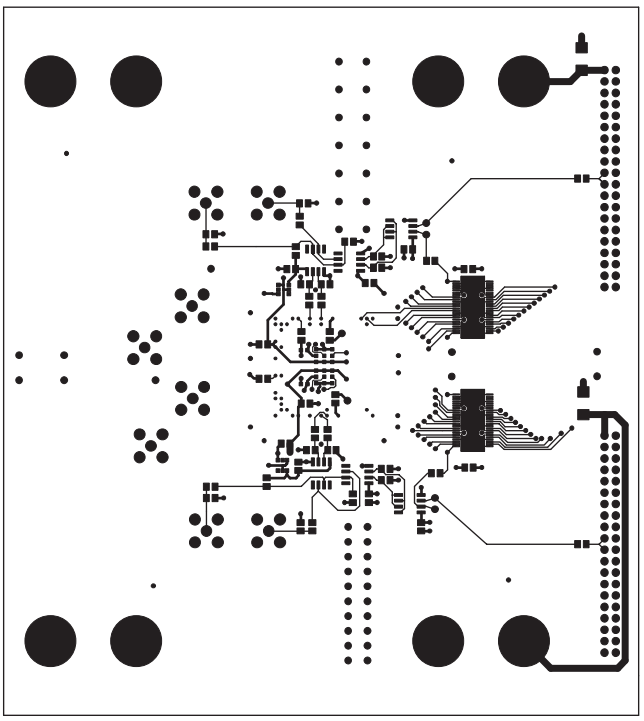


Figure 8c. Top View

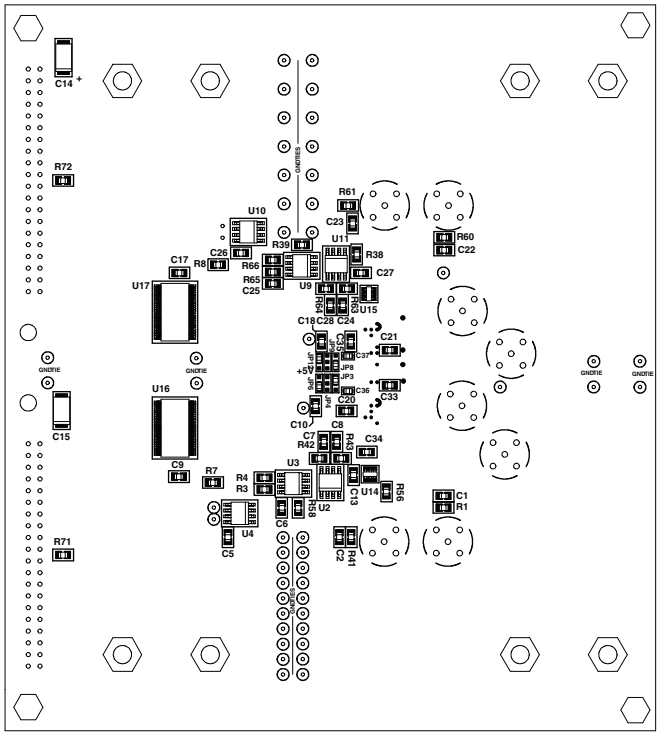


Figure 8b. Mechanical Layout Bottom View

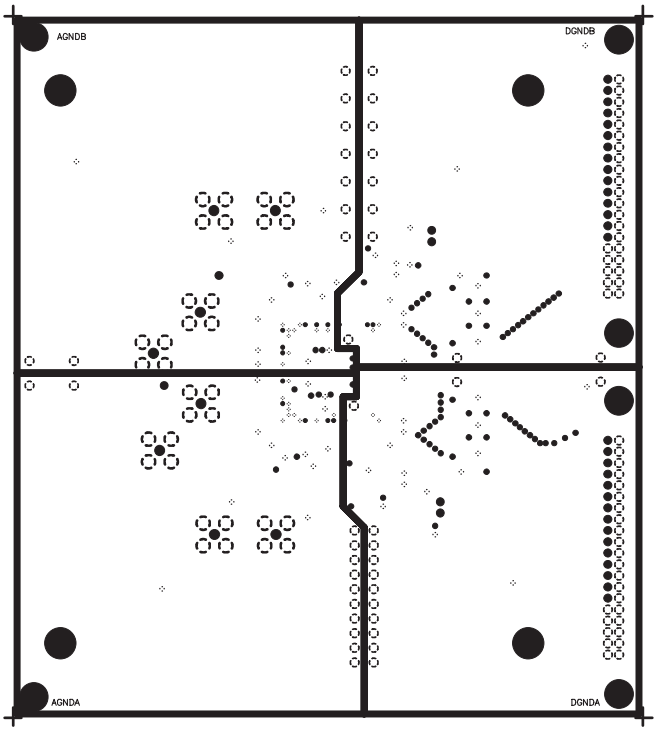


Figure 8d. Layer 2

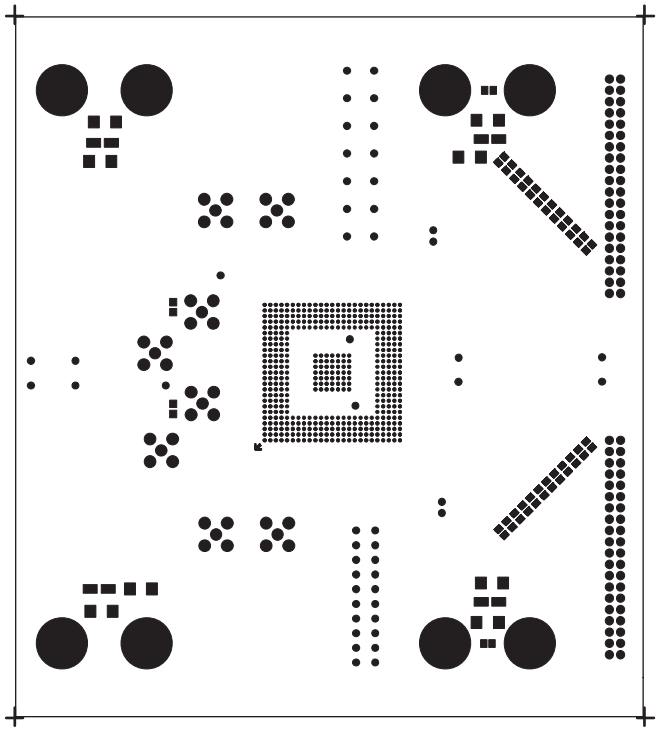


Figure 8e. Layer 3

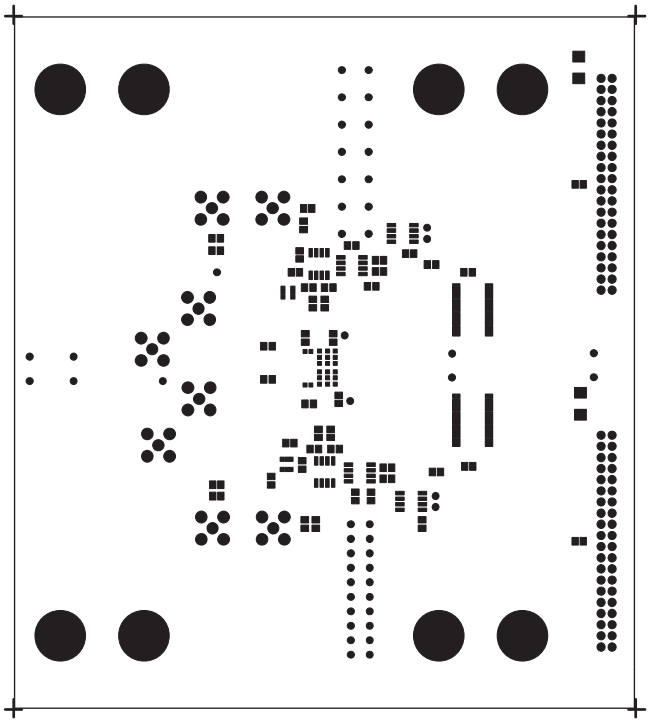


Figure 8g. Ground View 2

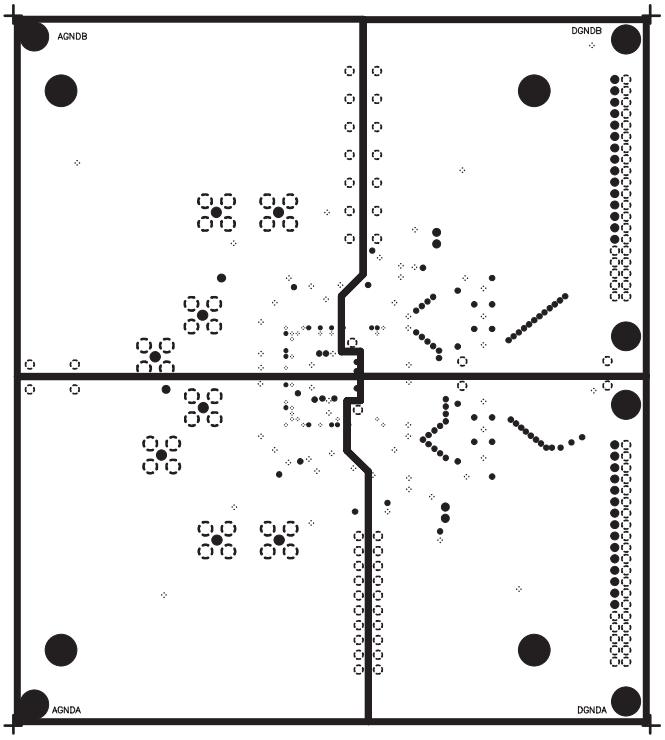
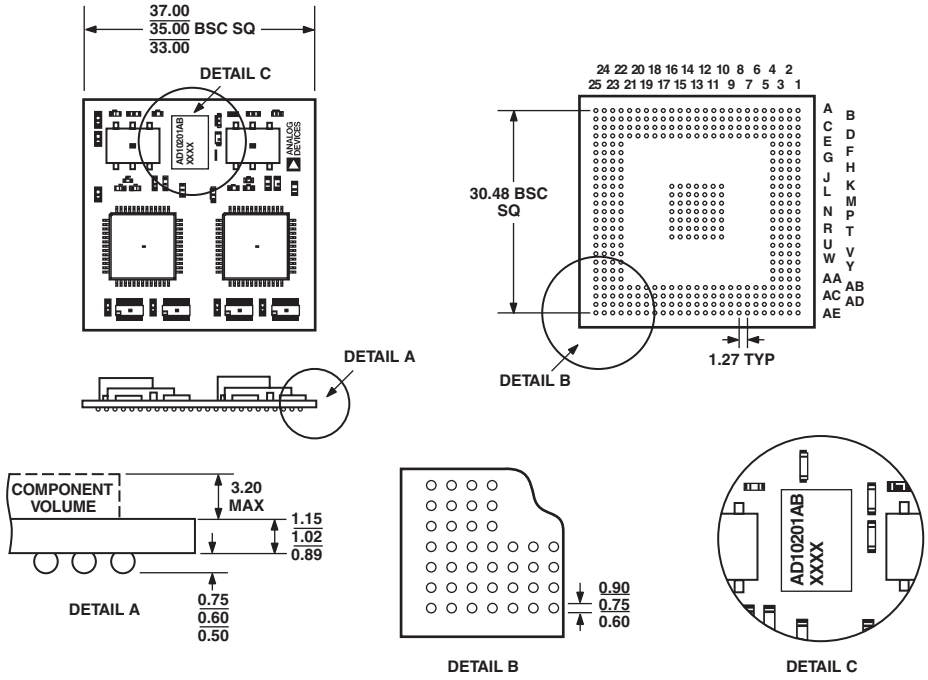


Figure 8f. Ground View 1

OUTLINE DIMENSIONS

Dimensions shown in millimeters (mm).

385-Lead Ball Grid Array (BGA)
(B-385)



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