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8XL196NP COMMERCIAL
CHMOS 16-BIT MICROCONTROLLER

- **14 MHz Operation at 2.7–3.3 Volts**
- **1 Mbyte of Linear Address Space**
- **Optional 4 Kbytes of ROM**
- **1000 Bytes of Register RAM**
- **Register-register Architecture**
- **32 I/O Port Pins**
- **16 Prioritized Interrupt Sources**
- **4 External Interrupt Pins and NMI Pin**
- **2 Flexible 16-bit Timer/Counters with Quadrature Counting Capability**
- **3 Pulse-width Modulator (PWM) Outputs with High Drive Capability**
- **Full-duplex Serial Port with Dedicated Baud-rate Generator**
- **Peripheral Transaction Server**
- **Event Processor Array (EPA) with 4 High-speed Capture/Compare Channels**

- **Chip-select Unit**
  - **6 Chip Select Pins**
  - **Dynamic Demultiplexed/Multiplexed Address/Data Bus for Each Chip Select**
  - **Programmable Wait States (0, 1, 2, or 3) for Each Chip Select**
  - **Programmable Bus Width (8- or 16-bit) for Each Chip Select**
  - **Programmable Address Range for Each Chip Select**
- **2.0μs 16 $\times$ 16 Unsigned Multiplication**
- **3.4μs 32/16 Unsigned Division**
- **100-pin SQFP or 100-pin QFP Package**
- **Complete System Development Support**
- **High-speed CHMOS Technology**

The 8XL196NP is a member of Intel's 16-bit MCS® 96 microcontroller family. The device features 1 Mbyte of linear address space, a demultiplexed bus, and a chip-select unit. The external bus can dynamically switch between multiplexed and demultiplexed operation. When operating at 14 MHz in demultiplexed mode, the 8XL196NP can access a 200 ns memory device with zero wait states. The 8XL196NP is available without ROM (80L196NP) or with 4 Kbytes of ROM (83L196NP).
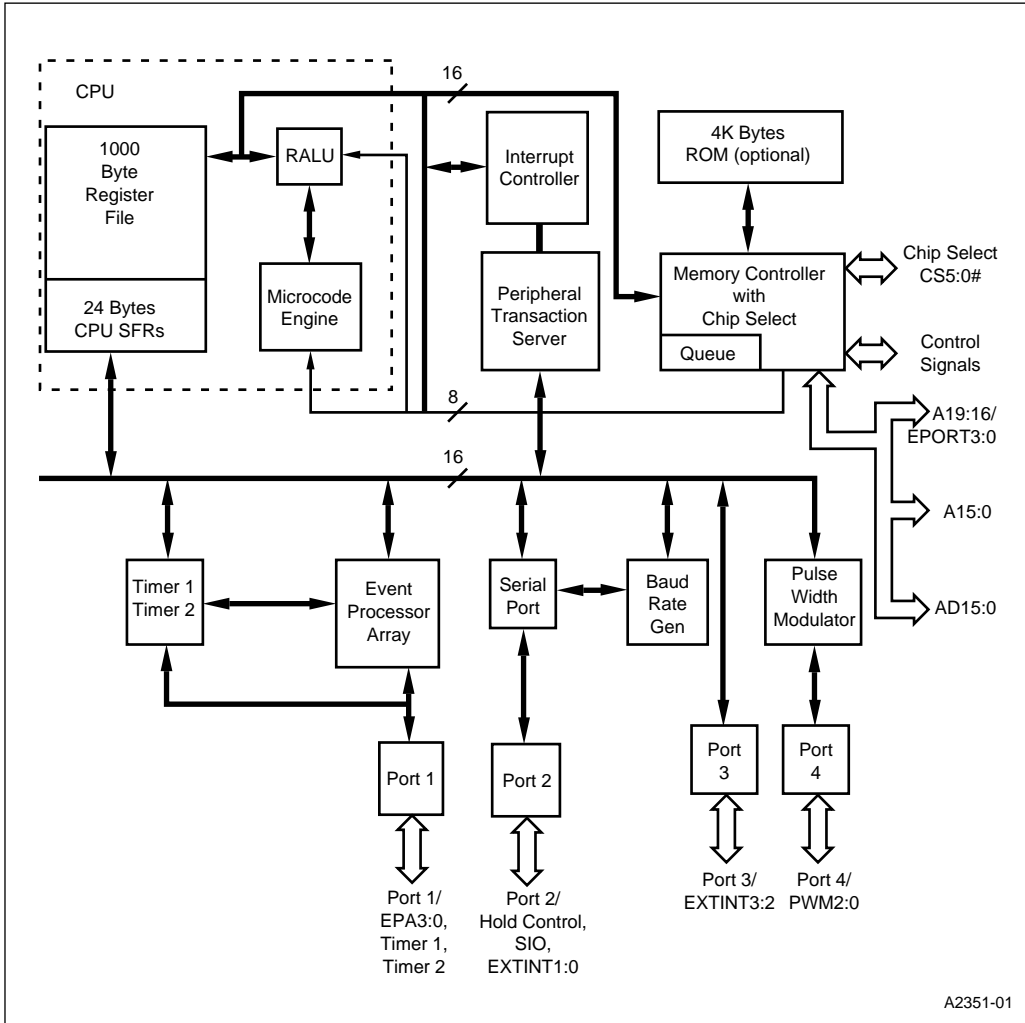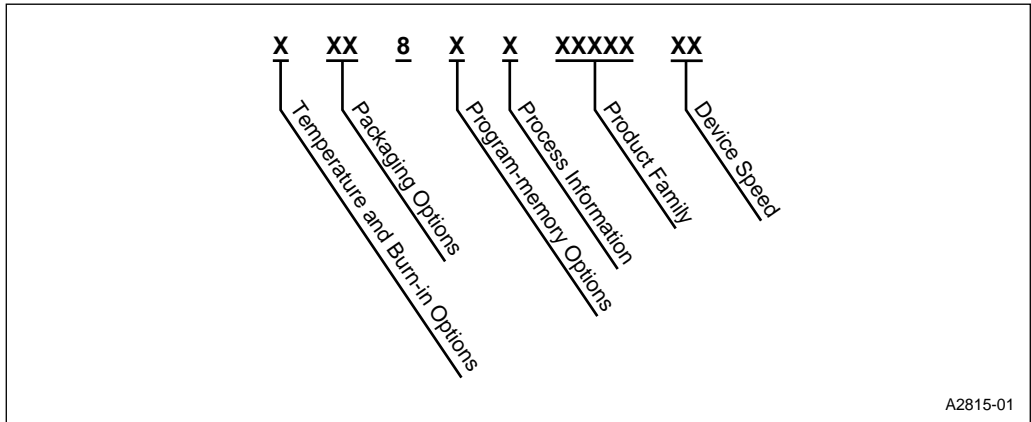
Figure 1. 8XL196NP Block Diagram

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1.0 NOMENCLATURE OVERVIEW

A2815-01

Figure 2. 8XL196NP Family Nomenclature

Table 1. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
Packaging Options	S SB	QFP SQFP
Program–memory Options	0 3	No ROM ROM
Process Information	L	Low Voltage CHMOS
Product Family	196NP	
Device Speed	no mark	14 MHz

2.0 PINOUT
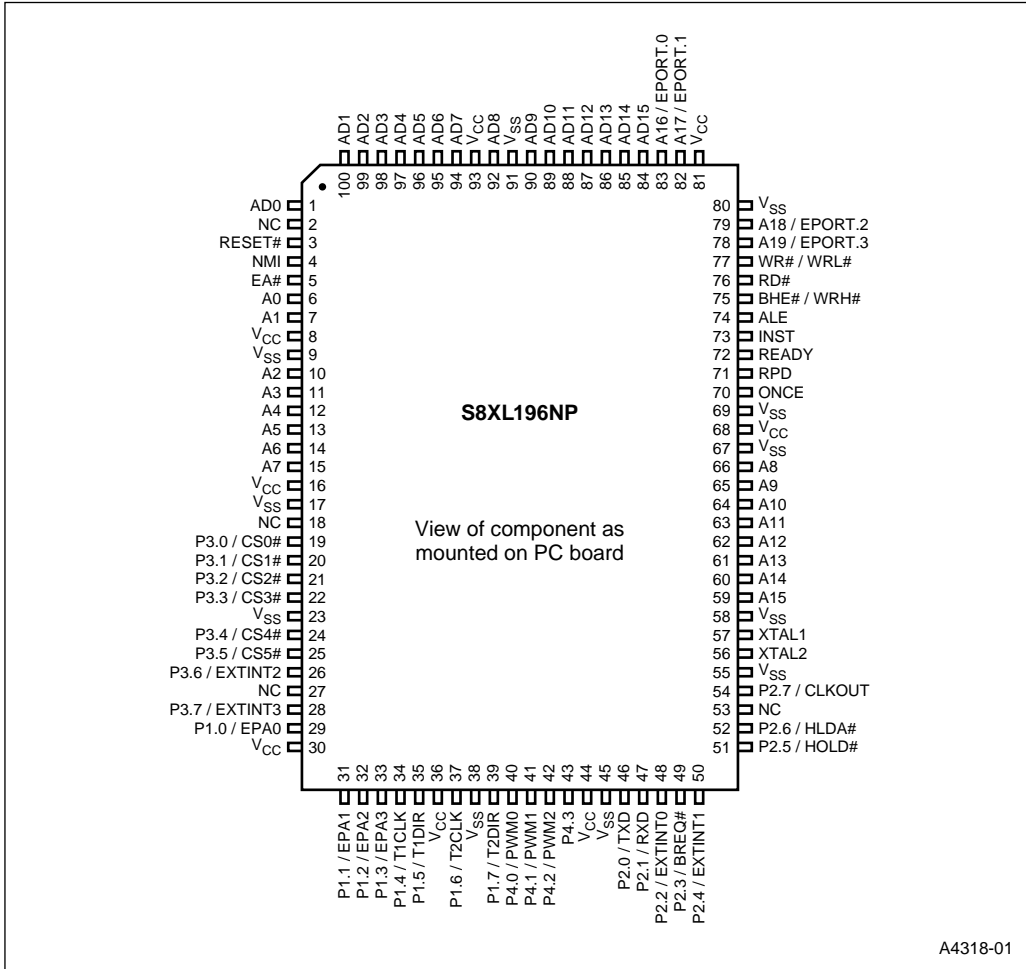
Figure 3. 8XL196NP 100-pin SQFP Package

Table 2. 8XL196NP 100-pin SQFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	RESET#	26	EXTINT3/P3.7	51	CLKOUT/P2.7	76	WR#/WRL#
2	NMI	27	EPA0/P1.0	52	NC†	77	EPORT.3/A19
3	EA#	28	V_{CC}	53	V_{SS}	78	EPORT.2/A18
4	A0	29	EPA1/P1.1	54	XTAL2	79	V_{SS}
5	A1	30	EPA2/P1.2	55	XTAL1	80	V_{CC}
6	V_{CC}	31	EPA3/P1.3	56	V_{SS}	81	EPORT.1/A17
7	V_{SS}	32	T1CLK/P1.4	57	NC†	82	EPORT.0/A16
8	A2	33	T1DIR/P1.5	58	A15	83	AD15
9	A3	34	V_{CC}	59	A14	84	AD14
10	A4	35	T2CLK/P1.6	60	A13	85	AD13
11	A5	36	V_{SS}	61	A12	86	AD12
12	A6	37	T2DIR/P1.7	62	A11	87	AD11
13	A7	38	PWM0/P4.0	63	A10	88	AD10
14	V_{CC}	39	PWM1/P4.1	64	A9	89	AD9
15	V_{SS}	40	PWM2/P4.2	65	A8	90	V_{SS}
16	NC†	41	P4.3	66	V_{SS}	91	AD8
17	NC†	42	V_{CC}	67	V_{CC}	92	V_{CC}
18	CS0#/P3.0	43	V_{SS}	68	V_{SS}	93	AD7
19	CS1#/P3.1	44	TXD/P2.0	69	ONCE	94	AD6
20	CS2#/P3.2	45	RXD/P2.1	70	RPD	95	AD5
21	CS3#/P3.3	46	EXTINT0/P2.2	71	READY	96	AD4
22	V_{SS}	47	BREQ#/P2.3	72	INST	97	AD3
23	CS4#/P3.4	48	EXTINT1/P2.4	73	ALE	98	AD2
24	CS5#/P3.5	49	HOLD#/P2.5	74	BHE#/WRH#	99	AD1
25	EXTINT2/P3.6	50	HLDA#/P2.6	75	RD#	100	AD0

† To be compatible with future versions of the Nx family, tie the no connection (NC) pins as follows: Pin 57 = V_{SS}, Pin 16 = V_{CC}, Pin 17 = V_{SS} (5 volts on this pin will enable a clock doubler on future devices), and Pin 52 = V_{CC}.

Table 3. 100-pin SQFP Pin Assignment Arranged by Functional Categories

Address & Data		Address & Data (cont)		Input/Output		Power & Ground	
Name	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**
A0	4	AD13	85	CS0#/P3.0	18	V_{CC}	6
A1	5	AD14	84	CS1#/P3.1	19	V_{CC}	14
A2	8	AD15	83	CS2#/P3.2	20	V_{CC}	28
A3	9			CS3#/P3.3	21	V_{CC}	34
A4	10	**Bus Control & Status**		CS4#/P3.4	23	V_{CC}	42
A5	11	**Name**	**Pin**	CS5#/P3.5	24	V_{CC}	67
A6	12	ALE	73	EPA0/P1.0	27	V_{CC}	80
A7	13	BHE#/WRH#	74	EPA1/P1.1	29	V_{CC}	92
A8	65	BREQ#	47	EPA2/P1.2	30	V_{SS}	7
A9	64	HOLD#	49	EPA3/P1.3	31	V_{SS}	15
A10	63	HLDA#	50	EPORT.0	82	V_{SS}	22
A11	62	INST	72	EPORT.1	81	V_{SS}	36
A12	61	RD#	75	EPORT.2	78	V_{SS}	43
A13	60	READY	71	EPORT.3	77	V_{SS}	53
A14	59	WR#/WRL#	76	P2.2	46	V_{SS}	56
A15	58			P2.3	47	V_{SS}	66
A16	82	**Processor Control**		P2.4	48	V_{SS}	68
A17	81	**Name**	**Pin**	P2.5	49	V_{SS}	79
A18	78	CLKOUT	51	P2.6	50	V_{SS}	90
A19	77	EA#	3	P2.7	51		
AD0	100	EXTINT0	46	P3.6	25	**No Connection**	
AD1	99	EXTINT1	48	P3.7	26	**Name**	**Pin**
AD2	98	EXTINT2	25	P4.3	41	NC	16
AD3	97	EXTINT3	26	PWM0/P4.0	38	NC	17
AD4	96	NMI	2	PWM1/P4.1	39	NC	52
AD5	95	ONCE	69	PWM2/P4.2	40	NC	57
AD6	94	RESET#	1	RXD/P2.1	45		
AD7	93	RPD	70	T1CLK/P1.4	32		
AD8	91	XTAL1	55	T1DIR/P1.5	33		
AD9	89	XTAL2	54	T2CLK/P1.6	35		
AD10	88			T2DIR/P1.7	37		
AD11	87			TXD/P2.0	44		
AD12	86						

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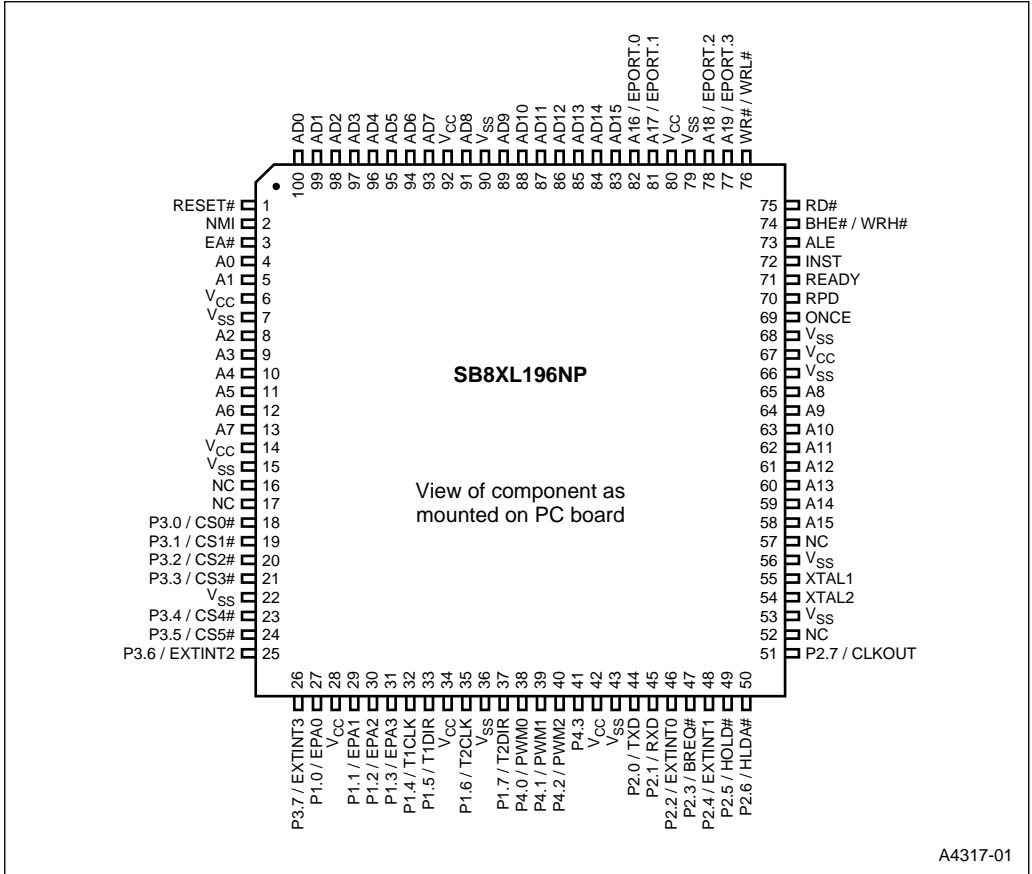
Figure 4. 8XL196NP 100-pin QFP Package

Table 4. 8XL196NP 100-pin QFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AD0	26	EXTINT2/P3.6	51	HOLD#/P2.5	76	RD#
2	No Connection	27	No Connection	52	HLDA#/P2.6	77	WR#/WRL#
3	RESET#	28	EXTINT3/P3.7	53	No Connection	78	EPORT.3/A19
4	NMI	29	EPA0/P1.0	54	CLKOUT/P2.7	79	EPORT.2/A18
5	EA#	30	V_{CC}	55	V_{SS}	80	V_{SS}
6	A0	31	EPA1/P1.1	56	XTAL2	81	V_{CC}
7	A1	32	EPA2/P1.2	57	XTAL1	82	EPORT.1/A17
8	V_{CC}	33	EPA3/P1.3	58	V_{SS}	83	EPORT.0/A16
9	V_{SS}	34	T1CLK/P1.4	59	A15	84	AD15
10	A2	35	T1DIR/P1.5	60	A14	85	AD14
11	A3	36	V_{CC}	61	A13	86	AD13
12	A4	37	T2CLK/P1.6	62	A12	87	AD12
13	A5	38	V_{SS}	63	A11	88	AD11
14	A6	39	T2DIR/P1.7	64	A10	89	AD10
15	A7	40	PWM0/P4.0	65	A9	90	AD9
16	V_{CC}	41	PWM1/P4.1	66	A8	91	V_{SS}
17	V_{SS}	42	PWM2/P4.2	67	V_{SS}	92	AD8
18	No Connection	43	P4.3	68	V_{CC}	93	V_{CC}
19	CS0#/P3.0	44	V_{CC}	69	V_{SS}	94	AD7
20	CS1#/P3.1	45	V_{SS}	70	ONCE	95	AD6
21	CS2#/P3.2	46	TXD/P2.0	71	RPD	96	AD5
22	CS3#/P3.3	47	RXD/P2.1	72	READY	97	AD4
23	V_{SS}	48	EXTINT0/P2.2	73	INST	98	AD3
24	CS4#/P3.4	49	BREQ#/P2.3	74	ALE	99	AD2
25	CS5#/P3.5	50	EXTINT1/P2.4	75	BHE#/WRH#	100	AD1

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Table 5. 100-pin QFP Pin Assignment Arranged by Functional Categories

Address & Data		Address & Data (cont)		Input/Output		Power & Ground	
Name	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**
A0	6	AD13	86	CS0#/P3.0	19	V_{CC}	8
A1	7	AD14	85	CS1#/P3.1	20	V_{CC}	16
A2	10	AD15	84	CS2#/P3.2	21	V_{CC}	30
A3	11			CS3#/P3.3	22	V_{CC}	36
A4	12	**Bus Control & Status**		CS4#/P3.4	24	V_{CC}	44
A5	13	**Name**	**Pin**	CS5#/P3.5	25	V_{CC}	68
A6	14	ALE	74	EPA0/P1.0	29	V_{CC}	81
A7	15	BHE#/WRH#	75	EPA1/P1.1	31	V_{CC}	93
A8	66	BREQ#	49	EPA2/P1.2	32	V_{SS}	9
A9	65	HOLD#	51	EPA3/P1.3	33	V_{SS}	17
A10	64	HLDA#	52	EPORT.0	83	V_{SS}	23
A11	63	INST	73	EPORT.1	82	V_{SS}	38
A12	62	RD#	76	EPORT.2	79	V_{SS}	45
A13	61	READY	72	EPORT.3	78	V_{SS}	55
A14	60	WR#/WRL#	77	P2.2	48	V_{SS}	58
A15	59			P2.3	49	V_{SS}	67
A16	83	**Processor Control**		P2.4	50	V_{SS}	69
A17	82	**Name**	**Pin**	P2.5	51	V_{SS}	80
A18	79	CLKOUT	54	P2.6	52	V_{SS}	91
A19	78	EA#	5	P2.7	54		
AD0	1	EXTINT0	48	P3.6	26	**No Connection**	
AD1	100	EXTINT1	50	P3.7	28	**Name**	**Pin**
AD2	99	EXTINT2	26	P4.3	43	NC	2
AD3	98	EXTINT3	28	PWM0/P4.0	40	NC	18
AD4	97	NMI	4	PWM1/P4.1	41	NC	27
AD5	96	ONCE	70	PWM2/P4.2	42	NC	53
AD6	95	RESET#	3	RXD/P2.1	47		
AD7	94	RPD	71	T1CLK/P1.4	34		
AD8	92	XTAL1	57	T1DIR/P1.5	35		
AD9	90	XTAL2	56	T2CLK/P1.6	37		
AD10	89			T2DIR/P1.7	39		
AD11	88			TXD/P2.0	46		
AD12	87						

3.0 SIGNALS

Table 6. Signal Descriptions

Name	Type	Description
A15:0	I/O	System Address Bus These address pins provide address bits 0–15 during the entire external memory cycle during both multiplexed and demultiplexed bus modes.
A19:16	I/O	Address Pins 16–19 These address pins provide address bits 16–19 during the entire external memory cycle during both multiplexed and demultiplexed bus modes, supporting extended addressing of the 1-Mbyte address space. **NOTE:** Internally, there are 24 address bits; however, only 20 external address pins (A19:0) are implemented. The internal address space is 16 Mbytes (000000–FFFFFFH) and the external address space is 1 Mbyte (00000–FFFFFH). The microcontroller resets to FF2080H in internal memory or F2080H in external memory. A19:16 share package pins with EPORT.3:0.
AD15:0	I/O	Address/Data Lines The function of these pins depends on the bus width and mode. **16-bit Multiplexed Bus Mode**: AD15:0 drive address bits 0–15 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle. **8-bit Multiplexed Bus Mode**: AD15:8 drive address bits 8–15 during the entire bus cycle. AD7:0 drive address bits 0–7 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle. **16-bit Demultiplexed Mode**: AD15:0 drive or receive data during the entire bus cycle. **8-bit Demultiplexed Mode**: AD7:0 drive or receive data during the entire bus cycle. AD15:8 drive the data that is currently on the high byte of the internal bus.
ALE	O	Address Latch Enable This active-high output signal is asserted only during external memory cycles. ALE signals the start of an external bus cycle and indicates that valid address information is available on the system address/data bus (A19:16 and AD15:0 for a multiplexed bus; A19:0 for a demultiplexed bus). An external latch can use this signal to demultiplex address bits 0–15 from the address/data bus in multiplexed mode.

Table 6. Signal Descriptions (Continued)

Name	Type	Description
BHE#	O	Byte High Enable[†] During 16-bit bus cycles, this active-low output signal is asserted for word and high-byte reads and writes to external memory. BHE# indicates that valid data is being transferred over the upper half of the system data bus. Use BHE#, in conjunction with address bit 0 (A0 for a demultiplexed address bus, AD0 for a multiplexed address/data bus), to determine which memory byte is being transferred over the system bus: **BHE# AD0 or A0 Byte(s) Accessed** 0 0 both bytes 0 1 high byte only 1 0 low byte only BHE# shares a package pin with WRH#. [†] When this pin is configured as a special-function signal (P5_MODE.5 = 1), the chip configuration register 0 (CCR0) determines whether it functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.
BREQ#	O	Bus Request This active-low output signal is asserted during a hold cycle when the bus controller has a pending external memory cycle. When the bus-hold protocol is enabled (WSR.7 is set), the P2.3/BREQ# pin can function only as BREQ#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared). The microcontroller can assert BREQ# at the same time as or after it asserts HLDA#. Once it is asserted, BREQ# remains asserted until HOLD# is deasserted. BREQ# shares a package pin with P2.4.
CLKOUT	O	Clock Output Output of the internal clock generator. The CLKOUT frequency is ½ the internal operating frequency (f). CLKOUT has a 50% duty cycle. CLKOUT shares a package pin with P2.7.
CS5#:0	O	Chip-select Lines 0–5 The active-low output CSx# is asserted during an external memory cycle when the address to be accessed is in the range programmed for chip select x. If the external memory address is outside the range assigned to the six chip selects, no chip-select output is asserted and the bus configuration defaults to the CS5# values. Immediately following reset, CS0# is automatically assigned to the range FF2000–FF20FFH (F2000–F20FFH if external). CS5:0# share package pins with P3.5:0.

Table 6. Signal Descriptions (Continued)

Name	Type	Description
EA#	I	External Access
		This input determines whether memory accesses to special-purpose and program memory partitions (FF2000–FF2FFFH) are directed to internal or external memory. These accesses are directed to internal memory if EA# is held high and to external memory if EA# is held low. For an access to any other memory location, the value of EA# is irrelevant.
		EA# is not latched and can be switched dynamically during normal operating mode. Be sure to thoroughly consider the issues, such as different access times for internal and external memory, before using this dynamic switching capability.
		Always connect EA# to V_{SS} when using a microcontroller that has no internal nonvolatile memory.
EPA3:0	I/O	Event Processor Array (EPA) Capture/Compare Channels
		High-speed input/output signals for the EPA capture/compare channels.
		EPA3:0 share package pins with P1.3:0.
EPORT.3:0	I/O	Extended Addressing Port
		This is a 4-bit, bidirectional, memory-mapped port.
		EPORT.3:0 share package pins with A.19:16.
EXTINT0 EXTINT1 EXTINT2 EXTINT3	I	External Interrupts
		In normal operating mode, a rising edge on EXTINT*x* sets the EXTINT*x* interrupt pending bit. EXTINT*x* is sampled during phase 2 (CLKOUT high). The minimum high time is one state time.
		In standby and powerdown modes, asserting the EXTINT*x* signal for at least 50 ns causes the device to resume normal operation. The interrupt does not need to be enabled, but the pin must be configured as a special-function input. If the EXTINT*x* interrupt is enabled, the CPU executes the interrupt service routine. Otherwise, the CPU executes the instruction that immediately follows the command that invoked the power-saving mode.
		In idle mode, asserting any enabled interrupt causes the device to resume normal operation.
		EXTINT0 shares a package pin with P2.2, EXTINT1 shares a package pin with P2.4, EXTINT2 shares a package pin with P3.6, and EXTINT3 shares a package pin with P3.7.
HLDA#	O	Bus Hold Acknowledge
		This active-low output indicates that the CPU has released the bus as the result of an external device asserting HOLD#. When the bus-hold protocol is enabled (WSR.7 is set), the P2.6/HLDA# pin can function only as HLDA#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared).

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Table 6. Signal Descriptions (Continued)

Name	Type	Description
HOLD#	I	Bus Hold Request
		An external device uses this active-low input signal to request control of the bus. When the bus-hold protocol is enabled (WSR.7 is set), the P2.5/HOLD# pin can function only as HOLD#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared).
		HOLD# shares a package pin with P2.5.
INST	O	Instruction Fetch
		When high, INST indicates that an instruction is being fetched from external memory. The signal remains high during the entire bus cycle of an external instruction fetch. INST is low for data accesses, including interrupt vector fetches and chip configuration byte reads. INST is low during internal memory fetches.
NMI	I	Nonmaskable Interrupt
		In normal operating mode, a rising edge on NMI generates a nonmaskable interrupt. NMI has the highest priority of all prioritized interrupts. Assert NMI for greater than one state time to guarantee that it is recognized.
ONCE	I	On-circuit Emulation
		Holding ONCE high during the rising edge of RESET# places the device into on-circuit emulation (ONCE) mode. This mode puts all pins into a high-impedance state, thereby isolating the device from other components in the system. The value of ONCE is latched when the RESET# pin goes inactive. While the device is in ONCE mode, you can debug the system using a clip-on emulator.
		To exit ONCE mode, reset the device by pulling the RESET# signal low. To prevent inadvertent entry into ONCE mode, connect the ONCE pin to V_{SS}.
P1.7:0	I/O	Port 1
		This is a standard, 8-bit, bidirectional port that shares package pins with individually selectable special-function signals.
		Port 1 shares package pins with the following signals: P1.0/EPA0, P1.1/EPA1, P1.2/EPA2, P1.3/EPA3, P1.4/T1CLK, P1.5/T1DIR, P1.6/T2CLK, and P1.7/T2DIR.
P2.7:0	I/O	Port 2
		This is a standard, 8-bit, bidirectional port that shares package pins with individually selectable special-function signals.
		Port 2 shares package pins with the following signals: P2.0/TXD, P2.1/RXD, P2.2/EXTINT0, P2.3/BREQ#, P2.4/EXTINT1, P2.5/HOLD#, P2.6/HLDA#, and P2.7/CLKOUT.
P3.7:0	I/O	Port 3
		This is a standard, 8-bit, bidirectional port that shares package pins with individually selectable special-function signals.
		Port 3 shares package pins with the following signals: P3.0/CS0#, P3.1/CS1#, P3.2/CS2#, P3.3/CS3#, P3.4/CS4#, P3.5/CS5#, P3.6/EXTINT2, and P3.7/EXTINT3.

Table 6. Signal Descriptions (Continued)

Name	Type	Description
P4.3:0	I/O	Port 4
		This ia a 4-bit bidirectional, standard I/O port with high-current drive capability.
		Port 4 shares package pins with the following signals: P4.0/PWM0, P4.1/PWM1, and P4.2/PWM2. P4.3 has a dedicated package pin.
PWM2:0	O	Pulse Width Modulator Outputs
		These are PWM output pins with high-current drive capability.
		PWM2:0 share package pins with P4.2:0.
RD#	O	Read
		Read-signal output to external memory. RD# is asserted only during external memory reads.
		RD# shares a package pin with OE#. (While most signals that share package pins are connected to the pin by programming their associated control registers, both of these signals are always connected to the pin.)
READY	I	Ready Input
		This active-high input can be used to insert wait states in addition to those programmed in the chip configuration byte 0 (CCB0) and the bus control x register (BUSCONx). CCB0 is programmed with the minimum number of wait states (0–3) for an external fetch of CCB1, and BUSCONx is programmed with the minimum number of wait states (0–3) for all external accesses to the address range assigned to the chip-select x channel. If READY is low when the programmed number of wait states is reached, additional wait states are added until READY is pulled high.
		READY shares a package pin with P5.6.
RESET#	I/O	Reset
		A level-sensitive reset input to and open-drain system reset output from the microcontroller. Either a falling edge on RESET# or an internal reset turns on a pull-down transistor connected to the RESET# pin for 16 state times. In the powerdown, standby, and idle modes, asserting RESET# causes the chip to reset and return to normal operating mode. After a device reset, the first instruction fetch is from FF2080H (or F2080H in external memory). For the 80L196NP, the program and special-purpose memory locations (FF2000–FF2FFFH) reside in external memory. For the 83L196NP, these locations can reside either in external memory or in internal ROM.
RPD	I	Return from Powerdown
		Timing pin for the return-from-powerdown circuit.
		If your application uses powerdown mode, connect a capacitor between RPD and V_{SS} if the internal oscillator is the clock source.
		The capacitor causes a delay that enables the oscillator and PLL circuitry to stabilize before the internal CPU and peripheral clocks are enabled.
		The capacitor is not required if your application uses powerdown mode and if an external clock input is the clock source.
		If your application does not use powerdown mode, leave this pin unconnected.

Table 6. Signal Descriptions (Continued)

Name	Type	Description
RXD	I/O	Receive Serial Data In modes 1, 2, and 3, RXD receives serial port input data. In mode 0, it functions as either an input or an open-drain output for data. RXD shares a package pin with P2.1.
T1CLK	I	Timer 1 External Clock External clock for timer 1. Timer 1 increments (or decrements) on both rising and falling edges of T1CLK. Also used in conjunction with T1DIR for quadrature counting mode. and External clock for the serial I/O baud-rate generator input (program selectable). T1CLK shares a package pin with P1.4.
T2CLK	I	Timer 2 External Clock External clock for timer 2. Timer 2 increments (or decrements) on both rising and falling edges of T2CLK. It is also used in conjunction with T2DIR for quadrature counting mode. T2CLK shares a package pin with P1.6.
T1DIR	I	Timer 1 External Direction External direction (up/down) for timer 1. Timer 1 increments when T1DIR is high and decrements when it is low. Also used in conjunction with T1CLK for quadrature counting mode. T1DIR shares a package pin with P1.5.
T2DIR	I	Timer 2 External Direction External direction (up/down) for timer 2. Timer 2 increments when T2DIR is high and decrements when it is low. It is also used in conjunction with T2CLK for quadrature counting mode. T2DIR shares a package pin with P1.7.
TXD	O	Transmit Serial Data In serial I/O modes 1, 2, and 3, TXD transmits serial port output data. In mode 0, it is the serial clock output. TXD shares a package pin with P2.0.
V_{CC}	PWR	Digital Supply Voltage Connect each V_{CC} pin to the digital supply voltage.
V_{SS}	GND	Digital Circuit Ground These pins supply ground for the digital circuitry. Connect each V_{SS} pin to ground through the lowest possible impedance path.
WR#	O	Write[†] This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes. WR# shares a package pin with WRL#. [†] When this pin is configured as a special-function signal (P5_MODE.2 = 1), the chip configuration register 0 (CCR0) determines whether it functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.

Table 6. Signal Descriptions (Continued)

Name	Type	Description
WRH#	O	Write High[†] During 16-bit bus cycles, this active-low output signal is asserted for high-byte writes and word writes to external memory. During 8-bit bus cycles, WRH# is asserted for all write operations. WRH# shares a package pin with BHE#. [†] When this pin is configured as a special-function signal (P5_MODE.5 = 1), the chip configuration register 0 (CCR0) determines whether it functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.
WRL#	O	Write Low[†] During 16-bit bus cycles, this active-low output signal is asserted for low-byte writes and word writes to external memory. During 8-bit bus cycles, WRL# is asserted for all write operations. WRL# shares a package pin with WR#. [†] When this pin is configured as a special-function signal (P5_MODE.2 = 1), the chip configuration register 0 (CCR0) determines whether it functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
XTAL1	I	Input Crystal/Resonator or External Clock Input Input to the on-chip oscillator and the internal clock generators. The internal clock generators provide the peripheral clocks, CPU clock, and CLKOUT signal. When using an external clock source instead of the on-chip oscillator, connect the clock input to XTAL1. The external clock signal must meet the V_{IH} specification for XTAL1.
XTAL2	O	Inverted Output for the Crystal/Resonator Output of the on-chip oscillator inverter. Leave XTAL2 floating when the design uses an external clock source instead of the on-chip oscillator.

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4.0 ADDRESS MAP

Table 7. 8XL196NP Address Map

Address (Note 1)	Description	Notes
FF FFFFH FF 3000H	External device (memory or I/O) connected to address/data bus	2
FF 2FFFH FF 2000H	Internal ROM or external device (memory or I/O) connected to address/data bus (determined by EA# pin)	2, 3
FF 1FFFH FF 0100H	External device (memory or I/O) connected to address/data bus	2
FF 00FFH FF 0000H	Reserved for ICE	4
FE FFFFH 0F 0000H	Overlaid memory (reserved for future devices); locations xF0000–xF00FFH are reserved for ICE	2
0E FFFFH 01 0000H	896 Kbytes of external device (memory or I/O) connected to address/data bus	2
00 FFFFH 00 3000H	External device (memory or I/O) connected to address/data bus	2
00 2FFFH 00 2000H	External device (memory or I/O) connected to address/data bus or remapped internal ROM	2, 5, 6
00 1FFFH 00 1FE0H	Memory-mapped peripheral special-function registers (SFRs)	2, 4, 7
00 1FDFH 00 1F00H	Internal peripheral special-function registers (SFRs)	4, 7, 9
00 1EFFH 00 0400H	External device (memory or I/O) (reserved for future devices)	6
00 03FFH 00 0100H	Upper register file (general-purpose register RAM)	8, 9
00 00FFH 00 0018H	Lower register file (general-purpose register RAM and stack pointer)	8, 10
00 0017H 00 0000H	Lower register file (CPU SFRs)	4, 7, 8, 10

NOTES:
1. Internally, there are 24 address bits (A23:0); however, only 20 address lines (A19:0) are bonded out. The external address space is 1 Mbyte (00000–FFFFFH).
2. Address with indirect, indexed, or extended modes.
3. The 8XL196NP resets to internal address FF2080H (FF2080H in internal ROM or F2080H in external memory).
4. Unless otherwise noted, write 0FFH to reserved memory locations and write 0 to reserved SFR bits.
5. These areas are mapped into internal ROM if the REMAP bit (CCB1.2) is set and EA# is at logic 1. Otherwise, they are mapped to external memory.
6. **WARNING**: The contents or functions of these memory locations may change with future device revisions, in which case a program that relies on one or more of these locations may not function properly.
7. Refer to the *8XC196NP, 80C196NU Microcontroller User's Manual*.
8. Code executed in locations 000000H to 0003FFH will be forced external.
9. Address with indirect, indexed, or extended modes or through register windows.
10. Address with direct, indirect, indexed, or extended modes.

5.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature .... −60°C to +150°C
Supply Voltage with Respect to V_{SS} .... −0.5 V to +7.0 V
Power Dissipation .... 1.5 W

OPERATING CONDITIONS*

T_A (Ambient Temperature Under Bias) ....0°C to +70°C
V_{CC} (Digital Supply Voltage) .... 2.7 V to 3.3 V
F_{XTAL1} (Input Frequency for V_{CC} = 2.7–3.3 V)
                         (Note 1).............. 8 MHz to 14 MHz

NOTES:
1.   This device is static and should operate below 1 Hz, but has been tested only down to 8 MHz.

NOTICE: This document contains information on products in the design phase of development. The specifications are subject to change without notice. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

*WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

5.1 DC Characteristics

Table 8. DC Characteristics at V_{CC} = 2.7 − 3.3 V

Symbol	Parameter	Min	Typ[1]	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current		28	40	mA	XTAL1 = 14MHz V_{CC} = 3.3V Device in Reset
I_{IDLE}	Idle Mode Current		14	25	mA	XTAL1 = 14MHz V_{CC} = 3.3 V
I_{PD}	Powerdown Mode Current (Note 2)		50	75	µA	V_{CC} = 3.3V
I_{LI}	Input Leakage Current (all input pins except RESET)			±10	µA	$V_{SS} < V_{IN} < V_{CC}$
V_{IL}	Input Low Voltage (all pins)	−0.5		0.4	V	
V_{IH}	Input High Voltage	0.2 V_{CC} +1.3		V_{CC} + 0.5	V	
V_{IL1}	Input Low Voltage XTAL1	−0.5		0.3 V_{CC}	V	
V_{IH1}	Input High Voltage XTAL1	0.7 V_{CC}		V_{CC} + 0.5	V	

NOTES:
1.   Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and with V_{CC} = 3.0 V.
2.   For temperatures below 100°C, typical is 10 µA.
3.   For all pins except P4.3:0, which have higher drive capability.
4.   If V_{OL} is held above 0.45 V or V_{OH} is held below Vcc–0.7 V, current on pins must be externally limited to the following values: I_{OL} and I_{OH} maximum on all output pins is 12 mA.
5.   For all pins that were weakly pulled high during RESET. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
6.   Pin capacitance is not tested. C_S is based on design simulations.

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Table 8. DC Characteristics at V_{CC} = 2.7 – 3.3 V(Continued)

Symbol	Parameter	Min	Typ[1]	Max	Units	Test Conditions
V_{OL}	Output Low Voltage (output configured as complementary) (Note 3,4)			0.3 0.45	V V	I_{OL} = 200 µA I_{OL} = 3.2 mA
V_{OH}	Output High Voltage (output configured as complementary) (Note 4)	V_{CC} − 0.3 V_{CC} − 0.7			V V	I_{OH} = −200 µA I_{OH} = −3.2 mA
V_{OH2}	Output High Voltage on XTAL2	V_{CC} − 0.3 V_{CC} − 0.7			V V	I_{OH} = −100 µA I_{OH} = −500 µA
V_{OL1}	Output Low Voltage on P4.x (output configured as complementary)			0.45 0.6	V V	I_{OL} = 8 mA I_{OL} = 10 mA
V_{OL2}	Output Low Voltage in RESET on ALE, INST, and NMI			0.45	V	I_{OL} = 2 µA
V_{OH1}	Output High Voltage in RESET (Note 5)	V_{CC} − 0.7			V	I_{OH} = −2 µA
V_{OL3}	Output Low Voltage in RESET for ONCE pin			0.8	V	I_{OL} = 30 µA
V_{OL4}	Output Low Voltage on XTAL2			0.3 0.45	V V	I_{OL} = 100 µA I_{OL} = 500 µA
V_{TH+}−$V_{TH−}$	Hysteresis voltage width on RESET# pin		0.3		V	
C_S	Pin Capacitance (any pin to V_{SS}) (Note 6)			10	pF	
R_{RST}	RESET Pull-up Resistor	9		95	kΩ	V_{CC} = 3.3V, V_{IN} = 2.0V

NOTES:
1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and with V_{CC} = 3.0 V.
2. For temperatures below 100°C, typical is 10 µA.
3. For all pins except P4.3:0, which have higher drive capability.
4. If V_{OL} is held above 0.45 V or V_{OH} is held below Vcc–0.7 V, current on pins must be externally limited to the following values: I_{OL} and I_{OH} maximum on all output pins is 12 mA.
5. For all pins that were weakly pulled high during RESET. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
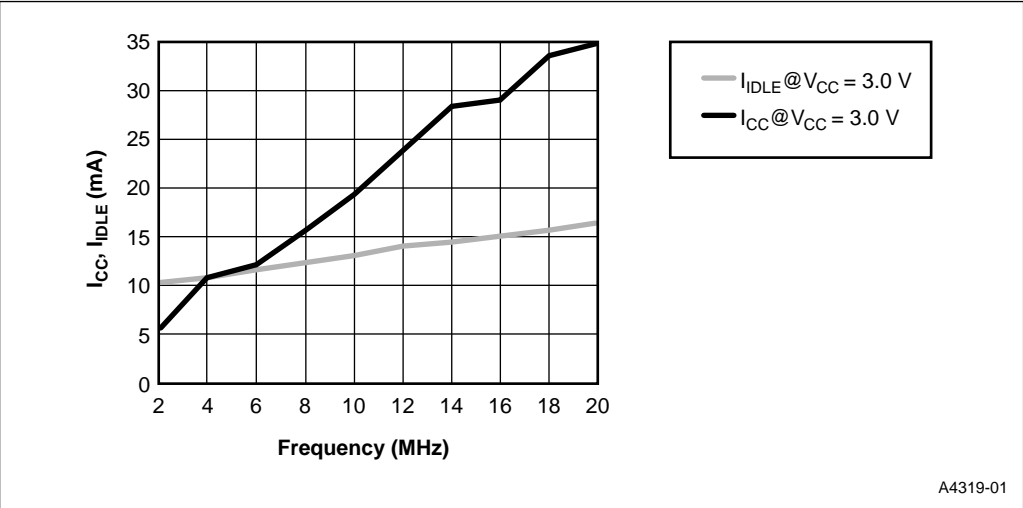6. Pin capacitance is not tested. C_S is based on design simulations.

Figure 5. I_{CC}, I_{IDLE} versus Frequency

5.2 AC Characteristics — Multiplexed Bus Mode

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 9. AC Characteristics, Multiplexed Bus Mode

Symbol	Parameter	V_{CC} = 2.7 V – 3.3 V		Units
		Min	Max	
The 8XL196NP Will Meet These Specifications				
F_{XTAL1}	Input frequency on XTAL1	8	14	MHz
T_{XTAL1}	Period, $1/F_{XTAL1}$	71	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High/Low	20	110	ns
T_{CLCL}	CLKOUT Cycle Time	$2T_{XTAL1}$		ns
T_{CHCL}	CLKOUT High Period	$T_{XTAL1} - 10$	$T_{XTAL1} + 15$	ns
T_{AVRL}	A15:0, CSx# Valid to RD# Low	$2T_{XTAL1} - 30$		ns
T_{AVWL}	A15:0, CSx# Valid to WR# Low	$2T_{XTAL1} - 15$		ns
T_{WHSH}	A19:16, CSx# Hold after WR# Rising Edge	0		
T_{RHSH}	A19:16, CSx# Hold after RD# Rising Edge	0		
T_{CLLH}	CLKOUT Low to ALE High	−12	10	ns
T_{LLCH}	ALE Low to CLKOUT High	−10	15	ns
T_{LHLH}	ALE Cycle Time	$4T_{XTAL1}$		ns (1)
T_{LHLL}	ALE High Period	$T_{XTAL1} - 15$	$T_{XTAL1} + 5$	ns
T_{AVLL}	AD15:0 Valid to ALE Low	$T_{XTAL1} - 18$		ns
T_{LLAX}	AD15:0 Hold after ALE Low	$T_{XTAL1} - 25$		ns
T_{LLRL}	ALE Low to RD# Low	$T_{XTAL1} - 30$		ns
T_{RLCL}	RD# Low to CLKOUT Low	5	30	ns
T_{RLRH}	RD# Low Period	$T_{XTAL1} - 10$		ns (1)
T_{RHLH}	RD# High to ALE High	$T_{XTAL1} - 5$	$T_{XTAL1} + 20$	ns (2)
T_{RLAZ}	RD# Low to Address Float		5	ns
T_{LLWL}	ALE Low to WR# Low	$T_{XTAL1} - 30$		ns
T_{CLWL}	CLKOUT Low to WR# Low	−18	10	ns
T_{QVWH}	Data Valid before WR# High	$T_{XTAL1} - 23$		ns (1)
T_{CHWH}	CLKOUT High to WR# High	−10	10	ns
T_{WLWH}	WR# Low Period	$T_{XTAL1} - 10$		ns (1)

NOTES:
1. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.
2. Assuming back-to-back bus cycles.
3. 8-bit bus only.

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Table 9. AC Characteristics, Multiplexed Bus Mode (Continued)

Symbol	Parameter	V_{CC} = 2.7 V – 3.3 V		Units
		Min	Max	
The 8XL196NP Will Meet These Specifications				
T_{WHQX}	Data Hold after WR# High	$T_{XTAL1} - 33$		ns
T_{WHLH}	WR# High to ALE High	$T_{XTAL1} - 12$	$T_{XTAL1} + 20$	ns (2)
T_{WHBX}	BHE#, INST Hold after WR# High	$T_{XTAL1} - 10$		ns
T_{WHAX}	A15:8 Hold after WR# High	$T_{XTAL1} - 30$		ns (3)
T_{RHBX}	BHE#, INST Hold after RD# High	$T_{XTAL1} - 10$		ns
T_{RHAX}	A15:8 Hold after RD# High	$T_{XTAL1} - 25$		ns (3)

NOTES:
1. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.
2. Assuming back-to-back bus cycles.
3. 8-bit bus only.

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Table 10. AC Characteristics, Multiplexed Bus Mode

| Symbol	Parameter	V_{CC} = 2.7 V – 3.3 V		Units
		Min	**Max**	
The External Memory System Must Meet These Specifications				
T_{AVYV}	AD15:0 Valid to READY Setup		$2T_{XTAL1} - 60$	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{XTAL1} - 20$	ns (1)
T_{AVDV}	AD15:0 Valid to Input Data Valid		$3T_{XTAL1} - 55$	ns (2)
T_{RLDV}	RD# Active to Input Data Valid		$T_{XTAL1} - 25$	ns (2)
T_{SLDV}	Chip-select Low, A19:16 Valid to Data Valid		$4T_{XTAL1} - 75$	
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{XTAL1} - 50$	ns
T_{RHDZ}	End of RD# to Input Data Float		$T_{XTAL1} - 10$	ns
T_{RXDX}	Data Hold after RD# Inactive	0		ns

NOTES:
1. Exceeding the maximum specification causes additional wait states.
2. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.

Table 11. AC Timing Symbol Definitions

Signals								Conditions	
A[†]	Address	H	HOLD#	S	CSx#			H	High
B	BHE#	HA	HLDA#	W	WR#, WRH#, WRL#			L	Low
C	CLKOUT	L	ALE	X	XTAL1			V	Valid
D	Data	Q	Data Out	Y	READY			X	No Longer Valid
G	Buswidth	R	RD#	BR	BREQ#			Z	Floating

[†] Address bus (demultiplexed mode) or Address/data bus (multiplexed mode)

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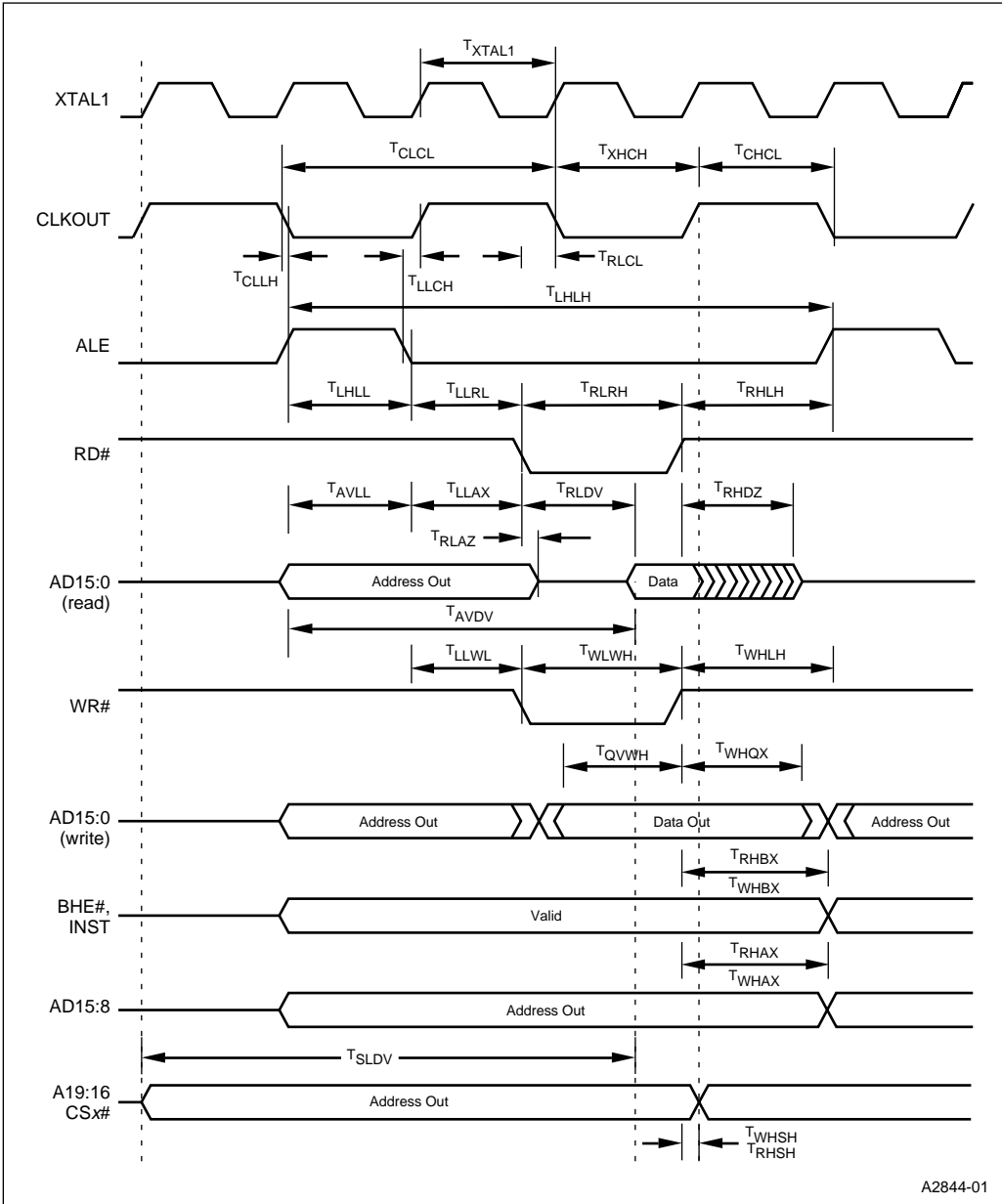
Figure 6. System Bus Timing Diagram (Multiplexed Bus Mode)

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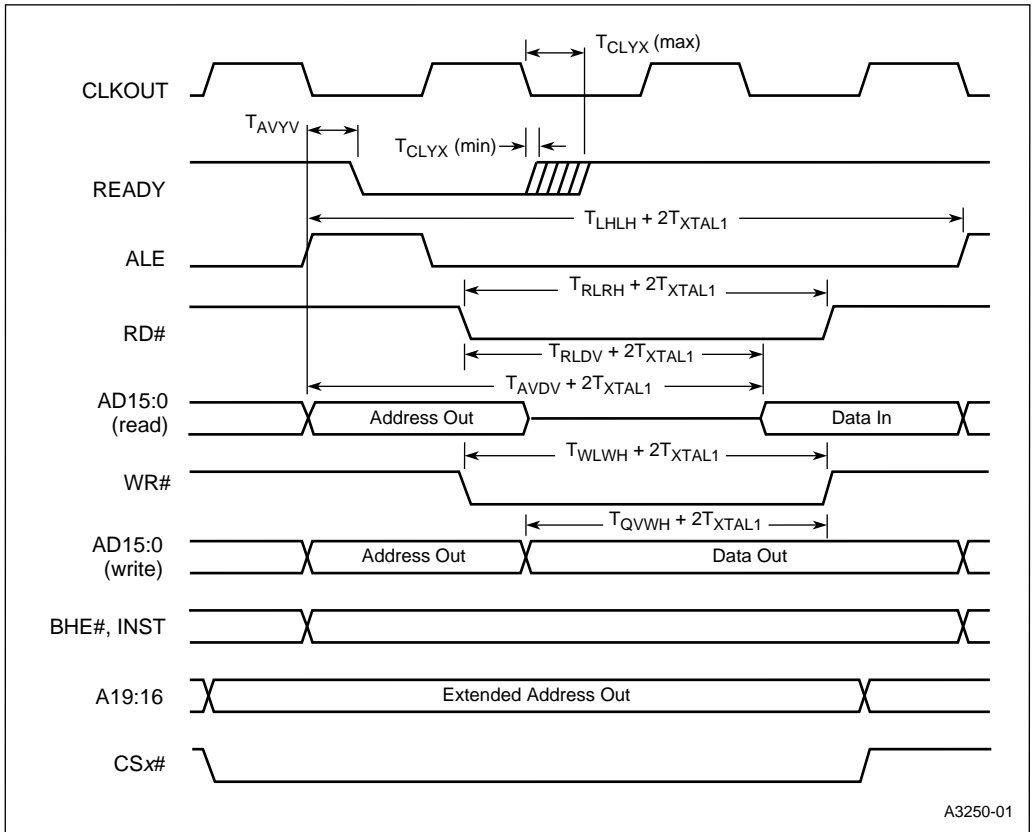
Figure 7. READY Timing Diagram (Multiplexed Bus Mode)

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5.3 AC Characteristics — Demultiplexed Bus Mode

Test Coditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 12. AC Characteristics, Demultiplexed Bus Mode

Symbol	Parameter	V_{CC} = 2.7 V – 3.3 V		Units
		Min	**Max**	
The 8XL196NP Will Meet These Specifications				
F_{XTAL1}	Input requency on XTAL1	8	14	MHz
T_{XTAL1}	Period, $1/F_{XTAL1}$	71	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High/Low	20	110	ns
T_{CLCL}	CLKOUT Cycle Time	$2T_{XTAL1}$		ns
T_{CHCL}	CLKOUT High Period	$T_{XTAL1} - 10$	$T_{XTAL1} + 15$	ns
T_{AVRL}	A19:0, CSx# Valid to RD# Low	$2T_{XTAL1} - 48$		ns
T_{AVWL}	A19:0, CSx# Valid to WR# Low	$2T_{XTAL1} - 37$		ns
T_{CLLH}	CLKOUT Low to ALE High	-12	10	ns
T_{LLCH}	ALE Low to CLKOUT High	-15	15	ns
T_{LHLH}	ALE Cycle Time	$4T_{XTAL1}$		ns (1)
T_{LHLL}	ALE High Period	$T_{XTAL1} - 12$	$T_{XTAL1} + 10$	ns
T_{RLCH}	RD# Low to CLKOUT High	-5	20	ns
T_{RLRH}	RD# Low Period	$2T_{XTAL1} - 10$		ns (1)
T_{RHLH}	RD# High to ALE High	$T_{XTAL1} - 5$	$T_{XTAL1} + 20$	ns (2)
T_{WLCH}	WR# Low to CLKOUT High	-10	10	ns
T_{QVWH}	Data Valid before WR# High	$3T_{XTAL1} - 55$		ns (1)
T_{CHWH}	CLKOUT High to WR# High	-15	5	ns
T_{WLWH}	WR# Low Period	$2T_{XTAL1} - 13$		ns (1)
T_{WHQX}	Data Hold after WR# High	$T_{XTAL1} - 25$		ns
T_{WHLH}	WR# High to ALE High	$T_{XTAL1} - 10$	$T_{XTAL1} + 20$	ns (2)
T_{WHBX}	BHE#, INST Hold after WR# High	$T_{XTAL1} - 10$		ns
T_{WHAX}	A19:0, CSx# Hold after WR# High	0		ns
T_{RHBX}	BHE#, INST Hold after RD# High	$T_{XTAL1} - 10$		ns
T_{RHAX}	A19:0, CSx# Hold after RD# High	0		ns

NOTES:
1. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.
2. Assuming back-to-back bus cycles.

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Table 13. AC Characteristics, Demultiplexed Bus Mode

Symbol	Parameter	V_{CC} = 2.7 V − 3.3 V		Units
		Min	**Max**	
The External Memory System Must Meet These Specifications				
T_{AVYV}	A19:0, CS*x*# Valid to READY Setup		$3T_{XTAL1} - 88$	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low		$T_{XTAL1} - 30$	ns (1)
T_{AVDV}	A19:0, CS*x*# Valid to Input Data Valid		$4T_{XTAL1} - 75$	ns (2)
T_{RLDV}	RD# Active to Input Data Valid		$2T_{XTAL1} - 33$	ns (2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{XTAL1} - 50$	ns
T_{RHDZ}	End of RD# to Input Data Float		$T_{XTAL1} - 5$	ns
T_{RXDX}	Data Hold after RD# Inactive	0		ns

NOTES:
1. Exceeding the maximum specification causes additional wait states.
2. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.
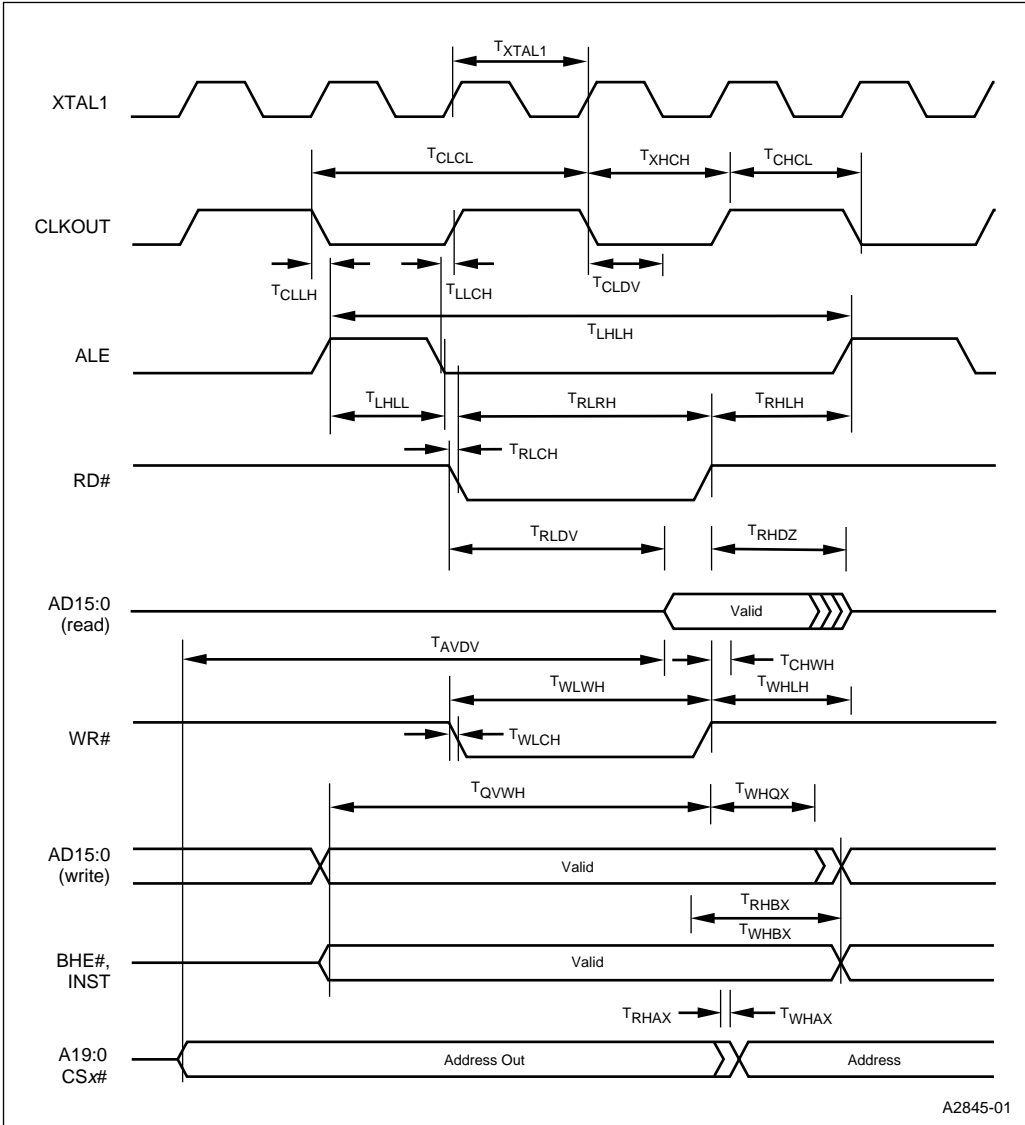
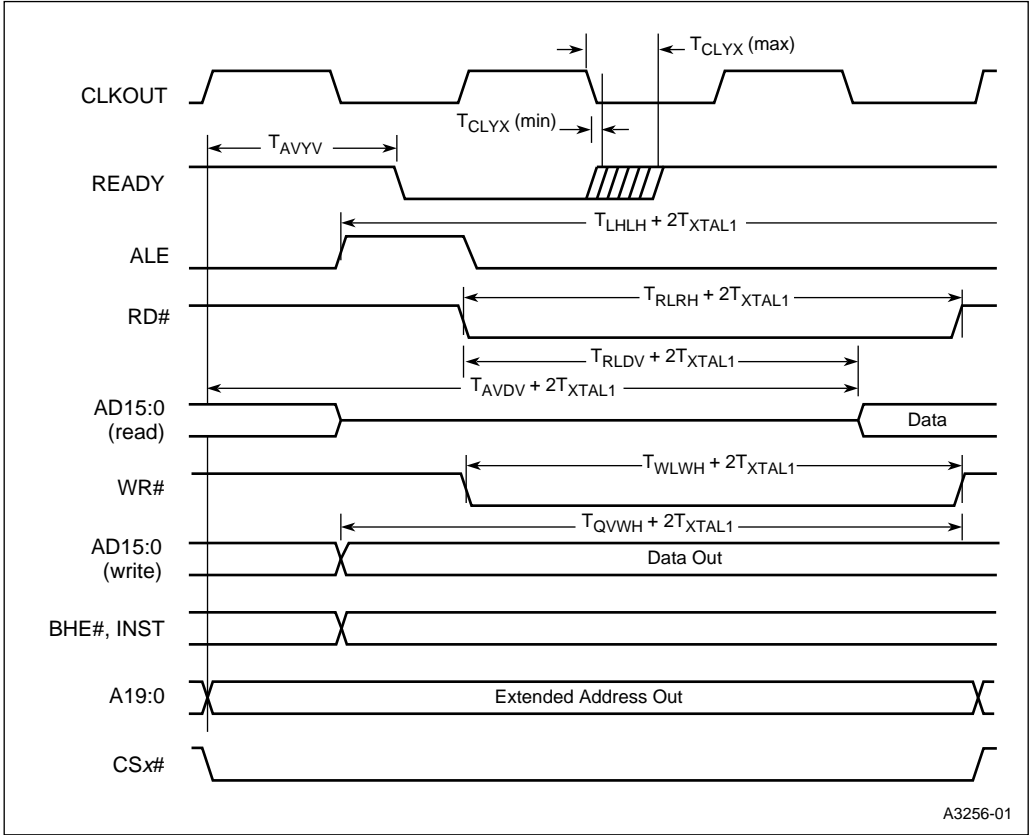**Figure 8. System Bus Timing Diagram (Demultiplexed Bus Mode)**

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Figure 9. READY Timing Diagram (Demultiplexed Bus Mode)

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5.4 HOLD#/HLDA# Timing

Table 14. HOLD#/HLDA# Timings

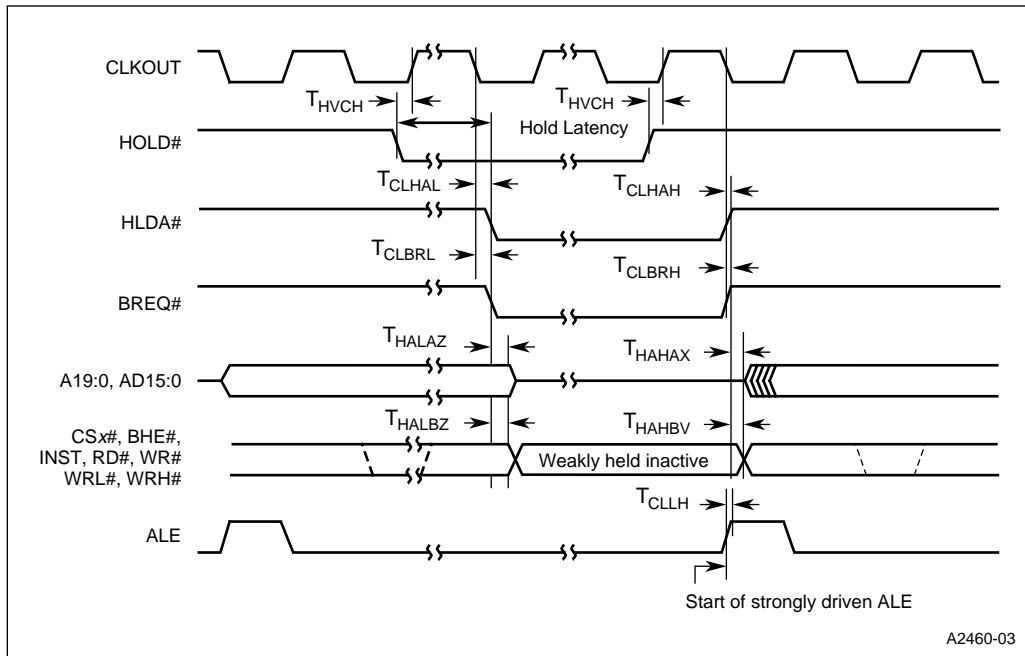| Symbol	Parameter	V_{CC} = 2.7 V – 3.3V		Units
		Min	Max	
T_{HVCH}	HOLD# Setup Time (to guarantee recognition at next clock)	83		ns
T_{CLHAL}	CLKOUT Low to HLDA# Low	−15	15	ns
T_{CLBRL}	CLKOUT Low to BREQ# Low	−15	15	ns
T_{HALAZ}	HLDA# Low to Address Float		33	ns
T_{HALBZ}	HLDA# Low to BHE#, INST, RD#, WR# Weakly Driven		25	ns
T_{CLHAH}	CLKOUT Low to HLDA# High	−25	15	ns
T_{CLBRH}	CLKOUT Low to BREQ# High	−25	25	ns
T_{HAHAX}	HLDA# High to Address No Longer Floating	−20		ns
T_{HAHBV}	HLDA# High to BHE#, INST, RD#, WR# Valid	−20		ns

Figure 10. HOLD#/HLDA# Timing Diagram

5.5 AC Characteristics — Serial Port, Shift Register Mode

Table 15. Serial Port Timing — Shift Register Mode

Symbol	Parameter	V_{CC} = 2.7 V – 3.3V		Units
		Min	**Max**	
T_{XLXL}	Serial Port Clock period (BRR ≥ x002H) (BRR = x001H) (Note 1)	$6T_{XTAL1}$ $4T_{XTAL1}$		ns ns
T_{QVXH}	Output data setup to clock high	$3T_{XTAL1} - 30$		ns
T_{XHQX}	Output data hold after clock high	$2T_{XTAL1} - 90$		ns
T_{XHQV}	Next output data valid after clock high		$2T_{XTAL1} + 50$	ns
T_{DVXH}	Input data setup to clock high	$2T_{XTAL1} + 50$		ns
T_{XHDX}	Input data hold after clock high	0		ns
T_{XHQZ}	Last clock high to output float		$5T_{XTAL1} + 30$	ns

NOTE:
1. The minimum baud-rate register value for receptions is x002H and the minimum baud-rate register value for transmissions is x001H.
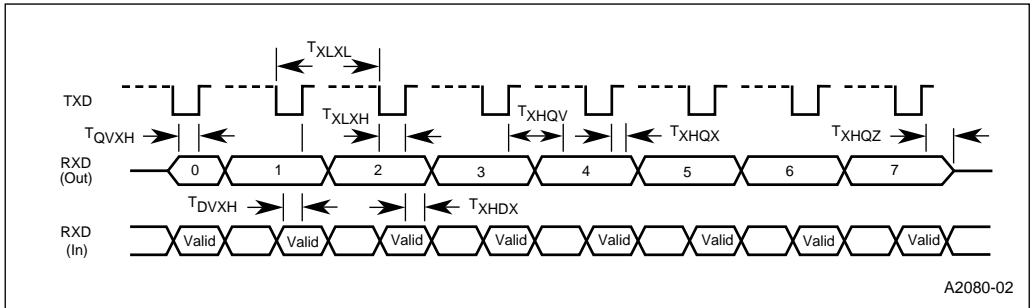

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Figure 11. Serial Port Waveform — Shift Register Mode

5.6 External Clock Drive

Table 16. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Input frequency	8	14	MHz
T_{XLXL}	Period (T_{XTAL1})	71	125	ns
T_{XHXX}	High Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXX}	Low Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

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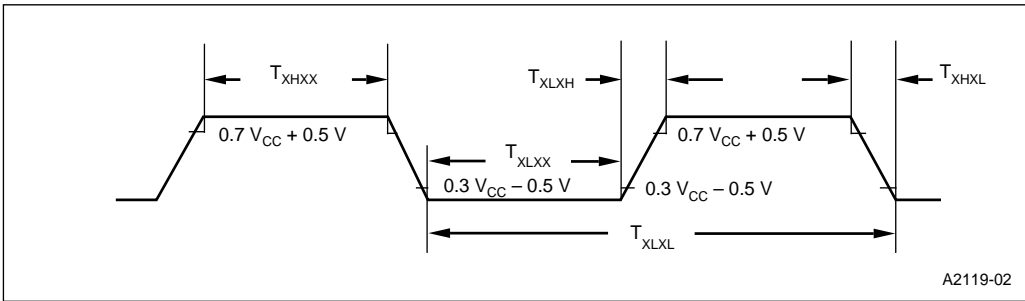
Figure 12. External Clock Drive Waveforms

5.7 Test Output Waveforms

AC testing inputs are driven at 2.5 V for a logic "1" and 0.25 V for a logic "0". Timing measurements are made at 1.6 V for a logic "1" and 0.5 V for a logic "0".

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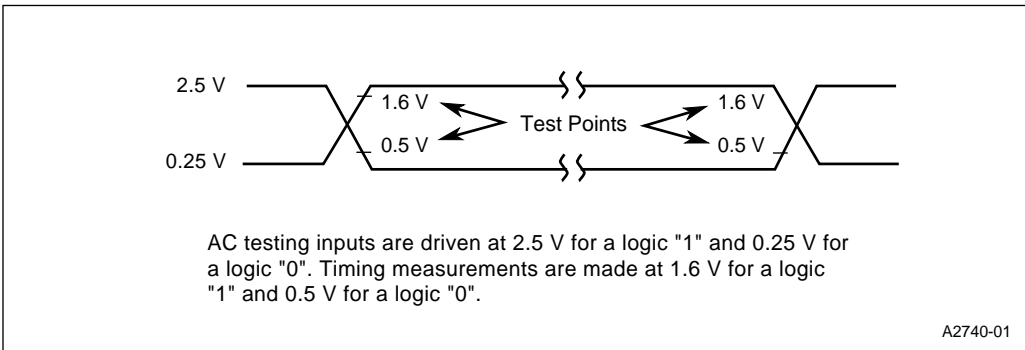
Figure 13. AC Testing Output Waveforms During 3.0 Volt Testing

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V_{LOAD} + 0.15 V

V_{LOAD}

V_{LOAD} − 0.15 V

Timing Reference Points

V_{OH} − 0.15 V

V_{OL} + 0.15 V

For timing purposes, a port pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} \leq 10$ mA.
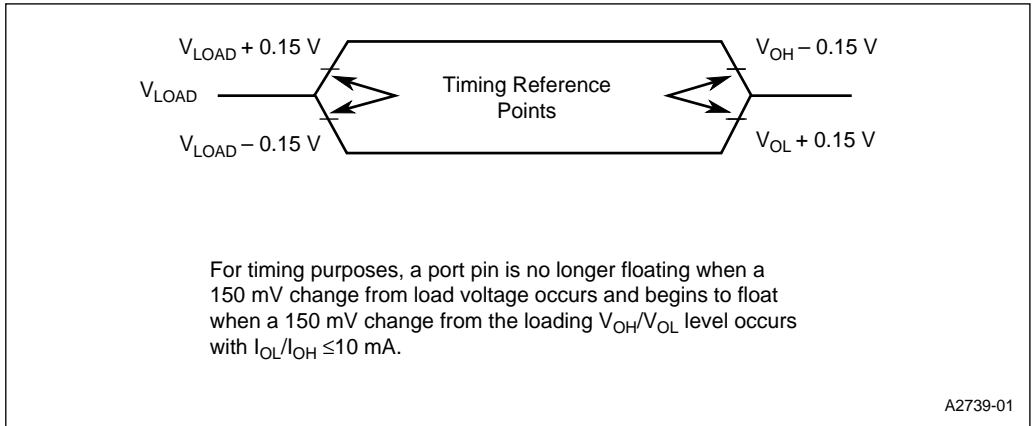
A2739-01

Figure 14. Float Waveforms During 3.0 Volt Testing

6.0 THERMAL CHARACTERISTICS

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values will change depending on operating conditions and the application. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology.

Table 17. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
100-pin SQFP	55°C/W	14°C/W
100-pin QFP	56°C/W	16°C/W

7.0 8XL196NP ERRATA

Change identifiers have been used on embedded products since 1990. The change identifier is the last character in the FPO number. The FPO number is typically a nine character number located on the second line of the topside package mark. The following errata listing is applicable to the B–step (denoted by a "B" or "C" at the end of the topside tracking number):

1. Any jump, conditional jump, or call instruction located within six bytes of the top of a page, i.e., 0FFFA–0FFFFH, may cause a jump to the wrong page. To ensure this problem does not occur, place at least six NOPs at the top of each page.

8.0 DATASHEET REVISION HISTORY

This datasheet is valid for devices with an "A" at the end of the topside tracking number. Datasheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

PRELIMINARY