Ordering number : EN 4365B

CMOS LSI

LC5852N

Four-Bit Single-Chip Microcontroller with On-Chip LCD Drivers for Small-Scale Control in Medium-Speed Applications

Overview

The LC5852N is a high-performance four-bit single-chip built-in LCD driver microprocessor that provides a variety of attractive features including low-voltage operation and low power dissipation. The LC5852N was developed as an upwardly compatible version of the LC5851N and provides a ROM capacity increased from 1024 to 2048 15-bit words and a RAM capacity increased from 64 × 4 bits to 128 × 4 bits.

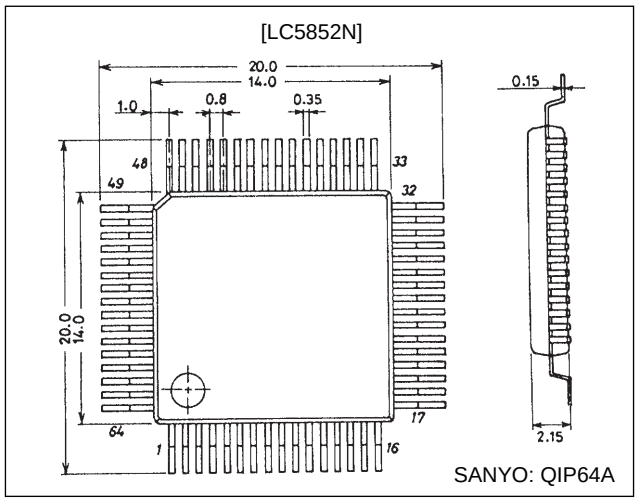
Applications

- System control and LCD display in cameras, radios and similar products
- System control and LCD display in miniature electronic test equipment and consumer health maintenance products
- The LC5852N is optimal for end products with LCD displays and, in particular, for battery operated products.

Package Dimensions

unit: mm

3057-QIP64A



Features

The LC5852N is an upwardly compatible version of the LC5851N and, as such, has the following features.

- Extremely broad allowable operating ranges

Power supply option	Cycle time	Power supply voltage range	Note
EXT-V	10 µs	$V_{SS}2$ = –4.0 to –5.5 V	When using an 800 kHz ceramic resonator
EXT-V	20 µs	$V_{SS}2$ = –4.0 to –5.5 V	When using a 400 kHz ceramic resonator
EXT-V	61 µs	$V_{SS}2$ = –2.3 to –5.5 V	When using a 65 kHz crystal oscillator
EXT-V	122 µs, 244 µs	$V_{SS}2$ = –2.0 to –5.5 V	When using a 32 kHz crystal oscillator
Li	122 µs, 244 µs	$V_{SS}2$ = –2.6 to –3.6 V*	When using a 32 kHz crystal oscillator
Ag	122 µs, 244 µs	$V_{SS}1$ = –1.3 to –1.65 V	When using a 32 kHz crystal oscillator

Note: * When the backup flag is set, the BAK pin is shorted to $V_{SS}2$. (See the user's manual for details.)

- Low current drain

		HALT mode (typical)
— Ceramic oscillator (CF):	400 kHz (5.0 V)	150 µA
— Crystal oscillator (Xtal):	32 kHz (1.5 V, Ag specifications)	2.0 µA (for LCD biases other than 1/3) 3.5 µA (for an LCD bias of 1/3)
— Crystal oscillator (Xtal):	32 kHz (3.0 V, Li specifications)	1.0 µA (for LCD biases other than 1/3) 5.0 µA (for an LCD bias of 1/3)

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
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- Timer functions
  - — One six-bit programmable timer
  - — Time base timer (for clock applications)
- Standby functions
  - — Clock standby function (HALT mode)
    The LC5852N provides a halt function that reduces power dissipation. In halt mode, only the oscillator, divider and LCD driver circuits operate. All other internal operations are stopped. This mode allows the LC5852N to easily implement a low-power clock function.
  - — Full standby function (HOLD mode)
  - — HALT mode is cleared by two external factors and two internal factors.
- Improved I/O functions
  - — External interrupt pins
  - — Input pins that can clear HALT mode (up to 9 pins)
  - — Input ports with software controllable input resistors: up to 8 pins
  - — Input ports with built-in floating prevention circuits: up to 8 pins
  - — LCD drivers; common: 4 pins, segment pins: 25 pins
  - — General-purpose I/O ports: 8 pins
  - — General-purpose inputs: 9 pins
  - — General-purpose outputs (1): 6 pins
    (ALM pin, LIGHT pin)
  - — General-purpose outputs (2): 25 pins
    (when all 25 LCD segment ports are used as general-purpose outputs)
  - — Pseudo-serial output port: 1 set
    (Three pins: output, BUSY, clock)

Function Overview

- Program ROM: 2048 × 15 bits
- On-chip RAM: 128 × 4 bits
- All instructions execute in a single cycle
- HALT mode clear and interrupt functions
  (External factors)
  Changes in the S and M port input signals
  Changes in the INT pin input signal
  (Internal factors)
  Overflow from the clock divider circuit
  Timer underflow
- Subroutines can be nested up to four levels (including interrupts)
- Powerful hardware to improve processing capabilities
  - — On-chip segment PLA circuit and segment decoder: The LCD driver outputs can handle LCD panel segment display without incurring software overhead.
  - — All LCD driver output pins can be switched to be used as output ports.
  - — One six-bit programmable timer
  - — Part of the RAM area can be used as a working area.
  - — Built-in clock oscillator and 15-stage divider (also used for LCD alternation signal generation)
- Highly flexible LCD panel drive output pins (25)

Supported drive types	Maximum number of segments	Required common pins
1/3 bias—1/4 duty	100 segments	4 pins
1/3 bias—1/3 duty	75 segments	3 pins
1/2 bias—1/4 duty	100 segments	4 pins
1/2 bias—1/3 duty	75 segments	3 pins
1/2 bias—1/2 duty	50 segments	2 pins
Static	25 segments	1 pin

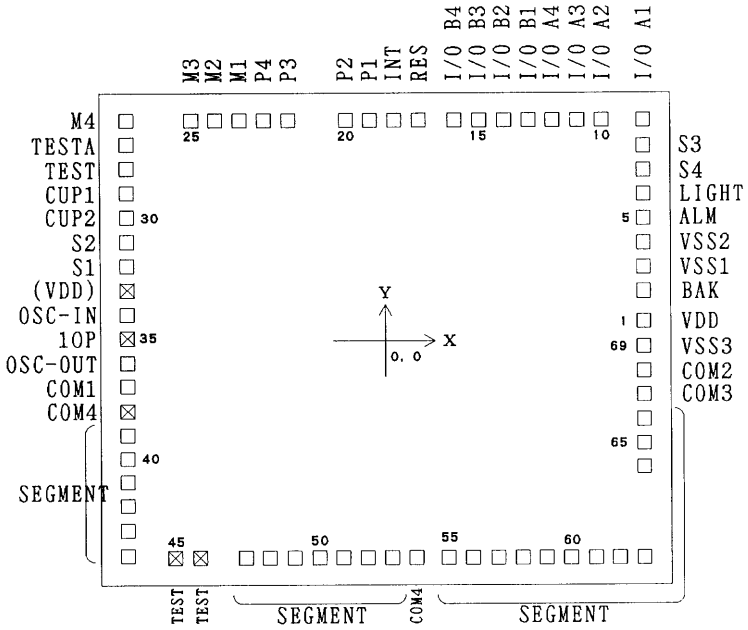
  - — The LCD output pins can be converted to use as general-purpose output pins.
    CMOS type: 25 pins (maximum)
    p-channel open drain type: 3 pins (maximum)
- An oscillator appropriate for the system specifications can be selected.
  32 or 65 kHz crystal oscillator, or
  400 or 800 kHz ceramic oscillator

Delivery formats

QIP-64A or chip product

Pin and Pad Assignment

Chip size: 4.19 × 3.66 mm
Pad size: 120 × 120 µm
Chip thickness: 480 µm (chip specification products)



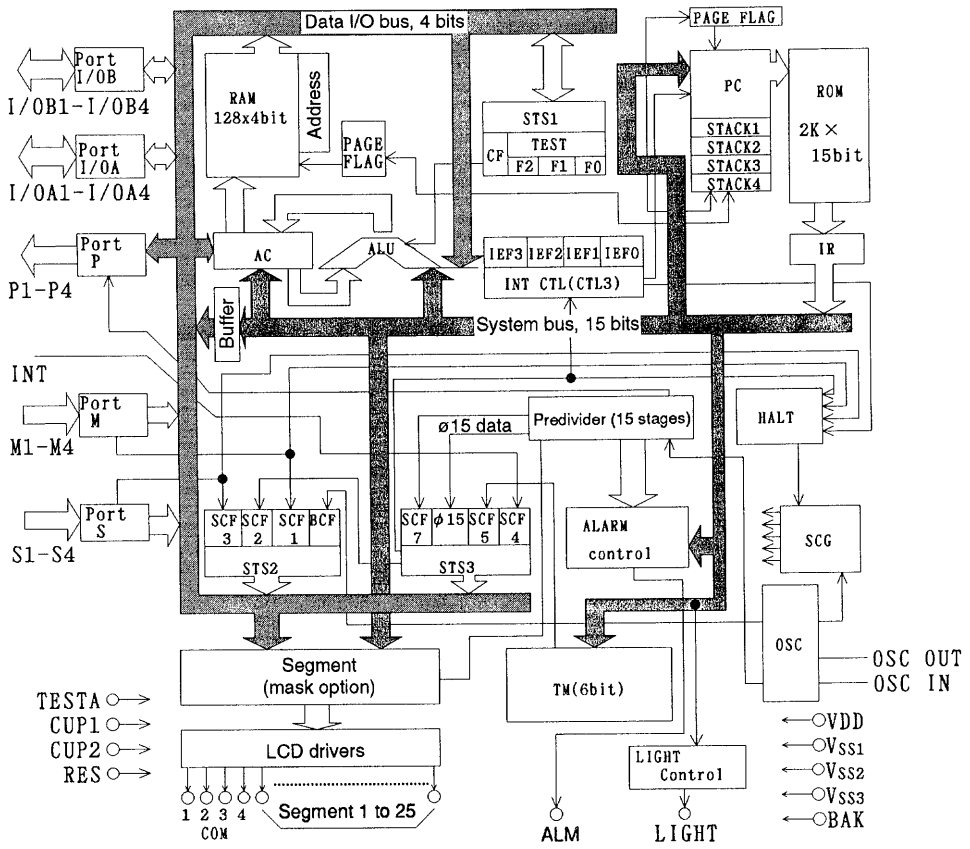
Pin No.	Pad No.	Symbol	Coordinates	
			Xµm	Yµm
40	1	V_{DD}	1899	138
41	2	BAK	1899	358
42	3	$V_{SS}1$	1899	538
43	4	$V_{SS}2$	1899	718
44	5	ALM	1899	898
45	6	LIGHT	1899	1078
46	7	S4	1899	1258
47	8	S3	1899	1438
48	9	I/O A1	1899	1630
49	10	I/O A2	1595	1630
50	11	I/O A3	1415	1630
51	12	I/O A4	1235	1630
52	13	I/O B1	1055	1630
53	14	I/O B2	875	1630
54	15	I/O B3	695	1630
55	16	I/O B4	515	1630
56	17	RES	253	1630
57	18	INT	73	1630
58	19	P1	–107	1630
59	20	P2	–287	1630
60	21	P3	–707	1630
61	22	P4	–887	1630
62	23	M1	–1067	1630

Pin No.	Pad No.	Symbol	Coordinates	
			Xµm	Yµm
63	24	M2	–1247	1630
64	25	M3	–1427	1630
1	26	M4	–1899	1630
2	27	TESTA	–1899	1450
3	28	TEST	–1899	1270
4	29	CUP1	–1899	1090
5	30	CUP2	–1899	910
6	31	S2	–1899	730
7	32	S1	–1899	550
—	33	(V_{DD})	–1899	370
8	34	OSC-IN	–1899	190
—	35	10P	–1899	10
9	36	OSC-OUT	–1899	–169
10	37	COM1	–1899	–349
—	38	COM4	–1899	–529
11	39	Seg01	–1899	–709
12	40	Seg02	–1899	–889
13	41	Seg03	–1899	–1069
14	42	Seg04	–1899	–1249
15	43	Seg05	–1899	–1429
16	44	Seg06	–1899	–1609
—	45	TEST	–1553	–1630
—	46	TEST	–1373	–1630

Pin No.	Pad No.	Symbol	Coordinates	
			Xµm	Yµm
17	47	Seg07	–1033	–1630
18	48	Seg08	–853	–1630
19	49	Seg09	–673	–1630
20	50	Seg10	–493	–1630
21	51	Seg11	–313	–1630
22	52	Seg12	–133	–1630
23	53	Seg13	46	–1630
24	54	COM4	226	–1630
25	55	Seg14	459	–1630
26	56	Seg15	639	–1630
27	57	Seg16	819	–1630
28	58	Seg17	999	–1630
29	59	Seg18	1179	–1630
30	60	Seg19	1359	–1630
31	61	Seg20	1539	–1630
32	62	Seg21	1719	–1630
33	63	Seg22	1899	–1630
34	64	Seg23	1899	–954
35	65	Seg24	1899	–774
36	66	Seg25	1899	–594
37	67	COM3	1899	–414
38	68	COM2	1899	–234
39	69	$V_{SS}3$	1899	–54

Note: 1. The pin numbers are those for the QIP-64A mass production package.
2. The pad coordinates given above take the center of the chip as the origin and specify the center of the pad.
3. TESTA pin (pin 2) in the QIP-64A product must be connected to the minus side of the power supply.
4. TEST pin (pin 3) in the QIP-64A product must be left open.
5. Pad 27 in the chip product must either be connected to the minus side of the power supply or left open.
6. Pads 28, 45 and 46 in the chip product must be left open.
7. If the chip product is used, the substrate must be connected to V_{DD}.
8. Do not use dip-soldering techniques to mount the QIP-64A package product.

System Block Diagram



LC5852N System Block Diagram

AC:	Accumulator
ALU:	Arithmetic and logic unit
INT CTL:	Interrupt control circuit
PC:	Program counter
TM:	Preset timer (6 bits)
IR:	Instruction register
HALT:	Intermittent control circuit
SCG:	System clock generator
STS1:	Status register 1
STS2:	Status register 2
STS3:	Status register 3
CF:	Carry flag
BCF:	Backup flag
SCF1:	M port flag
SCF2:	STS3 flag
SCF3:	S port flag
SCF4:	INT signal change flag
SCF5:	Timer overflow flag
ø15:	Contents of the fifteenth stage of the divider circuit
SCF7:	Divider circuit overflow flag

Pin Functions

Pin	I/O	QIP-64 Pin No.	Function	Option	At reset
V_{DD}	—	40	Power supply plus side		
BAK	—	41	LSI internal logic block minus power supply In Li specification products, connect a capacitor between BAK and V_{DD} to prevent incorrect operation.		Backup flag set Backup flag cleared (depending on the power supply option)
$V_{SS}1$ $V_{SS}2$ $V_{SS}3$	— — —	42 43 39	Power supply minus side • External component connections differ depending on mask options and other factors. In products for Ag use, connect $V_{SS}1$ to the power supply minus side. In other products, connect $V_{SS}2$ to the power supply minus side. • The pins other than the minus pin are used for the LCD driver power supply.	• Ag specifications • Li specifications • EXT-V specifications	
CUP1 CUP2	— —	4 5	Connections for the LCD drive voltage boost (cut) capacitor.		
OSC-IN	Input	8	Used for real-time clock and the system clock.	• Crystal oscillator use (XT option) • Ceramic resonator use (CF option) The CF option can only be specified for EXT-V specification products.	
OSC-OUT	Output	9			
10P	—	—	Connected to OSC-IN or OSC-OUT and used for the oscillator phase compensation capacitor. Can only be used in the chip product.		
S1 S2 S3 S4	Input	7 6 47 46	Dedicated input port • Includes either a ø10 (32 ms), ø8 (8 ms), or ø2 (2 ms) chattering exclusion circuit (PLA mask option). * These values are for the case where a 32.768 kHz crystal is used. • Pull-down resistors are built in.	Inclusion (or exclusion) of a low level hold transistor	The pull-down resistor transistor is on.
M1 M2 M3 M4	Input	62 63 64 1	Dedicated input port • Input connections for acquiring data to internal RAM • Pull-down resistors are built in.	Inclusion (or exclusion) of a low level hold transistor	The pull-down resistor transistor is on.
I/O A1 I/O A2 I/O A3 I/O A4	I/O	48 49 50 51	I/O port • Input connections for acquiring data to internal RAM • Output connections for data output from internal RAM • The input or output state can be switched by two instructions.		Input mode
I/O B1 I/O B2 I/O B3 I/O B4	I/O	52 53 54 55	I/O port • Input connections for acquiring data to internal RAM • Output connections for data output from internal RAM • The input or output state can be switched by two instructions.		Input mode
P1 P2 P3 P4	Output	58 59 60 61	Output port • Output connections for data output from internal RAM		Either a high- or low-level output. (Undefined)
ALM	Output	44	Dedicated output This pin can output a signal modulated either at 4 kHz or 2 kHz, or at 4 kHz or 1 kHz under program control. Alternatively, an unmodulated signal can be output. * These values are for the case where a 32.768 kHz crystal is used.	• Modulated signals (4 kHz, 2 kHz, or unmodulated) • Modulated signals (4 kHz, 1 kHz, or unmodulated)	Low-level output
LIGHT	Output	45	Dedicated output This pin can drive a power transistor.		Low-level output

Continued on next page.

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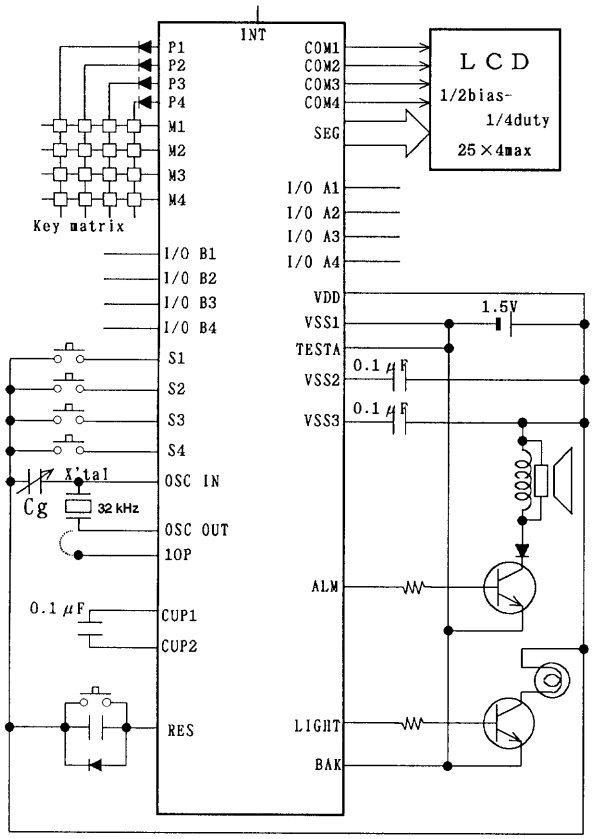
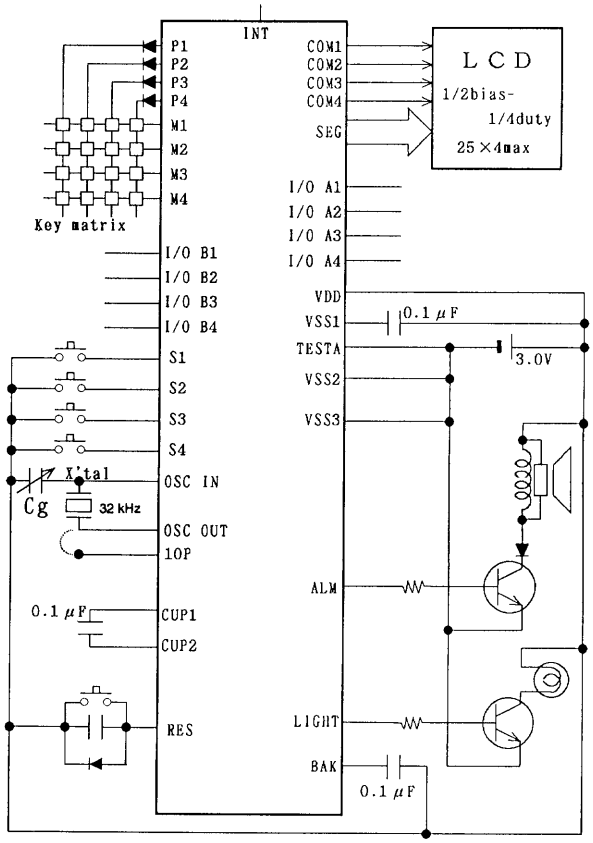
<table>
<tr><th>Pin</th><th>I/O</th><th>QIP-64
Pin No.</th><th>Function</th><th>Option</th><th>At reset</th></tr>
<tr><td>RES</td><td>Input</td><td>56</td><td>LSI internal reset input
• Reset can be performed on either a high or low input level.
• Built-in pull-up or pull-down resistor
Note: The applied signal must be held for at least 500 µs.</td><td>Pull-up or pull-down resistor selection</td><td></td></tr>
<tr><td>INT</td><td>Input</td><td>57</td><td>External interrupt request input
• Interrupt detection can be performed for either falling or rising edges.
• Built-in pull-up or pull-down resistor</td><td>• Pull-up or pull-down resistor selection
• Signal change type (rising or falling) selection</td><td></td></tr>
<tr><td>TESTA</td><td>Input</td><td>2</td><td>Test input
• QIP-64 products: connect to the power supply – side
• Chip products: Leave open or connect to the power supply – side</td><td></td><td></td></tr>
<tr><td>TEST</td><td>—</td><td>3</td><td>Test input
This pin must be left open. (It cannot be used in user systems.)</td><td></td><td></td></tr>
<tr><td>Seg1
Seg2 to Seg25</td><td>Output</td><td>11
12 to36</td><td>• LCD drive/general-purpose output pins
— LCD drive
I STATIC
II 1/2 bias – 1/2 duty
III 1/2 bias – 1/3 duty
IV 1/2 bias – 1/4 duty
V 1/3 bias – 1/3 duty
VI 1/3 bias – 1/4 duty
Items I to V are specified as master options.
• General-purpose output mode (CMOS output)
— LCD/general-purpose output control under program control is disabled by adoption of the segment PLA.
— Arbitrary combinations of LCD drive and general purpose outputs are possible.</td><td>• Switching between LCD drive outputs and general-purpose outputs
• LCD drive method switching
— STATIC
— 1/2 bias – 1/2 duty
— 1/2 bias – 1/3 duty
— 1/2 bias – 1/4 duty
— 1/3 bias – 1/3 duty
— 1/3 bias – 1/4 duty
• General-purpose outputs
— CMOS</td><td>• LCD drive
— All segments lit
— All segments off
* Set by a mask option
• General-purpose outputs
— High level
— Low level
* Set by a mask option</td></tr>
<tr><td>COM1
COM2
COM3
COM4</td><td>Output</td><td>10
38
37
24</td><td>LCD common polarity drive outputs
These pins are used as follows depending on the LCD drive method used.
(Note that these are typical specifications for 32.768 kHz when ø0 is used for the alternation frequency.)
<table>
<tr><th></th><th>Static</th><th>1/2 duty</th><th>1/3 duty</th><th>1/4 duty</th></tr>
<tr><td>COM1</td><td>❍</td><td>❍</td><td>❍</td><td>❍</td></tr>
<tr><td>COM2</td><td>×</td><td>❍</td><td>❍</td><td>❍</td></tr>
<tr><td>COM3</td><td>×</td><td>×</td><td>❍</td><td>❍</td></tr>
<tr><td>COM4</td><td>×</td><td>×</td><td>×</td><td>❍</td></tr>
<tr><td>Alternation frequency</td><td>32 Hz</td><td>32 Hz</td><td>42.7 Hz</td><td>32 Hz</td></tr>
</table>
Note: An × indicates that the corrsponding common pin is not used with that LCD drive method.
LCD drive type. Do not use hold mode in CF specification products that use the LCD driver.
(The alternation frequency signal is stopped in hold mode.)</td><td></td><td></td></tr>
</table>

Application Circuit Examples

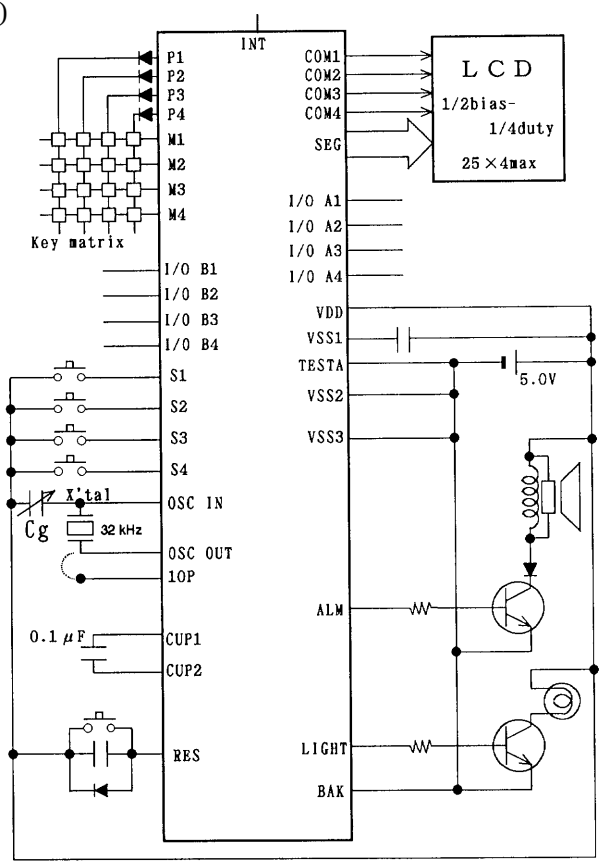
1. Representative application for Ag specification products (1/3 bias - 1/4 duty)



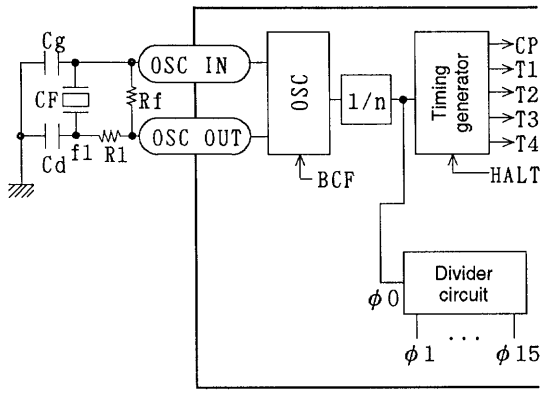
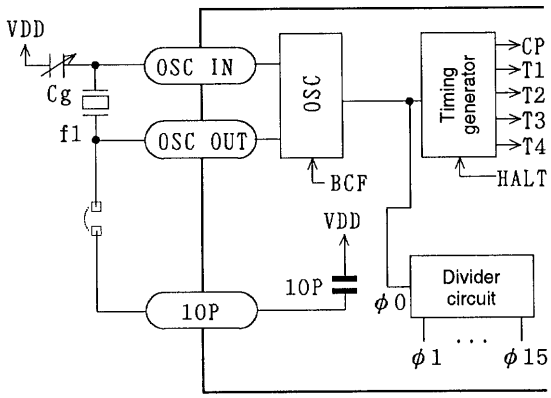
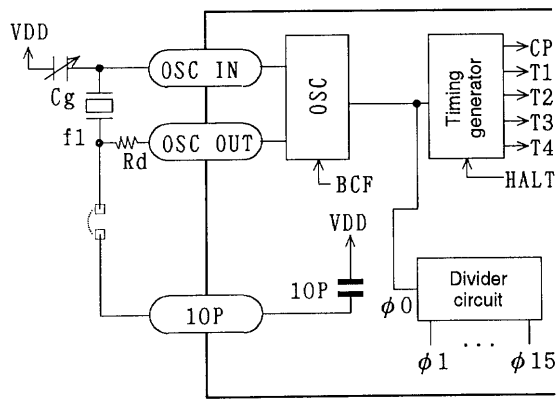
2. Representative application for lithium specification products (1/2 bias - 1/4 duty)



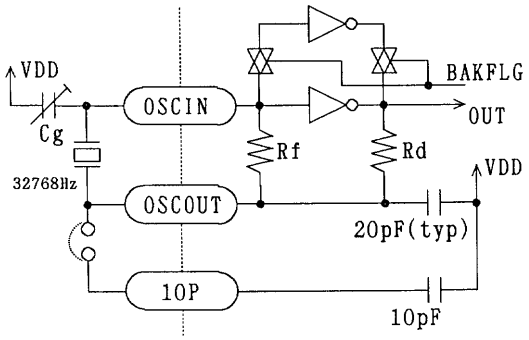
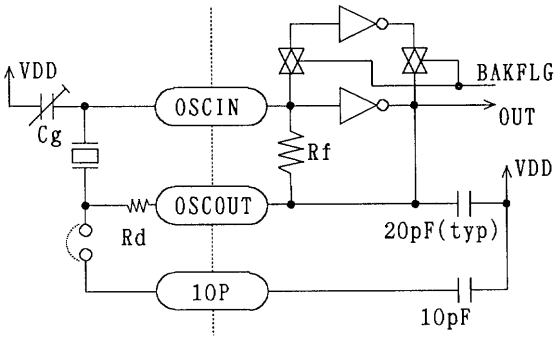
3. Representative application for EXT-V specification products (1/2 bias - 1/4 duty)



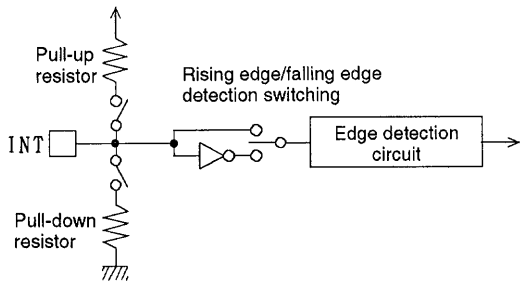
Oscillator Circuit Options

Option	Circuit Form	Note
CF • 400 kHz • 800 kHz		• The cycle time is 4 × n times the f1 period (n : 2). • The divider outputs (ø1 to ø15) are used, for example, as the LCD drive waveform generation clock and as the S and K port chattering prevention clock.
Xtal (32.768 kHz)		• The cycle time is four times the f1 period. • The divider outputs (ø1 to ø15) are used, for example, as the LCD drive waveform generation clock, as the S and K port chattering prevention clock and as a clock time base. • The 10P connection can only be used in chip products.
Xtal (65 kHz)		• The cycle time is four times the f1 period. (Used when the cycle time is 61 µs.) • The divider outputs (ø1 to ø15) are used, for example, as the LCD drive waveform generation clock and as the S and K port chattering prevention clock. • The 10P connection can only be used in chip products.

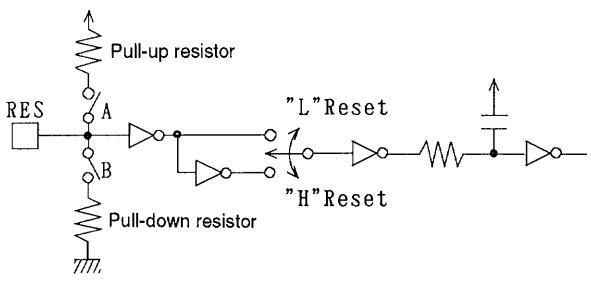
Crystal Oscillator Options

Option	Circuit Form	Note
32 kHz		The resistor Rd for use with a 32 kHz frequency is built in.
65 kHz		

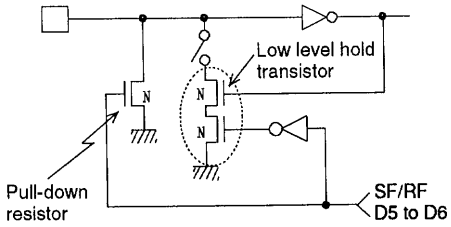
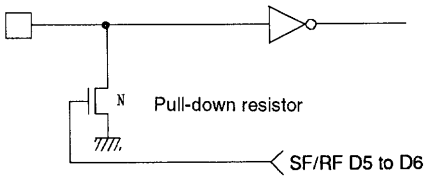
INT Pin Options

Option	Circuit Form	Note
Pull-up resistor, pull-down resistor, or resistor open selection		Built-in resistor selection • Use of the pull-up resistor • Use of the pull-down resistor • Open
Rising edge, falling edge detection selection		Signal change edge detection selection • Rising edge detection • Falling edge detection

RES Pin Options

Option	Circuit Form	Note
Pull-up resistor, pull-down resistor, or resistor open and level selection		Built-in resistor and polarity selection • Pull-up resistor and reset on low • Pull-down resistor and reset on high • Both resistors open and reset on low • Both resistors open and reset on high

Input Port Options

Option	Circuit Form	Note
Use of the hold transistor (low level hold transistor)		This option can be specified individually for each pin in S1 to S4 and M1 to M4. When use of the hold transistor is selected: • This transistor is used to reduce the current drain in the pull-up or pull-down resistor when, for example, a push-button switch is used for S1 or a slide switch is used for S2. • When the input open specifications are used, this transistor turns the resistor on prior to reading the input value and then turns the resistor off after the input value is read. If the input is floating when read, the low-level input hold transistor will operate and hold that level.
Hold transistor unused (open)		When the hold transistor is unused: • The pull-down transistor can be used as a pull-down resistor. • The pull-down transistor can be turned on and off under program control. • The pull-down resistor can be used in the on state without change. • Select the unused option if the input is connected to an external control signal line that will never go to the floating state. • On reset — The resistor will be in the on state during the reset period. — The resistor will keep up the on state when reset is cleared.

The use of the low level hold transistor can be specified individually for each pin in the S1 to S4 and M1 to M4 ports.

1. The S port includes independent (in bit units) chattering exclusion circuits with periods of ø10, ø8, or ø6.
2. The M port includes chattering exclusion circuits that operate for halt mode clear request signals.
   These circuits exclude chattering for periods of ø10, ø8, or ø6 when three of the ports are at the low level and a signal change occurs on the remaining port.

LCD Output Options

Option	Circuit Form
LCD drive	• Used as LCD segment drive pins • The LCD drive type is specified independently. The LCD drive type is common to all LCD drive pins and can be selected from the following set: static, 1/2 bias—1/2 duty, 1/2 bias—1/3 duty, 1/2 bias—1/4 duty, 1/3 bias—1/3 duty, or 1/3 bias—1/4 duty.
CMOS output port	• General-purpose CMOS output ports
P-channel open-drain output port	• General-purpose p-channel open-drain output ports This option can be specified for three specific ports using PLA option specification. Available ports...Pads 64 to 66 (pins 34 to 36)

Mask Option Overview

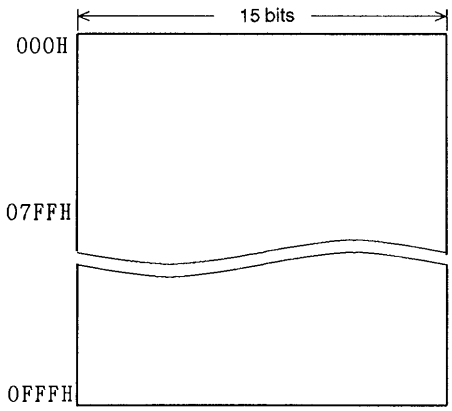
1. Power supply specification selection
   - Ag (Silver battery/1.5 V) specifications
   - Li (Lithium battery/3.0 V) specifications
   - EXT-V specifications (the operating voltage range depends on the oscillator used)
2. Oscillator selection
   - Crystal oscillator (32.768 kHz)
   - Crystal oscillator (65.536 kHz)
   - Ceramic oscillator
3. LCD drive
   - Static
   - 1/2 bias—1/2 duty
   - 1/2 bias—1/3 duty
   - 1/2 bias—1/4 duty
   - 1/3 bias—1/3 duty
   - 1/3 bias—1/4 duty

Note: The LCD ports can all be used as general-purpose outputs. In this case, specify the “UNUSE” option.

6. LCD alternation frequency
   - SLOW (OSC/2048)
   - TYP (OSC/1024)
   - FAST (OSC/512)
   - STOP
5. S port low-level hold transistor
   - Level hold transistor present
   - No level hold transistor
6. M port low-level hold transistor
   - Level hold transistor present
   - No level hold transistor
7. S and M port chattering exclusion frequency
   - SLOW (OSC/1024)
   - TYP (OSC/256)
   - FAST (OSC/64)
8. INT pin resistor selection and signal edge type selection
   - Pull-up resistor (negative)
   - Pull-down resistor (positive)
   - Open (negative)
   - Open (positive)
9. External reset
   - RES pin
   - Simultaneous input to S1 through S4
10. RES pin
    - Pull-up resistor (low-level reset)
    - Pull-down resistor (high-level reset)
    - Open (low-level reset)
    - Open (high-level reset)
11. Power-on reset function (internal reset)
    - USE
    - UNUSE
12. Timer input clock
    - SLOW (OSC/512)
    - FAST (OSC/8)
13. Alarm modulation base frequency
    - SLOW (OSC/8, OSC/32)
    - TYP (OSC/8, OSC/16)
14. Cycle time
    - SLOW (OSC/8)
    - FAST (OSC/4)

Note: Specify “SLOW” for this option if a ceramic oscillator is used.

Internal Register Functions

<table>
<tr><th>Symbol</th><th>R/W</th><th>Function</th><th>Initialization value at reset</th></tr>
<tr><td>PC</td><td>—</td><td>
Program counter
The PC is an 11-bit counter that specifies the program memory (ROM) address of the next instruction to be executed.
Normally, the PC is incremented on each instruction execution, from 000H to 7FFH. However, when a branch or subroutine call is executed, or when an interrupt or initializing reset occurs, the PC is set to a value corresponding to the particular operation. The table below shows how the PC is set for these operations.
<table>
<tr><th>PC / Operation</th><th>PC10</th><th>PC9</th><th>PC8</th><th>PC7</th><th>PC6</th><th>PC5</th><th>PC4</th><th>PC3</th><th>PC2</th><th>PC1</th><th>PC0</th></tr>
<tr><td colspan="2">Initializing reset</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td rowspan="4"></td><td>INT pin external interrupt</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>S or M port external interrupt</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Timer internal interrupt</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Divider internal interrupt</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td colspan="2">Unconditional jump (JMP)</td><td>Page</td><td>P9</td><td>P8</td><td>P7</td><td>P6</td><td>P5</td><td>P4</td><td>P3</td><td>P2</td><td>P1</td><td>P0</td></tr>
<tr><td colspan="2">Conditional jump (BAB0, BAB1, BAB2, BAB3, BAZ, BANZ, BCH, BCNH)</td><td>Page</td><td>P9</td><td>P8</td><td>P7</td><td>P6</td><td>P5</td><td>P4</td><td>P3</td><td>P2</td><td>P1</td><td>P0</td></tr>
<tr><td colspan="2">Subroutine call instruction (CALL)</td><td>Page</td><td>P9</td><td>P8</td><td>P7</td><td>P6</td><td>P5</td><td>P4</td><td>P3</td><td>P2</td><td>P1</td><td>P0</td></tr>
<tr><td colspan="2">Return instruction (RTS, RTSR)</td><td colspan="9">CALL address + 1</td></tr>
</table>
Page: ROM paging performed in 1024 word pages
Pages are specified with the SF and RF instructions.
P0 – P9: Instruction code bits (immediate data)
</td><td></td></tr>
<tr><td>ROM</td><td>R/O</td><td>
Program memory
The on-chip ROM consists of 2048 15-bit words and holds the user programs to be executed.


</td><td></td></tr>
<tr><td>RAM</td><td>R/W</td><td>
Data memory
The on-chip RAM consists of 128 4-bit digits of static RAM in two pages with 64 4-bit digits per page.
This RAM has the following features:
• RAM addresses can be specified directly (immediate addressing) as values in the range 00H to 3FH.
• Arithmetic operations can be performed between the AC and any RAM location.
• Due to the provision of the segment PLA circuit, RAM dedicated to display is not required.
• RAM locations 38H to 3FH have a function that allows direct arithmetic operations with other data without using the AC.
• The AC is used for RAM input, i.e., writing.
</td><td>Undefined</td></tr>
</table>

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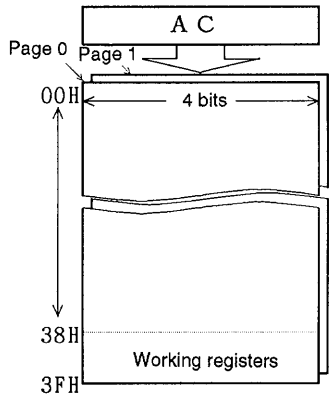
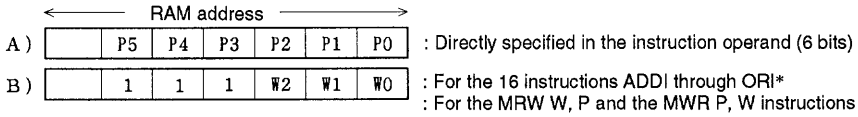
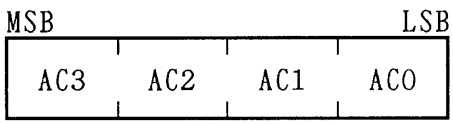
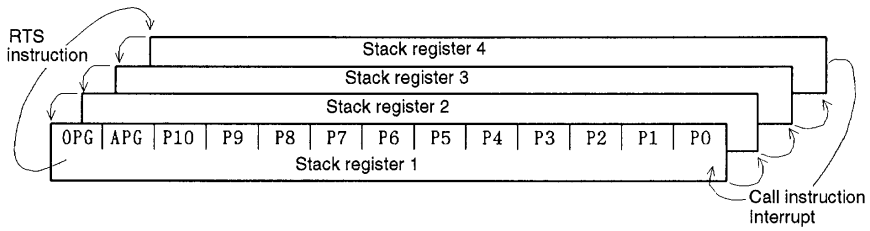
Symbol	R/W	Function	Initialization value at reset
RAM	R/W	 	Undefined
AC	R/W	Accumulator 	Undefined
STACK	R/W	Stack pointer The stack consists of four 13-bit words supporting subroutine calls and interrupts up to four levels deep.  P0 to P10: Program counter (PC) APG: RAM page flag OPG: ROM page flag	01H
APG	R/W	RAM page flag The RAM page flag is a single bit that allows the RAM to be expanded to two pages, where a single RAM page is 64 × 4 bits.	00H
OPG	R/W	ROM page flag The ROM page flag is a single bit that allows the ROM to be expanded to two pages, where a single ROM page is 1024 × 15 bits.	00H
TIM	W	Timer counter The timer is a 6-bit down counter. The timer is set from immediate data in an instruction.	Undefined

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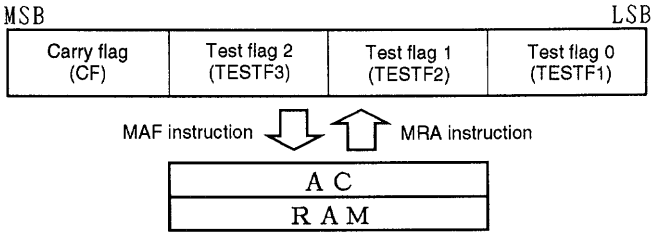
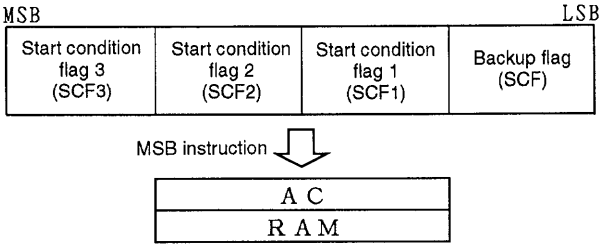
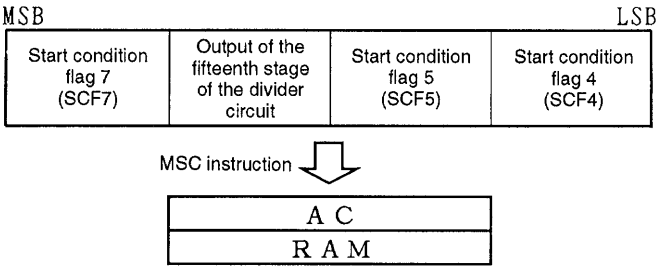
Symbol	R/W	Function	Initialization value at reset
STS1	R/W	Status register 1 (STS1) Status register 1 is a four-bit register whose bits are used as shown below.  * The test flags cannot be used by application programs.	00H
STS2	R/O	Status register 2 (STS2) Status register 2 is a four-bit register whose bits are used as shown below.  SCF1: Set when there was a change in an M port signal (when enabled by an SSW instruction). SCF2: Set when any bit in STS3 is set. SCF3: Set when there was a change in an S port signal (when enabled with an SSW instruction).	Undefined
STS3	R/O	Status register 3 (STS3) Status register 3 is a four-bit register whose bits are used as shown below.  SCF4: Set when there was a change in the INT pin signal (when enabled by an SIC instruction). SCF5: Timer underflow (when enabled by an SIC instruction) SCF4: Divider overflow (when enabled by an SIC instruction)	Undefined

Specifications

These electrical specifications are provisional and subject to change.

EXT-V Specifications

Absolute Maximum Ratings at V_{DD} = 0 V

Parameter	Symbol	Conditions/Pins	min	typ	max	Unit
Maximum supply voltage	$V_{SS}1$		–7.0		+0.3	V
	$V_{SS}2$		–7.0		+0.3	V
	$V_{SS}3$	LCD drive method (1/3 bias)	–8.5		+0.3	V
	$V_{SS}3$	LCD drive method (Any method other than 1/3 bias)	–7.0		+0.3	V
Maximum input voltage	$V_{IN}1$	S1 to 4, M1 to 4, I/OA1 to 4, I/OB1 to 4, INT, RES, OSCIN, 10P, TESTA (with I/OA1 to 4 and I/OB1 to 4 in input mode, 10P is for chip products)	$V_{SS}2$ – 0.3		+0.3	V
Maximum output voltage	$V_{OUT}1$	ALM, LIGHT, P1 to 4, CUP2, OSCOUT, TEST, I/OA1 to 4, I/OB1 to 4 (with I/OA and I/OB in output mode)	$V_{SS}2$ – 0.3		+0.3	V
	$V_{OUT}2$	SEGOUT, COM1 to 4, CUP1	$V_{SS}3$			V
Operating temperature	Topr		–20		+70	°C
Storage temperature	Tstg		–30		+125	°C

Allowable Operating Ranges at Ta = –20 to +70°C, V_{DD} = 0 V

Parameter	Symbol	Conditions/Pins		min	typ	max	Unit
Supply voltage	$V_{SS}1$	32 kHz crystal oscillator specifications		–5.5		–1.3	V
	$V_{SS}2$			–5.5		–2.0	V
	$V_{SS}3$			–8.25		–2.0	V
Supply voltage	$V_{SS}1$	65 kHz crystal oscillator specifications		–5.5		–1.3	V
	$V_{SS}2$			–5.5		–2.3	V
	$V_{SS}3$			–8.25		–2.3	V
Supply voltage	$V_{SS}1$	External input used		–5.5		–1.7	V
	$V_{SS}2$			–5.5		–3.5	V
	$V_{SS}3$			–8.25		–3.5	V
Supply voltage	$V_{SS}1$	400 kHz CF specifications		–5.5		–2.0	V
	$V_{SS}2$			–5.5		–4.0	V
	$V_{SS}3$			–8.25		–4.0	V
Input high level voltage	$V_{IH}1$	All input ports except OSCIN		$0.3 \times V_{SS}2$		0	V
Input low level voltage	$V_{IL}1$			$V_{SS}2$		$0.7 \times V_{SS}2$	V
Input high level voltage	$V_{IH}2$	OSCIN pin, when external input used, Figure 8		$0.2 \times V_{SS}2$		0	V
Input low level voltage	$V_{IL}2$			$V_{SS}2$		$0.8 \times V_{SS}2$	V
Operating frequency	fopg1	$V_{SS}2$ = –2.0 to –5.5 V	OSCIN/OSCOUT, 32 kHz crystal oscillator, Figure 2	32		33	kHz
Operating frequency	fopg2	$V_{SS}2$ = –2.3 to –5.5 V	OSCIN/OSCOUT, 65 kHz crystal oscillator, Figure 2	60		66	kHz
Operating frequency	fopg3	$V_{SS}2$ = –3.5 to –5.5 V	OSCIN external input, Figure 8	32		220	kHz
Operating frequency	fopg4	$V_{SS}2$ = –4.0 to –5.5 V	OSCIN/OSCOUT, CF 400 kHz, Figure 1	360	400	440	kHz
Operating frequency	fopg5	$V_{SS}2$ = –4.0 to –5.5 V	OSCIN/OSCOUT, CF 800 kHz, Figure 1	720	800	880	kHz

Continued on next page.

Electrical Characteristics at Ta = –20 to +70°C, V_{DD} = 0 V

Parameter	Symbol	Conditions/Pins		min	typ	max	Unit
Input resistance	R_{IN}1A	$V_{SS}2$ = –2.9 V, V_{IN} = 0.8 × $V_{SS}2$	Low-level hold transistor*, Figure 3	10		200	kΩ
	R_{IN}1B	$V_{SS}2$ = –2.9 V, V_{IN} = V_{DD}	Low-level pull-in transistor*, Figure 3	200	700	2000	kΩ
	R_{IN}2A	$V_{SS}2$ = –2.9 V, V_{IN} = $V_{SS}2$	INT pin pull-up resistor	200	700	2000	kΩ
Input resistance	R_{IN}2B	$V_{SS}2$ = –2.9 V, V_{IN} = V_{DD}	INT pin pull-down resistor	200	700	2000	kΩ
	R_{IN}3	$V_{SS}2$ = –2.9 V, V_{IN} = V_{DD} or $V_{SS}2$	RES	5		50	kΩ
Output high level voltage	V_{OH} (1)	$V_{SS}2$ = –2.4 V, I_{OH} = 1 mA	ALM	–1	–0.3		V
Output low level voltage	V_{OL} (1)	$V_{SS}2$ = –2.4 V, I_{OL} = 1 mA	ALM		$V_{SS}2$ + 0.3	$V_{SS}2$ + 1	V
Output high level voltage	V_{OH} (2)	$V_{SS}2$ = –2.4 V, I_{OH} = 0.3 mA	LIGHT, Port P	–1	–0.3		V
Output low level voltage	V_{OL} (2)	$V_{SS}2$ = –2.4 V, I_{OL} = 0.5 mA	LIGHT, Port P		$V_{SS}2$ + 0.3	$V_{SS}2$ + 1	V
Output high level voltage	V_{OH} (3)	$V_{SS}2$ = –2.4 V, I_{OH} = 0.1 mA	I/O ports	–1	–0.3		V
Output high level voltage	V_{OH} (4)	$V_{SS}2$ = –2.4 V, I_{OH} = –50 µA	I/O ports	–0.6	–0.2		V
Output low level voltage	V_{OL} (4)	$V_{SS}2$ = –2.4 V, I_{OL} = 0.1 mA	I/O ports		$V_{SS}2$ + 0.3	$V_{SS}2$ + 1	V
Segment driver output impedances • When used as CMOS output ports							
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –2.4 V, I_{OH} = –10 µA	Segment Pads 62 to 64, QIP64 pins 34 to 36	–1	–0.3		V
Output low level voltage	V_{OL} (5)	$V_{SS}2$ = –2.4 V, I_{OL} = 100 µA			$V_{SS}2$ + 0.3	$V_{SS}2$ + 1	V
Output high level voltage	V_{OH} (6)	$V_{SS}2$ = –2.4 V, I_{OH} = –5 µA	Segment Pads 38 to 41 and 44 to 61, QIP64 pins 11 to 23 and 25 to 33	–1	–0.3		V
Output low level voltage	V_{OL} (6)	$V_{SS}2$ = –2.4 V, I_{OL} = 20 µA			$V_{SS}2$ + 0.3	$V_{SS}2$ + 1	V
• When used as p-channel open-drain output ports							
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –2.4 V, I_{OH} = –10 µA	Segment Pads 62 to 64, QIP64 pins 34 to 36	–1	–0.3		V
Output off leakage current	I_{OFF}	$V_{SS}2$ = –2.9 V, V_{OL} = $V_{SS}2$				1	µA
• Static drive							
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –2.4 V, I_{OH} = –0.4 µA,	All segments	–0.2			V
Output low level voltage	V_{OL} (5)	$V_{SS}2$ = –2.4 V, I_{OL} = 0.4 µA				$V_{SS}2$ + 0.2	V
Output high level voltage	V_{OH} (7)	$V_{SS}2$ = –2.4 V, I_{OH} = –4 µA	COM1	–0.2			V
Output low level voltage	V_{OL} (7)	$V_{SS}2$ = –2.4 V, I_{OL} = 4 µA				$V_{SS}2$ + 0.2	V
• Duplex drive (1/2 bias—1/2 duty)							
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –2.4 V, I_{OH} = –0.4 µA	All segments	–0.2			V
Output low level voltage	V_{OL} (5)	$V_{SS}2$ = –2.4 V, I_{OL} = 0.4 µA				$V_{SS}2$ + 0.2	V
Output high level voltage	V_{OH} (7)	$V_{SS}2$ = –2.4 V, I_{OH} = –4 µA	COM1, 2	–0.2			V
Output middle level voltage	V_{OM}	$V_{SS}2$ = –2.4 V, I_{OH} = –4µA, I_{OL} = 4 µA		$V_{SS}2/2$ – 0.2		$V_{SS}2/2$ + 0.2	V
Output low level voltage	V_{OL} (7)	$V_{SS}2$ = –2.4 V, I_{OL} = 4 µA				$V_{SS}2$ + 0.2	V

Note: * S1, S2, S3, S4, M1, M2, M3, M4

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Parameter	Symbol	Conditions		min	typ	max	Unit
• 1/2 bias—1/3 duty and 1/2 bias—1/4 duty methods							
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –2.4 V, I_{OH} = –0.4 µA	All segments	–0.2			V
Output low level voltage	V_{OL} (5)	$V_{SS}2$ = –2.4 V, I_{OL} = 0.4 µA				$V_{SS}2$ + 0.2	V
Output high level voltage	V_{OH} (7)	$V_{SS}2$ = –2.4 V, I_{OH} = –4 µA	COM1 to 3 (for 1/3 duty methods) COM1 to 4 (for 1/4 duty methods)	–0.2			V
Output middle level voltage	V_{OM}	$V_{SS}2$ = –2.4 V, I_{OH} = –4 µA, I_{OL} = 4 µA		$V_{SS}2/2$ – 0.2		$V_{SS}2/2$ + 0.2	V
Output low level voltage	V_{OL} (7)	$V_{SS}2$ = –2.4 V, I_{OL} = 4 µA				$V_{SS}2$ + 0.2	V
• 1/3 bias—1/3 duty and 1/3 bias—1/4 duty methods							
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –2.4 V, I_{OH} = –0.4 µA	All segments	–0.2			V
Output middle level voltage	$V_{OM}1$-1	$V_{SS}2$ = –2.4 V, I_{OH} = –0.4 µA		$V_{SS}2/2$ – 0.2		$V_{SS}2/2$ + 0.2	V
	$V_{OM}1$-2	I_{OL} = 0.4 µA		$V_{SS}2$ – 0.2		$V_{SS}2$ + 0.2	V
Output low level voltage	V_{OL} (5)	$V_{SS}2$ = –2.4 V, I_{OL} = 0.4 µA				$V_{SS}3$ + 0.2	V
Output high level voltage	V_{OH} (7)	$V_{SS}2$ = –2.4 V, I_{OH} = –4 µA	COM1 to 3 (for 1/3 duty methods) COM1 to 4 (for 1/4 duty methods)	–0.2			V
Output middle level voltage	$V_{OM}2$-1	$V_{SS}2$ = –2.4 V, I_{OH} = –4 µA		$V_{SS}2/2$ –0.2		$V_{SS}2/2$ +0.2	V
	$V_{OM}2$-2	I_{OL} = 4 µA		$V_{SS}2$ – 0.2		$V_{SS}2$ + 0.2	V
Output low level voltage	V_{OL} (7)	$V_{SS}2$ = –2.4 V, I_{OL} = 4 µA				$V_{SS}3$ + 0.2	V

Electrical Characteristics at Ta = –20 to +70°C, V_{DD} = 0 V

Parameter	Symbol	Conditions		min	typ	max	Unit
Input resistance	R_{IN}1A	$V_{SS}2$ = –5.0 V, V_{IN} = 0.8 · $V_{SS}2$	Low-level hold transistor*, Figure 3	10	45	150	kΩ
	R_{IN}1B	$V_{SS}2$ = –5.0 V, V_{IN} = V_{DD}	Low-level pull-in transistor*, Figure 3	100	350	1000	kΩ
	R_{IN}2A	$V_{SS}2$ = –5.0 V, V_{IN} = $V_{SS}2$	INT pin pull-up resistor	100	350	1000	kΩ
	R_{IN}2B	$V_{SS}2$ = –5.0 V, V_{IN} = V_{DD}	INT pin pull-down resistor	100	350	1000	kΩ
	R_{IN}3	$V_{SS}2$ = –5.0 V, V_{IN} = V_{DD} or $V_{SS}2$	RES	10	20	50	kΩ
Output high level voltage	V_{OH} (1)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –1.5 mA	ALM	–1	–0.3		V
Output low level voltage	V_{OL} (1)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OL} = 1.5 mA	ALM		$V_{SS}2$ + 0.3	$V_{SS}2$ + 1	V
Output high level voltage	V_{OH} (2)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –0.5 mA	LIGHT, Port P	–1	–0.3		V
Output low level voltage	V_{OL} (2)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OL} = 0.7 mA	LIGHT, Port P		$V_{SS}2$ + 0.3	$V_{SS}2$ + 1	V
Output high level voltage	V_{OH} (3)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –0.13 mA	I/O ports	–1	–0.3		V
Output high level voltage	V_{OH} (4)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –50 µA	I/O ports	–0.6	–0.2		V
Output low level voltage	V_{OL} (4)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OL} = 0.13 mA	I/O ports		$V_{SS}2$ + 0.3	$V_{SS}2$ + 1	V

Note: * S1, S2, S3, S4, M1, M2, M3, M4

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Parameter	Symbol	Conditions		min	typ	max	Unit
Segment driver output impedances • When used as CMOS output ports							
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –15 µA	Segment Pads 62 to 64, QIP64 pins 34 to 36	–1	–0.3		V
Output low level voltage	V_{OL} (5)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OL} = 150 µA			$V_{SS}2$ + 0.3	$V_{SS}2$ + 1	V
Output high level voltage	V_{OH} (6)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –10 µA	Segment Pads 38 to 41 and 44 to 61, QIP64 pins 11 to 23 and 25 to 33	–1	–0.3		V
Output low level voltage	V_{OL} (6)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OL} = 60 µA			$V_{SS}2$ + 0.3	$V_{SS}2$ + 1	V
• When used as p-channel open-drain output ports							
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –15 µA	Segment Pads 62 to 64, QIP64 pins 34 to 36	–1	–0.3		V
Output off leakage current	I_{OFF}	$V_{SS}2$ = –3.5 to –5.25 V, V_{OL} = $V_{SS}2$				1	µA
• Static drive							
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –0.4 µA	All segments	–0.2			V
Output low level voltage	V_{OL} (5)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OL} = 0.4 µA				$V_{SS}2$ + 0.2	V
Output high level voltage	V_{OH} (7)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –4 µA	COM1	–0.2			V
Output low level voltage	V_{OL} (7)	$V_{SS}2$ = – 3.5 to –5.25 V, I_{OL} = 4 µA				$V_{SS}2$ + 0.2	V
• Duplex drive (1/2 bias—1/2 duty)							
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –0.4 µA	All segments	–0.2			V
Output low level voltage	V_{OL} (5)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OL} = 0.4 µA				$V_{SS}2$ + 0.2	V
Output high level voltage	V_{OH} (7)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –4 µA	COM1, 2	–0.2			V
Output middle level voltage	$V_{OM}2$-1	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –4 µA, I_{OL} = 4 µA		$V_{SS}2/2$ – 0.2		$V_{SS}2/2$ +0.2	V
Output low level voltage	V_{OL} (7)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OL} = 4 µA				$V_{SS}2$ +0.2	V
• 1/2 bias—1/3 duty and 1/2 bias—1/4 duty methods							
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –0.4 µA	All segments	–0.2			V
Output low level voltage	V_{OL} (5)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OL} = 0.4 µA				$V_{SS}2$ + 0.2	V
Output high level voltage	V_{OH} (7)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –4 µA	COM1 to 3 (for 1/3 duty methods) COM1 to 4 (for 1/4 duty methods)	–0.2			V
Output middle level voltage	$V_{OM}2$-1	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –4 µA, I_{OL} = 4 µA		$V_{SS}2/2$ – 0.2		$V_{SS}2/2$ +0.2	V
Output low level voltage	V_{OL} (7)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OL} = 4 µA				$V_{SS}2$ + 0.2	V
• 1/3 bias—1/3 duty and 1/3 bias—1/4 duty methods							
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –0.4 µA	All segments	–0.2			V
Output middle level voltage	$V_{OM}1$-1	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –0.4 µA, I_{OL} = 0.4 µA		$V_{SS}2/2$ – 0.2		$V_{SS}2/2$ +0.2	V
	$V_{OM}1$-2			$V_{SS}2$ – 0.2		$V_{SS}2$ + 0.2	V
Output low level voltage	V_{OL} (5)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OL} = 0.4 µA				$V_{SS}3$ + 0.2	V
Output high level voltage	V_{OH} (7)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –0.4 µA	COM1 to 3 (for 1/3 duty methods) COM1 to 4 (for 1/4 duty methods)	–0.2			V
Output low level voltage	$V_{OM}2$-1	$V_{SS}2$ = –3.5 to –5.25 V, I_{OH} = –4 µA, I_{OL} = 4 µA		$V_{SS}2/2$ – 0.2		$V_{SS}2/2$ +0.2	V
	$V_{OM}2$-2			$V_{SS}2$ – 0.2		$V_{SS}2$ + 0.2	V
Output low level voltage	V_{OL} (7)	$V_{SS}2$ = –3.5 to –5.25 V, I_{OL} = 4 µA				$V_{SS}3$ + 0.2	V

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Parameter	Symbol	Conditions		min	typ	max	Unit
Power supply leakage current	I_{LEK}	$V_{SS}2 = V_{SS}3 = -4.5$ V	Ta = 25°C			10	µA
Input leakage current	I_{IN}	$V_{SS}2 = -2.0$ to $+4.5$ V	$V_{IN} = V_{SS}2$ to V_{DD}	–1		+1	µA
Output voltage	$V_{SS}1$	$V_{SS}2 = -2.9$ V	C1 = C2 = C3 = 0.1 µF, fopg = 32.768 kHz, Ta = 25°C, Figure 7		–1.45	–1.35	V
	$V_{SS}3$	$V_{SS}2 = -2.9$ V			–4.35	–4.1	V
Output voltage	$V_{SS}1$	$V_{SS}2 = -4.5$ V	C1 = C2 = C3 = 0.1 µF, fopg = 32.768 kHz, Ta = 25°C, Figure 7		–2.25	–2.2	V
	$V_{SS}3$	$V_{SS}2 = -4.5$ V			–6.70	–6.6	V
Power supply current	$\lvert I_{DD}1 \rvert$	$V_{SS}2 = -2.9$ V, Ta = 25°C, HALT mode	C1 = C2 = 0.1 µF, Cl = 25 kΩ, fopg = 32.768 kHz, Cg = 20 pF		3.0	6.0	µA
	$\lvert I_{DD}2 \rvert$	$V_{SS}2 = -4.5$ V, Ta = 25°C, HALT mode, Stack: Figure 9, 1/3 bias—1/3 duty: Figure 7, other methods: Figure 4			7	13	µA
Power supply current	$\lvert I_{DD}3 \rvert$	$V_{SS}2 = -4.5$ V, Ta = 25°C, HALT mode Stack: Figure 9, 1/3 bias—1/3 duty: Figure 7, other methods: Figure 4	C1 = C2 = 0.1 µF, Cl = 25 kΩ, fopg = 65.536 kHz, Cg = 10 pF		10	20	µA
Power supply current	$\lvert I_{DD}4 \rvert$	$V_{SS}2 = -4.5$ V, Ta = 25°C, HALT mode	C1 = C2 = 0.1 µF, fopg = 400 kHz, Cg = Cd = 100 pF or 330 pF, Rf = 1 MΩ, Figure 6		90	150	µA
Power supply current	$\lvert I_{DD}5 \rvert$	$V_{SS}2 = -4.5$ V, Ta = 25°C, HALT mode	C1 = C2 = 0.1 µF, fopg = 800 kHz, Cg = Cd = 100 pF, Rf = 1 MΩ, Figure 6		130	200	µA
Oscillator hold voltage	$\lvert V_{HOLD}1 \rvert$	Ta = 25°C, Stack: Figure 9, 1/3 bias—1/3 duty: Figure 7, other methods: Figure 4	C1 = C2 = 0.1 µF, Cl = 25 kΩ, fopg = 32.768 kHz, Cg = 20 pF	2.0		5.5	V
Oscillator hold voltage	$\lvert V_{HOLD}2 \rvert$	Ta = 25°C	C1 = C2 = 0.1 µF, Cl = 25 kΩ, fopg = 65.536 kHz, Cg = 10 pF	2.3		5.5	V
Oscillator start voltage	| VStt1 |	Stack: Figure 10, 1/3 bias—1/3 duty: Figure 7, other methods: Figure 4, Ta = 25°C	C1 = C2 = 0.1 µF, Cl = 25 kΩ, Figure 5, fopg = 32.768 kHz, Cg = 20 pF			2.2	V
Oscillator start voltage	| VStt2 |	Ta = 25°C	C1 = C2 = 0.1 µF, Cl = 25 kΩ, Figure 5, fopg = 65.536 kHz, Cg = 10 pF			2.6	V
Oscillator start time	TStt1	$V_{SS}2 = -2.9$ V, Ta = 25°C, $V_{SS}2 = -4.5$ V, Ta = 25°C	C1 = C2 = 0.1 µF, Cl = 25 kΩ, Figure 5, fopg = 32.768 kHz, Cg = 20 pF			10	S
						10	S
Oscillator start time	TStt2	$V_{SS}2 = -2.9$ V, Ta = 25°C, $V_{SS}2 = -4.5$ V, Ta = 25°C	C1 = C2 = 0.1 µF, Cl = 25 kΩ, Figure 5, fopg = 65.536 kHz, Cg = 10 pF			10	S
						10	S
Oscillator start voltage	| VStt4 |	Ta = 25°C	fopg = 400 kHz, Figure 6, Cg = Cd = 100 pF or 330 pF, Rf = 1 MΩ			4.0	V
Oscillator hold voltage	$\lvert V_{HOLD}4 \rvert$	Ta = 25°C	fopg = 400 kHz, Figure 6, Cg = Cd = 100 pF or 330 pF, Rf = 1 MΩ	3.5		5.5	V
Oscillator start time	TStt4	$V_{SS}2 = -4.5$ V, Ta = 25°C	fopg = 400 kHz, Figure 6, Cg = Cd = 100 pF or 330 pF, Rf = 1 MΩ			30	ms

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Parameter	Symbol	Conditions		min	typ	max	Unit
Oscillator start voltage	| VStt5 |	Ta = 25°C	fopg = 800 kHz, Figure 6, Cg = Cd = 100 pF, Rf = 1 MΩ			4.0	V
Oscillator hold voltage	| $V_{HOLD}5$ |	Ta = 25°C	fopg = 800 kHz, Figure 6, Cg = Cd = 100 pF, Rf = 1 MΩ	3.5		5.5	V
Oscillator start time	TStt5	$V_{SS}2$ = –4.5 V, Ta = 25°C	fopg = 800 kHz, Figure 6, Cg = Cd = 100 pF, Rf = 1 MΩ			30	ms
Oscillator correction capacitance	10P	$V_{SS}2$ = –2.9 V	10P pin (chip products only)		10		pF
	10P	$V_{SS}2$ = –4.5 V	10P pin (chip products only)		10		pF
	20P	$V_{SS}2$ = –2.9 V	OSCOUT pin		20		pF
	20P	$V_{SS}2$ = –4.5 V	OSCOUT pin		20		pF

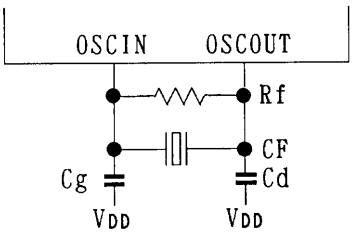

Figure 1 Ceramic Oscillator Specifications

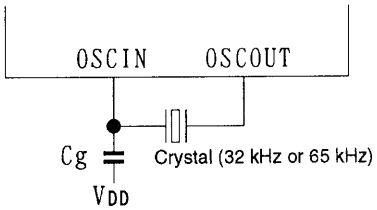

Figure 2 Crystal Oscillator Specifications (32 kHz or 65 kHz)

Recommended Ceramic Oscillators

Manufacturer	Murata				Kyocera			
Item frequency	Type number	Cg (pF)	Cd (pF)	Rf (MΩ)	Type number	Cg (pF)	Cd (pF)	Rf (MΩ)
400 kHz	CSB400P	100	100	1	KBR-400B	330	330	1
800 kHz	CSB800J	100	100	1	KBR-800H	100	100	1

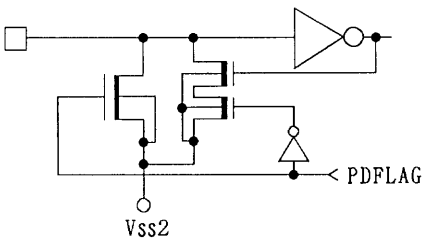

Figure 3 S1 to S4 and M1 to M4 Input Circuits

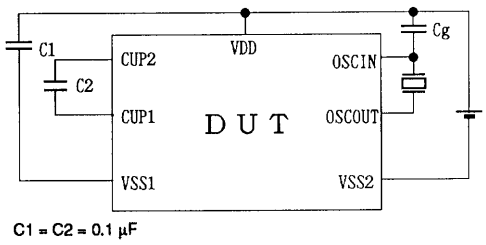

Figure 4 Power Supply Current and Oscillator Hold Voltage Test Circuit

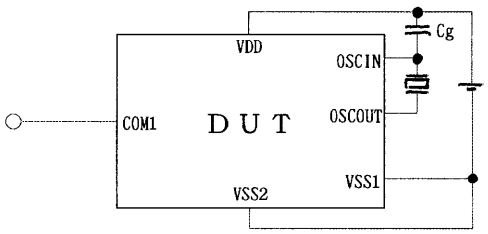

Figure 5 Oscillator Start Voltage, Oscillator Start Time and Frequency Stability Test Circuit

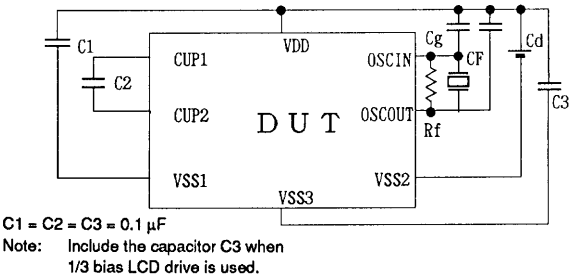

Figure 6 Oscillator Start Voltage, Oscillator Start Time, Power Supply Current and Oscillator Hold Voltage Test Circuit

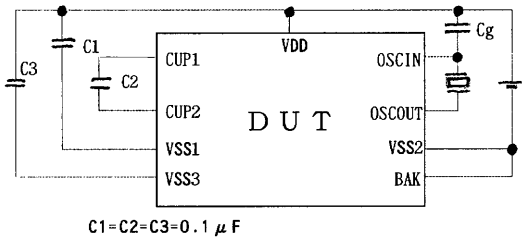

Figure 7 Power Supply Current and Oscillator Hold Voltage Test Circuit

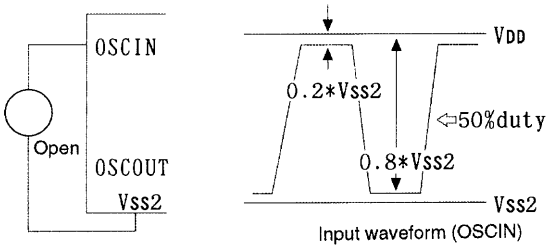

Figure 8 External Input Specifications

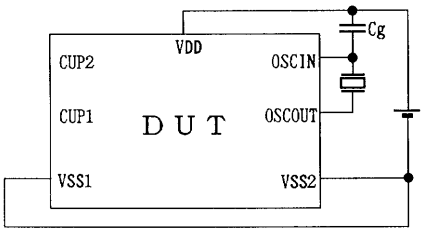

Figure 9 Power Supply Current and Oscillator Hold Time Test Circuit

These electrical specifications are provisional and subject to change.

Ag Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{DD} = 0 V

Parameter	Symbol	Conditions/Pins	min	typ	max	Unit
Maximum supply voltage	$V_{SS}1$		–4.0		+0.3	V
	$V_{SS}2$		–4.0		+0.3	V
	$V_{SS}3$	LCD drive method (1/3 bias)	–5.5		+0.3	V
	$V_{SS}3$	LCD drive method (methods other than 1/3 bias)	–4.0		+0.3	V
Maximum input voltage	$V_{IN}1$	S1 to 4, M1 to 4, I/OA1 to 4, I/OB1 to 4, INT, TESTA (with I/OA1 to 4 and I/OB1 to 4 in input mode), 1OP, OSCIN, RES, BAK	$V_{SS}1$ – 0.3		+0.3	V
Maximum output voltage	$V_{OUT}1$	ALM, LIGHT, P1 to 4, I/OA1 to 4, I/OB1 to 4, CUP2 (with I/OA1 to 4 and I/OB1 to 4 in output mode), TESTA, OSCOUT	$V_{SS}1$ – 0.3		+0.3	V
	$V_{OUT}3$	SEGOUT, COM1 to 4, CUP1	$V_{SS}1$ – 0.3		+0.3	V
Operating temperature	Topr		–20		+65	°C
Storage temperature	Tstg		–30		+125	°C

Allowable Operating Ranges at Ta = 25 ± 2°C, V_{DD} = 0 V

Parameter	Symbol	Conditions/Pins	min	typ	max	Unit
Supply voltage	$V_{SS}1$	$V_{BAK} = V_{SS}1$	–1.65		–1.3	V
	$V_{SS}2$		–3.3		–2.4	V
	$V_{SS}3$	LCD drive method (1/3 bias)	–4.95		–3.7	V
	$V_{SS}3$	LCD drive method (methods other than 1/3 bias)	$V_{SS}3 = V_{SS}2$			
Input high level voltage	V_{IH}	S1 to 4, M1 to 4, I/OA1 to 4, I/OB1 to 4, RES, INT (with I/OA1 to 4 and I/OB1 to 4 in input mode)	–0.2		0	V
Input low level voltage	V_{IL}	S1 to 4, M1 to 4, I/OA1 to 4, I/OB1 to 4, INT (with I/OA1 to 4 and I/OB1 to 4 in input mode)	$V_{SS}1$		$V_{SS}1$ + 0.2	V
Operating frequency	fopg	Ta = –20 to +65°C	32		33	kHz

Electrical Characteristics at Ta = 25 ± 2°C, V_{DD} = 0 V

Parameter	Symbol	Conditions/Pins		min	typ	max	Unit
Input resistance	$R_{IN}1A$	$V_{SS}1$ = –1.55 V, $V_{IL} = V_{SS}1$ + 0.2 V	Low-level hold transistor*, Figure 1	10	50	200	kΩ
	$R_{IN}1B$	$V_{SS}1$ = –1.55 V	Low-level pull-down resistor*, Figure 1	200	550	2000	kΩ
	$R_{IN}2A$	VSS1 = –1.55 V, $V_{IL} = V_{SS}1$	INT pull-up resistor	200	400	2000	kΩ
	$R_{IN}2B$	$V_{SS}1$ = –1.55 V, $V_{IH} = V_{DD}$	INT pull-down resistor	200	550	2000	kΩ
	$R_{IN}3$	$V_{SS}1$ = –1.55 V, $V_{IH} = V_{DD}$	RES pull-down resistor	5		50	kΩ
Output high level voltage	V_{OH} (1)	V_{SS} = –1.35 V, I_{OH} = –250 µA	ALM, LIGHT	–0.65			V
Output low level voltage	V_{OL} (1)	$V_{SS}1$ = –1.35 V, I_{OL} = 250 µA	ALM, LIGHT			$V_{SS}1$ + 0.65	V
Output high level voltage	V_{OH} (2)	V_{SS} = –1.55 V, I/OA1 to 4, I/OB1 to 4, I_{OH} = –20 µA, P1 to 4 (with I/OA1 to 4 and I/OB1 to 4 in output mode)		–0.2			V
Output low level voltage	V_{OL} (2)	$V_{SS}1$ = –1.55 V, I/OA1 to 4, I/OB1 to 4, I_{OL} = 20 µA, P1 to 4 (with I/OA1 to 4 and I/OB1 to 4 in output mode)				$V_{SS}1$ + 0.2	

Note: * S1, S2, S3, S4, M1, M2, M3, M4

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Parameter	Symbol	Conditions/Pins		min	typ	max	Unit
Segment driver output impedances							
• When used as CMOS output ports							
Output high level voltage	V_{OH} (3)	$V_{SS}1$ = –1.55 V, I_{OH} = –3 µA	Segment Pads 38 to 41 and 44 to 61, QIP64 pins 11 to 23 and 25 to 33		–0.3		V
Output low level voltage	V_{OL} (3)	$V_{SS}1$ = –1.55 V, I_{OL} = 3 µA			$V_{SS}2$ + 0.3		V
• When used as p-channel open drain outputs							
Output high level voltage	V_{OH} (3)	$V_{SS}1$ = –1.55 V, I_{OH} = –3 µA	Segment Pads 62 to 64, QIP64 pins 34 to 36	–1	–0.3		V
Output off leakage current	I_{OFF}	$V_{SS}1$ = –1.55 V, V_{OL} = $V_{SS}1$				1	µA
• Static drive							
Output high level voltage	V_{OH} (3)	$V_{SS}1$ = –1.55 V, I_{OH} = –0.4 µA	SEGOUT	–0.2			V
Output low level voltage	V_{OL} (3)	$V_{SS}1$ = –1.55 V, I_{OL} = 0.4 µA				$V_{SS}2$ + 0.2	V
Output high level voltage	V_{OH} (4)	$V_{SS}1$ = –1.55 V, I_{OH} = –4 µA	COM1	–0.2			V
Output low level voltage	V_{OL} (4)	$V_{SS}1$ = –1.55 V, I_{OL} = 4 µA				$V_{SS}2$ + 0.2	V
• Duplex drive (1/2 bias—1/2 duty)							
Output high level voltage	V_{OH} (3)	$V_{SS}1$ = –1.55 V, I_{OH} = –0.4 µA	SEGOUT	–0.2			V
Output low level voltage	V_{OL} (3)	$V_{SS}1$ = –1.55 V, I_{OL} = 0.4 µA				$V_{SS}2$ + 0.2	V
Output high level voltage	V_{OH} (4)	$V_{SS}1$ = –1.55 V, I_{OH} = –4 µA	COM1, 2	–0.2			V
Output middle level voltage	V_{OM}	$V_{SS}1$ = –1.55 V, I_{OH} = –4 µA, I_{OL} = 4 µA		$V_{SS}1$ – 0.2		$V_{SS}1$ + 0.2	V
Output low level voltage	V_{OL} (4)	$V_{SS}2$ = –1.55 V, I_{OL} = 4 µA				$V_{SS}2$ + 0.2	V
• 1/2 bias—1/3 duty and 1/2 bias—1/4 duty methods							
Output high level voltage	V_{OH} (3)	$V_{SS}1$ = –1.55 V, I_{OH} = –0.4 µA	SEGOUT	–0.2			V
Output low level voltage	V_{OL} (3)	$V_{SS}1$ = –1.55 V, I_{OL} = 0.4 µA				$V_{SS}2$ + 0.2	V
Output high level voltage	V_{OH} (4)	$V_{SS}1$ = –1.55 V, I_{OH} = –4 µA	COM1 to 3 (for 1/3 duty methods) COM 1 to 4 (for 1/4 duty methods)	–0.2			
Output middle level voltage	V_{OM}	$V_{SS}1$ = –1.55 V, I_{OH} = –4 µA, I_{OL} = 4 µA		$V_{SS}1$ – 0.2		$V_{SS}1$ + 0.2	V
Output low level voltage	V_{OL} (4)	$V_{SS}2$ = –1.55 V, I_{OL} = 4 µA				$V_{SS}2$ + 0.2	V
• 1/3 bias—1/3 duty and 1/3 bias—1/4 duty methods							
Output high level voltage	V_{OH} (3)	$V_{SS}1$ = –1.55 V, I_{OH} = –0.4 µA	SEGOUT	–0.2			V
Output M1 level voltage	$V_{OM}1$-3	$V_{SS}1$ = –1.55 V, I_{OH} = –0.4 µA, I_{OL} = 0.4 µA		$V_{SS}1$ – 0.2		$V_{SS}1$ + 0.2	V
Output M2 level voltage	$V_{OM}2$-3	$V_{SS}1$ = –1.55 V, I_{OH} = –0.4 µA, I_{OL} = 0.4 µA		$V_{SS}2$ – 0.2		$V_{SS}2$ + 0.2	V
Output low level voltage	V_{OL} (3)	$V_{SS}1$ = –1.55 V, I_{OL} = 0.4 µA				$V_{SS}3$ + 0.2	V
Output high level voltage	V_{OH} (4)	$V_{SS}1$ = –1.55 V, I_{OH} = –4 µA	COM1 to 3 (for 1/3 duty methods) COM 1 to 4 (for 1/4 duty methods)	–0.2			
Output M1 level voltage	$V_{OM}1$-4	$V_{SS}1$ = –1.55 V, I_{OH} = –4 µA, I_{OL} = 4 µA		$V_{SS}1$ – 0.2		$V_{SS}1$ + 0.2	V
Output M2 level voltage	$V_{OM}2$-4	$V_{SS}1$ = –1.55 V, I_{OH} = –4 µA, I_{OL} = 4 µA		$V_{SS}2$ – 0.2		$V_{SS}2$ + 0.2	V
Output low level voltage	V_{OL} (4)	$V_{SS}2$ = –1.55 V, I_{OL} = 4 µA				$V_{SS}3$ + 0.2	V

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Parameter	Symbol	Conditions/Pins		min	typ	max	Unit
• Output voltage							
LCD drive: 1/3 bias methods (doubler)	$V_{SS}2$	$V_{SS}1$ = –1.35 V, C1 to 4 = 0.1 µF	fopg = 32.768 kHz, Figure 7			–2.5	V
(tripler)	$V_{SS}3$	$V_{SS}1$ = –1.35 V, C1 to 4 = 0.1 µF	fopg = 32.768 kHz, Figure 7			–3.75	V
LCD drive: 1/2 bias methods (doubler)	$V_{SS}2$	$V_{SS}1$ = –1.35 V, C1 = C2 = 0.1 µF	fopg = 32.768 kHz, Figure 2			–2.5	V
• Supply current (when the backup flag is cleared to zero)							
LCD drive: 1/3 bias methods	$\lvert I_{DD} \rvert$	$V_{SS}1$ = –1.55 V, C1 to 4 = 0.1 µF Cd = Cg = 20 pF	In HALT mode, Cl = 25 kΩ, Figure 7, 32.768 kHz, X'tal		1.3	4.5	µA
LCD drive: methods other than 1/3 bias	$\lvert I_{DD} \rvert$	$V_{SS}1$ = –1.55 V, C1 = C2 = 0.1 µF Cd = Cg = 20 pF	In HALT mode, Cl = 25 kΩ, Figure 2, 32.768 kHz, X'tal		1.1	4.5	µA
Oscillator start voltage $V_{SS}1$	| Vstt |	Cd = Cg = 20 pF	Cl = 25 kΩ, Figure 3, 32.768 kHz, X'tal			1.35	V
Oscillator hold voltage $V_{SS}1$	$\lvert V_{HOLD} \rvert$	Cd = Cg = 20 pF	Cl = 25 kΩ, Figure 2, 32.768 kHz, X'tal	1.3		1.6	V
Oscillator start time	Tstt	$V_{SS}1$ = –1.35 V, Cd = Cg = 20 pF	Cl = 25 kΩ, Figure 3, 32.768 kHz, X'tal			10	s
Oscillator correction capacitance	10P	External connection (for chip products)		8	10	12	pF
	20P	OSCOUT		16	20	24	pF

These electrical specifications are provisional and subject to change.

Li Specifications

Absolute Maximum Ratings at Ta = 25 ± 2°C, V_{DD} = 0 V

Parameter	Symbol	Conditions/Pins	min	typ	max	Unit
Maximum supply voltage	$V_{SS}1$	V_{BAK} = $V_{SS}1$ or $V_{SS}2$	–4.0		+0.3	V
	$V_{SS}2$		–4.0		+0.3	V
	$V_{SS}3$	LCD drive: 1/3 bias methods	–5.5		+0.3	V
	$V_{SS}3$	LCD drive: methods other than 1/3 bias	–4.0		+0.3	V
Maximum input voltage	$V_{IN}1$	10P, OSCIN	V_{BAK} – 0.3		+0.3	V
	$V_{IN}2$	S1 to 4, M1 to 4, I/IA1 to 4, I/OB1 to 4, RES, INT, TESTA, (with I/OA1 to 4 and I/OB1 to 4 in input mode)	$V_{SS}2$ – 0.3		+0.3	V
Maximum output voltage	$V_{OUT}1$	TEST, OSCOUT	V_{BAK} – 0.3		+0.3	V
	$V_{OUT}2$	ALM, LIGHT, P1 to 4, I/OA1 to 4, I/OB1 to 4, CUP2 (with I/OA1 to 4 and I/OB1 to 4 in output mode)	$V_{SS}2$ – 0.3		+0.3	V
	$V_{OUT}3$	SEGOUT, COM1 to 4, CUP1	$V_{SS}3$ – 0.3		+0.3	V
Operating temperature	Topr		–20		+65	°C
Storage temperature	Tstg		–30		+125	°C

Allowable Operating Ranges at Ta = 25 ± 2°C, V_{DD} = 0 V

Parameter	Symbol	Conditions/Pins	min	typ	max	Unit
Supply voltage	V_{BAK}		–3.6		–1.3	V
	$V_{SS}2$	V_{BAK} = $V_{SS}2$/2 (with the backup flag cleared to zero)	–3.6		–2.6	V
	$V_{SS}2$	V_{BAK} = $V_{SS}2$ (with the backup flag cleared to zero)	–3.6		–1.3	V
	$V_{SS}3$	LCD drive: 1/3 bias methods	–4.95		–3.7	
	$V_{SS}3$	LCD drive: methods other than 1/3 bias	$V_{SS}3$ = $V_{SS}2$			
Input high level voltage	V_{IH}	S1 to 4, M1 to 4, I/OA1 to 4, I/OB1 to 4, INT (with I/OA1 to 4 and I/OB1 to 4 in input mode)	–0.4		0	V
Input low level voltage	V_{IL}	S1 to 4, M1 to 4, I/OA1 to 4, I/OB1 to 4, INT (with I/OA1 to 4 and I/OB1 to 4 in input mode)	$V_{SS}2$		$V_{SS}2$ + 0.4	V
Operating frequency	fopg	Ta = –20 to +65°C	32		33	kHz

Electrical Characteristics at Ta = 25 ± 2°C, V_{DD} = 0 V

Parameter	Symbol	Conditions/Pins		min	typ	max	Unit
Input resistance	$R_{IN}1A$	$V_{SS}2$ = –2.9 V, V_{IL} = $V_{SS}2$ + 0.4 V	Low-level hold transistor*, Figure 1	10		200	kΩ
	$R_{IN}1B$	$V_{SS}2$ = –2.9 V,	Pull-down resistor*, Figure 4	200		2000	kΩ
	$R_{IN}2A$	$V_{SS}2$ = –2.9 V, V_{IL} = $V_{SS}2$	INT pull-up resistor	200		2000	kΩ
	$R_{IN}2B$	$V_{SS}2$ = –2.9 V, V_{IH} = V_{DD}	INT pull-down resistor	200		2000	kΩ
	$R_{IN}3$	$V_{SS}2$ = –2.9 V, V_{IH} = V_{DD}	RES pull-down resistor	5		50	kΩ

Note: * S1, S2, S3, S4, M1, M2, M3, M4

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Parameter	Symbol	Conditions/Pins		min	typ	max	Unit
Output high level voltage	V_{OH} (1)	$V_{SS}2$ = –2.4 V, I_{OH} = –250 µA	ALM	–0.65			V
Output low level voltage	V_{OL} (1)	$V_{SS}2$ = –2.4 V, I_{OH} = 250 µA	ALM			$V_{SS}2$ + 0.65	V
Output high level voltage	V_{OH} (2)	$V_{SS}2$ = –2.9 V, I/OA1 to 4, I/OB1 to 4, I_{OH} = –40 µA, P1 to 4 (with I/OA1 to 4 and I/OB1 to 4 in output mode)		–0.4			V
Output low level voltage	V_{OL} (2)	$V_{SS}2$ = –2.9 V, I/OA1 to 4, I/OB1 to 4, I_{OL} = 40 µA, P1 to 4 (with I/OA1 to 4 and I/OB1 to 4 in output mode)				$V_{SS}2$ + 0.4	V
Output high level voltage	V_{OH} (3)	$V_{SS}2$ = –2.9 V, I_{OH} = –150 µA	LIGHT	–1.5			V
Output low level voltage	V_{OL} (3)	$V_{SS}2$ = –2.9 V, I_{OL} = 150 µA	LIGHT			$V_{SS}2$ + 1.5	V
Segment driver output impedances							
• When used as CMOS output ports							
Output high level voltage	V_{OH} (4)	$V_{SS}2$ = –2.9 V, I_{OH} = –5 µA	Segment Pads 38 to 41 and 44 to 61, QIP64 pins 11 to 23 and 25 to 33		–0.3		V
Output low level voltage	V_{OL} (4)	$V_{SS}2$ = –2.9 V, I_{OL} = 5 µA			$V_{SS}2$ + 0.3		V
• When used as p-channel open-drain output ports							
Output high level voltage	V_{OH} (4)	$V_{SS}2$ = –2.4 V, I_{OH} = –10 µA	Segment Pads 62 to 64, QIP64 pins 34 to 36	–1	–0.3		V
Output off leakage current	I_{OFF}	$V_{SS}2$ = –2.9 V, V_{OL} = $V_{SS}2$				1	µA
• Static drive							
Output high level voltage	V_{OH} (4)	$V_{SS}2$ = –2.9 V, I_{OH} = –0.4 µA	All SEGOUT pins	–0.2			V
Output low level voltage	V_{OL} (4)	$V_{SS}2$ = –2.9 V, I_{OL} = 0.4 µA				$V_{SS}2$ + 0.2	V
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –2.9 V, I_{OH} = –4 µA	COM1	–0.2			V
Output low level voltage	V_{OL} (5)	$V_{SS}2$ = –2.9 V, I_{OL} = 4 µA				$V_{SS}2$ + 0.2	V
• Duplex drive (1/2 bias—1/2 duty)							
Output high level voltage	V_{OH} (4)	$V_{SS}2$ = –2.9 V, I_{OH} = –0.4 µA	All SEGOUT pins	–0.2			V
Output low level voltage	V_{OL} (4)	$V_{SS}2$ = –2.9 V, I_{OL} = 0.4 µA				$V_{SS}2$ + 0.2	V
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –2.9 V, I_{OH} = –4 µA	COM1 to 4	–0.2			V
Output middle level voltage	V_{OM}	$V_{SS}2$ = –2.9 V, I_{OH} = –4 µA, I_{OL} = 4 µA		$V_{SS}2/2$ – 0.2		$V_{SS}2/2$ +0.2	V
Output low level voltage	V_{OL} (5)	$V_{SS}2$ = –2.9 V, I_{OL} = 4 µA				$V_{SS}2$ + 0.2	V
• 1/2 bias—1/3 duty and 1/2 bias—1/4 duty methods							
Output high level voltage	V_{OH} (4)	$V_{SS}2$ = –2.9 V, I_{OH} = –0.4 µA	All SEGOUT pins	–0.2			V
Output low level voltage	V_{OL} (4)	$V_{SS}2$ = –2.9 V, I_{OL} = 0.4 µA				$V_{SS}2$ + 0.2	V
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –2.9 V, I_{OH} = –4 µA	COM1 to 3 (for 1/3 duty methods) COM1 to 4 (for 1/4 duty methods)	–0.2			V
Output middle level voltage	V_{OM}	$V_{SS}2$ = –2.9 V, I_{OH} = –4 µA, I_{OL} = 4 µA		$V_{SS}2/2$ – 0.2		$V_{SS}2/2$ +0.2	V
Output low level voltage	V_{OL} (5)	$V_{SS}2$ = –2.9 V, I_{OL} = 4 µA				$V_{SS}2$ + 0.2	V

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Parameter	Symbol	Conditions/Pins		min	typ	max	Unit
• 1/3 bias—1/3 duty and 1/3 bias—1/4 duty methods							
Output high level voltage	V_{OH} (4)	$V_{SS}2$ = –2.9 V, I_{OH} = –0.4 µA	All SEGOUT pins	–0.2			V
Output M1 level voltage	$V_{OM}1$-4	$V_{SS}2$ = –2.9 V, I_{OH} = –0.4 µA, I_{OL} = 0.4 µA		$V_{SS}2/2$ – 0.2		$V_{SS}2/2$ +0.2	V
Output M2 level voltage	$V_{OM}2$-4	$V_{SS}2$ = –2.9 V, I_{OH} = –0.4 µA, I_{OL} = 0.4 µA		$V_{SS}2$ – 0.2		$V_{SS}2$ + 0.2	V
Output low level voltage	V_{OL} (4)	$V_{SS}2$ = –2.9 V, I_{OL} = 0.4 µA				$V_{SS}3$ + 0.2	V
Output high level voltage	V_{OH} (5)	$V_{SS}2$ = –2.9 V, I_{OH} = –4 µA	COM1 to 3 (for 1/3 duty methods) COM1 to 4 (for 1/4 duty methods)	–0.2			V
Output M1 level voltage	$V_{OM}1$-5	$V_{SS}2$ = –2.9 V, I_{OH} = –4 µA, I_{OL} = 4 µA		$V_{SS}2/2$ – 0.2		$V_{SS}2/2$ +0.2	V
Output M2 level voltage	$V_{OM}2$-5	$V_{SS}2$ = –2.9 V, I_{OH} = –4 µA, I_{OL} = 4 µA		$V_{SS}2$ – 0.2		$V_{SS}2$ + 0.2	V
Output low level voltage	V_{OL} (5)	$V_{SS}2$ = –2.9 V, I_{OL} = 4 µA				$V_{SS}3$ + 0.2	V
• Output voltage							
LCD drive: 1/3 bias methods (halver)	$V_{SS}1$	$V_{SS}2$ = –2.9 V, C1 to 3 = 0.1 µF	fopg = 32.768 kHz, Figure 7			–1.35	V
(tripler)	$V_{SS}3$	$V_{SS}2$ = –2.9 V, C1 to 3 = 0.1 µF	fopg = 32.768 kHz, Figure 7			–4.1	V
LCD drive: 1/2 bias methods (halver)	$V_{SS}1$	$V_{SS}2$ = –2.9 V, C1 = C2 = 0.1 µF	fopg = 32.768 kHz, Figure 4			–1.35	V
• Supply current (when the backup flag is cleared to zero)							
LCD drive: 1/3 bias methods	$\lvert I_{DD} \rvert$	$V_{SS}2$ = –2.9 V, C1 to 3 = 0.1 µF, Cd = Cg = 20 pF	In HALT mode, Cl = 25 kΩ, Figure 7, 32.768 kHz Xtal		0.8	3.0	µA
LCD drive: methods other than 1/3 bias	$\lvert I_{DD} \rvert$	$V_{SS}2$ = –2.9 V, C1 = C2 = 0.1 µF, Cd = Cg = 20 pF	In HALT mode, Cl = 25kΩ, Figure 4, 32.768 kHz Xtal		0.7	3.0	µA
Oscillator start voltage $V_{SS}2$	$\lvert$ Vstt $\rvert$	V_{BAK} = $V_{SS}2$, Cd = Cg = 20 pF	Cl = 25 kΩ, Figure 5, 32.768 kHz Xtal			1.35	V
Oscillator hold voltage $V_{SS}2$ (when the backup flag is cleared to zero)	$\lvert V_{HOLD}$ (1) $\rvert$	V_{BAK} = $V_{SS}2/2$, Cd = Cg = 20 pF	Cl = 25kΩ, Figure 4, 32.768 kHz Xtal	2.6		3.6	V
(when the backup flag is cleared to zero)	$\lvert V_{HOLD}$ (2) $\rvert$	V_{BAK} = $V_{SS}2$, Cd = Cg = 20 pF	Cl = 25kΩ, Figure 4, 32.768 kHz Xtal	1.3		3.6	V
Oscillator start time	Tstt	V_{BAK} = $V_{SS}2$ = –2.9 V, Cd = Cg = 20 pF	Cl = 25kΩ, Figure 5, 32.768 kHz Xtal			10	s
Oscillator correction capacitance	10P	External connection		8	10	12	pF
	20P	OSCOUT		16	20	24	pF

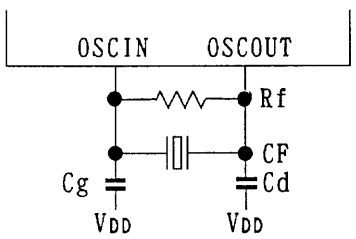

Figure 1 Ceramic Oscillator Specifications

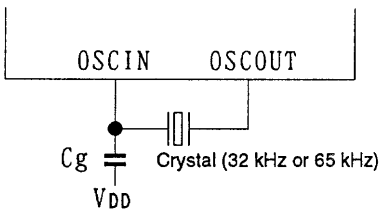

Figure 2 Crystal Oscillator Specifications (32 kHz or 65 kHz)

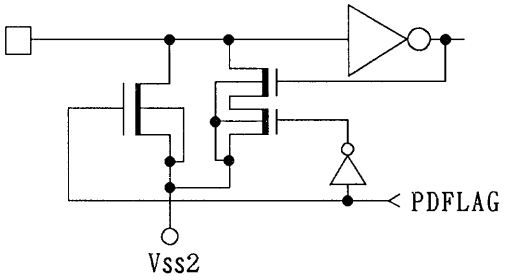

Figure 3 S1 to S4 and M1 to M4 Input Circuits

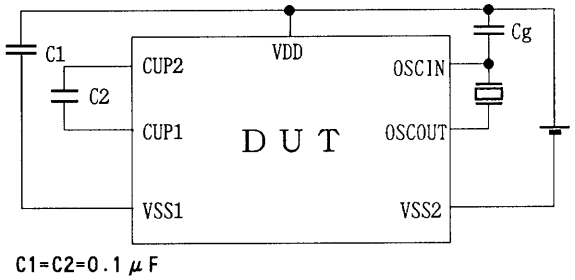

Figure 4 Power Supply Current and Oscillator Hold Voltage Test Circuit

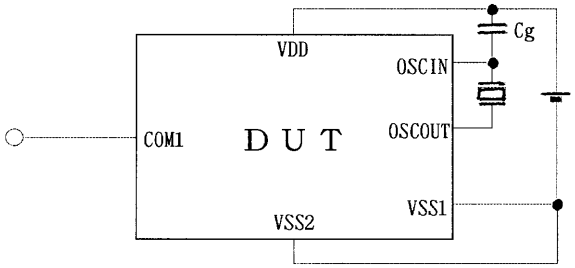

Figure 5 Oscillator Start Voltage, Oscillator Start Time and Frequency Stability Test Circuit

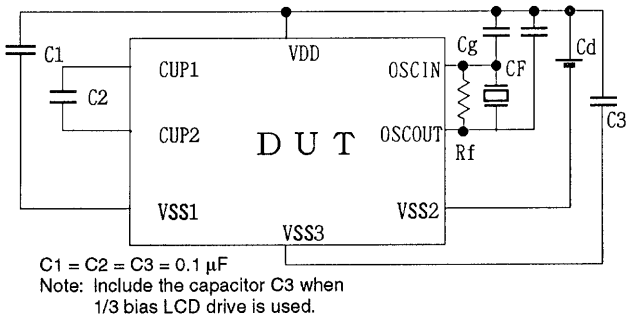

Figure 6 Oscillator Start Voltage, Oscillator Start Time, Power Supply Current and Oscillator Hold Voltage Test Circuit

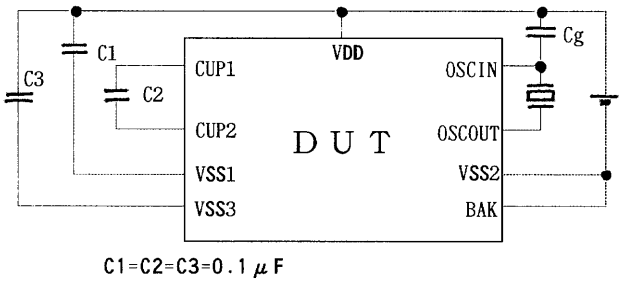

Figure 7 Power Supply Current and Oscillator Hold Voltage Test Circuit

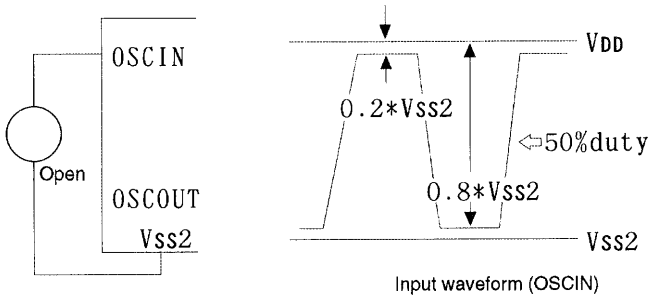

Figure 8 External Input Specifications

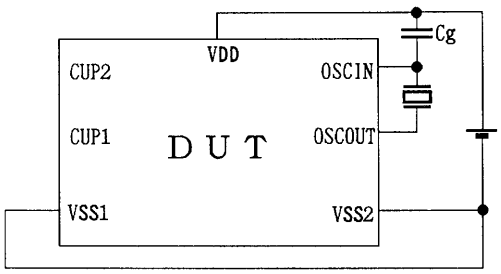

Figure 9 Power Supply Current and Oscillator Hold Time Test Circuit