FEATURES

- Integrates two full-featured CEPT E1 performance monitors in a single device.
- Provides analog circuitry for receiving CCITT G.703 or ANSI DSX-1A signals.
- Recovers clock and data from AMI or HDB3 encoded signals and indicates low level signal, pulse density violation and loss of signal.
- Clock and data recovery may be disabled, allowing unipolar (clock and data) streams to be directly monitored.
- Frames to a CEPT E1 signal within 1 ms. Frames to the channel associated signalling (CAS) multiframe alignment when enabled. Frames to the CRC multiframe alignment when enabled.
- Compatible with CCITT G.704 and G.706 specifications and G.732 alarm recommendations for a 2048 kbit/s interface. Compatible with ANSI T1.102 specifications for a DSX-1A interface.
- Indicates the reception of Remote Alarm and Remote Signalling Multiframe Alarm as per Recommendation O.162.
- Integrates and declares RED Alarm when an out of frame condition has persisted for at least 100 ms, as per Recommendation Q.516.
- Integrates and declares received AIS Alarm when an unframed all-ones signal has been received for at least 100 ms, as per Recommendation Q.516. The algorithm operates up to a 10^{-3} bit error rate.
- Detects violation of the ANSI T1.403 12.5% pulse density violation rule for AMI applications.
- Counts up to 1000 CRC-4 errors, 127 frame synchronization bit errors, 8191 line code violations, and 1000 far end block errors per second.
- Optionally extracts National bit 4 (or any combination of the National bits) or timeslot 16 and outputs it as a data link, along with a data link clock.
- Detects bit-oriented codes in the extracted data link and provides an HDLC interface for CCITT Q.921 LAPD message reception on the extracted data link.
- Synchronizes to framed or unframed 2^{15}-1 test sequences as defined in Recommendation O.151 and accumulates bit errors detected using this pseudo-random pattern.

- Provides a generic 8-bit microprocessor bus interface for configuration, control and status monitoring.
- Customizable design based on PMC's Telecom System Block megacells. Pin for pin compatible with the PM4322 DXPM Dual DSX-1 Performance Monitor which performs the analogous function for T1 systems.
- Low power CMOS technology.
- 68-pin PLCC package.

APPLICATIONS

- Continuous performance monitors for CEPT E1 Network Management Systems.
- Hand-held CEPT E1 testers and continuous performance monitors in CEPT E1 test equipment.
- CSUs with integrated performance monitors.
- Multiplexers with integrated performance monitors.
- DACS with integrated performance monitors.

REFERENCES

- CCITT Blue Book, Recommendation G.703 - "Physical/Electrical Characteristics of Hierarchical Digital Networks", Vol. III, Fascicle III.4, 1988.
- CCITT Blue Book, Recommendation G.704 - "Functional Characteristics of Interfaces Associated with Network Nodes", Vol. III, Fascicle III.4, 1988.
- CCITT Blue Book, Recommendation G.704, - "Synchronous Frame Structures Used at Primary and Secondary Hierarchical Levels", Vol. III, Fascicle III.4 , 1988.
- CCITT Blue Book, Recommendation G.706, - "Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704", Vol. III, Fascicle III.4, 1988.
- CCITT Blue Book, Recommendation G.732, - "Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s", Vol. III, Fascicle III.4, 1988.
- CCITT Blue Book, Recommendation G.735, - "Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s and Offering Digital Access at 384 kbit/s and/or Synchronous Digital Access at 64 kbit/s", Vol. III, Fascicle III.4, 1988.
- CCITT Blue Book, Recommendation O.151, - "Specifications for digital-type measurement equipment", Vol. IV, Fascicle IV.4, 1988.
- CCITT Blue Book, Recommendation O.162, - "Specification for an Instrument to Monitor the Frame Alignment Signal of Frame Structures (Frame Alignment Signal Monitor)", Vol. IV, Fascicle IV.4, 1988.
- CCITT Blue Book, Recommendation Q.506, - "Operations and maintenance functions", Vol. VI, Fascicle VI.5, 1988.
- CCITT Blue Book, Recommendation Q.516, - "Operations and maintenance functions", Vol. VI, Fascicle VI.5, 1988.
- CCITT Blue Book, Recommendation G.821 - "Error Performance of an International Digital Connection Forming Part of an Integrated Services Digital Network", Volume III, Fascicle III.5, 1988.
- CCITT Blue Book, Recommendation Q.921. - "ISDN User-Network Interface Data Link Layer Specification", Volume VI, Fascicle VI.10, 1988..
- American National Standard for Telecommunications, T1X1.4/90-004R3 - "Editorial Report and Update of Baseline Document for Revision of ANSI T1.102-1987".

DESCRIPTION

The PM6322 E1PM Dual CEPT E1 Performance Monitor provides the functions necessary to monitor the transmission characteristics of most CEPT E1 connections. It also provides analog circuitry for receiving each E1 signal with the addition of an external transformer and passive components. Direct input of a unipolar E1 signal and recovered clock is also supported. The E1PM recovers clock and data with excellent jitter tolerance and can be configured to frame to a basic E1 signal as well as the CRC multiframe and the CAS multiframe.

The E1PM supports detection of various alarm conditions such as loss of signal (LOS), pulse density violation, red alarm, remote alarm, alarm indication signal (AIS), remote multiframe alarm, and timeslot 16 AIS alarm. Line and path performance monitoring are supported through counters that allow accumulation of line code violations (LCV), framing bit errors, CRC-4 errors, and far end block errors (FEBE). These counters are intended to be polled once per second and are sized so as not to saturate at a 10^{-3} bit error rate. As an aid in identifying improperly configured equipment, the E1PM also detects conditions such as four successive zeros, and HDB3 signatures.

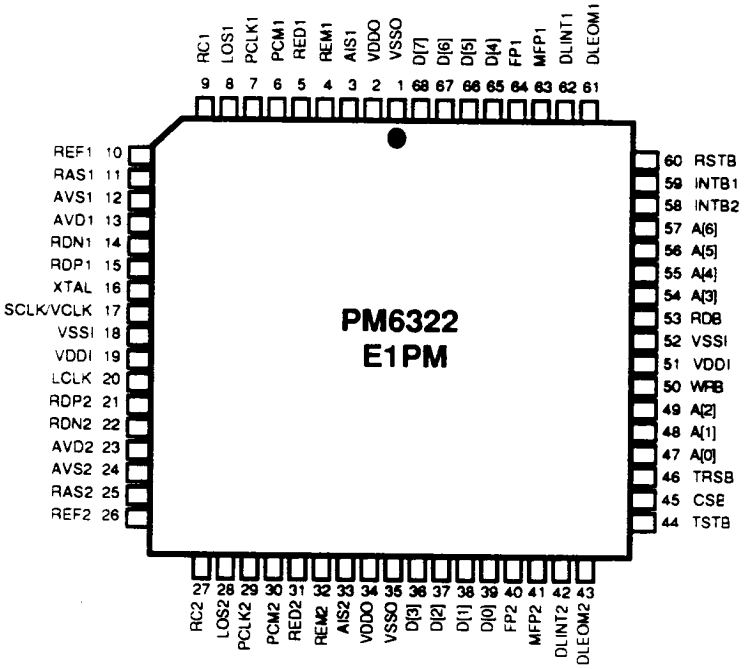
The E1PM synchronizes to framed or unframed 2^{15}-1 test sequences and accumulates bit errors detected using this pseudo-random pattern.

Termination of the national bit 4 (or any combination of the national bits) or timeslot 16 data link is supported through an integral HDLC receiver and a bit oriented code detector. The HDLC receiver supports polled, interrupt-driven and DMA servicing.

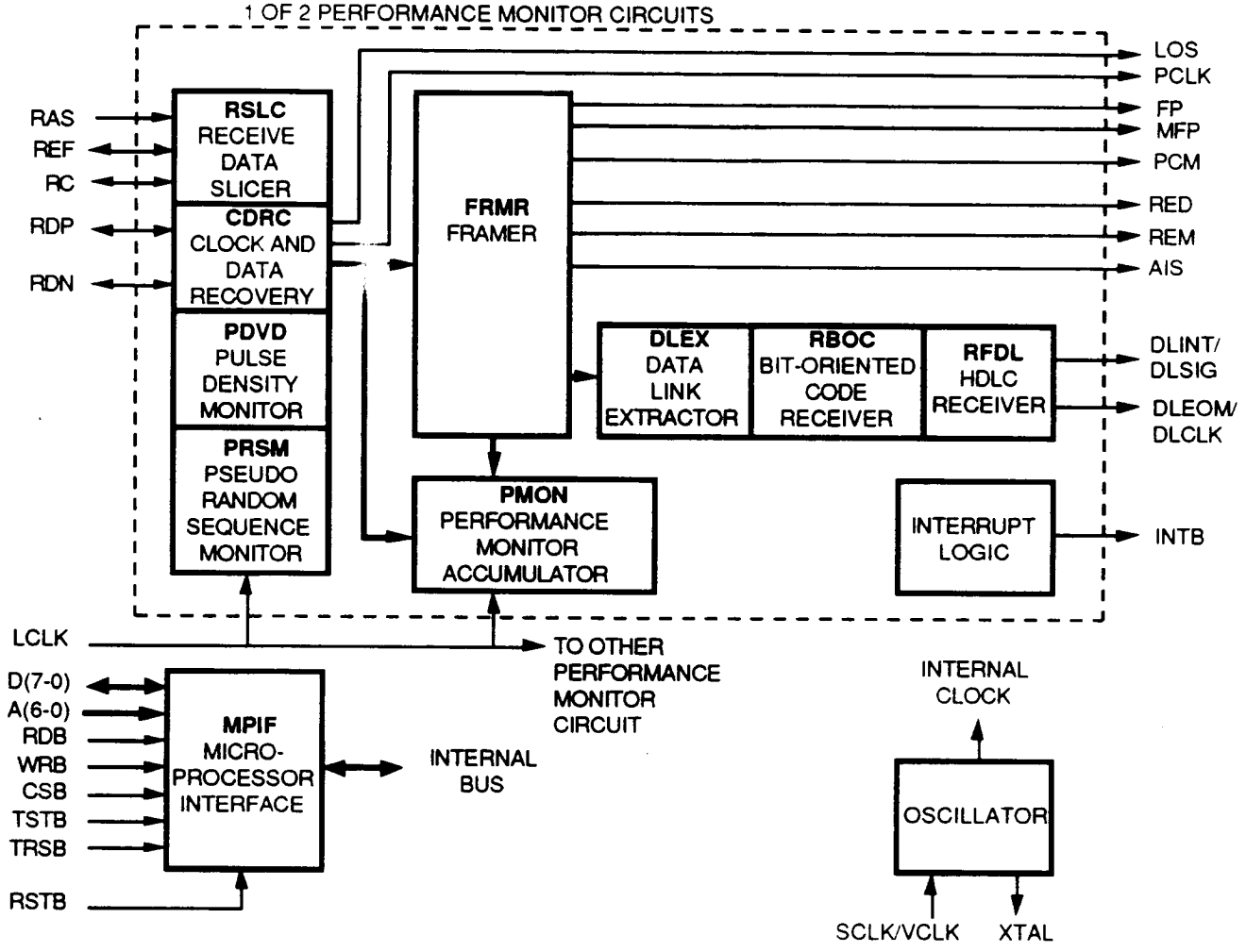
Timing for the E1PM may be provided by an on-chip 16.384 MHz crystal oscillator, or an external clock source.

The E1PM is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. The E1PM is pin compatible with the PM4322 DXPM Dual DSX-1 Performance Monitor which performs a similar function for T1 systems.

PIN DIAGRAM



BLOCK DIAGRAM



CONNECTOR DESCRIPTION

Connector Name	Type	Pin No.	Function
SCLK/ VCLK	Input	17	The system clock (SCLK) provides timing for E1PM clock recovery. SCLK is nominally a 16.384 MHz, 50% duty cycle clock. SCLK may be driven externally or connected to a 16.384 MHz crystal. When clock recovery is disabled, SCLK should be connected to VSS. The test vector clock (VCLK) signal is used during E1PM production test to verify internal functionality.
XTAL	Output	16	The crystal output (XTAL) may be connected to a 16.384 MHz crystal in conjunction with SCLK to form a crystal oscillator. When not used, XTAL should be left unconnected.
RDP1	I/O	15	The receive digital positive pulse 1 (RDP1) signal represents positive pulses. When PM-1 is not using the receive data slicer, RDP1 is the input pin for receiving positive line pulses. When PM-1 is using the receive data slicer, RDP1 outputs the positive pulses extracted from the analog CEPT E1 signal. When clock recovery is disabled, RDP1 is the input pin for the PM-1 unipolar E1 data stream, and is sampled by the rising edge of the E1 clock, RDN1.
RDP2	I/O	21	The receive digital positive pulse 2 (RDP2) signal represents positive pulses. When PM-2 is not using the receive data slicer, RDP2 is the input pin for receiving positive line pulses. When PM-2 is using the receive data slicer, RDP2 outputs the positive pulses extracted from the analog CEPT E1 signal. When clock recovery is disabled, RDP2 is the input pin for the PM-2 unipolar E1 data stream, and is sampled by the rising edge of the E1 clock, RDN2.

RDN1	I/O	14	The receive digital negative pulse 1 (RDN1) signal represents negative pulses. When PM-1 is not using the receive data slicer, RDN1 is the input pin for receiving negative line pulses. When PM-1 is using the receive data slicer, RDN1 outputs the negative pulses extracted from the analog CEPT E1 signal. When clock recovery is disabled, RDN1 is the input pin for the PM-1 unipolar E1 stream clock (nominally 2.048 MHz, 50% duty cycle), and samples the E1 data stream (RDP1) on the rising edge.
RDN2	I/O	22	The receive digital negative pulse 2 (RDN2) signal represents negative pulses. When PM-2 is not using the receive data slicer, RDN2 is the input pin for receiving negative line pulses. When PM-2 is using the receive data slicer, RDN2 outputs the negative pulses extracted from the analog CEPT E1 signal. When clock recovery is disabled, RDN2 is the input pin for the PM-2 unipolar E1 stream clock (nominally 2.048 MHz, 50% duty cycle), and samples the E1 data stream (RDP2) on the rising edge.
RAS1	Input	11	The receive analog signal 1 (RAS1) input connects the line coupling transformer to the receive data slicer used by PM-1. This input may be left unconnected when the receive data slicer used by PM-1 is disabled.
RAS2	Input	25	The receive analog signal 2 (RAS2) input connects the line coupling transformer to the receive data slicer used by PM-2. This input may be left unconnected when the receive data slicer used by PM-2 is disabled.
REF1	I/O	10	The reference 1 (REF1) signal provides a bias voltage for the line coupling transformer associated with PM-1. During normal operation REF1 must be decoupled to ground with a 0.1 µF capacitor. This I/O connection should be left unconnected when the receive data slicer used by PM-1 is disabled.
REF2	I/O	26	The reference 2 (REF2) signal provides a bias voltage for the line coupling transformer associated with PM-2. During normal operation REF2 must be decoupled to ground with a 0.1 µF capacitor. This I/O connection should be left unconnected when the receive data slicer used by PM-2 is disabled.

RC1	I/O	9	The external peak detector RC network 1 (RC1) signal connects the peak detector of the receive data slicer used by PM-1 to an external RC network. During normal operation RC1 must be connected to ground through a parallel RC network consisting of a 316 kΩ resistor and a 47 nF capacitor. This I/O connection should be left unconnected when the receive data slicer used by PM-1 is disabled.
RC2	I/O	27	The external peak detector RC network 2 (RC2) signal connects the peak detector of the receive data slicer used by PM-2 to an external RC network. During normal operation RC2 must be connected to ground through a parallel RC network consisting of a 316 kΩ resistor and a 47 nF capacitor. This I/O connection should be left unconnected when the receive data slicer used by PM-2 is disabled.
LOS1	Output	8	The loss of signal indication 1 (LOS1) signal is set high upon detection of 11, 16, 32, 64 or 176 (programmable) consecutive zero bit intervals on the PM-1 PCM stream. The LOS1 output is reset (low) upon the next occurrence of a PCM line pulse. The PCM stream is examined prior to HDB3 decoding.
LOS2	Output	28	The loss of signal indication 2 (LOS2) signal is set high upon detection of 11, 16, 32, 64 or 176 (programmable) consecutive zero bit intervals on the PM-2 PCM stream. The LOS2 output is reset (low) upon the next occurrence of a PCM line pulse. The PCM stream is examined prior to HDB3 decoding.
LCLK	Input	20	The latch clock (LCLK) triggers sample and hold of the internal performance monitor counters in PM-1 and PM-2 when it is brought high. The recommended accumulation interval is one second and thus LCLK should be driven with a 1 Hz clock signal. Note that an equivalent action may be triggered through register accesses if use of LCLK is not desired.
RED1	Output	5	The red alarm indication 1 (RED1) signal indicates whether PM-1 has declared a red carrier fail alarm.
RED2	Output	31	The red alarm indication 2 (RED2) signal indicates whether PM-2 has declared a red carrier fail alarm.

REM1	Output	4	The remote alarm indication 1 (REM1) signal indicates whether PM-1 has declared a remote carrier fail alarm.
REM2	Output	32	The remote alarm indication 2 (REM2) signal indicates whether PM-2 has declared a remote carrier fail alarm.
AIS1	Output	3	The alarm indication signal 1 (AIS1) signal indicates whether PM-1 has declared an AIS carrier fail alarm.
AIS2	Output	33	The alarm indication signal 2 (AIS2) signal indicates whether PM-2 has declared an AIS carrier fail alarm.
PCLK1	Output	7	The recovered PCM clock 1 (PCLK1) is derived from the CEPT E1 signal processed by PM-1 and is nominally a 2.048 MHz, 40-60% duty cycle clock. Note that PCLK1 has jitter due to the clock recovery process and jitter due to the reference CEPT E1 signal.
PCLK2	Output	29	The recovered PCM clock 2 (PCLK2) is derived from the CEPT E1 signal processed by PM-2 and is nominally a 2.048 MHz, 40-60% duty cycle clock. Note that PCLK2 has jitter due to the clock recovery process and jitter due to the reference CEPT E1 signal.
PCM1	Output	6	The decoded PCM 1 (PCM1) signal outputs data recovered from the CEPT E1 signal processed by PM-1 after HDB3 or AMI decoding has been performed. PCM1 is updated on the falling edge of PCLK1.
PCM2	Output	30	The decoded PCM 2 (PCM2) signal outputs data recovered from the CEPT E1 signal processed by PM-2 after HDB3 or AMI decoding has been performed. PCM2 is updated on the falling edge of PCLK2.
FP1	Output	64	The active high frame pulse 1 (FP1) signal indicates that the framing bit position (bit 1 of the 256 bit frame) is present in the E1 stream. This output remains high for one clock period and is updated on the falling edge of PCLK1 when clock recovery is enabled, and on the falling edge of RDN1 when clock recovery is disabled.

FP2	Output	40	The active high frame pulse 2 (FP2) signal indicates that the framing bit position (bit 1 of the 256 bit frame) is present in the E1 stream. This output remains high for one clock period and is updated on the falling edge of PCLK2 when clock recovery is enabled, and on the falling edge of RDN2 when clock recovery is disabled.
MFP1	Output	63	The active high multiframe pulse 1 (MFP1) signal indicates that the CRC multiframe bit position (bit 1 in the first frame of the 16 frame CRC multiframe) is present in the E1 stream. This output remains high for one clock period and is updated on the falling edge of PCLK1 when clock recovery is enabled, and on the falling edge of RDN1 when clock recovery is disabled. Alternatively, MFP1 may be enabled to mark bit 1 in the first frame of the 16 frame CAS multiframe, or MFP1 may be enabled to go high coincident with the first bit of the CAS multiframe and go low during the bit position immediately following the CRC multiframe bit position, allowing both multiframes to be identified.
MFP2	Output	41	The active high multiframe pulse 2 (MFP2) signal indicates that the CRC multiframe bit position (bit 1 in the first frame of the 16 frame CRC multiframe) is present in the E1 stream. This output remains high for one clock period and is updated on the falling edge of PCLK2 when clock recovery is enabled, and on the falling edge of RDN2 when clock recovery is disabled. Alternatively, MFP2 may be enabled to mark bit 1 in the first frame of the 16 frame CAS multiframe, or MFP2 may be enabled to go high coincident with the first bit of the CAS multiframe and go low during the bit position immediately following the CRC multiframe bit position, allowing both multiframes to be identified.

DLINT1/ DLSIG1	Output	62	The data link interrupt 1 (DLINT1) signal indicates that the internal HDLC receiver in PM-1 is requesting servicing. DLINT1 is valid when the internal HDLC receiver is enabled in PM-1. When the internal HDLC receiver is disabled in PM-1, this output becomes data link signal 1 (DLSIG1). DLSIG1 carries the data link extracted from the national bits or timeslot 16 of the E1 frame, as selected through internal register bits. DLSIG1 is updated on the falling edge of DLCLK1.
DLINT2/ DLSIG2	Output	42	The data link interrupt 2 (DLINT2) signal indicates that the internal HDLC receiver in PM-2 is requesting servicing. DLINT2 is valid when the internal HDLC receiver is enabled in PM-2. When the internal HDLC receiver is disabled in PM-2, this output becomes data link signal 2 (DLSIG2). DLSIG2 carries the data link extracted from the national bits or timeslot 16 of the CEPT E1 frame, as selected through internal register bits. DLSIG2 is updated on the falling edge of DLCLK2.
DLEOM1/ DLCLK1	Output	61	The data link end of message 1 (DLEOM1) signal indicates that the internal HDLC receiver in PM-1 has received the final byte in a message and requires servicing. DLEOM1 is useful when interfacing to an external DMA controller and is valid when the internal HDLC receiver is enabled in PM-1. When the internal HDLC receiver is disabled in PM-1, this output becomes data link clock 1 (DLCLK1). DLCLK1 provides timing for the data link extracted from the CEPT E1 frame. DLCLK1 operates at selectable rates between 4 kHz and 20 kHz (derived from a gapped 1.024 MHz clock) when extracting the national bits and at 64 kHz when extracting timeslot 16.

DLEOM2/ DLCLK2	Output	43	The data link end of message 2 (DLEOM2) signal indicates that the internal HDLC receiver in PM-2 has received the final byte in a message and requires servicing. DLEOM2 is useful when interfacing to an external DMA controller and is valid when the internal HDLC receiver is enabled in PM-2. When the internal HDLC receiver is disabled in PM-2, this output becomes data link clock 2 (DLCLK2). DLCLK2 provides timing for the data link extracted from the CEPT E1 frame. DLCLK2 operates at selectable rates between 4 kHz and 20 kHz (derived from a gapped 1.024 MHz clock) when extracting the national bits and at 64 kHz when extracting timeslot 16.
INTB1	Output	59	The active low, open-drain interrupt 1 (INTB1) signal is asserted when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that the internal PM-1 HDLC receiver also has a separate interrupt output (DLINT1).
INTB2	Output	58	The active low, open-drain interrupt 2 (INTB2) signal is asserted when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that the internal PM-2 HDLC receiver also has a separate interrupt output (DLINT2).
CSB	Input	45	The active low chip select (CSB) signal is low during E1PM register accesses.
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	68 67 66 65 36 37 38 39	The bidirectional data bus (D[7:0]) is used during E1PM register accesses.
RDB	Input	53	The active low read enable (RDB) signal is low during an E1PM read access. The E1PM drives the D[7:0] bus with the addressed register's contents while RDB and CSB are low.
WRB	Input	50	The active low write strobe (WRB) signal is low during an E1PM write access. The D[7:0] bus contents are clocked into the addressed normal mode register on the rising edge of WRB while CSB is low.

TSTB	Input	44	The active low test mode select (TSTB) signal is low during E1PM production test. TSTB is high during normal operation. This pin has an internal pullup resistor.
RSTB	Input	60	The active low reset (RSTB) signal is low to provide an asynchronous E1PM reset. This pin has an internal pullup resistor and is a schmitt trigger input.
TRSB	Input	46	The test register select (TRSB) signal discriminates between normal and test mode register accesses. TRSB is low during test register accesses, and is high during normal mode register accesses. TRSB is high during normal operation. This pin has an internal pullup resistor.
A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	57 56 55 54 49 48 47	The address bus (A[6:0]) selects specific registers during E1PM register accesses.
VDDO[1] VDDO[0]	Power	2 34	The pad ring power (VDDO[1:0]) connections provide power for pad ring circuitry. VDDO[1:0] must be connected to a well decoupled +5 V DC supply. Both connections must be utilized. VDDO[1:0] and VDDI[1:0] should be externally connected to the same supply in a manner that minimizes switching noise coupling from VDDO[1:0] to VDDI[1:0].
VDDI[1] VDDI[0]	Power	51 19	The core power (VDDI[1:0]) connections provide power for core circuitry. VDDI[1:0] must be connected to a well decoupled +5 V DC supply. Both connections must be utilized.
VSSO[1] VSSO[0]	Ground	1 35	The pad ring ground (VSSO[1:0]) connections provide ground for pad ring circuitry. Both connections must be utilized. VSSO[1:0] and VSSI[1:0] should be externally connected to the same ground in a manner that minimizes switching noise coupling from VSSO[1:0] to VSSI[1:0].
VSSI[1] VSSI[0]	Ground	52 18	The core ground (VSSI[1:0]) connections provide ground for core circuitry. Both connections must be utilized.

AVD1	Power	13	The analog power 1 (AVD1) connection provides power for the receive data slicer associated with PM-1. AVD1 must be connected to a well decoupled +5 V DC supply. AVD1 should be connected to AVS1 to disable the receive data slicer used by PM-1.
AVD2	Power	23	The analog power 2 (AVD2) connection provides power for the receive data slicer associated with PM-2. AVD2 must be connected to a well decoupled +5 V DC supply. AVD2 should be connected to AVS2 to disable the receive data slicer used by PM-2.
AVS1	Ground	12	The analog ground 1 (AVS1) connection provides ground for the receive data slicer associated with PM-1.
AVS2	Ground	24	The analog ground 2 (AVS2) connection provides ground for the receive data slicer associated with PM-2.

Notes on Pin Description:

1. VDDI and VSSI are the +5 V and ground connections, respectively, for the core circuitry of the device. VDDO and VSSI are the +5 V and ground connections, respectively, for the pad ring circuitry of the device. These power supply connections must all be utilized and must all connect to a common +5 V or ground rail, as appropriate. There is no low impedance connection within the PM6322 between the core and pad ring supply rails. Failure to properly make these connections may result in improper operation or damage to the device.
2. AVD and AVS are the +5 V and ground connections, respectively, for the receive analog circuitry of the device. These power supply connections need only be used if the receive analog function is desired and should then connect to a common +5 V or ground rail, as appropriate, with the core and pad ring supply rails. There is no low impedance connection within the PM6322 between the receive analog supply rail and other supply rails. When the receive analog function is not desired, AVD should be connected to AVS. Care must be taken to avoid coupling of noise into the receive analog supply rails.
3. Inputs RSTB, TSTB and TRSB have integral pull-up resistors.

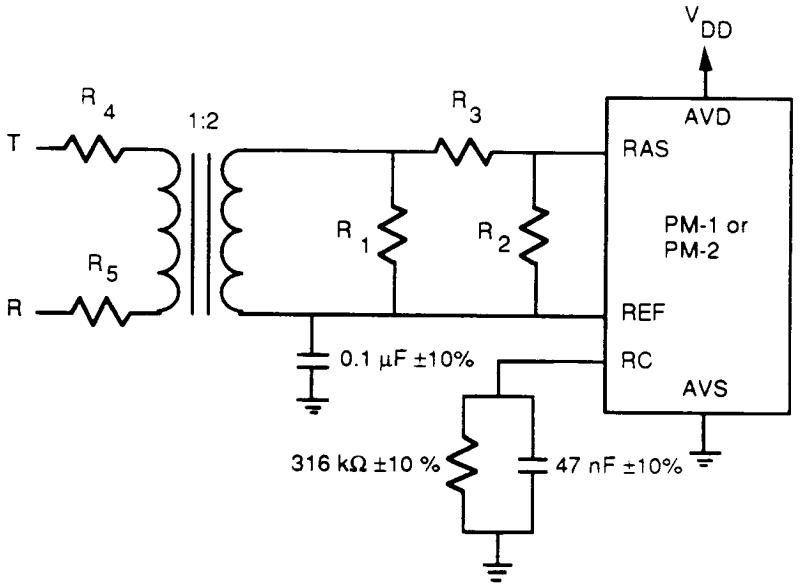
FUNCTIONAL DESCRIPTION

Receive Data Slicer

The Receive Data Slicer (RSLC) block provides the first stage of signal conditioning for an E1 serial data stream by converting bipolar line signals to dual rail RZ pulses. Before an RZ pulse is generated by the RSLC block, bipolar input signals must rise to 50% or 67% of their peak amplitude. This level is referred to as the slicing level and it is configurable, via the RSLC Configuration Register, as 50% or 67%. The threshold criteria insures accurate pulse or mark recognition in the presence of noise. The 50% level is appropriate for CCITT G.703 interfaces and the 67% level is suitable for ANSI DSX-1A interfaces.

The RSLC block has a squelch alarm state that is entered when input pulses are below the squelching level threshold. In this state, data is not sliced, which prevents the detection of noise on an idle transmission line. The squelch alarm state is entered when the pulse amplitude at the RAS input measured with respect to REF falls below 105 mV P (for the 67% slicing level), or below 140 mV P (for the 50% slicing level). The squelch alarm status may be polled via the RSLC Interrupt Enable/Status Register. The E1PM can be configured to generate an interrupt when the squelch alarm state changes.

Fig. 1 External Analog Interface Circuit (100Ω Line)

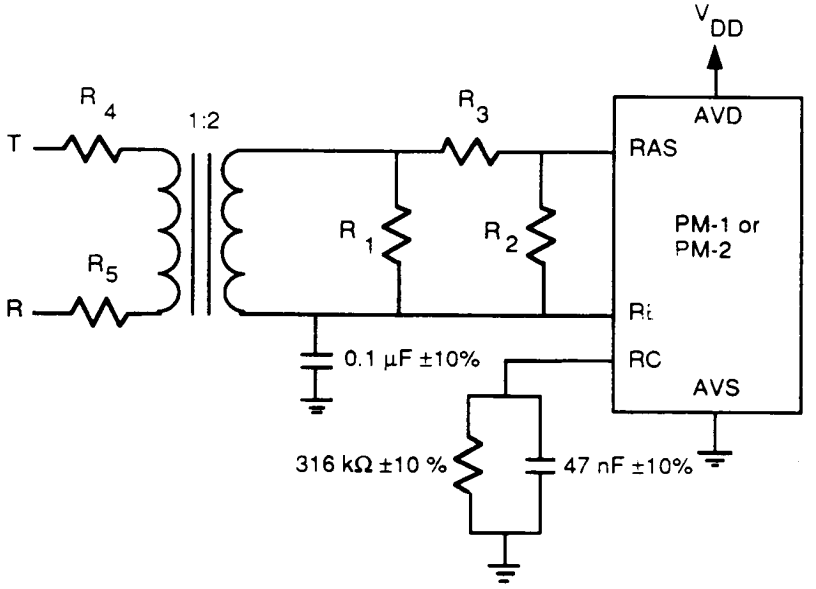


Terminate Mode	Bridging Mode
R_1 = 412 Ω ± 1%	R_1 = 400 Ω ± 1%
R_2 = 1.1 kΩ ± 1%	R_2 = Open Circuit
R_3 = 9.0 kΩ ± 1%	R_3 = Closed Circuit
R_4 = R_5 = Closed Circuit	R_4 = R_5 = 432 Ω ± 5 %

1. All capacitors ceramic
2. R_4 and R_5 are part of a DSX bridge-tap
3. Recommended Transformer: Pulse Engineering 64931
   BH Electronics 500-1775

The RSLC block is configured via an off-chip attenuator pad and a line coupling transformer to operate in one of two modes: terminating mode or bridging mode. Figure 1 shows typical configurations for interfacing with 100Ω twisted pair cable. Figures 2 and 3 show analogous configurations for interfacing to 75Ω coaxial cable and 120Ω twisted pair cable. In all examples it is assumed that a 1:2 transformer is used and (for the bridging mode) that 20 dB of attenuation is provided; other configurations are possible. Through the choice of attenuation network and transformer turns ratio, the pulse amplitude at the RAS input measured with respect to REF must be constrained to be between 213 mV P and 1.3 V P for proper operation. While this represents a dynamic range of over 15 dB, it is recommended that no more than 6 dB of loss be dispersive (cable) loss (measured at 1.024 MHz) and that the balance be flat loss due to pulse magnitude tolerances at the source and component tolerances in the attenuation network.

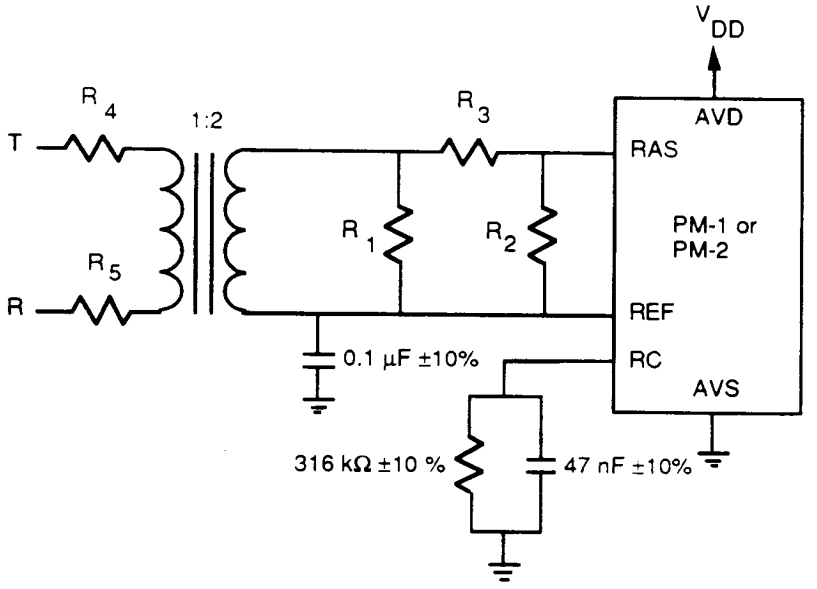
Fig. 2 External Analog Interface Circuit (75Ω Line)



Terminate Mode	Bridging Mode
R_1 = 309 Ω ± 1%	R_1 = 300 Ω ± 1%
R_2 = 1.1 kΩ ± 1%	R_2 = Open Circuit
R_3 = 9.0 kΩ ± 1%	R_3 = Closed Circuit
R_4 = R_5 = Closed Circuit	R_4 = 648 Ω ± 5 % R_5 = Closed Circuit

1. All capacitors ceram.
2. R_4 and R_5 are part of cross-connect bridge-tap
3. Recommended Transformer: Pulse Engineering 64931
   BH Electronics 500-1775

Fig. 3 External Analog Interface Circuit (120Ω Line)



Terminate Mode	Bridging Mode
R_1 = 504 Ω ± 1%	R_1 = 480 Ω ± 1%
R_2 = 1.1 kΩ ± 1%	R_2 = Open Circuit
R_3 = 9.0 kΩ ± 1%	R_3 = Closed Circuit
R_4 = R_5 = Closed Circuit	R_4 = R_5 = 520 Ω ± 5 %

1. All capacitors ceramic
2. R_4 and R_5 are part of a cross-connect bridge-tap
3. Recommended Transformer: Pulse Engineering 64931
   BH Electronics 500-1775

When the RSLC block is active, the positive and negative line pulses of the E1 signal extracted from analog inputs are output on the RDP and RDN pins, respectively. The RSLC block can be disabled by strapping the analog power pin, AVD, to ground. When the RSLC block is disabled, the E1PM accepts either digital RZ input pulses, or a unipolar clock and data signal, as selected via the Master Configuration Register, on the RDP1, RDN1, RDP2, and RDN2 pins.

Clock and Data Recovery

The Clock and Data Recovery (CDRC) block provides clock and PCM data recovery, HDB3 decoding, line code violation detection, 4 consecutive zeros detection, and loss of signal detection functions. The CDRC block recovers the clock from the incoming RZ data pulses using a digital phase-locked-loop. NRZ data is restored and HDB3 substitution is performed when enabled. The use of AMI or HDB3 line

code format is user-selectable. Bipolar violations which form part of the HDB3 line code are only reported as line code violations when AMI line code is selected. The detection of HDB3 signatures and 4 consecutive zeros is always reported, regardless of the selected line code. A programmable loss of signal threshold is provided. Loss of signal is indicated when no line pulse is detected for 11, 16, 32, 64, or 176 consecutive bit periods, and is cleared after the occurrence of a single line pulse. If enabled, an interrupt is generated upon the occurrence of line events and/or alarms.

Fig. 4 Typical External Crystal Oscillator Circuit

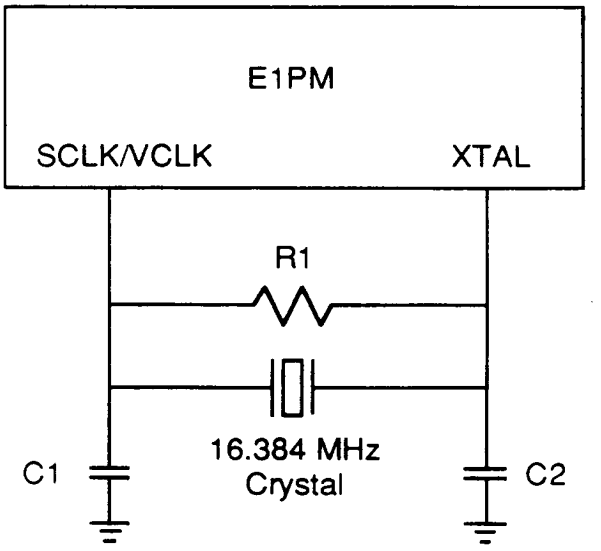


Figure 4 shows a typical circuit using an external crystal for timing generation. Typically, R1 has a value of 1 MΩ or greater. The values of the two capacitors are dependent upon the specified load capacitance of the crystal. An AT cut crystal with a parallel resonant frequency of 16.384 MHz for an 18 pF load is recommended. For the recommended crystal, the capacitors, C1 and C2 each have a value of 30 pF (taking into account the capacitance of the pins). The performance monitors in the E1PM share the same timing source.

Framer

The Framer (FRMR) block searches for frame alignment, CRC multiframe alignment, and channel associated signalling (CAS) multiframe alignment in the incoming recovered PCM stream.

Once the FRMR has found basic frame alignment, the incoming PCM data is continuously monitored for FAS/NFAS framing bit errors. Once the FRMR has found CAS multiframe alignment, the PCM data is continuously monitored for CAS multiframe alignment pattern errors. Once the FRMR has found CRC multiframe

alignment, the PCM data is continuously monitored for CRC multiframe alignment pattern errors, and CRC-4 errors. The FRMR also detects and indicates loss of frame, loss of CAS multiframe, and loss of CRC multiframe, based on user-selectable criteria. The reframe operation can be initiated by software (via the FRMR Frame Alignment Options Register), by excessive CRC errors, or when CRC multiframe alignment is not found within 8 ms. The FRMR also identifies the position of the frame, the CAS multiframe, and the CRC multiframe.

The FRMR extracts timeslot 16 for optional use as a data link and also extracts the contents of the International bits (from both the FAS frames and the NFAS frames), the National bits, and the Extra bits (from timeslot 16 of frame 0 of the CAS multiframe), and stores them in the FRMR International/National Bits Register, and the FRMR Extra Bits Register respectively.

The FRMR identifies the raw bit values for Remote Alarm (bit 3 in timeslot 0 of NFAS frames) and Remote Signalling Multiframe Alarm (bit 6 of timeslot 16 of frame 0 of the CAS multiframe) via the FRMR International/National Bits Register, and the FRMR Extra Bits Register respectively. Access is also provided to the "debounced" Remote Alarm and Remote Signalling Multiframe Alarm bits which are set when the corresponding signals have been a logic 1 for 2 or 3 consecutive occurrences. Detection of AIS and timeslot 16 AIS are provided; AIS is also integrated and an AIS Alarm is indicated if the AIS condition has persisted for at least 100 ms. The out of frame (OOF=1) condition is also integrated, indicating a red Alarm if the OOF condition has persisted for at least 100 ms.

An interrupt may be generated to signal a change in the state of any status bits (OOF, OOSMF, OOCMF, AIS, or RED), and to signal when any event (RRA, RRMA, AISD, T16AISD, COFA, FER, SMFER, CMFER, CRCE, or FEBE) has occurred.

Frame Find Block

The Frame Find Block searches for frame alignment using one of two user-selectable algorithms, as defined in Recommendation G.732. Optionally, a two frame check sequence can be added to either algorithm to provide protection against false frame alignment in the presence of random mimic patterns.

The first algorithm finds frame alignment by using the following sequence:

1. Search for the presence of the correct 7-bit FAS;

2. Check that the FAS is absent in the following frame by verifying that bit 2 of the assumed timeslot 0 byte is a logic 1;

3. Check that the correct 7-bit FAS is present in the assumed timeslot 0 byte of the next frame.

If either of the conditions in steps 2 or 3 are not met, a new search for frame alignment is initiated in the bit immediately following the errored timeslot 0 byte location.

The second algorithm is similar to the first, but adds a one frame "hold-off" in step 2 to begin a new search in the bit immediately following the second 7-bit FAS that is checked. This "hold-off" is performed if either of the conditions in steps 2 or 3 fail, providing a more robust algorithm which allows the framer to operate correctly in the presence of fixed timeslot data imitating the FAS pattern.

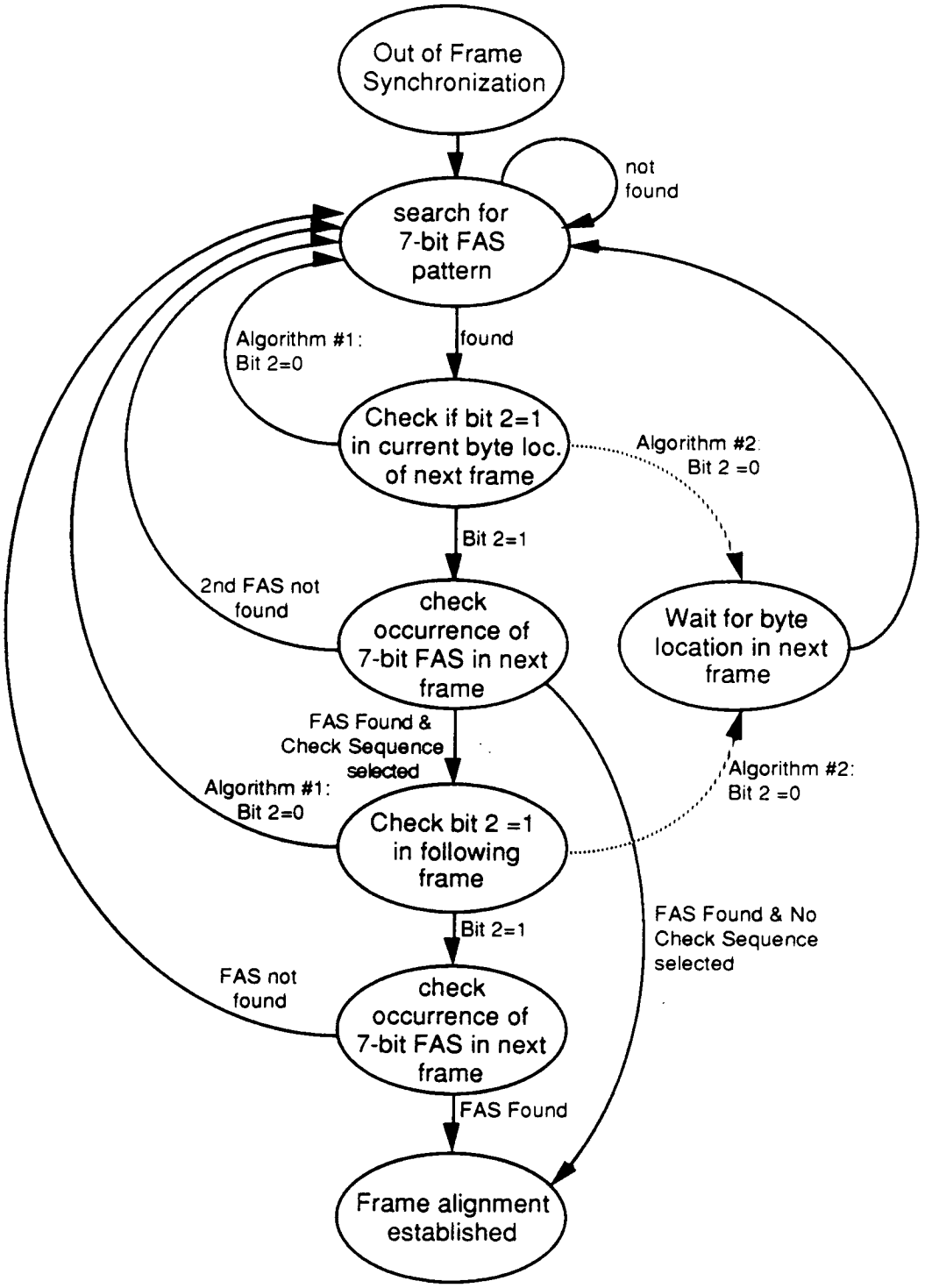
A check sequence can be added to either algorithm to verify correct frame alignment in the presence of random imitative FASs. Note that this check sequence should be enabled when monitoring an unframed 2^15 -1 pseudo random sequence to avoid framing to the single mimic framing pattern contained in the sequence. The check consists of verifying correct frame alignment for an additional two frames, as follows:

- once frame alignment (in frame "n") is determined, check that the FAS is absent in the following frame (frame "n+1") by verifying that bit 2 of timeslot 0 is a logic 1;
- then, check that the correct 7-bit FAS is present in timeslot 0 of the next frame (frame "n+2").

If either of the two conditions in the check sequence are not met, a new search for frame alignment is initiated in the bit immediately following the errored byte location when using the first algorithm, and is initiated in the bit immediately following the byte location in frame "n+2" when using the second algorithm.

These algorithms are illustrated in Figure 5.

Fig. 5 Basic Framing Algorithm Flowchart



These algorithms provide robust framing operation even in the presence of random bit errors: framing with algorithm #1 or #2 provides a 99.98% probability of finding frame alignment within 1 ms in the presence of 10^{-3} bit error rate and no mimic patterns.

Once frame alignment is found, the block sets the OOF indication low, indicates a change of frame alignment (if it occurred), and monitors the frame alignment signal, indicating errors occurring in the 7-bit FAS pattern and in bit 2 of NFAS frames, and indicating the debounced value of the Remote Alarm bit (bit 3 of NFAS frames). Using debounce, the Remote Alarm bit has <0.00001% probability of being falsely indicated in the presence of a 10^{-3} bit error rate. The block declares loss of frame alignment if 3 or 4 consecutive FASs have been received in error or, additionally, if bit 2 of NFAS frames has been in error for 3 consecutive occasions. In the presence of a random 10^{-3} bit error rate the frame loss criteria provides a mean time to falsely lose frame alignment of >12 minutes.

The Frame Find Block can be forced to initiate a frame search at any time when any of the following conditions are met:

- the software re-frame bit in the Frame Alignment Options Register goes to logic 1;
- the CRC Frame Find Block is unable to find CRC multiframe alignment; or
- the CRC Frame Find Block accumulates excessive CRC evaluation errors (≥ 915 CRC errors in 1 second) and is enabled to force a re-frame.

CRC Frame Find Block

The CRC Frame Find Block searches for CRC multiframe alignment by observing whether the International bits (bit 1 of timeslot 0) of NFAS frames follow the CRC multiframe alignment pattern. Multiframe alignment is declared if at least two valid CRC multiframe alignment signals are observed within 8 ms, with the time separating two alignment signals being a multiple of 2 ms.

Once CRC multiframe alignment is found, the block sets the OOCMF indication low, and monitors the multiframe alignment signal, indicating errors occurring in the 6-bit pattern, and indicating the value of the FEBE bits (bit 1 of frames 13 and 15 of the multiframe).The block declares loss of CRC multiframe alignment if four consecutive CRC multiframe alignment signals have been received in error, or if frame alignment has been lost.

The CRC Frame Find Block will force the Frame Find Block to initiate a frame search when CRC multiframe alignment has not been found for 8 ms.

CRC Check and AIS Detect Block

The CRC Check and AIS Detect Block computes the 4-bit CRC checksum for each incoming sub-multiframe and compares this 4-bit result to the received CRC remainder bits in the subsequent sub-multiframe. The block also accumulates CRC errors over 1 second intervals, monitoring for excessive CRC errors and optionally, forcing the Frame Find Block to initiate a frame search when ≥ 915 CRC errors occur in 1 second. The number of CRC errors accumulated during the previous second is available by reading the FRMR CRC Error Counter Registers.

The block also detects the occurrence of an unframed all-ones receive data stream, indicating the AIS by setting the AISD indication when less than 3 zero bits are received in 2 frames (512 consecutive bits); the AISD indication is reset when 3 or more zeros in the E1 stream are observed, or when frame alignment is found.

Signalling Frame Find Block

The Signalling Frame Find Block searches for CAS multiframe alignment using one of two user-selectable algorithms, one of which is compatible with Recommendation G.732. Once frame alignment has been found, the first algorithm monitors timeslot 16 of each frame; it declares CAS multiframe alignment when 15 consecutive frames with bits 1-4 of timeslot 16 not containing the alignment pattern are observed to precede a frame with timeslot 16 containing the correct alignment pattern. The second algorithm, compatible with G.732, also monitors timeslot 16 of each frame, and declares CAS multiframe alignment when non-zero bits 1-4 of timeslot 16 are observed to precede a timeslot 16 containing the correct alignment pattern.

Once CAS multiframe alignment has been found, the block sets the OOSMF indication to logic 0, and monitors the CAS multiframe alignment signal, indicating errors occurring in the 4-bit pattern, and indicating the debounced value of the Remote Signalling Multiframe Alarm bit (bit 6 of timeslot 16 of frame 0 of the multiframe). Using debounce, the Remote Signalling Multiframe Alarm bit has < 0.00001% probability of being falsely indicated in the presence of a 10^{-3} bit error rate. This block also indicates the reception of timeslot 16 AIS when timeslot 16 has been all-ones for two consecutive frames while out of CAS multiframe. The block declares loss of CAS multiframe alignment if two consecutive CAS multiframe alignment signals have been received in error, or additionally, if all the bits in timeslot 16 are logic 0 for 1 or 2 (selectable) CAS multiframes. Loss of CAS multiframe alignment is also declared if frame alignment has been lost.

Alarm Integrator Block

The Alarm Integrator Block monitors the OOF and the AISD indications, verifying that each condition has persisted for 104 ms (±6 ms) before indicating the alarm condition. The alarm is removed when the condition has been absent for 104 ms (±6 ms).

The AIS alarm algorithm accumulates the occurrences of AISD over a 4 ms interval and indicates a valid AIS presence when 13 or more AISD indications have been received. Each interval with a valid AIS presence indication increments an interval counter which declares AIS Alarm when 25 valid intervals have been accumulated. An interval with no valid AIS presence indication decrements the interval counter; the AIS Alarm declaration is removed when the counter reaches 0. This algorithm provides a 99.8% probability of declaring an AIS Alarm in the presence of a 10^{-3} mean bit error rate.

The red alarm algorithm monitors occurrences of OOF over a 4 ms interval, indicating a valid OOF interval when one or more OOF indications occurred during the interval, and indicating a valid in frame (INF) interval when no OOF indication occurred for the entire interval. Each interval with a valid OOF indication increments an interval counter which declares Red Alarm when 25 valid intervals have been accumulated. An interval with valid INF indication decrements the interval counter; the RED Alarm declaration is removed when the counter reaches 0. This algorithm biases OOF occurrences, leading to declaration of red alarm when intermittent loss of frame alignment occurs.

Pulse Density Violation Detector

The Pulse Density Violation Detector (PDVD) block detects pulse density violations of the requirement that there be 'N' ones in each and every time window of 8(N+1) data bits (where 'N' can equal from 1 to 23). This function may be used for alternate mark inversion (AMI) facility pulse density monitoring.

Pulse density violation detection is indicated via the PDVD Enable/Status Register. The E1PM can be programmed to generate an interrupt to signal a change of state in the pulse density violation indication.

Performance Monitor Accumulator

The Performance Monitor (PMON) block accumulates CRC error events, frame synchronization bit error events, line code violation events, and far end block error events with saturating counters over consecutive intervals as defined by the period (typically 1 second) of the supplied latch clock signal, LCLK. A single LCLK input serves both performance monitors in the E1PM. An internal latch clock signal, unique to each performance monitor in the E1PM, can be generated by writing to any of the PMON holding registers. A write to any PMON holding register in PM-1 generates an internal latch clock pulse for PM-1 and similarly a write to any PMON holding register in PM-2 generates an internal latch clock pulse for PM-2. On the rising edge of the latch clock signal, the counter values are transferred into the holding registers and the counters are reset. The counters are reset in a manner such that error events occurring during the reset are not missed. The counter sizes are chosen such that there is negligible chance of saturation when operating at a 10^{-3} bit error rate if polled at 1 second intervals.

If enabled, an interrupt is generated whenever counter data is transferred into the holding registers. If the holding registers are not read between successive transfer clocks, an overrun is set in the PMON Control/Status Register.

Bit Oriented Code Detector

The Bit Oriented Code Detector (RBOC) block detects the presence of 63 of the 64 possible bit oriented codes (BOCs) transmitted in the data link. The 64th code ("111111") is similar to the HDLC flag sequence and is ignored by the RBOC. A 4 kbit/s data link may be carried in national bit 4.

Bit oriented codes are received on the data link as 16-bit sequences each consisting of 8 ones, a zero, 6 code bits, and a trailing zero ("111111110xxxxxx0"). BOCs are repeated at least 10 times when transmitted. The RBOC block can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the RBOC Control Register.

Valid BOCs are indicated through the RBOC Interrupt Status Register. The BOC bits are set to all ones ("111111") if no valid code has been detected. The E1PM can be programmed to generate an interrupt when a detected code has been validated. The E1PM can also be programmed to generate an interrupt when there is a return to idle code (all ones).

HDLC Receive Facility Data Link

The Receive Facility Data Link (RFDL) block is a microprocessor peripheral used to receive LAPD/HDLC frames on the data link. A 4 kbit/s data link may be carried in national bit 4. The RFDL block detects the change from flag characters to the first data frame byte, removes stuffed bits from the frame data, and computes the frame check sequence (CRC-CCITT) associated with the frame.

The RFDL places received data into a four-byte FIFO buffer. Interrupts can be enabled to occur after one, two, or three frame bytes have been received (programmable FIFO fill level), or disabled completely. Software selects the interrupt generation interval by assigning values to two bits in the RFDL Interrupt Enable/Status Register. Each read of the RFDL Receive Data Register should be followed by a read of the RFDL Status Register. The RFDL Status Register contains a FIFO status bit (FE) that indicates the full/empty status of the four-byte FIFO. If the FE bit is a zero, the FIFO is not empty, so successive reads of the RFDL Receive Data Register must be performed followed by reads of the RFDL Status Register until the FE bit is a one (i.e. until the FIFO buffer is empty). The RFDL Receive Data Register must not be read if the FE bit is a one.

If the software selects the FIFO fill level to be two bytes before an interrupt is generated (i.e. 4 msec for a 4 kbit/s data link), the corresponding maximum interrupt service time is 6 msec (i.e. 3 frame byte periods). If the maximum interrupt service time is exceeded, the overrun bit (OVR) in the RFDL Status Register is set to

one, and an interrupt is immediately generated. An interrupt is also generated upon reception of an abort sequence while the link is active. The FLG bit in the RFDL Status Register is set to zero upon reception of an abort sequence.

Initialization

Upon reset, the RFDL Configuration Register is set to 00H, and the RFDL is disabled. The RFDL Interrupt Status/Control Register must be written to select the FIFO fill level for which an interrupt is generated.

After the RFDL Interrupt Enable/Status Register has been written, the RFDL can be enabled at any time by setting the EN bit in the RFDL Configuration Register to one. When the RFDL is enabled, it assumes the link status is idle (all ones) and immediately begins searching for flags. When the first flag is found, an interrupt is generated, regardless of the FIFO fill level. An RFDL Status Register read following an RFDL Receive Data Register read returns EOM=1 and FLG=1. The first interrupt and data byte read after the RFDL is enabled is an indication of the link status and the data byte should be discarded. It is up to the controlling software to keep track of the link state as idle (all ones or bit oriented messages active) or active (flags received).

Servicing

The microprocessor interrupt service routine should process data the following order:

1) Read the RFDL Receive Data Register
2) Read the RFDL Status Register to check for underrun (status register returned 00H), OVR, FLG, EOM and if more data is available (FE), in that order.
3) If underrun (status register returned 00H), then discard last byte and wait for next interrupt.
4) If OVR=1, discard last packet and wait for next interrupt.
5) If FLG=0 (abort) and the link state was active, set the link state to inactive, discard the last packet and wait for the next interrupt.
6) If FLG=1 and the link state was inactive, set the link state to active, discard the last packet and wait for the next interrupt.
7) Otherwise save the last data byte read.
8) If EOM=1, check the CRC bit and process the packet.
9) If FE=0, go to step 1, or else wait for the next interrupt.

The link state is a local software variable. The link state is inactive if the RFDL is receiving all ones or receiving bit oriented codes which contain a sequence of eight ones. The link state is active if the RFDL is receiving flags or data.

The DLEOM status output is provided for interfacing the E1PM to a DMA controller.

Pseudo Random Sequence Monitor

The Pseudo Random Sequence Monitor (PRSM) block monitors the recovered PCM data for the presence of a framed or unframed 2^{15}-1 test sequence as defined in Recommendation O.151 and accumulates bit errors detected using this pseudo-random pattern. The test sequence is inverted before being checked against the generated pattern. The sequence monitor does not synchronize to an all zeros pattern. The PRSM declares synchronization when less than 15 sequence errors are detected in 125 µsec (256 bit periods). Using this threshold, synchronization is achieved within 125 µsec, 99.9% of the time, in the presence of a 10^{-2} bit error rate. Once synchronized, the mean time between loss of synchronization events is greater than 103 minutes, in the presence of a 10^{-2} bit error rate. When the test sequence is no longer present (as indicated by a bit error rate greater than 10^{-1}) the PRSM will lose synchronization in 2 µsec, 99.9% of the time. In the presence of random data (a bit error rate of 0.5) the mean time between false synchronization events is greater than 184 years.

The PRSM block accumulates bit error events with a saturating counter over consecutive intervals as defined by the period (typically 1 second) of the supplied latch clock signal, LCLK. A single LCLK input serves both pseudo random sequence monitors in the E1PM. An internal latch clock signal, unique to each pseudo random sequence monitor in the E1PM, can be generated by writing to any of the PMON holding registers. A write to any PMON holding register in PM-1 generates an internal latch clock pulse for PM-1, and similarly a write to any PMON holding register in PM-2 generates an internal latch clock pulse for PM-2. On the rising edge of the latch clock signal, the counter values are transferred into the PRSM holding registers and the counters are reset. The counters are reset in a manner such that error events occurring during the reset are not missed. The counter sizes are chosen such that there is negligible chance of saturation when operating at a 10^{-2} bit error rate if polled at 1 second intervals.

If enabled, an interrupt is generated whenever counter data is transferred into the PRSM holding registers. If the holding registers are not read between successive transfer clocks, the overrun (OVR) bit in the PRSM Control/Status Register is set.

An indication of whether or not the pseudo random sequence monitor is synchronized is provided via the PRSM Control/Status Register and, if enabled, an interrupt is generated whenever a loss of synchronization or resynchronization occurs.

Data Link Extractor

The Data Link Extractor (DLEX) block allows any combination of the National bits to be extracted to form a data link to be processed by the RBOC and RFDL blocks or

routed off-chip under the control of the DLEX Data Link Extract Options Register, and the Master Configuration Register. Alternatively, timeslot 16 may be extracted in place of the National bits. By default, National bit 4 is extracted. In addition, the E1PM may be enabled to generate an interrupt upon a change of state in the National bits that are not being extracted for use as a data link. The state of these bits may be polled via the FRMR International/National Bits Register.

Microprocessor Interface

The Microprocessor Interface (MPIF) block allows for device level configuration of each performance monitor (PM) in the E1PM. The low-power modes and the use of the internal or an external HDLC controller are configured via the Master Configuration Register. The interrupts from each block in each PM are masked and monitored with the Master Interrupt Enable Register and the Master Interrupt Status Register, respectively. A software reset mode and E1PM version identification is provided via the Master Reset Register.

The MPIF block also serves as the physical interface between the microprocessor and the internal blocks. Functions such as data bus buffering and address decoding are provided by the MPIF block.

Normal Mode Register Memory Map

PM-1	PM-2	REGISTER DESCRIPTION
00H	40H	MASTER CONFIGURATION
01H	41H	MASTER INTERRUPT ENABLE
02H	42H	MASTER INTERRUPT STATUS
03H	43H	MASTER RESET
04H	44H	RFDL CONFIGURATION
05H	45H	RFDL INTERRUPT ENABLE/STATUS
06H	46H	RFDL STATUS
07H	47H	RFDL RECEIVE DATA
08H	48H	PMON CONTROL/STATUS
09H	49H	PMON FRAMING BIT ERROR EVENT COUNT
0AH	4AH	PMON FEBE EVENT COUNT LSB
0BH	4BH	PMON FEBE EVENT COUNT MSB
0CH	4CH	PMON CRC ERROR EVENT COUNT LSB
0DH	4DH	PMON CRC ERROR EVENT COUNT MSB
0EH	4EH	PMON LINE CODE VIOLATION EVENT COUNT LSB
0FH	4FH	PMON LINE CODE VIOLATION EVENT COUNT MSB
10H	50H	FRMR FRAME ALIGNMENT OPTIONS
11H	51H	FRMR MAINTENANCE MODE OPTIONS
12H	52H	FRMR FRAMING STATUS INTERRUPT ENABLE

13H	53H	FRMR MAINTENANCE/ALARM STATUS INT. ENABLE
14H	54H	FRMR FRAMING STATUS INTERRUPT INDICATION
15H	55H	FRMR MAINTENANCE/ALARM STATUS INT. IND.
16H	56H	FRMR FRAMING STATUS
17H	57H	FRMR MAINTENANCE/ALARM STATUS
18H	58H	FRMR INTERNATIONAL/NATIONAL BITS
19H	59H	FRMR EXTRA BITS
1AH	5AH	FRMR CRC ERROR COUNT LSB
1BH	5BH	FRMR CRC ERROR COUNT LSB
1CH	5CH	CDRC CONFIGURATION
1DH	5DH	CDRC INTERRUPT CONTROL
1EH	5EH	CDRC INTERRUPT STATUS
1FH	5FH	Reserved for CDRC test
20H	60H	RBOC ENABLE
21H	61H	RBOC INTERRUPT STATUS
22H	62H	Reserved for PDVD test
23H	63H	PDVD ENABLE/STATUS
24H	64H	DLEX DATA LINK EXTRACT OPTIONS
25H	65H	Reserved for DLEX test
26H	66H	RSLC CONFIGURATION
27H	67H	RSLC INTERRUPT ENABLE/STATUS
28H	68H	Reserved for PRSM test
29H	69H	PRSM CONTROL/STATUS
2AH	6AH	PRSM BIT ERROR EVENT COUNT LSB
2BH	6BH	PRSM BIT ERROR EVENT COUNT MSB
2CH-3FH	6CH-7FH	Unused

Note: All register bits are cleared to zero upon activation of E1PM reset unless otherwise noted.

NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the E1PM. Normal mode registers (as opposed to test mode registers) are selected when TRSB is high.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the E1PM to determine the programming state of the chip.

3. Writeable normal mode register bits are cleared to zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect E1PM operation unless otherwise noted.

Internal Registers

Register 00H, 40H: Master Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5	R/W	CMFPE
Bit 4	R/W	SMFPE
Bit 3	R/W	NRZE
Bit 2	R/W	PATHE
Bit 1	R/W	LINEE
Bit 0	R/W	EXHDLC

This register allows software to configure the associated performance monitor (address 00H for PM-1, address 40H for PM-2) in the E1PM package. The state of the EXHDLC (external HDLC) bit determines whether the PM uses the internal HDLC receiver or provides the data and clock signals for an external HDLC receiver. When the EXHDLC bit is a logic 0, the DLINT/DLSIG pin is configured to output the interrupt signal (DLINT) from the internal HDLC receiver and the DLEOM/DLCLK pin is configured to output the end-of-message signal (DLEOM) from the internal HDLC receiver. When the EXHDLC bit is a logic 1, the DLINT/DLSIG pin is configured to output the facility data link data stream (DLSIG) and the DLEOM/DLCLK pin is configured to output the facility data link clock signal (DLCLK) for use by an external HDLC receiver. Upon reset of a PM, the EXHDLC bit is cleared to zero, thus the internal HDLC receiver is selected.

The line enable (LINEE) and path enable (PATHE) bits select whether the PM is enabled to monitor the line or the path, respectively. When the PM is only enabled to monitor the line, the following blocks are deactivated: DLEX, RFDL and RBOC . When the path is being monitored, all blocks are active. When neither the line nor the path is being monitored, the PM is in low-power mode. In low-power mode, only

the CDRC and RSLC blocks are active. The mode selection is given in the following table:

PATHE	LINEE	DESCRIPTION
0	0	Low-power mode; only CDRC and RSLC are active
0	1	Line monitoring mode; RBOC, DLEX and RFDL inactive
1	X	Path monitoring mode; all blocks active

Upon reset of the PM, both the PATHE and LINEE bits are cleared to zero which places the PM in low-power mode.

The NRZ input enable bit, NRZE, allows the E1PM to be configured to accept a single rail digital E1 signal. When the NRZE bit is logic 1, the pin RDP is configured to accept single rail data and the pin RDN is expected to be a 2.048 MHz clock. RDP is then sampled on the rising edge of RDN. When the NRZE bit is a logic 0, the RDP and RDP inputs are configured to accept dual rail RZ data from which clock is recovered. The NRZE bit has no affect if the RSLC analog block is powered (i.e. if AVD is connected to +5 Volts). When configured for single rail operation, PCM data is routed directly to the FRMR block, bypassing the CDRC and PDVD blocks, and the CDRC and PDVD blocks are held reset to save power. In this configuration, it is not necessary to provide a 16.384 MHz clock on the SCLK input.

The CAS multiframe enable (SMFPE) and CRC multiframe enable (CMFPE) bits select whether the PM is enabled to indicate the CAS multiframe or CRC multiframe, or both, on the MFP output. The mode selection is given in the following table:

SMFPE	CMFPE	DESCRIPTION
0	0	Default; CRC multiframe is indicated only
0	1	CRC multiframe indication only
1	0	CAS multiframe indication only
1	1	Both CRC and CAS multiframe are indicated

Register 01H, 41H:
Master Interrupt Enable

Bit	Type	Function
Bit 7	R/W	DLINTE
Bit 6	R/W	PDVDE
Bit 5	R/W	RBOCE
Bit 4	R/W	PMONE
Bit 3	R/W	PRSME
Bit 2	R/W	FRMRE
Bit 1	R/W	CDRCE
Bit 0	R/W	RSLCE

This register provides an interrupt enable bit for each of the blocks comprising one performance monitor in the E1PM. Interrupts may still be masked at the source block level. Interrupts enabled at the block level but masked by this register are reported in the Master Interrupt Status Register. Interrupts disabled at the block level are not reported by the Master Interrupt Status Register. The RFDL block also generates a separate, active high, interrupt output (DLINT). Interrupts on the DLINT pin are not maskable with this register. Note that the enable for the FRMR block also enables interrupts from the associated DLEX block.

Register 02H, 42H:
Master Interrupt Status

Bit	Type	Function
Bit 7	R	DLINTI
Bit 6	R	PDVDI
Bit 5	R	RBOCI
Bit 4	R	PMONI
Bit 3	R	PRSMI
Bit 2	R	FRMRI
Bit 1	R	CDRCI
Bit 0	R	RSLCI

This register identifies the block which is the source of a pending interrupt. After identifying the block which generated the interrupt, it may be necessary to read the interrupt status register of that block to determine the actual event which generated

the interrupt. This register is provided as a convenience to the user since the source block of an interrupt can be determined by polling the interrupt status registers of every block in the E1PM. Unlike the interrupt status registers associated with each block, this register only reports interrupt sources capable of generating a hardware interrupt, that is interrupts masked at the block interrupt enable register level are not reported by this register. The RFDL block also generates a separate, active high, interrupt output (DLINT). Note that the interrupt indication for the FRMR block may also indicate an interrupt from the associated DLEX block.

Register 03H, 43H:
Master Reset

Bit	Type	Function
Bit 7	R/W	RESET
Bit 6	R	TYPE
Bit 5	R	ID[5]
Bit 4	R	ID[4]
Bit 3	R	ID[3]
Bit 2	R	ID[2]
Bit 1	R	ID[1]
Bit 0	R	ID[0]

This register allows software to asynchronously reset the associated performance monitor (address 03H for PM-1 and address 43H for PM-2) in the E1PM package; the two performance monitors in the E1PM package have independent software resets. The software reset is equivalent to setting the RSTB input pin to low, except that only one performance monitor is affected. Setting the RESET bit to logic 1 causes the associated PM to be reset; clearing the RESET bit to logic 0 disables the reset mode. In reset mode, all bits in all PM registers are reset except for the RESET bit itself. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register. The E1PM RSTB pin resets both performance monitors in the E1PM package and clears the RESET bit in this register to logic 0, disabling the software reset mode.

The device identification bit, TYPE, is set to 1 to identify the E1PM. The version identification bits, ID[5:0], are set to a fixed value representing the version number of the E1PM. The identification bits can be used to determine the E1PM version via software. The identification bits of each PM are identical.

RFDL Registers

Register 04H, 44H: RFDL Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R/W	TR
Bit 0	R/W	EN

The enable bit, EN, controls the overall operation of the RFDL block. When EN is set to logic 1, the RFDL is enabled; when EN is reset to logic 0 the RFDL is disabled. When the RFDL is disabled, the FIFO and interrupts are cleared. The programming of the Enable/Status Register is not affected. When the RFDL is enabled, it immediately begins to look for flag sequences in the data link. An interrupt is generated when the first flag is detected.

Setting the terminate reception, TR, bit forces the RFDL to immediately terminate the reception of the current LAPD frame, empty the FIFO, clear the interrupts, and begin searching for a new flag sequence. The RFDL handles the TR input in the same manner as if the EN bit had been cleared and then set. The TR bit in the Configuration Register resets itself following a rising and a falling edge on the CLK input to the RFDL TSB after the write to this register has completed and the WRB signal becomes inactive. If the Configuration Register is read after this time, the TR bit value will be zero.

Register 05H, 45H: RFDL Interrupt Enable/Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2	R/W	INTC[1]
Bit 1	R/W	INTC[0]
Bit 0	R	INT

The interrupt control bits, INTC[1] and INTC[0], control interrupt generation as follows:

INTC[1]	INTC[0]	Description
0	0	Disable interrupts (All sources)
0	1	Enable interrupt when FIFO receives data
1	0	Enable interrupt when FIFO has 2 bytes of data
1	1	Enable interrupt when FIFO has 3 bytes of data

The interrupt bit, INT, reflects the status of the external interrupt unless the INTC[1] and INTC[0] bits are set to disable interrupts. If interrupts are disabled, the external interrupt output is forced to 0, but the INT bit of the Enable/Status Register reflects the state of the internal interrupt latch.

In addition to the FIFO fill status, interrupts are also generated for EOM (end of message), OVR (FIFO overrun), detection of the abort sequence while not receiving all ones and on detection of the first flag while receiving all ones. The interrupt is reset by a Receive Data Register read that empties the FIFO, unless the cause of the interrupt was due to a FIFO overrun. The interrupt due to a FIFO overrun is cleared by reading the Status Register, by disabling the RFDL, or by setting TR high.

The contents of the Enable/Status Register should only be changed when the RFDL TSB is disabled (EN=0) to prevent any erroneous interrupt generation. When the E1PM is reset, the INTC[1] and INTC[0] bits are reset to 0; therefore, interrupt generation is disabled.

Register 06, 46H: RFDL Status

Bit	Type	Function
Bit 7	R	FE
Bit 6	R	OVR
Bit 5	R	FLG
Bit 4	R	EOM
Bit 3	R	CRC
Bit 2	R	NVB[2]
Bit 1	R	NVB[1]
Bit 0	R	NVB[0]

The NVB[2:0] bit positions indicate the number of valid bits in the Receive Data Register byte. It is possible that not all of the bits in the Receive Data Register are valid when the last data byte is read since the data frame can be any number of bits in length and not necessarily an integral number of bytes. The Receive Data Register is filled from the MSB to the LSB bit position, with one to eight data bits being valid. The number of valid bits is equal to 1 plus the value of NVB[2:0]. A NVB[2:0] value of zero ("000") indicates that only the MSB in the register is valid. NVB[2:0] is only valid when the EOM bit is logic 1, the FLG bit is logic 1 and the OVR bit is logic 0.

The CRC bit is set to logic 1 if a CRC error was detected in the last received LAPD frame. The CRC bit is only valid when the EOM bit is logic 1, FLG is logic 1 and OVR is logic 0. On an interrupt generated from the detection of the first flag, reading the Status Register returns invalid NVB[2:0] and CRC bits, even though the EOM bit is logic 1 and the FLG bit is logic 1.

The end of message bit (EOM) follows the EOM output. It is set when: the last byte in the LAPD frame (EOM) is being read from the Receive Data Register, an abort sequence is detected while not in the receiving all-ones state and the byte, written to the FIFO due to the detection of the abort sequence, is being read from the FIFO, the first flag has been detected and the dummy byte, written into the FIFO when the RFDL changes from the receiving all-ones state to the receiving flags state, is being read from the FIFO, or a FIFO overrun is detected. The EOM bit is passed through the FIFO with the data so that the status corresponds to the data just read from the FIFO.

The flag bit (FLG) is set to logic 1 if the RFDL has detected the presence of the LAPD flag sequence ("01111110") on the data link. FLG is reset to logic 0 only when the LAPD abort sequence ("01111111") is detected in the data or when the RFDL is

disabled. This bit is passed through the FIFO with the data so that the status corresponds to the data just read from the FIFO. The reception of bit oriented codes over the data link will also force an abort due to the eight ones pattern in the bit oriented codes.

The receiver overrun (OVR) bit is set to logic 1 when data overwrites unread data in the FIFO. The OVR bit is not reset until after the Status Register is read. While OVR is high, the RFDL and FIFO are held in the reset state, which causes the FLG and EOM bits in the Status Register to be reset as well.

The FIFO empty (FE) bit is logic 1 when the last FIFO entry is read and changes to logic 0 when the FIFO is loaded with new data.

If the Receive Data Register is read while there is no valid data in the FIFO, then a FIFO underrun condition occurs. The underrun condition is reflected in the Status Register by forcing all bits to logic 0 on the first Status Register read immediately following the Received Data Register read which caused the underrun condition.

Register 07H, 47H:
RFDL Receive Data

Bit	Type	Function
Bit 7	R	RD[7]
Bit 6	R	RD[6]
Bit 5	R	RD[5]
Bit 4	R	RD[4]
Bit 3	R	RD[3]
Bit 2	R	RD[2]
Bit 1	R	RD[1]
Bit 0	R	RD[0]

This register is actually a 4-level FIFO buffer. RD[0] corresponds to the first bit of the serial byte received on the data link. If data is available, the FE bit in the Status Register is logic 0. If INTC[1:0] (in the Enable/Status Register) is set to "01", the Receive Data Register must be read within 31 data bit periods to prevent an overrun. If INTC[1:0] is set to "11" the Receive Data Register must be read within 15 data bit periods.

When an overrun is detected, an interrupt is generated and the FIFO is held cleared until the Status Register is read. When the LAPD abort sequence ("01111111") is detected in the data an ABORT interrupt is generated and the data that has been shifted into the serial-to-parallel converter is written into the FIFO.

Reading the Receive Data Register increments the FIFO pointer at the end of the operation. If the Receive Data Register read causes a FIFO underrun, then the pointer is not incremented. The underrun condition is signalled in the next Status Register read by returning all zeros.

PMON Registers

Register 08H, 48H: PMON Control/Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2	R/W	INTE
Bit 1	R	INT
Bit 0	R	OVR

This register enables an interrupt to be generated whenever counter data is transferred into the holding registers. This register also contains status information as to whether the holding registers have been overrun.

The INTE bit controls the generation of a microprocessor interrupt when the transfer clock has caused the counter values to be stored in the Holding Registers. A logic 1 bit in the INTE position enables the generation of an interrupt; a logic 0 bit in the INTE position disables the generation of an interrupt. When the E1PM is reset, the INTE is set to 0, disabling the interrupt. The interrupt is cleared (acknowledged) by reading this register.

The INT bit is the current status of the interrupt signal. A logic 1 in this bit position indicates that a transfer has occurred. A logic 0 indicates that no transfer has occurred.

The OVR bit holds the overrun status of the Holding Registers. A logic 1 in this bit position indicates that a previous interrupt has not been acknowledged before the next transfer clock has been issued and that the contents of the Holding Registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register.

Latching Performance Data

The Performance Monitor (PMON) holding registers (09H-0FH, 49H-4FH) are updated by the rising edge of LCLK. The time between successive rising edges of LCLK determines the accumulation interval which is nominally one second. A single LCLK input serves both performance monitors in the E1PM. A microprocessor write to any of the PMON holding registers also causes an update of the PMON holding registers associated with that performance monitor in the E1PM. The PMON block is loaded with new performance data within 4 PCLK periods of the rising edge of LCLK. With PCLK at its nominal frequency of 2.048 MHz, the PMON registers should not be read until 2 µsec have elapsed since the rising edge of LCLK. The data contained in the holding registers is subsequently read by the microprocessor. The loading is synchronized to the internal event timing so that no events are missed.

Register 09H, 49H:
PMON Framing Bit Error Event Count

Bit	Type	Function
Bit 7		Unused
Bit 6	R	FER[6]
Bit 5	R	FER[5]
Bit 4	R	FER[4]
Bit 3	R	FER[3]
Bit 2	R	FER[2]
Bit 1	R	FER[1]
Bit 0	R	FER[0]

This holding register indicates the number of FAS framing bit error events that occurred during the previous accumulation interval. The content of this register is valid 2 µs after a transfer is triggered by a rising edge on LCLK or a write to any PMON holding register address.

Register 0AH, 4AH:
PMON Far End Block Error Event Count LSB

Bit	Type	Function
Bit 7	R	FEBE[7]
Bit 6	R	FEBE[6]
Bit 5	R	FEBE[5]
Bit 4	R	FEBE[4]
Bit 3	R	FEBE[3]
Bit 2	R	FEBE[2]
Bit 1	R	FEBE[1]
Bit 0	R	FEBE[0]

Register 0BH, 4BH:
PMON Far End Block Error Event Count MSB

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R	FEBE[9]
Bit 0	R	FEBE[8]

These holding registers indicate the number of far end block error events that occurred during the previous accumulation interval. The contents of these registers are valid 2 µs after a transfer is triggered by a rising edge on LCLK or a write to any PMON holding register address.

Register 0CH, 4CH:
PMON CRC Error Event Count LSB

Bit	Type	Function
Bit 7	R	CRCE[7]
Bit 6	R	CRCE[6]
Bit 5	R	CRCE[5]
Bit 4	R	CRCE[4]
Bit 3	R	CRCE[3]
Bit 2	R	CRCE[2]
Bit 1	R	CRCE[1]
Bit 0	R	CRCE[0]

Register 0DH, 4DH:
PMON CRC Error Event Count MSB

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R	CRCE[9]
Bit 0	R	CRCE[8]

These holding registers indicate the number of CRC error events that occurred during the previous accumulation interval. The contents of these registers are valid 2 µs after a transfer is triggered by a rising edge on LCLK or a write to any PMON holding register address.

Register 0EH, 4EH: PMON Line Code Violation Event Count LSB

Bit	Type	Function
Bit 7	R	LCV[7]
Bit 6	R	LCV[6]
Bit 5	R	LCV[5]
Bit 4	R	LCV[4]
Bit 3	R	LCV[3]
Bit 2	R	LCV[2]
Bit 1	R	LCV[1]
Bit 0	R	LCV[0]

Register 0FH, 4FH: PMON Line Code Violation Event Count MSB

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R	LCV[12]
Bit 3	R	LCV[11]
Bit 2	R	LCV[10]
Bit 1	R	LCV[9]
Bit 0	R	LCV[8]

These holding registers indicate the number of LCV error events that occurred during the previous accumulation interval. The contents of these registers are valid 2 µs after a transfer is triggered by a rising edge on LCLK or a write to any PMON holding register address.

FRMR Registers

Register 10H, 50H: FRMR Frame Alignment Options

Bit	Type	Function
Bit 7	R/W	CRCEN
Bit 6	R/W	CASDIS
Bit 5	R/W	AFAA
Bit 4	R/W	CHKSEQ
Bit 3	R/W	CASA
Bit 2	R/W	REFR
Bit 1	R/W	REFCRCE
Bit 0	R/W	REFRDIS

This register selects the various framing formats and framing algorithms supported by the FRMR.

The CRCEN bit enables the FRMR to frame to the CRC multiframe. A logic 1 in the CRCEN bit position enables the search for CRC multiframe alignment and monitoring of errors in the alignment. A logic 0 in the CRCEN bit position disables searching for CRC multiframe and suppresses the CRCE, CMFER, and FEBE outputs, forcing them low; OOCMF is forced high. When the CRCEN bit is logic 0, the ICMFP output pulses high every 16th frame, indicating the FAS frame.

The CASDIS bit enables the FRMR to frame to the Channel Associated Signalling multiframe. A logic 0 in the CASDIS bit position enables the search for CAS multiframe alignment and monitoring of errors in the alignment. A logic 1 in the CASDIS bit position disables searching for CAS multiframe alignment and suppresses the SMFER output, forcing it low; the OOSMF is forced high. When the CASDIS bit is logic 1, the ISMFP output pulses high every 16th frame.

The AFAA bit selects the algorithm to be used to search for and verify frame alignment. A logic 1 in the AFAA bit position enables the use of algorithm #2 with the "hold-off" to verify the correct frame alignment in the presence of fixed imitative FASs; a logic 0 enables the use of the algorithm #1.

The CHKSEQ bit enables the use of the check sequence in addition to the basic frame find algorithms to verify the correct frame alignment in the presence of random imitative FASs. A logic 1 in the CHKSEQ bit position enables the use of the check sequence algorithm; a logic 0 disables the algorithm. This bit should be set to a logic 1 when monitoring an unframed 2^15 - 1 pseudorandom sequence. This

sequence contains a single mimic framing pattern which is rejected when the CHKSEQ bit is set.

The CASA bit selects the algorithm to be used to find Channel Associated Signalling multiframe alignment. A logic 0 in the CASA bit position selects the G.732-compatible algorithm; a logic 1 selects the alternative framing algorithm.

A transition from logic 0 to logic 1 in the REFR bit position forces the FRMR to initiate a search for frame alignment. The bit must be cleared to logic 0, then set to logic 1 again to initiate subsequent searches for frame alignment.

A logic 1 in the REFCRCE bit position enables excessive CRC errors (≥ 915 errors one second) to force the FRMR to search for a new frame alignment. A logic 0 disables reframe due to excessive CRC errors.

The REFRDIS bit disables reframing under any error condition once frame alignment has been found, leaving reframing to be initiated only by software via the REFR bit, or via the external EXREFR input. A logic 1 in the REFRDIS bit position causes the FRMR to remain "locked in frame" once initial frame alignment has been found. A logic 0 allows reframing to occur based on the various error criteria (FER, excessive CRC errors, etc).

Register 11H, 51H:
FRMR Maintenance Mode Options

Bit	Type	Function
Bit 7	R/W	FASC
Bit 6	R/W	BIT2C
Bit 5	R/W	SMFASC
Bit 4	R/W	T16C
Bit 3	R/W	RADEB
Bit 2	R/W	RMADEB
Bit 1	R	CMFACT
Bit 0	R	EXCRCE

The FASC bit selects the criterion used to declare loss of frame alignment signal (FAS): loss of frame alignment is declared after 3 consecutive frame alignment patterns have been received in error if FASC is a logic 0; if FASC is a logic 1, it is declared after 4 consecutive frame alignment patterns have been received in error.

A logic 1 in the BIT2C bit position enables the additional criterion that loss of frame is declared when bit 2 in timeslot 0 of NFAS frames has been received in error on 3

consecutive occasions; a logic 0 in BIT2C enables declaration of loss of frame alignment based on the setting of FASC, only.

The SMFASC bit selects the criterion used to declare loss of CAS multiframe alignment signal: a logic 0 in the SMFASC bit position enables declaration of loss of CAS multiframe alignment when 2 consecutive multiframe alignment patterns have been received in error; a logic 1 in the SMFASC bit position enables declaration of loss of CAS multiframe when the above condition is met or when timeslot 16 contains logic 0 in all bit positions for 1 or 2 multiframes, based on the criterion selected by T16C. A logic 0 in the T16C bit position enables declaration of loss of CAS multiframe alignment when timeslot 16 contains logic 0 in all bit positions for 1 multiframe; a logic 1 in the T16C bit position enables declaration of loss of CAS multiframe when timeslot 16 contains logic 0 in all bit positions for 2 consecutive CAS multiframes.

The RADEB bit selects the amount of debouncing applied to the Remote Alarm Indication before the RRA is permitted to change state: a logic 0 in the RADEB bit position enables the RRA output to change to the logic value contained in the Remote Alarm bit position (bit 3 of NFAS frames) when the received Remote Alarm bit value has been in the same state for 2 consecutive NFAS frames; a logic 1 in the RADEB bit position enables the RRA output to change when the Remote Alarm bit has been in the same state for 3 consecutive NFAS frames.

The RMADEB bit selects the amount of debouncing applied to the Remote Signalling Multiframe Alarm Indication before the RRMA is allowed to change state: a logic 0 in the RMADEB bit position enables the RRMA output to change to the logic value contained in the Remote Signalling Multiframe Alarm bit position (bit 6 of timeslot 16 of frame 0 of the CAS multiframe) when the received Remote Signalling Multiframe Alarm bit value has been in the same state for 2 consecutive CAS multiframes; a logic 1 in the RMADEB bit position enables the RRMA output to change when the Remote Signalling Multiframe Alarm bit has been in the same state for 3 consecutive CAS multiframes.

The CMFACT bit is an active high status bit which indicates that the CRC Multiframe Find algorithm has been active for more than 8 ms, and indicates that a search for new frame alignment has been initiated. The CMFACT bit is forced low while CRCEN is at logic 0. The CMFACT bit is reset to logic 0 after this register is read.

The EXCRCE bit is an active high status bit which indicates that excessive CRC evaluation errors (≥915 error in one second) have occurred. A search for new frame alignment is initiated if the REFCRCE is set high. The EXCRCE bit is reset to logic 0 after this register is read.

Register 12H, 52H:
FRMR Framing Status Interrupt Enable

Bit	Type	Function
Bit 7		Unused
Bit 6	R/W	OOFE
Bit 5	R/W	OOSMFE
Bit 4	R/W	OOCMFE
Bit 3	R/W	COFAE
Bit 2	R/W	FERE
Bit 1	R/W	SMFERE
Bit 0	R/W	CMFERE

This register selects which of the possible interrupt sources are enabled to generate an interrupt. A logic 1 in the OOFE, OOSMFE, or OOCMFE enable bit positions enables a change of state of the corresponding status to generate an interrupt. A logic 1 in the FERE, SMFERE, CMFERE, or COFAE enable bit positions enables the occurrence of the corresponding event to generate an interrupt. A logic 0 in any bit position disables the corresponding status change or event from generating an interrupt.

Register 13H, 53H:
FRMR Maintenance/Alarm Status Interrupt Enable

Bit	Type	Function
Bit 7	R/W	RRAE
Bit 6	R/W	RRMAE
Bit 5	R/W	AISDE
Bit 4	R/W	T16AISDE
Bit 3	R/W	REDE
Bit 2	R/W	AISE
Bit 1	R/W	FEBEE
Bit 0	R/W	CRCEE

This register selects which of the possible interrupt sources are enabled to erate an interrupt. A logic 1 in the RRAE, RRMAE, AISDE, T16AISDE, REDE, or E enable bit positions enables a change of state of the corresponding status generate an interrupt. A logic 1 in the FEBEE or CRCE enable bit positions enables

the occurrence of the corresponding event to generate an interrupt. A logic 0 in any bit position disables the corresponding status change or event from generating an interrupt.

Register 14H, 54H:
FRMR Framing Status Interrupt Indication

Bit	Type	Function
Bit 7		Unused
Bit 6	R	OOFI
Bit 5	R	OOSMFI
Bit 4	R	OOCMFI
Bit 3	R	COFAI
Bit 2	R	FERI
Bit 1	R	SMFERI
Bit 0	R	CMFERI

This register indicates which of the possible interrupt sources generated an interrupt.

A logic 1 in the OOFI, OOSMFI, or OOCMFI status bit positions indicates that the corresponding status has changed state. A logic 1 in the FERI, SMFERI, CMFERI, or COFAI indicates the detection of the corresponding event. These bits will be set to logic 1 if one or more events have occurred on the corresponding signal since the last register read.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The contents of this register are cleared to logic 0 after the register is read.

Register 15H, 55H: FRMR Maintenance/Alarm Status Interrupt Indication

Bit	Type	Function
Bit 7	R	RRAI
Bit 6	R	RRMAI
Bit 5	R	AISDI
Bit 4	R	T16AISDI
Bit 3	R	REDI
Bit 2	R	AISI
Bit 1	R	FEBEI
Bit 0	R	CRCEI

This register indicates which of the possible interrupt sources generated an interrupt.

A logic 1 in the RRAI, RRMAI, AISDI, T16AISDI, REDI, or AISI status bit positions indicates that the corresponding status has changed state. A logic 1 in the FEBEI, or CRCEI indicates the detection of the corresponding error event. These bits will be set to logic 1 if one or more events have occurred on the corresponding signal since the last register read.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The contents of this register are cleared to logic 0 after the register is read.

Register 16H, 56H:
FRMR Framing Status

Bit	Type	Function
Bit 7		Unused
Bit 6	R	OOF
Bit 5	R	OOSMF
Bit 4	R	OOCMF
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0		Unused

Reading this register returns the current state value of the OOF, OOSMF, and OOCMF framing status signals.

Register 17H, 57H:
FRMR Maintenance/Alarm Status

Bit	Type	Function
Bit 7	R	RRA
Bit 6	R	RRMA
Bit 5	R	AISD
Bit 4	R	T16AISD
Bit 3	R	RED
Bit 2	R	AIS
Bit 1		Unused
Bit 0		Unused

Reading this register returns the current state value of the RRA, RRMA, AISD, T16AISD, RED, and AIS maintenance/alarm status signals.

Register 18H, 58H: FRMR International/National Bits

Bit	Type	Function
Bit 7	R	Si[1]
Bit 6	R	Si[0]
Bit 5	R	RAWRA
Bit 4	R	Sn[4]
Bit 3	R	Sn[3]
Bit 2	R	Sn[2]
Bit 1	R	Sn[1]
Bit 0	R	Sn[0]

Reading this register returns the current bit value of the International and National bits collected over 2 consecutive frames. The Si[1] bit position corresponds to the value contained in the International bit position in the FAS frame; the Si[0], RAWRA, and Sn[4:0] bit positions correspond to the values contained in the International, Remote Alarm Indication, and National bit positions in the NFAS frame. The register bits Sn[4:0] correspond to the National bits Sa4-Sa8 described in Recommendation G.704. This register is updated after timeslot 0 of every NFAS frame and the contents are valid for 2 frames (250 µs) while in frame; the contents are frozen while OOF is high. The contents of this register are latched during the read, however the individual bits should not be considered to constitute a byte value (i.e., the 5 national bits should not be considered as indicating 1 of 32 possible values since it is possible that the individual bits are not all from the same time instant due to the asynchronous nature of the microprocessor reads). If the bits are to be interpreted as binary values, care should be taken to ensure a coherent set of bit values by reading the register at least twice.

The contents of this register are unaffected by resetting the E1PM.

Register 19H, 59H: FRMR Extra Bits

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	R	X[3]
Bit 2	R	RAWRMA
Bit 1	R	X[1]
Bit 0	R	X[0]

Reading this register returns the current bit value of the Extra bits and the Remote Signalling Multiframe Alarm collected from timeslot 16 of frame 0 of CAS multiframes. The X[3], RAWRMA, X[1], X[0] bit positions corresponds to the value contained in bit positions 5, 6, 7, and 8 in timeslot 16 of frame 0 of the CAS multiframe. This register is updated once per CAS multiframe (the contents remain valid for 2 ms) while in frame; the contents are frozen while OOSMF is high. If the X[3], X[1], X[0] bits are to be interpreted as binary values, care should be taken to ensure a coherent set of bit values by reading the register at least twice.

The contents of this register are unaffected by resetting the E1PM.

Register 1AH, 5AH:
FRMR CRC Error Counter - LSB

Bit	Type	Function
Bit 7	R	CRCE[7]
Bit 6	R	CRCE[6]
Bit 5	R	CRCE[5]
Bit 4	R	CRCE[4]
Bit 3	R	CRCE[3]
Bit 2	R	CRCE[2]
Bit 1	R	CRCE[1]
Bit 0	R	CRCE[0]

Register 1BH, 5BH:
FRMR CRC Error Counter - MSB

Bit	Type	Function
Bit 7	R	OVR
Bit 6	R	NEWDATA
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R	CRCE[9]
Bit 0	R	CRCE[8]

These registers contain the 10-bit CRC error counter value, updated every second, the NEWDATA flag, and the OVR flag.

The NEWDATA flag bit indicates that the counter register contents have been updated with a new count value accumulated over the last 1 second interval. It is set to logic 1 when the CRC error counter data is transferred into the counter registers, and is reset to logic 0 when this register is read. This bit can be polled to determine the 1 second timing boundary used by the FRMR.

The OVR flag bit indicates that the counter register contents have not been read within the last 1 second interval, and have therefore been overrun. It is set to logic 1

if CRC error counter data is transferred into the counter registers before the previous data has been read out, and is reset to logic 0 when this register is read.

Both registers should be read at least twice to ensure a coherent count value.

CDRC Registers

Register 1CH, 5CH: CDRC Configuration

Bit	Type	Function
Bit 7	R/W	AMI
Bit 6	R/W	LOS[1]
Bit 5	R/W	LOS[0]
Bit 4	R/W	DCR
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0		Unused

The alternate mark inversion (AMI) bit specifies the line coding of the incoming E1 signal. A logic 1 selects AMI line coding by disabling HDB3 decoding. A logic 0 selects HDB3 line coding by substituting an HDB3 signature with four zeros on the RPCM output.

The loss of signal threshold is set by the state of the AMI, LOS[1] and LOS[0] bits:

AMI	LOS[1]	LOS[0]	Threshold (PCM periods)
0	0	0	10
1	0	0	15
X	0	1	31
X	1	0	63
X	1	1	175

When the number of consecutive zeros on the incoming PCM line exceeds the programmed threshold, the LOS output is set high. For example, if the threshold is set to 10, the 11th zero causes the LOS output to go high.

A logic 1 in the DCR bit position disables clock recovery. The DCR bit must be set to 0 for proper operation in this application.

Register 1DH, 5DH:
CDRC Interrupt Control

Bit	Type	Function
Bit 7	R/W	LCVE
Bit 6	R/W	LOSE
Bit 5	R/W	HDB3E
Bit 4	R/W	Z4DE
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0		Unused

The Z4DE, HDB3E, LOSE, and LCVE (bits 4 to 7) of this register are interrupt enable bits used to select which of the outputs (four consecutive zeros, HDB3 pattern, loss of signal, or line code violation) will generate an interrupt when their status changes, as follows:

- Four zeros or an HDB3 signature is detected.
- The LOS output changes from low to high or from high to low.
- A line code violation is detected.

The occurrence of any of these events will generate an interrupt if there is a logic 1 in the corresponding bit position. When the E1PM is reset, Z4DE, HDB3E, LOSE, and LCVE are set to logic 0, disabling any interrupt generation.

Register 1EH, 5EH: CDRC Interrupt Status

Bit	Type	Function
Bit 7	R	LCVI
Bit 6	R	LOSI
Bit 5	R	HDB3I
Bit 4	R	Z4DI
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0	R	LOSV

The Z4DI, HDB3I, LOSI and LCVI (bits 4 to 7) of this register indicate which of the status events generated an interrupt. A logic 1 in any of these bit positions indicates that the corresponding event was detected and has generated an interrupt; a logic 0 in any of these bit positions indicates that the corresponding event has not been detected. The Z4DI, HDB3I and LCVI bits are set on the occurrence of the corresponding event. The LOSI bit is set high on any transition of the LOS output. Bits Z4DI, HDB3I, LOSI and LCVI are returned to logic 0 by reading this register. The LOSV bit reflects the status of the LOS output.

RBOC Registers

Register 20H, 60H: RBOC Configuration/Interrupt Enable

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2	R/W	IDLE
Bit 1	R/W	AVC
Bit 0	R/W	INTE

This register selects the validation criteria to be used in determining a valid bit oriented code (BOC) and enables generation of an interrupt at code validation.

The AVC bit position selects the validation criterion used in determining a valid BOC. A logic 0 selects the 8 out of 10 matching BOC criterion; a logic 1 in the AVC bit position selects the "alternate" validation criterion of 4 out of 5 matching BOCs.

The INTE bit position enables or disables the generation of an interrupt when a valid BOC is detected. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation. When the E1PM is reset, INTE is reset to logic 0; therefore, interrupt generation is disabled.

The IDLE bit position enables or disables the generation of an interrupt when a return to idle detected (i.e. when a valid BOC is no longer present).. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation. When the E1PM is reset, IDLE is reset to logic 0; therefore, interrupt generation is disabled.

Register 21H, 61H: RBOC Interrupt Status

Bit	Type	Function
Bit 7	R	IDLEI
Bit 6	R	BOCI
Bit 5	R	BOC[5]
Bit 4	R	BOC[4]
Bit 3	R	BOC[3]
Bit 2	R	BOC[2]
Bit 1	R	BOC[1]
Bit 0	R	BOC[0]

This register indicates whether an interrupt was generated by a detection of a valid BOC and indicates the current state value of the BOC[5:0] bits. A logic 1 in the BOCI bit position indicates that a validated BOC code has generated an interrupt; a logic 0 in the BOCI bit position indicates that no BOC has been detected. A logic 1 in the IDLEI bit position indicates that a return to idle has generated an interrupt; a logic 0 in the IDLEI bit position indicates that no such transition has been detected. Since the bit oriented code "111111" is not recognized by the RBOC, the BOC[5:0] bits are set to all ones ("111111") if no valid code has been detected. The BOCI and IDLEI bit positions are cleared when this register is read.

PDVD Register

Register 23H, 63H: PDVD Interrupt Enable/Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R	PDV
Bit 3	R	Z16DI
Bit 2	R	PDVI
Bit 1	R/W	Z16DE
Bit 0	R/W	PDVE

This register indicates the current state of the PDV output, selects which events can generate interrupts and identifies the source of the pending interrupt. The PDV bit indicates the current state of the pulse density violation detect (PDV) output.

The PDVE bit is an interrupt enable bit. When the PDVE bit is set to logic 1, an interrupt is generated whenever the state of the PDV output changes. When the PDVE bit is logic 0, interrupt generation by changes in the state of PDV is disabled. When the Z16DE interrupt enable bit is set to logic 1, an interrupt is generated wher the Z16D output goes high. When the Z16DE bit is logic 0, interrupt generation by Z16D is disabled.

The PDVI and Z16DI bits identify the source of a generated interrupt. PDVI is a logic 1 if a change in the state of the PDV output generated an interrupt. Z16DI is a logic 1 whenever the Z16D output goes high. PDVI and Z16DI are cleared when this register is read. Regardless of whether interrupts are enabled or disabled, the PDVI and Z16DI bits retain their event capture function.

DLEX Register

Register 24H, 64H: DLEX Data Link Extract Options

Bit	Type	Function
Bit 7		Unused
Bit 6	R/W	NBCE
Bit 5	R	NBCI
Bit 4	R/W	NBE[4]
Bit 3	R/W	NBE[3]
Bit 2	R/W	NBE[2]
Bit 1	R/W	NBE[1]
Bit 0	R/W	NBE[0]

This register selects the National bits that are to be extracted and routed off-chip or processed on-chip by the RBOC and RFDL blocks as a data link. Setting any of the NBE[4:0] bits selects the corresponding National bits to be included in the data link. After reset, NBE[4] is set to logic 1 which causes the default configuration to be use of National bit 4 as a 4 kbit/s data link. If all NBE[4:0] bits are set to logic 0, Timeslot 16 is extracted and treated as a data link.

The NBCE bit enables the generation of an interrupt whenever there is a change in the National bits that are not extracted to form a data link. The value of the National bits can be read in the FRMR International/National Bits Register. The NBCI bit is set to logic one whenever an interrupt due to a change in the National bits is activated. The NBCI bit is cleared following a read of this register.

PRSM Registers

Register 29H, 69H: PRSM Control/Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5	R/W	OOSE
Bit 4	R	OOSI
Bit 3	R	OOS
Bit 2	R/W	INTE
Bit 1	R	INT
Bit 0	R	OVR

This register enables an interrupt to be generated whenever counter data is transferred into the PRSM holding registers. The configuration register also contains status information as to whether the holding registers have been overrun.

The INTE bit controls the generation of a microprocessor interrupt when the transfer clock has caused the counter values to be stored in the Holding Registers. A logic 1 bit in the INTE position enables the generation of an interrupt; a logic 0 bit in the INTE position disables the generation of an interrupt. When the E1PM is reset, the INTE is set to 0, disabling the interrupt. The interrupt is cleared (acknowledged) by reading this register.

The INT bit is the current status of the interrupt signal. A logic 1 in this bit position indicates that a transfer has occurred. A logic 0 indicates that no transfer has occurred. The INT bit is cleared following a read of this register.

The OVR bit holds the overrun status of the Holding Registers. A logic 1 in this bit position indicates that a previous interrupt has not been acknowledged before the next transfer clock has been issued and that the contents of the Holding Registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register.

This register also enables an interrupt to be generated whenever synchronization is lost or regained.

The OOSE bit controls the generation of a microprocessor interrupt when a change of synchronization state occurs A logic 1 bit in the OOSE position enables the generation of an interrupt; a logic 0 bit in the OOSE position disables the generation

of an interrupt. When the E1PM is reset, the OOSE is set to 0, disabling the interrupt. The interrupt is cleared (acknowledged) by reading this register.

The OOSI bit is the current status of the interrupt signal. A logic 1 in this bit position indicates that an interrupt has occurred. A logic 0 indicates that no interrupt has occurred. The OOSI bit is cleared following a read of this register.

The OOS bit indicates the synchronization status of the PRSM block. A logic 1 in this bit position indicates that the PRSM block is out of sync. When out of sync, bit error events are not accumulated. A logic 0 indicates that the PRSM block is synchronized and accumulating bit error events.

Latching Performance Data

The Pseudo Random Sequence Monitor (PRSM) holding registers (1AH-1BH, 6AH-6BH) are updated by the rising edge of LCLK. The time between successive rising edges of LCLK determines the accumulation interval which is nominally one second. A single LCLK input serves both pseudo random sequence monitors in the E1PM. A microprocessor write to any of the PMON holding registers also causes an update of the PRSM holding registers associated with that pseudo random sequence monitor in the E1PM. The PRSM block is loaded with new performance data within 4 PCLK periods of the rising edge of LCLK. With PCLK at its nominal frequency of 2.048 MHz, the PRSM holding registers should not be read until 2 µsec have elapsed since the rising edge of LCLK. The data contained in the holding registers is subsequently read by the microprocessor. The loading is synchronized to the internal event timing so that no events are missed.

Register 1AH, 6AH:
PRSM Bit Error Event Count LSB

Bit	Type	Function
Bit 7	R	BER[7]
Bit 6	R	BER[6]
Bit 5	R	BER[5]
Bit 4	R	BER[4]
Bit 3	R	BER[3]
Bit 2	R	BER[2]
Bit 1	R	BER[1]
Bit 0	R	BER[0]

Register 1BH, 6BH:
PRSM Bit Error Event Count MSB

Bit	Type	Function
Bit 7	R	BER[15]
Bit 6	R	BER[14]
Bit 5	R	BER[13]
Bit 4	R	BER[12]
Bit 3	R	BER[11]
Bit 2	R	BER[10]
Bit 1	R	BER[9]
Bit 0	R	BER[8]

These holding registers indicate the number of bit error events that occurred during the previous accumulation interval. The contents of these registers are valid 2 µs after a transfer is triggered by a rising edge on LCLK or a write to any PMON holding register address.

RSLC Registers

Register 26H, 66H: RSLC Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0	R/W	THS

The THS bit controls the selection of the slicing threshold. When THS is set to logic 1, the 50% slicing threshold is used (suitable for CCITT G.703 interfaces). When THS is set to logic 0, the 67% slicing threshold is used (suitable for ANSI DSX-1A interfaces). THS is initialized to a logic 0 upon activation of the E1PM reset.

Register 27H, 67H: RSLC Interrupt Enable/Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2	R	SQ
Bit 1	R	SQI
Bit 0	R/W	SQE

The SQ bit indicates whether or not the RSLC block is squelching the generation of digital pulses due to low signal levels. When the SQ bit is high, squelching is occurring. The SQE bit is an interrupt enable for the squelch alarm. When SQE is logic 1, a squelching event will generate an interrupt. The SQI bit indicates that a squelch alarm generated an interrupt. The SQI bit and the interrupt is cleared when

this register is read. Regardless of whether interrupts are enabled or disabled, the SQI bit retains its event capture function.

TEST FEATURES DESCRIPTION

The E1PM may be placed into a tri-state test mode in which all of the E1PM outputs, including the data bus, are held in a high impedance state. The E1PM tri-state mode is active while RDB, WRB and CSB are held low (normally an illegal combination of input states).

Test mode registers are used to apply test vectors during production test of the E1PM. Test mode registers (as opposed to normal mode registers) are selected when TRSB is low.

Test mode 0 provides access to the values on the E1PM's primary inputs and control of the primary outputs. Test mode 0 can be used to facilitate board level testing. Test modes other than those described in this section are reserved for production test to verify the internal circuitry of the device.

For further information on testability features, refer to the PMC "Telecom System Block User's Manual".

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Register 01H: Test Mode Select

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	W	DBCTRL
Bit 2	W	IOTST
Bit 1	W	HIZDATA
Bit 0	W	HIZIO

This register is used to select E1PM test features. All bits are reset to zero by a hardware reset of the E1PM; a software reset of either PM in the E1PM does not affect the state of the bits in this register.

The IOTST bit is used to allow normal microprocessor access to the test registers in each block in the E1PM. When IOTST is a logic 1, all blocks are held in test mode (i.e. the TSTB line to each block is asserted internally) and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the chip (refer to the section "Test Mode 0" for details). When IOTST is a logic 0, the timing and signals associated with test mode 0 are not compatible with normal microprocessor bus cycles.

The HIZIO and HIZDATA bits control the tri-state modes of the E1PM. While the HIZIO bit is a logic 1, all output pins in the E1PM are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. These bits may be used to facilitate board level testing.

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the E1PM to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads during production test.

Test Mode 0

In test mode 0, the E1PM allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

To enable test mode 0, the TSTB and TRSB inputs must be set low (the IOTST bit in the Test Mode Select Register may be set to logic 1 in lieu of the TSTB line being asserted) and the following addresses must be written with 00H: 05H, 09H, 11H, 15H, 21H, 23H, 25H, 27H, 29H, 45H, 49H, 51H, 55H, 61H, 63H, 65H, 67H, 69H.

Reading the following address locations returns the values for the indicated inputs :

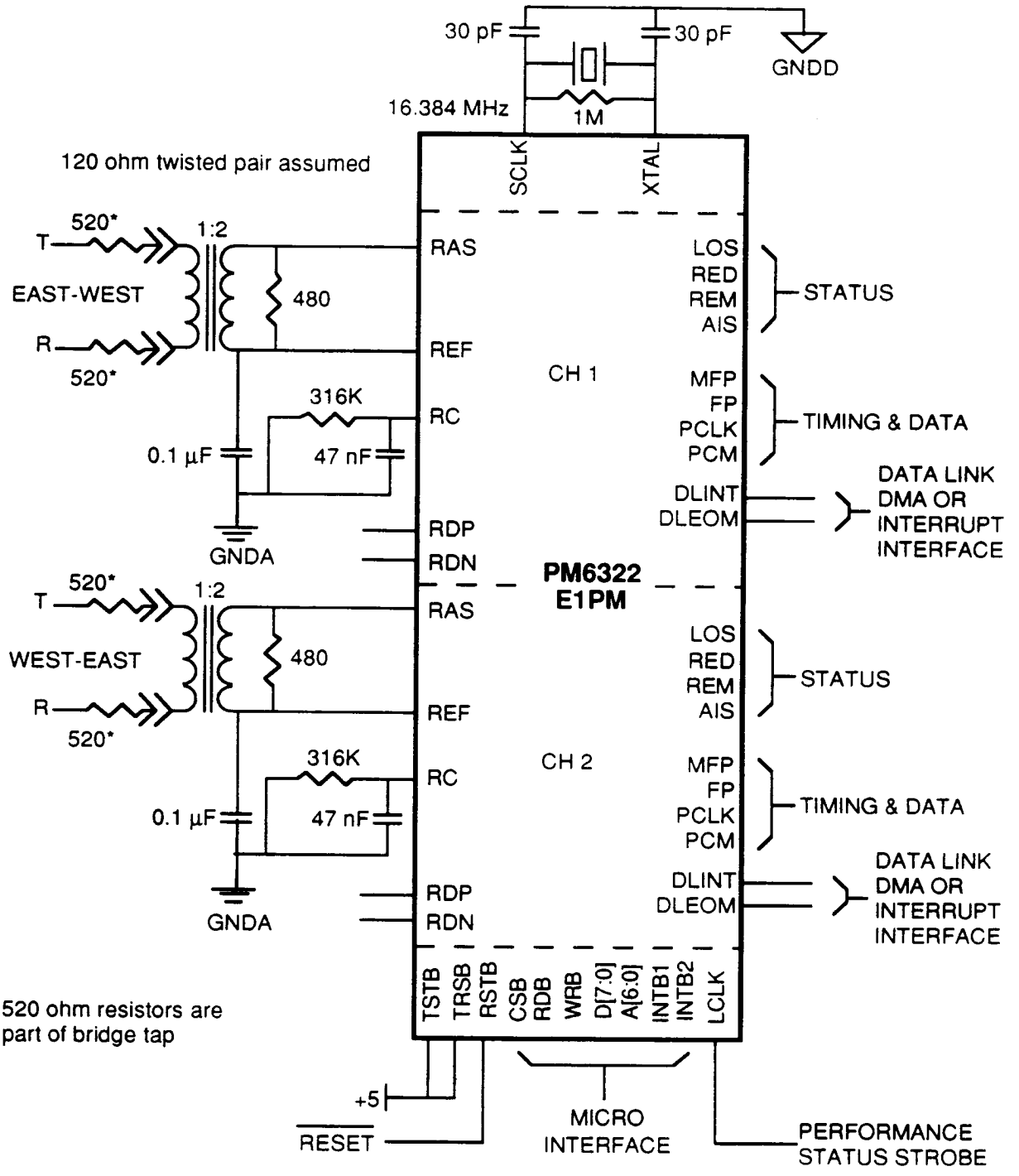
PM-1	PM-2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08H	48H				LCLK				
1CH	5CH					RDP	RDN		SCLK

Writing following address ations forces the outputs to the value in the corresp ng bit position:

PM-1	PM-2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04H	44H							DLEOM	DLINT
08H	48H								PMONI†
10H	50H					FP		MFP	
16H	56H	REM							
17H	57H				RED	AIS	DLSIG	DLCLK	FRMRI†
1CH	5CH		CDRCI†			LOS		PCM	PCLK
20H	60H		RBOCI†						
22H	62H					PDVDI†			
26H	66H								RSLCI†

†Note: the active high block interrupt lines (PMONI, CDRCI, FRMRI, RBOCI, PDVDI and RSLCI) may be masked by the Master Interrupt Enable Register and thus not assert the active low INTB output. Any of the unmasked block interrupt signals can assert the INTB output.

TYPICAL APPLICATION



FUNCTIONAL TIMING

Clock and Data Recovery

Fig. 6 Clock Recovery

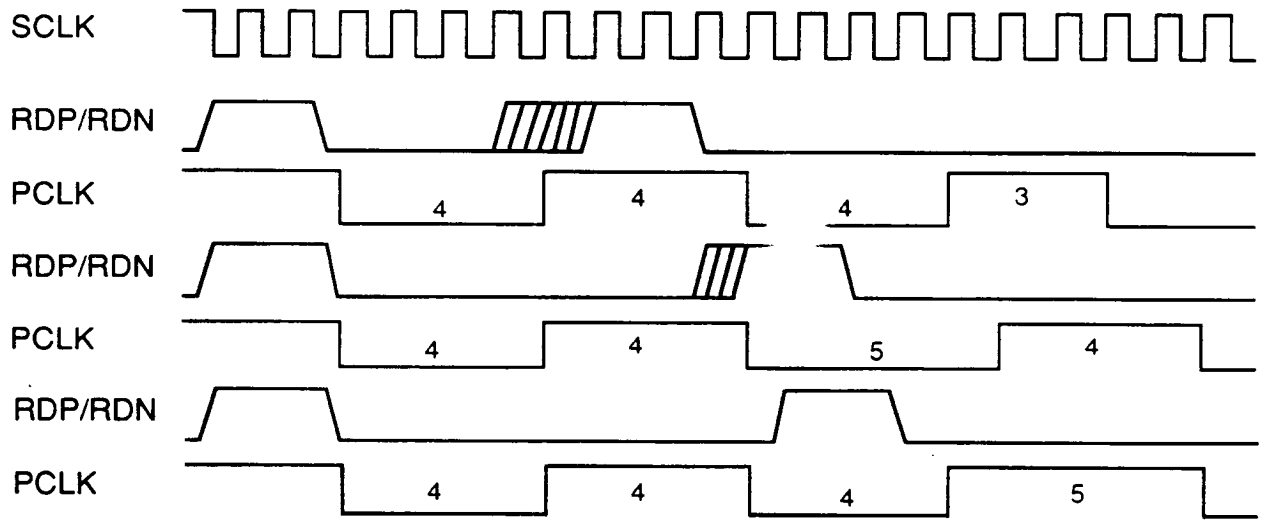


Figure 6 shows the recovery of the PCM clock, PCLK, by the CDRC block. The nominal period of PCLK is 8 SCLK cycles but the period may be from 7 to 9 SCLK cycles. The early arrival of an RDP/RDN pulse causes the instantaneous frequency of PCLK to increase as shown in the first PCLK trace (note that PCLK may be high for three SCLK cycles but it may not be for three SCLK cycles). The late arrival of an RDP/RDN pulse causes the instantaneous frequency of PCLK to decrease as shown in the second and third PCLK trace (note that PCLK may be either high or low for five SCLK cycles).

Frame Alignment

Fig. 7 Frame Alignment with Either Multiframe

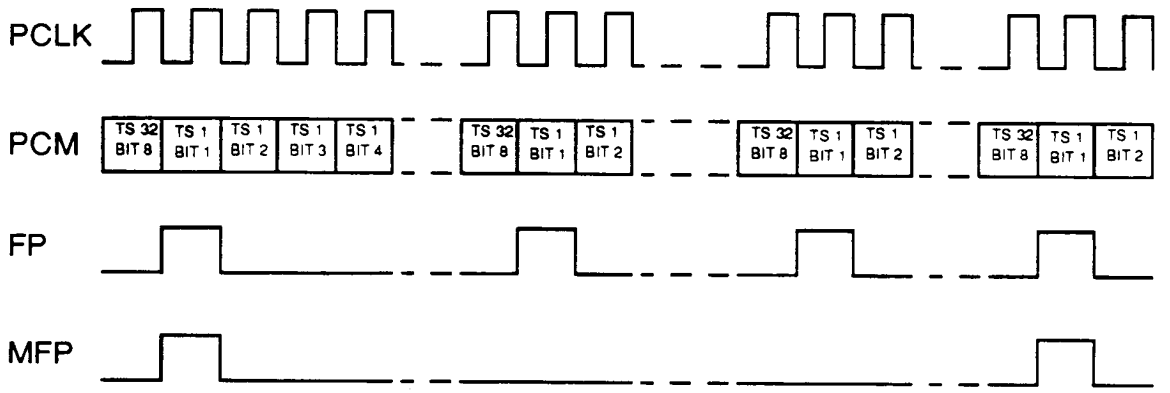


Figure 7 shows the relationship between the PCM clock (PCLK), the PCM data (PCM) and the framing pulses (FP and MFP) for the case where either multiframe is being indicated on MFP. For the case where CRC multiframe is being indicated, the MFP pulse occurs every sixteen frames (during the first bit of frame one) marking the first frame of the CRC multiframe. For the case where CAS multiframe is being indicated, the MFP pulse occurs every sixteen frames (during the first bit of frame one) marking the first frame of the CAS multiframe.

Fig. 8 Frame Alignment with Both Multiframes

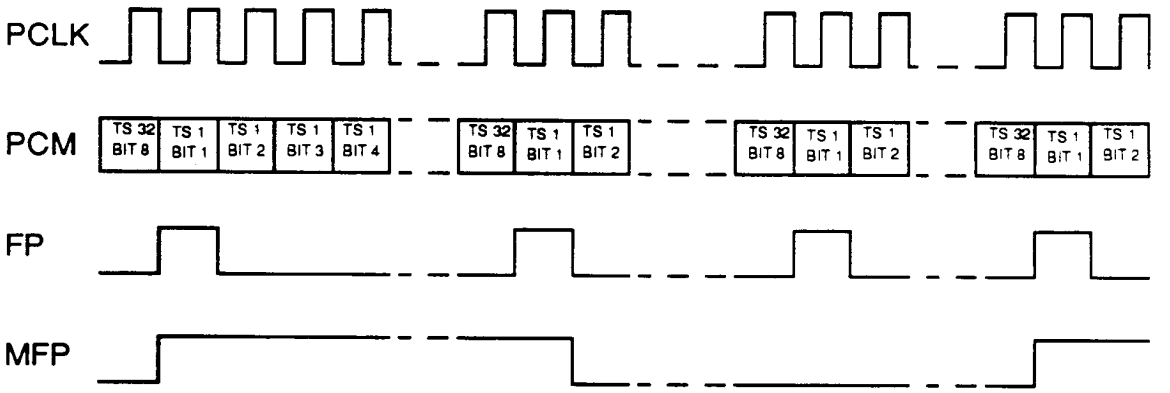


Figure 8 shows the relationship between the PCM clock (PCLK), the PCM data (PCM) and the framing pulses (FP and MFP) for the case where both multiframes are being indicated on MFP. The MFP output goes high coincident with FP to mark the first frame of the sixteen frame CAS multiframe. The MFP output goes low coincident with FP to mark the first frame of the sixteen frame CRC multiframe. The two multiframes may have any one of sixteen phase relationships to each other.

Note that if the two multiframes happen to be coincident, then the MFP output will pulse high for a single bit period marking the beginning of both multiframes.

Remote Alarm

Fig. 9 Remote Alarm Assertion

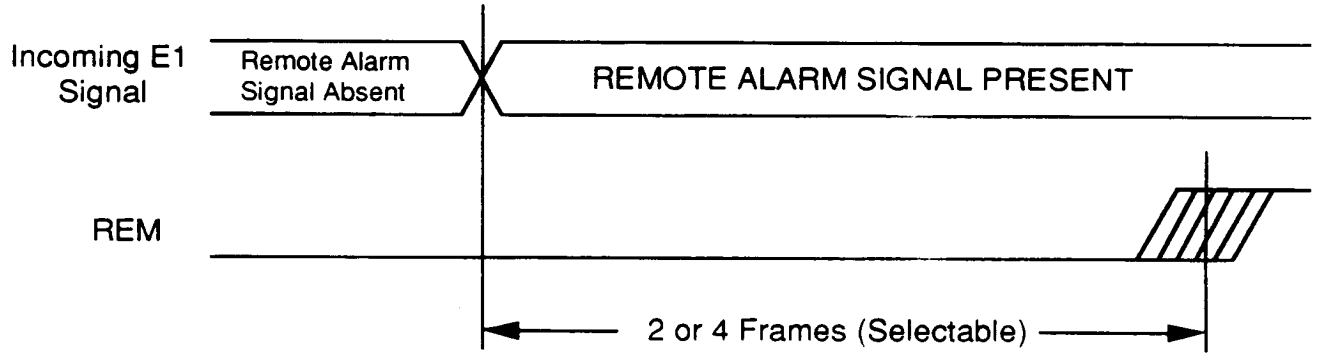


Figure 9 illustrates the assertion of the REM output following the detection of an incoming Remote Alarm signal.

Fig. 10 Remote Alarm Deassertion

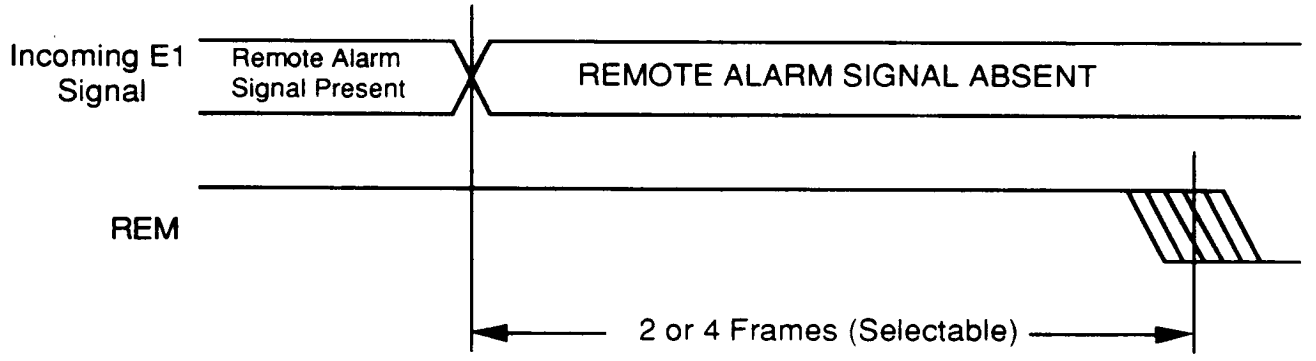


Figure 10 illustrates the deassertion of the REM output following the detection of the lack of the Remote Alarm signal in the input data data stream.

Red Alarm

Fig. 11 Red Alarm Assertion

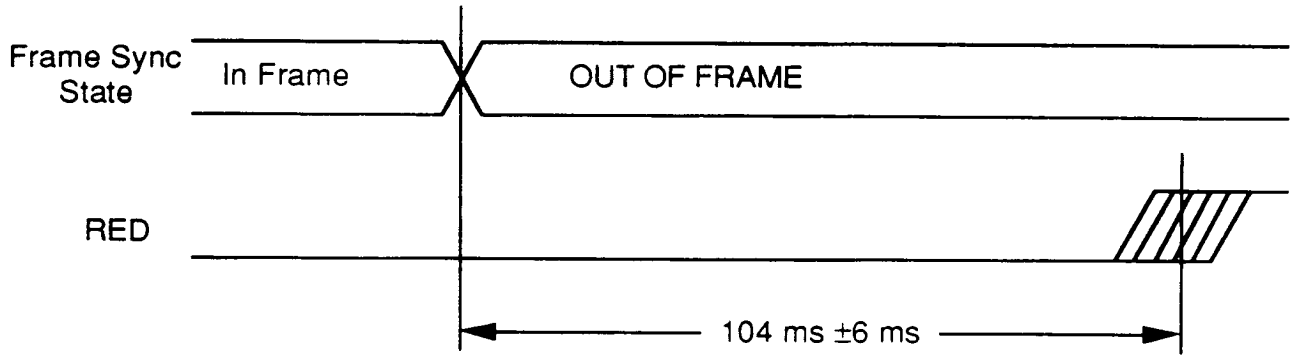


Figure 11 shows the assertion of the RED output following the out-of-frame.

Fig. 12 Red Alarm Deassertion

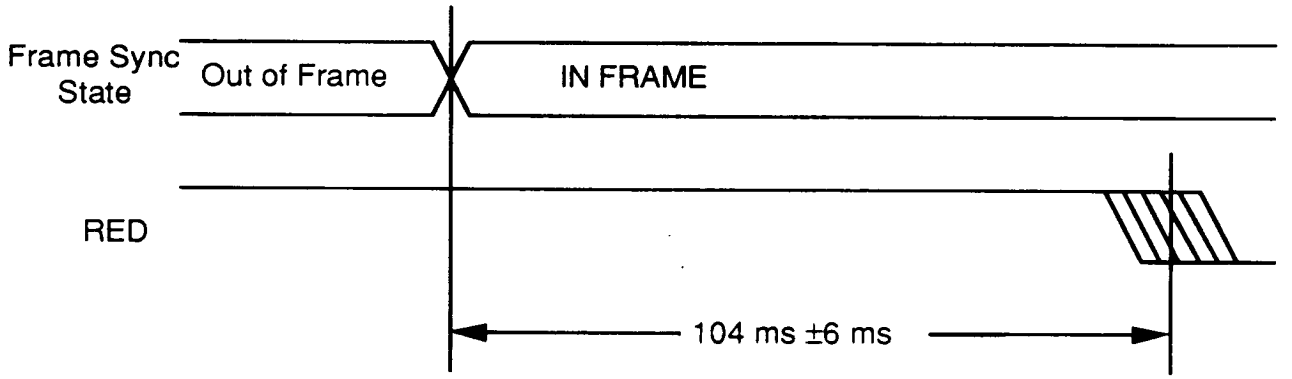


Figure 12 shows the deassertion of the RED output following frame synchronization.

Alarm Indication Signal

Fig. 13 AIS Assertion

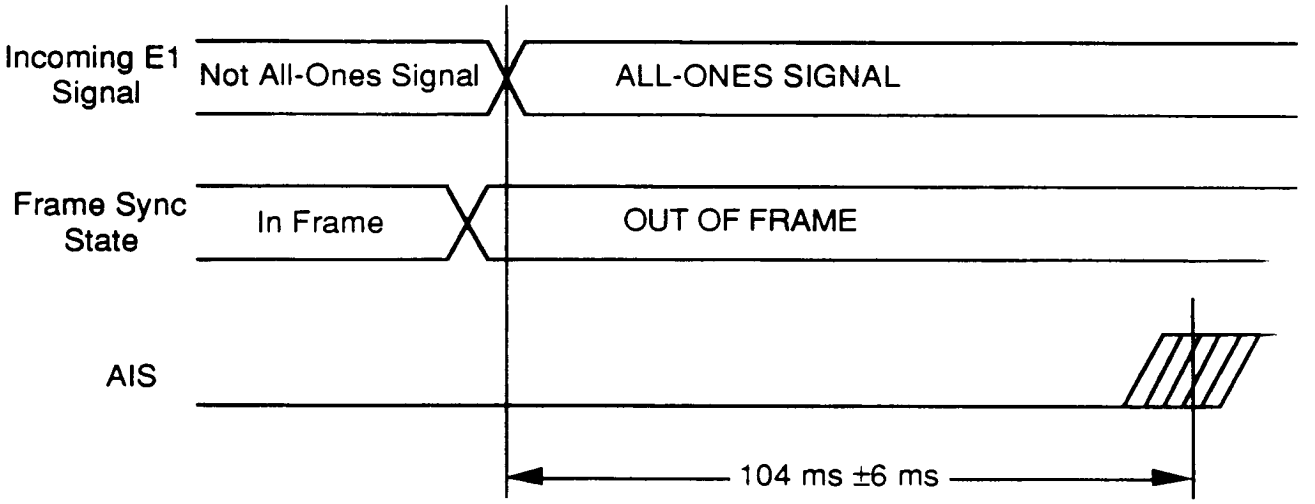


Figure 13 shows the assertion of the AIS output following the out-of-frame synchronization and the detection of the all-ones signal on the input.

Fig. 14 AIS Deassertion (Frame Synchronization)

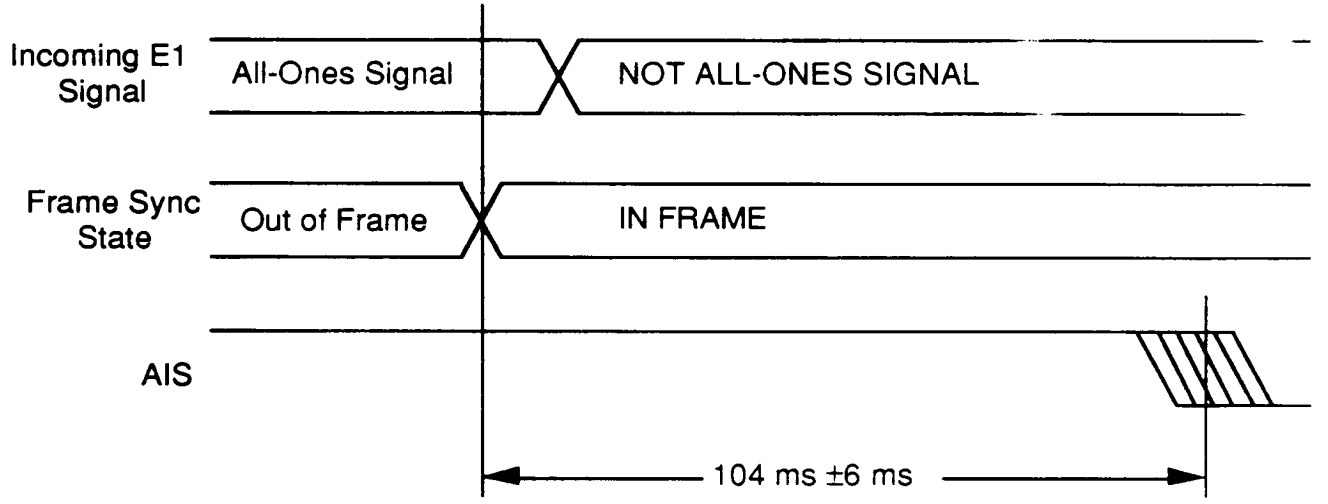


Figure 14 shows the deassertion of the AIS output following frame synchronization.

Fig. 15 AIS Deassertion (All-Ones Signal)

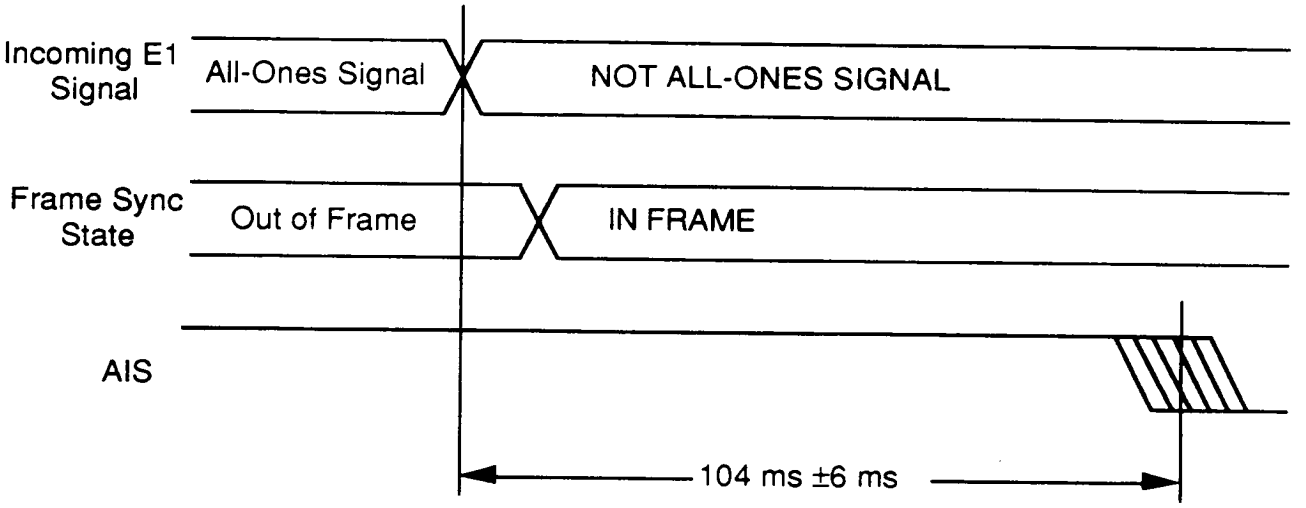
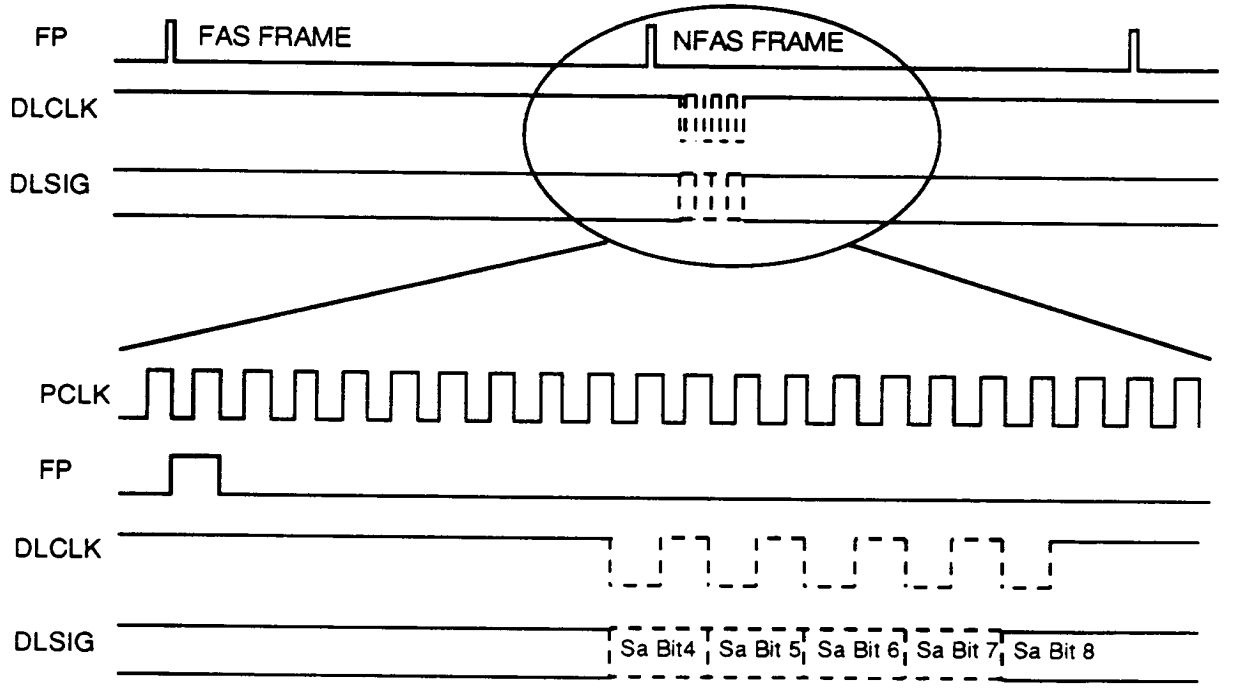


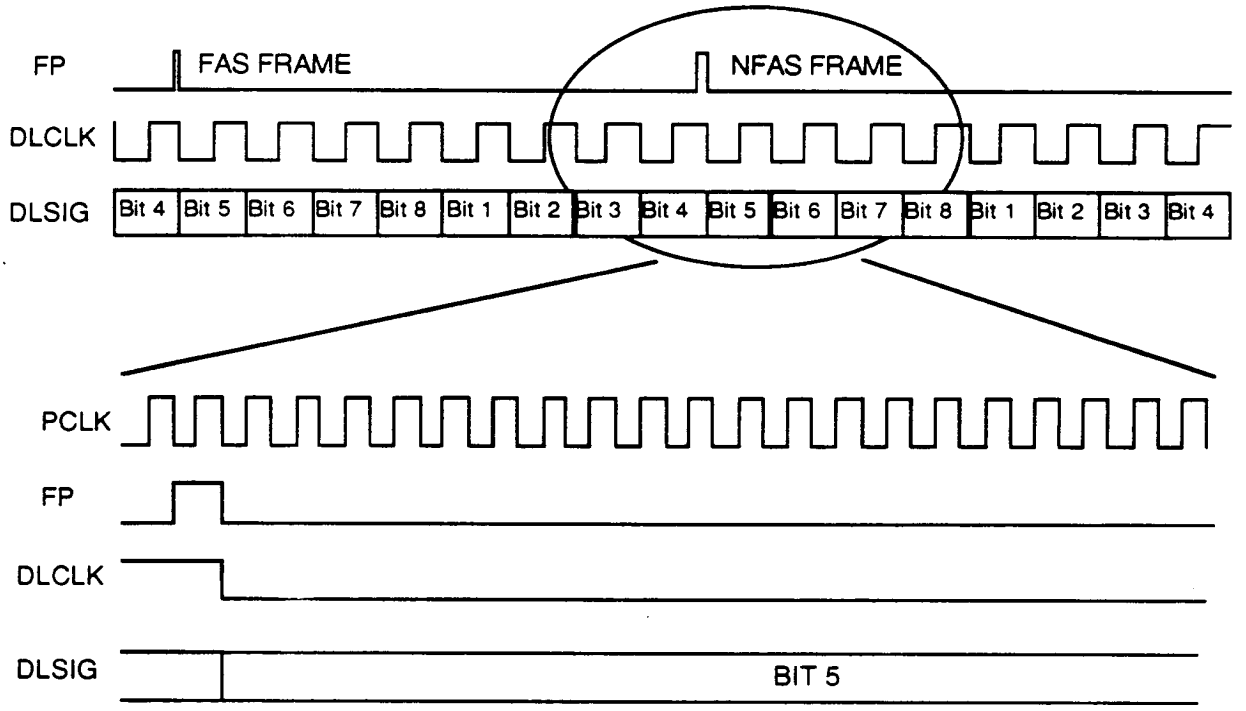
Figure 15 shows the deassertion of the AIS output after the all-ones signal has not existed on the input data.

Fig. 16 National Bit Data Link Extraction



The National Bit Data Link Extraction timing diagram (Fig. 16) shows the relationship between the E1 frame, and the national bits extracted during each NFAS frame. The DLCLK signal is a gapped 1.024 MHz clock which can pulse between 1 and 5 times every 250 µsec as illustrated. The DLSIG signal contains the extracted national bits as determined by the value in the DLEX Data Link Extract Options Register. When the performance monitor is out of frame, the DLSIG output is forced to all ones.

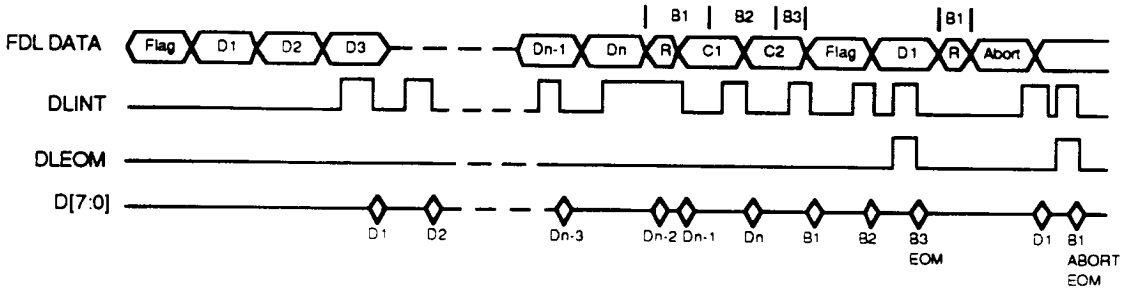
Fig. 17 Timeslot 16 Data Link Extraction



The Timeslot 16 Data Link Extraction timing diagram (Fig. 17) shows the relationship between the E1 frame, and the timeslot 16 bits extracted during each frame. The DLCLK signal is a 64 kHz clock. The DLSIG signal contains the timeslot 16 data when enabled via the DLEX Data Link Extract Options Register. When the performance monitor is out of frame, the DLSIG output is forced to all ones.

HDLC Interface

Fig. 18 Normal Data and Abort Sequence



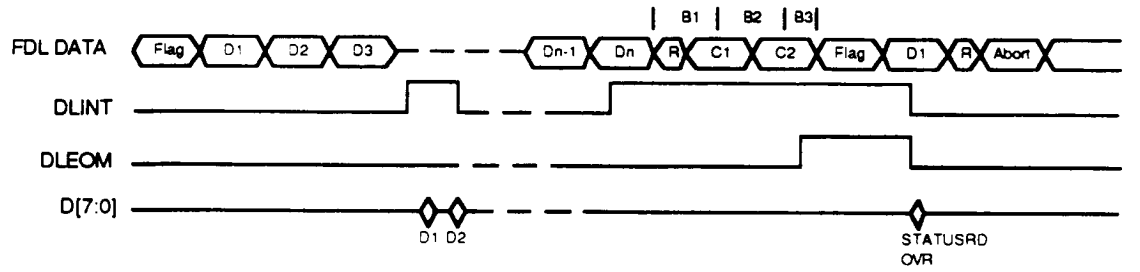
The Normal Data and Abort Sequence timing diagram (Fig. 18) shows the relationship between the facility data link and the DLINT and DLEOM outputs for the case where interrupts are programmed to occur when one byte is present in the FIFO. The RFDL block is assumed to be operating in the interrupt driven mode. Each read shown is composed of two reads, first a read of the RFDL Receive Data Register followed by a read of the RFDL Status Register. The data register reads clear the DLINT output if no more data exists in the FIFO. The state of the FE bit returned from the status register indicates the FIFO fill status as well. The data register read Dn-2 is shown to occur after two bytes have been written into the FIFO. The DLINT output is not cleared after the first data read because a data byte still remains to be read. The DLINT output is cleared after data register read Dn-1. The FE bit will be 0 in status register read Dn-2 and 1 in status register read Dn-1.

The DLEOM signal is asserted as soon as the last byte in the frame is read from the RFDL Receive Data Register. The DLINT output is cleared if the FIFO is empty. The following status register read returns EOM = 1, FLG = 1 and causes the DLEOM output to return to zero.

In the next frame, the first data byte is received and after a delay of 10 bit periods, it is written to the FIFO. After the interrupt the byte is read by the processor. When the ABORT sequence is detected, the data received up to the abort is written to the FIFO and an interrupt generated. The processor then reads the partial byte from the received data register and the DLEOM output is asserted. The processor then reads the status register which returns EOM = 1, FLG = 0 and clears the DLEOM output. The FIFO is not cleared when an abort is detected. All bytes received up to the abort are available to be read.

After an abort, the RFDL state machine is in the receiving all ones state and the data link is in the inactive state. When the first flag is detected, a new interrupt is generated with a dummy data byte loaded into the FIFO to indicate that the data link is active.

Fig. 19 FIFO Overrun



The FIFO Overrun timing diagram (Fig. 19) shows the relationship between the facility data link and the DLINT and DLEOM outputs for the case where interrupts are programmed to occur when two data bytes are present in the FIFO. Each read is composed of two reads as described above. In this example, data is not read by the end of B2. An overrun occurs since unread data (Dn-3) has been overwritten by B1. This sets DLEOM high and resets both the RFDL and FIFO. The RFDL is held disabled until the RFDL Status Register is read. The start flag sequence is not detected since the RFDL is still disabled when it occurs. Consequently, the RFDL ignores the entire frame including the abort sequence (since it did not occur in a valid frame nor during flag reception according to the RFDL).

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +85°C
Storage Temperature	-40°C to +125°C
Voltage on V_{DD} with Respect to GND	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to +6.0V
Static Discharge Voltage	2000 V
Latch-Up Current (T_A = 0°C to +85°C)	400 mA

CAPACITANCE

Symbol	Parameter	Min	Max	Unit	Conditions
CIN	Input Capacitance		10	pF	T_A = 25°C, f = 1 MHz (sampled only)
COUT	Output Capacitance		10	pF	T_A = 25°C, f = 1 MHz (sampled only)
CIO	Bidirectional Capacitance		10	pF	T_A = 25°C, f = 1 MHz (sampled only)

DC CHARACTERISTICS

(T_A = 0°C to +85°C, V_{DD} = 5 V ±10%)

Symbol	Parameter	Min	Max	Unit	Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	2.0	V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
V_{RAS}	Analog Input Voltage	A_{VS} - 0.6	A_{VD} + 0.6	Volts	
V_{REF}	Analog Reference Voltage	1.5	1.9	Volts	REF Unloaded
V_{OL}	Output or Bidirectional Low Voltage		0.4	Volts	V_{DD} = min, I_{OL} = -4 mA for Data Bus Pins and 2 mA for others, Note 3
V_{OH}	Output or Bidirectional High Voltage	2.4		Volts	V_{DD} = min, I_{OL} = 4 mA for Data Bus Pins and 2 mA for others, Note 3
V_T	Reset Input High Voltage	2.3	2.8	Volts	
V_{TH}	Reset Input Hysteresis Voltage	0.5	1.2	Volts	
I_{ILPU}	Input Low Current	-26	-110	µA	$V_{IL} \leq 1.65$ V, Notes 1, 3
I_{IHPU}	Input High Current	-26	-110	µA	$V_{IH} \geq 3.85$ V, Notes 1, 3
I_{IL}	Input Low Current	-10	0	µA	$V_{IL} \leq 1.65$ V, Notes 2, 3
I_{IH}	Input High Current	-10	10	µA	$V_{IH} \geq 3.85$ V, Notes 2, 3

Symbol	Parameter	Min	Max	Unit	Conditions
I_{DDOP1}	Active Current		27	mA	V_{DD}=5.5V, Outputs Unloaded, Path Monitoring Enabled, Line Monitoring Enabled, at TSB Nominal Operating Frequencies, Note 4
I_{DDOP2}	Active Current		25	mA	V_{DD}=5.5V, Outputs Unloaded, Path Monitoring Disabled, Line Monitoring Enabled, at TSB Nominal Operating Frequencies, Note 4
I_{DDOP3}	Active Current		8	mA	V_{DD}=5.5V, Outputs Unloaded, Path and Line Monitoring Disabled, at TSB Nominal Operating Frequencies, Note 4
I_{DDSB}	Idle Current		100	µA	V_{DD}=5.5 V, A_{VD}=0 V, Outputs Unloaded, Device Unclocked
I_{ADOP}	Active Current		27	mA	A_{VD}=5.5 V, V_{DD}=5.5V, Outputs Unloaded, All Ones Signal
I_{ADSB}	Idle Current		24	mA	A_{VD}=5.5 V, V_{DD}=5.5 V, Outputs Unloaded, Device Unclocked

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistors.
2. Input pin or bidirectional pin without internal pull-up resistors
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. I_{DDOP} can increase by 1 mA maximum with external crystal.

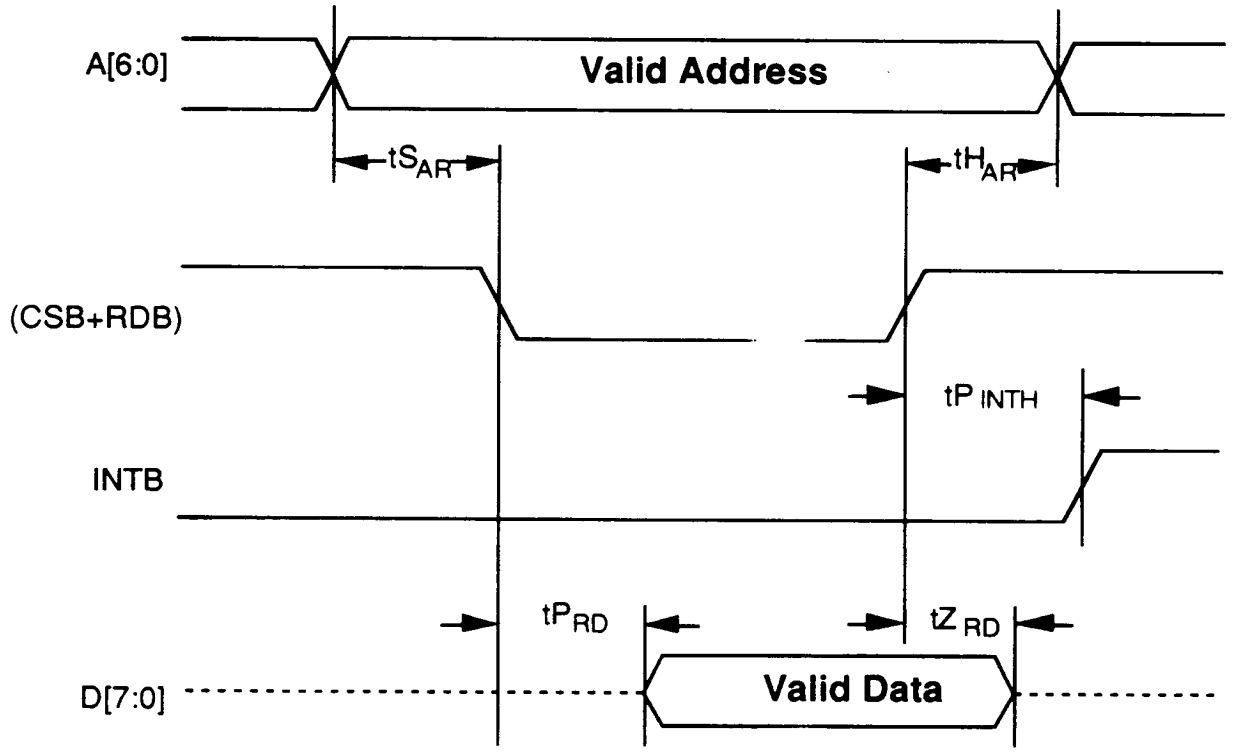
MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = 0°C to +85°C, V_{DD} = 5 V ±10%)

Microprocessor Read Access (Fig. 20)

Symbol	Parameter Min	Max	Units	
tS_{AR}	Address to Valid Read Set-up Time	20		ns
tH_{AR}	Address to Valid Read Hold Time	20		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		100	ns
tZ_{RD}	Valid Read Deasserted to Output Tri-state		40	ns
tP_{INTH}	Valid Read Deasserted to Interrupt Deasserted		100	ns

Fig. 20 Microprocessor Read Access Timing



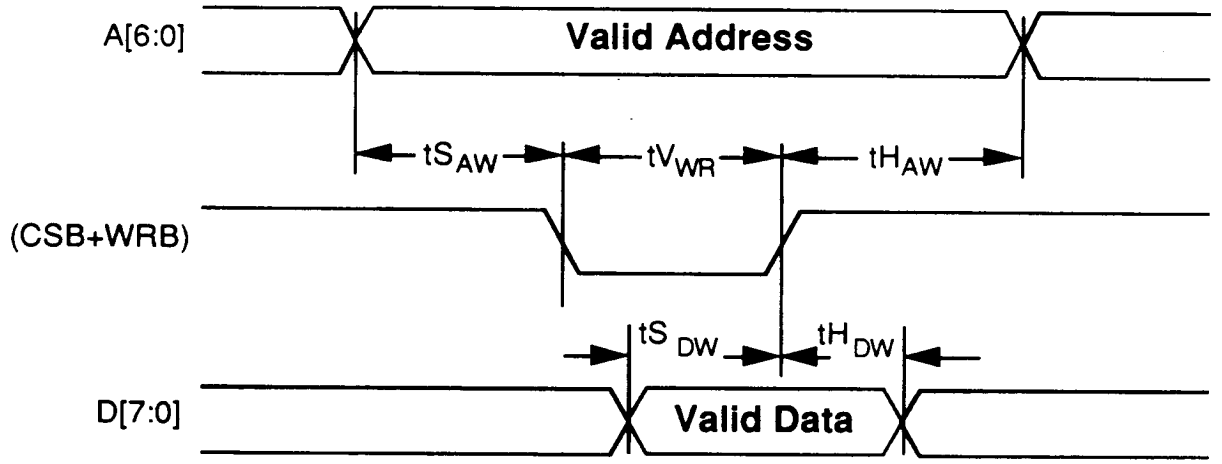
Notes on Microprocessor Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays are measured with a 50 pF load on the microprocessor data bus, (D[7:0]).
3. A valid read cycle is defined as the logical OR of the CSB and the RDB signals.
4. Microprocessor timing applies to normal mode register accesses only.

Microprocessor Write Access (Fig. 21)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	20		ns
tS_{DW}	Data to Valid Write Set-up Time	40		ns
tH_{DW}	Data to Valid Write Hold Time	40		ns
tH_{AW}	Address to Valid Write Hold Time	20		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Fig. 21 Microprocessor Write Access Timing



Notes on Microprocessor Write Timing:

1. A valid write cycle is defined as the logical OR of the CSB and the WRB signals.
2. Microprocessor timing applies to normal mode register accesses only.

E1PM TIMING CHARACTERISTICS

(T_A = 0° to +85°C, V_{DD} = 5 V ±10%)

Input Timing (Fig. 22, 23 & 24)

Symbol	Description	Min	Max	Units
	SCLK frequency (typically 16.384 MHz)	16.382	16.386	MHz
	SCLK duty cycle	30	70	%
tP_{AIN}	RAS analog input pulse width	226	305	ns
tP_{DIN}	RDP/RDN digital input pulse width	80		ns
	RDN frequency (Unipolar mode only)	2.047	2.2	MHz
	RDN duty cycle (Unipolar mode only)	30	70	%
tS_{RDP}	RDP to RDN Set-up Time (Unipolar mode only)	40		ns
tH_{RDP}	RDP to RDN Hold Time (Unipolar mode only)	40		ns

Fig. 22 Analog Input Timing

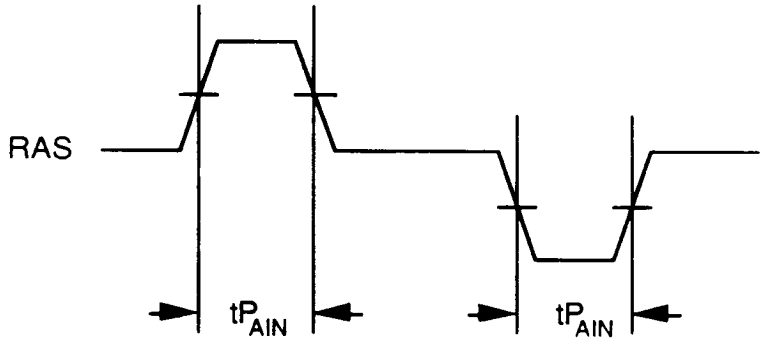


Fig. 23 Digital Input Timing

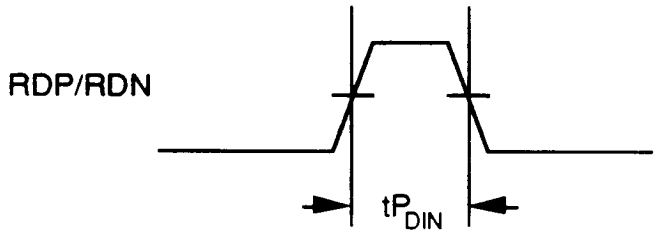
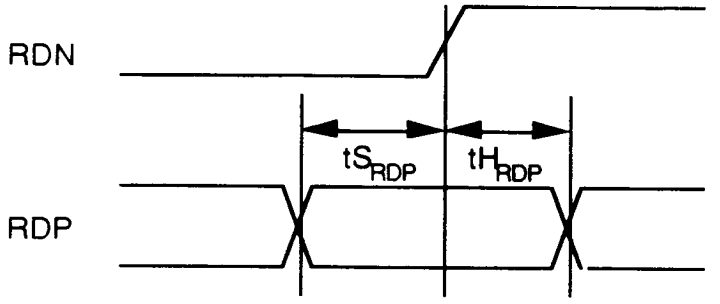


Fig. 24 Unipolar Input Timing



Output Timing (Fig. 25, 26, 27, 28 & 29)

Symbol	Description	Min	Max	Units
tP_{PCLK}	PCLK propagation delay		60	ns
tP_{PCM}	PCM propagation delay		25	ns
tP_{FP}	FP propagation delay		60	ns
tP_{MFP}	MFP propagation delay		60	ns
tP_{RED}	RED propagation delay		70	ns
tP_{REM}	REM propagation delay		70	ns
tP_{AIS}	AIS propagation delay		70	ns
tP_{INTB}	INTB propagation delay		100	ns
tP_{DLSIG}	DLSIG propagation delay		30	ns
tP_{DLINT}	DLINT assertion propagation delay		100	ns
tP_{DLINTL}	DLINT negation from RDB assertion		70	ns
tP_{DLEOM}	DLEOM assertion from PCLK delay		70	ns
tP_{DLEOMH}	DLEOM assertion (Data Register read)		70	ns
$tP_{RHDLEOM}$	DLEOM negation (Status Register read)		45	ns
$tP_{RLDLEOM}$	DLEOM negation (OVR Status Register read)		70	ns

Fig. 25 SCLK Timing

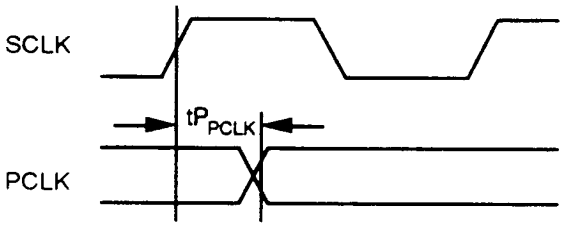


Fig. 26 PCLK Timing

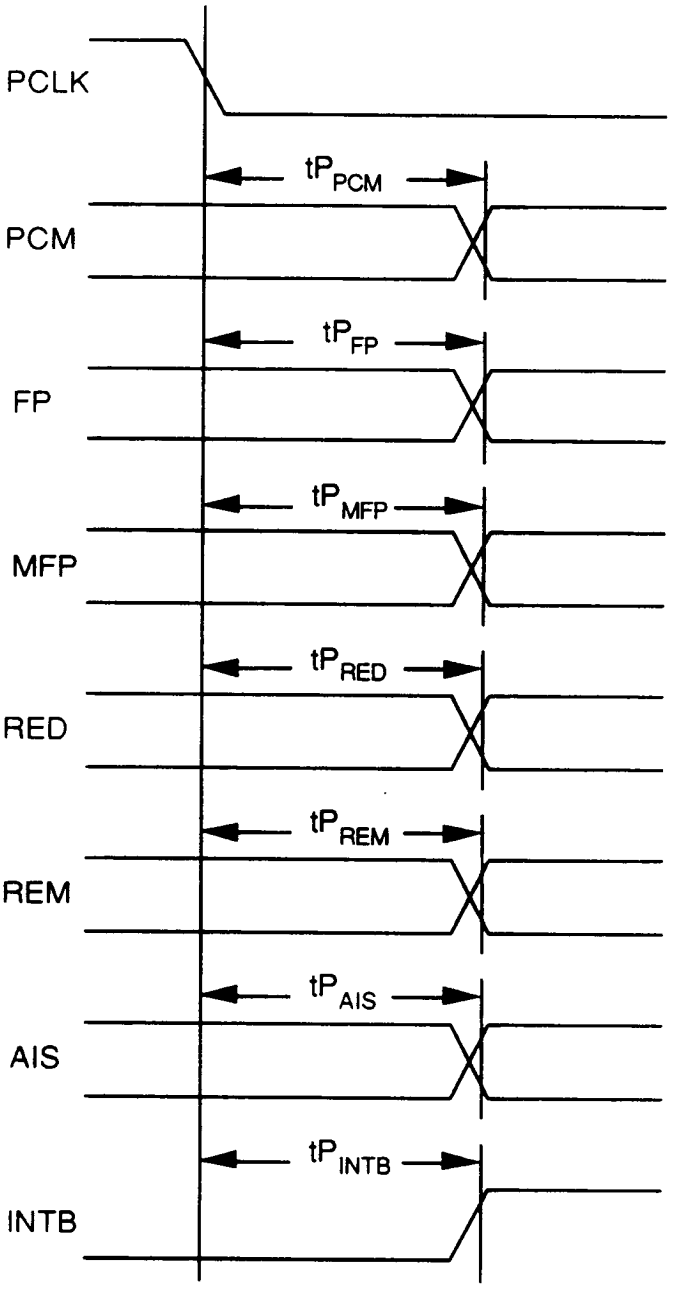


Fig. 27 Data Link Clock and Signal Timing

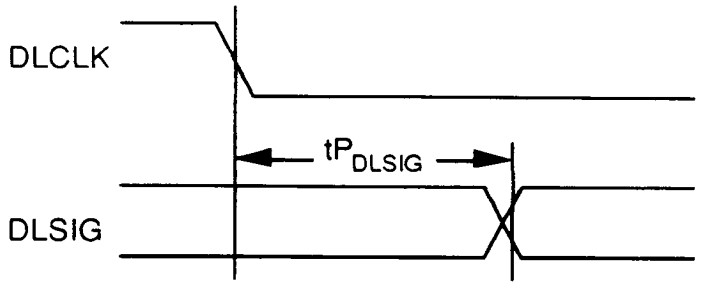


Fig. 28 HDLC Receiver PCLK Associated Timing

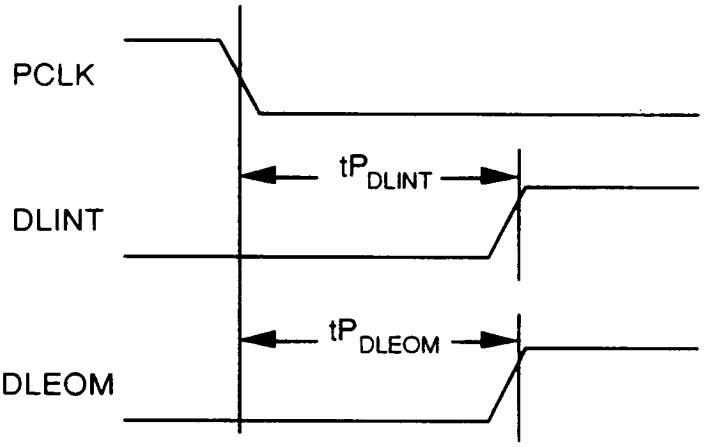
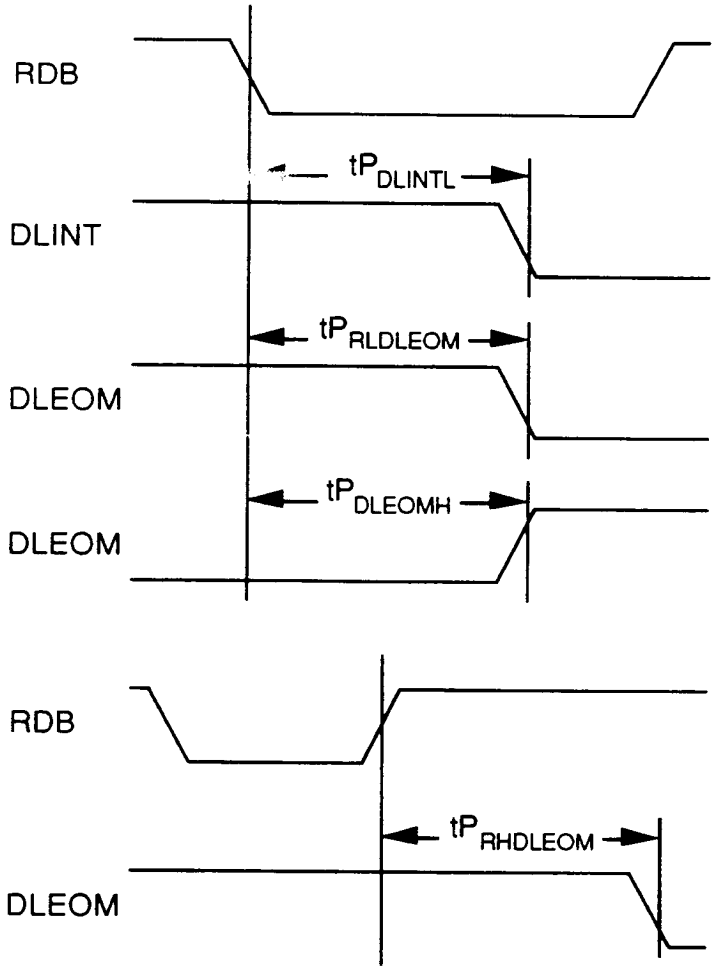


Fig. 29 HDLC Receiver RDB Associated Timing



Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays are measured with a 50 pF load on the outputs.

NOTES

910507P2 ref 910506P3 Issue date: August, 1991.

Printed in Canada