

PRELIMINARY

INS8048/8049/8048L/8049L/8048I/8049I NS87P50/8050U/8040U/87P50U/8050UI/8050UL Microcomputer/Microprocessor Family

General Description

The members of this family of microcomputers are self-contained, 8-bit parallel, 40-pin dual-in-line devices fabricated using National Semiconductor's scaled N-channel, silicon gate MOS process, XMOSTM. The 48-Series devices contain the system timing, control logic, ROM (where applicable) program memory, RAM data memory and 27 I/O lines necessary to implement dedicated control functions. All 48-Series devices are pin-compatible, differing only in the size of on-board ROM (where applicable) and RAM as shown below.

For applications requiring microwire serial communication, the NS8050U provides this feature.

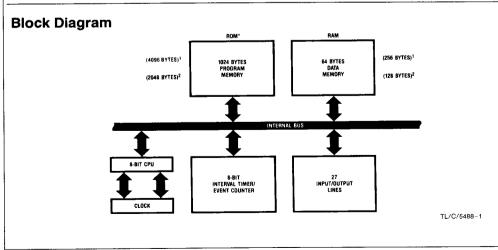
MICROWIRE/PLUSTM consists basically of a three-wire communication port with a clocked 8-bit shift register. The three lines consist of a Serial Output (SO), a Serial Input (SL), and a Serial Clock (SK). The shift register is referred to as the serial input/output register. One 8050U must be designated as the master. The master supplies the clock for the MICROWIRE/PLUS system and initiates all data transfers. All transfers are between the master and one or more slaves. A slave may be any MICROWIRE™ peripheral or another 8050U with MICROWIRE/PLUS. MICROWIRE/ PLUS communicates with a variety of MICROWIRE peripherals, such as the COP472 LCD Display Driver, COP494 EEPROM, or other 8050's configured as a peripheral. MICROWIRE/PLUS makes efficient use of the I/O lines. Thus, the MICROWIRE/PLUS expands the capability of the 3050U family.

*Supersedes all data sheets and data books.

Features

- The master/slave feature is programmable
- NS87P50 MICROWIRE/PLUS Piggy-back Microcomputer
- NS8040U MICROWIRE/PLUS ROM-less
- NS8050U MICROWIRE/PLUS in 40-pin package
- Transparent enhancement to the standard 8050 Microcomputer
- Ready interface to the MICROWIRE peripheral family
- Testable shifter "Done" flag available
- Selectable shift rate
- Two new MICROWIRE/PLUS control instructions
- Serial data exchange with only three wires
- 8-bit timer/control
- Binary and BCD arithmetic
- Single 5V power supply
- Low standby power
- Low voltage standby
- Expandable memory and I/O
- 1.36 µs cycle, 11 MHz clock

Device	RAM Array	ROM Array
INS8048, 48L, 48I	64 x 8	1k x 8
INS8049, 49L, 48I	128 x 8	2k x 8
NS8050U, 50UL, 50UI	256 x 8	4k x8
INS8035, 35L, 35I	64 x 8	N/A
INS8039, 39L, 39I	128 x 8	N/A
NS8040U, 40UL, 40UI	256 x 8	N/A
NS87P50U	64/128/256 x 8	1k/2k/4k x 8



Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

87P50 Series	1
8048 Series	8048I Series
8048L Series	-
-20°C to +85°C	-50°C to +100°C
-65°C to +150°C	-65°C to +150°C
$-0.5V \text{ to } \pm 7V$	-0.5V to +7V

Temperature Under Bias
Storage Temperature
All Input or Output Voltages with Respect to V_{SS}
Power Dissipation

Power Dissipation 1.5W 1.5W

Note: Absolute Maximum Ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

	Features	INS8048 Series	INS8048L Series	INS8048i Series	NS87P50 Series
■ -40	to +85°C Operation			Х	
■ 8-Bit	CPU, RAM, ROM, I/O in a Single Package	х	x	X	
■ 2.5 μ	s Cycle, 6 MHz Clock; 1.36 μs Cycle, 11 MHz Clock	х	x	x	Х
■ Very	Low Power, High Speed Operation		х		
■ On-C	thip Oscillator Circuit and Clock (or External Source)	Х	х	×	Х
27 1/0	O Lines	х	x	×	Х
■ Expa	ndable Memory and I/O	х	x	×	Х
■ 8-Bit	Timer/Counter	х	х	×	Х
■ Single	e-Level Interrupt	Х	×	×	Х
■ 96 In:	structions (Most Single-Byte)	Х	х	×	х
■ Binar	y and BCD Arithmetic	Х	×	×	Х
■ Single	e + 5V Power Supply	X	x	×	Х
■ Low 9	Standby Power Mode	X	X	х	Х
■ Low\	Voltage Standby	2.2V Min	2.2V Min	2.2V Min	2.6V Min

INS8048/INS8049/INS8048L/INS8049L/INS8048I/INS8049I/NS8050U/NS 8040U/NS87P50U/NS8050UL/NS8050UI/NS87P50

DC Electrical Characteristics

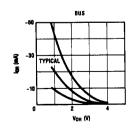
 $T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{CC} = +5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise specified. (NS8048, INS8048L)

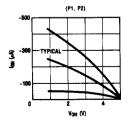
 $T_A = 40$ °C to +85°C, $V_{CC} = +5V \pm 10$ %, $V_{SS} = 0$ V, unless otherwise specified. (NS8048I) (Note 2)

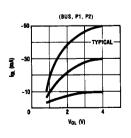
Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
V _{IL}	Input Low Voltage (Except XTAL1, XTAL2, RESET)		-0.5		0.8	٧
V _{IL1}	Input Low Voltage (XTAL1, XTAL2, RESET)		-0.5		0.6	V
V _{IH}	Input High Voltage (Except XTAL1, XTAL2, RESET)		2.0		Vcc	V
V _{IH1}	Input High Voltage (XTAL1, XTAL2, RESET)		3.8		Vcc	٧
V _{OL}	Output Low Voltage (Bus)	I _{OL} = 2 mA			0.45	V
V _{OL1}	Output Low Voltage (RD, WR, PSEN, ALE)	I _{OL} = 1.8 mA			0.45	٧
V _{OL2}	Output Low Voltage (PROG)	I _{OL} = 1.0 mA			0.45	٧
V _{OL3}	Output Low Voltage (Ports and Others)	I _{OL} = 1.6 mA			0.45	٧
V _{OH}	Output High Voltage (Bus)	I _{OH} = -400 μA	2.4			٧
V _{OH1}	Output High Voltage (RD, WR, PSEN, ALE)	$I_{OH} = -100 \mu\text{A}$	2.4			٧
V _{OH2}	Output High Voltage (Ports and Others)	$I_{OH} = -40 \mu\text{A}$	2.4			٧
l _{Ll}	Input Leakage Current (T1, INT, EA)	V _{SS} ≤ V _{IN} ≤ V _{CC}			±10	μА
I _{LI1}	Input Leakage Current Ports	$V_{SS} + 0.45 \le V_{IN} \le V_{CC}$			-500	μΑ
I _{Li2}	Input Leakage Current (SS, RESET)	$V_{SS} + 0.45 \le V_{IN} \le V_{CC}$			-300	μΑ
lLO	Output Leakage Current (Bus, T ₀) High Impedance State	V _{SS} + 0.45 ≤ V _{IN} ≤ V _{CC}			± 10	μΑ
I _{DD} 64	Standby Current (Note 1)	8048, 8048I, 8048L			5/4	mA
I _{DD} 128	Standby Current (Note 1)	8049, 8049I, 8049L			7/5	mA
I _{DD} 256	Standby Current (Note 1)	8050, 8050I, 8050L			10/10	mA
I _{DD} + I _{CC}	Total Supply (Note 1)	8048, 8048I, 8048L			65/55	mA
I _{DD} + I _{CC}	Total Supply (Note 1)	8049, 8049I, 8049L			70/60	mA
I _{DD} + I _{CC}	Total Supply (Note 1)	8050, 8050I, 8050L			80/65	mA
V _{DD}	Standby Power Supply (8048, 8048I, 8048L Series)		2.2		Vcc	v

Note 1: For industrial device $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

Note 2: Combination of low power and industrial temperature devices not accepted.







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Symbol	Parameter	f(t _{CY})	11 MHz		Unit	
Эушьог	Parameter	(Note 3)	Min	Max	Office	
t _{LL}	ALE Pulse Width (Note 1)	7/30 t _{CY} - 170	150		ns	
t _{AL}	Address Setup to ALE (Note 1)	2/15 t _{CY} - 110	70		ns	
t _{LA}	Address Hold from ALE (Note 1)	1/15 t _{CY} - 40	50		ns	
t _{CC1}	Control Pulse Width (RD, WR) (Note 1)	1/2 t _{CY} - 200	480		ns	
t _{CC2}	Control Pulse Width (PSEN) (Note 1)	2/5 t _{CY} - 200	350		ns	
t _{DW}	Data Setup Before WR (Note 1)	13/30 t _{CY} - 200	390		ns	
t _{WD}	Data Hold After WR (Notes 1, 2)	1/15 t _{CY} - 50	40		ns	
t _{DR}	Data Hold (RD, PSEN) (Notes 1, 4)	1/10 t _{CY} - 30	0	110	ns	
t _{RD1}	RD to Data in (Note 1)	2/5 t _{CY} - 170		370	ns	
t _{RD2}	PSEN to Data in (Note 1)	3/10 t _{CY} - 170		240	ns	
t _{AW}	Address Setup to WR (Note 1)	1/3 t _{CY} - 150	300		ns	
t _{AD1}	Address Setup to Data (RD) (Note 1)	21/30 t _{CY} - 220		730	ns	
t _{AD2}	Address Setup to Data (PSEN) (Note 1)	1/2 t _{CY} - 200		480	ns	
tAFC1	Address Float to RD, WR (Notes 1, 2)	2/15 t _{CY} - 40	140		ns	
t _{AFC2}	Address Float to PSEN (Notes 1, 2)	1/30 t _{CY} - 40	10		ns	
tLAFC1	ALE to Control (RD, WR) (Note 1)	1/5 t _{CY} - 75	200		ns	
tLAFC2	ALE to Control (PSEN) (Note 1)	1/10 t _{CY} - 75	60		ns	
t _{CA1}	Control to ALE (RD, WR, PROG) (Note 1)	1/15 t _{CY} - 40	50		ns	
t _{CA2}	Control to ALE (PSEN) (Note 1)	4/15 t _{CY} - 40	320		ns	
t _{CP}	Port Control Setup to PROG (Note 1)	1/10 t _{CY} -80	50		ns	
t _{PC}	Port Control Hold from PROG (Note 1)	4/15 t _{CY} - 260	100		ns	
t _{PR}	PROG to P2 Input Valid (Note 1)	17/30 t _{CY} - 140		630	ns	
tpF	Input Data Hold from PROG (Notes 1, 4)	1/10 t _{CY}	0	140	ns	
t _{DP}	Output Data Setup (Note 1)	2/5 t _{CY} - 290	260		ns	
t _{PD}	Output Data Hold (Note 1)	1/10 t _{CY} - 90	40		ns	
tpp	PROG Pulse Width (Note 1)	7/10 t _{CY} - 250	700		ns	
t _{PL}	Port 2 I/O Setup to ALE (Note 1)	4/15 t _{CY} - 200	160		ns	
t _{LP}	Port 2 I/O Hold to ALE (Note 1)	1/10 t _{CY} - 120	15		ns	
tpv	Port Output From ALE (Note 1)	3/10 t _{CY} + 100		510	ns	
tcy	Cycle Time (Note 3)		1.36	15	μs	
toprr	T ₀ Rep Rate	3/15 t _{CY}	270		ns	

Note 1: Control outputs $C_L = 80$ pF, Bus outputs $C_L = 150$ pF.

Note 2: Bus High Impedance Load = 20 pF.

Note 3: t_{CY} = 15/f (assumes 50% duty cycle).

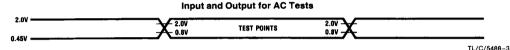
Note 4: Maximum spec listed is for user information only to prevent system bus contention.

Note 5: $V_{IH} = 3.8V$, $V_{IL} = 0.45V$.

AC Electrical Characteristics for NS8050U/NS8040U

Symbol	Parameter	f(t _{CY})	11 !	Units	
Symbol	Parameter	t _{CY} = 1.36 μs	Min Typ		Office
tc ÷ 1	Divide by One SK	tcy	1360	1360	ns
tc ÷ 4	Divide by Four SK	4 t _{CY}	5440	5440	ns
t _{setup}	SI Setup to SK ↑		200	140	ns
t _{hold}	SI Hold from SK ↑		100	50	ns
t _{valid} ÷ 1	SO Valid Setup to Next SK ↑	½ t _{CY} - 180	500	650	ns *
t _{valid} ÷ 4	SO Valid Setup to Next SK ↑	½ t _{CY} 180	1860	2000	ns

Note: Absolute Maximum Ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics. DC Electrical Characteristics are specified in INS8048-Series Data Sheet.



Note: AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Output timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0" (except X1, X2, and RESET) (Note 5).

The INS8048/49/50-Series

The devices are designed to be efficient controllers. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory is derived from an instruction set comprised predominantly of single bytes. The remaining instructions are two bytes in length. Additional external memory may be added up to a maximum of 4k bytes of program memory and 256 bytes of data memory without paging.

The INS8048L/49L/50L-Series

The XMOS 8048L Family now makes it possible for the designers to significantly reduce their power supply requirements. This will allow new designs where low power operation is a requirement for portability or battery back-up. The

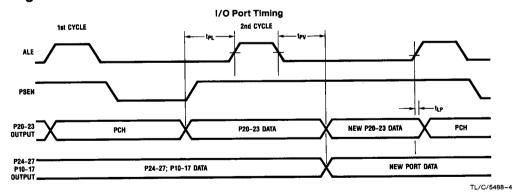
8048 Low Power Family will also mean longer product life and reliability because of the reduction in chip temperature within the package.

Due to the capabilities of the XMOS process and improvements in circuit design, the 8048L devices consume approximately 25% les than normal N-channel MOS devices available to the marketplace.

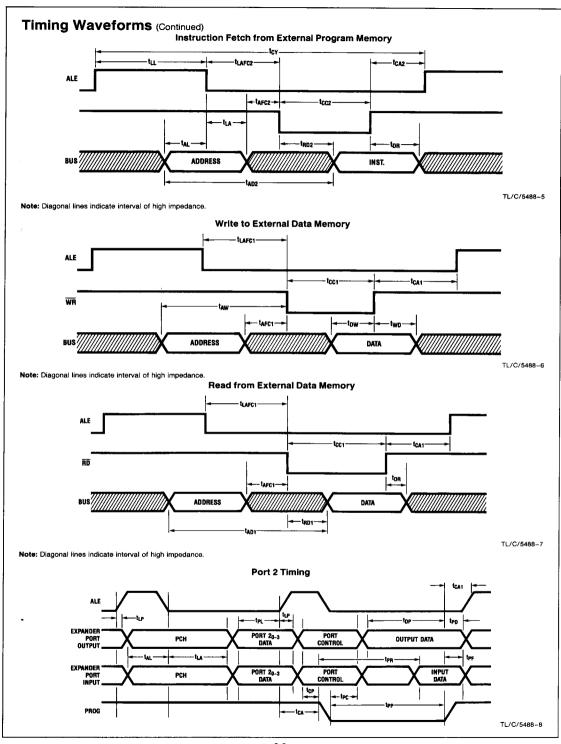
The INS8048I/49I/50I-Series

These devices are designed to be efficient controllers in extended temperature range environments (-40° C to $+85^{\circ}$ C). Similar in every way to the standard devices, the industrial parts are differentiated only by extensive testing and screening to guarantee full functionality in the extended industrial temperature range.

Timing Waveforms

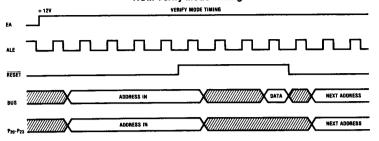


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ROM Verify Mode Timing

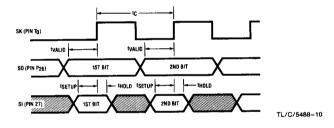


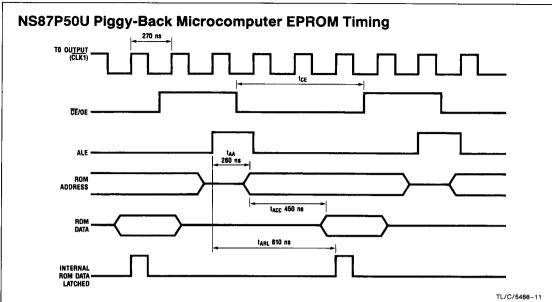
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Recommended Test Methods:

- 1. RESET must be low before EA goes high.
- 2. Sync to falling edge of ALE. Falling edge of ALE is machine cycle 4.
- 3. Force address in with RESET low for 21 machine cycles starting machine cycle 5.
- 4. Force address in with RESET high for 4 machine cycles.
- 5. Force RESET high for 12 machine cycles.
- 6. Force RESET high for 4 machine cycles. Data is valid on bus.
- 7. Force RESET low for 4 machine cycles.
- 8. Repeat steps 3 through 7 for other addresses.

NS8050U MICROWIRE/PLUS Timing





Frequency = 11 MHz

AC Electrical Characteristics

 $T_A = 0$ °C to +70°C, $V_{CC} = +5V \pm 10$ %, $V_{SS} = 0$ V, $V_{DD} = 3.6$ V to 5.5V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
tACC	ROM Address Setup to ROM Data (6 MHz Access Time)	6 MHz			850	ns
tACC	ROM Address Setup to ROM Data (11 MHz Access Time)	11 MHz			450	ns
t _{CE}	Chip Enable and Output Enable Active	11 MHz			870	ns
t _{AA}	ALE to ROM Address Setup	11 MHz			260	ns
tarl	ALE to ROM Data Latch	11 MHz			810	ns

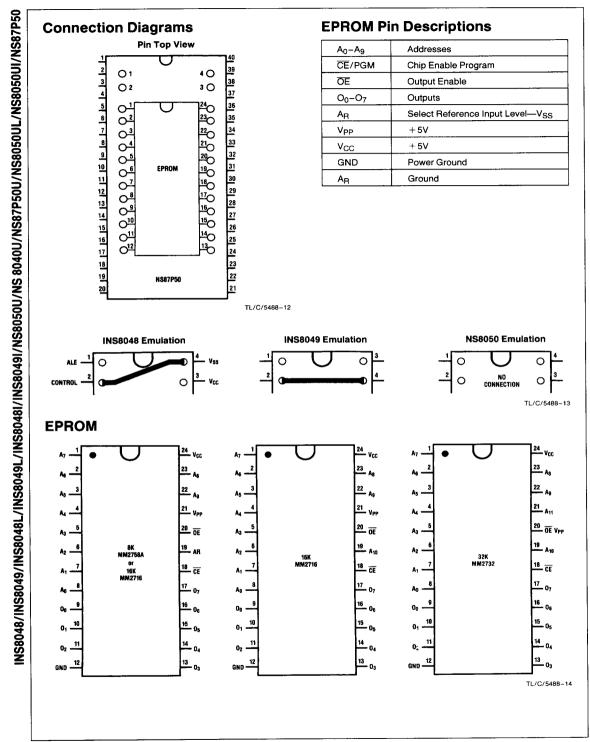
Other AC Electrical Characteristics same as 48-Series.

DC Electrical Characteristics

 T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ±10%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
I _{CC1}	Current Available to EPROM	V _{CC} = 5V			150	mA
lpp	V _{PP} Current	V _{PP} = 5V			5	mA
I _{DD}	256 Words on Standby Current				20	mA
IDD + ICC	Total Supply Current (without EPROM)	T _A = 25°C All Outputs Open		60	100	mA
V _{DD}	Standby Power Supply		2.6		Vcc	V

Other DC Electrical Characteristics same as 48-Series.



Functional Pin Descriptions

INPUT SIGNALS

Reset (RESET): An active low (0) input that initializes the processor and is used to verify program memory.

Single Step (SS): Active low (0) input which, in conjunction with ALE, can single step the processor through each instruction.

External Access (EA): An active high (1) input that forces all program memory fetches to reference external program memory.

Testable Input 0 (T0): Testable input pin using conditional branch functions JT0 (T0 = 1) or JNT0 (T0 = 0). T0 can be designated as the clock output using instruction ENTO CLK. For NS8050U, T0 is also used as the SK clock output for MASTER and SK clock input for SLAVE in the MICROWIRE/PLUS mode. Done FLIP FLOP is tested by testing T0.

Testable Input 1 (T1): Testable input pin using conditional branch functions JT1 (T1 = 1) or JNT1 (T1 = 0). T1 can be designated as the Timer/Counter input from an external source using instruction STRT CNT.

Interrupt (INT): An active low input that initiates an interrupt when interrupt is enabled. Interrupt is disabled after a RE-SET. Also can be tested with instruction JNI (INT = 0).

OUTPUT SIGNALS

Read Strobe (RD): An active low output strobe activated during a Bus read. Can be used to enable data onto the Bus from an external device. Used as a Read Strobe to External Data Memory.

Write Strobe (\overline{WR}): An active low output strobe activated during a Bus write. Used as a Write Strobe to External Data Memory.

Program Store Enable (PSEN): An active low output that occurs only during an external program memory fetch.

Address Latch Enable (ALE): An active high output that occurs once during each cycle and is useful as a clock output. The negative going edge of ALE strobes the address into External Data or Program Memory.

Program (PROG): This output (active out) provides the output strobe for INS8243 I/O Expander.

INPUT/OUTPUT SIGNALS

Crystal Input (XTAL1, XTAL2): These two pins connect the crystal for internal oscillator operation. XTAL1 is the timing input for external source.

Port 1 (P10-P17): 8-bit quasi-bidirectional port.

Port 2 (P20-P27): 8-bit quasi-bidirectional port. During an external program memory fetch, the 4 high-order program counter bits occur at P20-P23. They also serve as a 4-bit I/O Expander Bus when the INS8243 I/O Expander is used.

Bus (DB₀-DB₇): True bidirectional port, either statically latched or synchronous. Can be written to using WR Strobe, or Read from using RD Strobe. During an External Program Memory fetch, the 8 lower-order program counter bits are present at this port. The addressed instruction appears on this bus when PSEN is low. During an external RAM data transaction, this port presents address and data under control of ALE, RD, WR.

Vss: Processor Ground potential.

V_{DD}: V_{DD} functions as the Low Power Standby Voltage. Can be tied to V_{CC} if power-down operation is not required.

V_{CC} (Pin 40): Primary power source for 48-Series devices.

NS8050U MICROWIRE Mode Pin Descriptions

Pin 1, Serial Clock (SK): Input or output clocking signal to the MICROWIRE/PLUS serial circuitry.

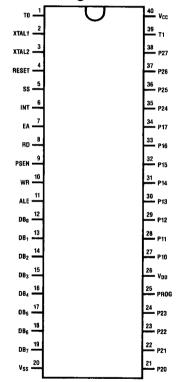
Pin 38, Serial Input (SI): Serial input to the 8-bit MICRO-WIRE/PLUS shift register.

Pin 37, Serial Output (SO): Serial output from the 8-bit MI-CROWIRE/PLUS shift register.

Pin 3, XTAL2: High-impedance input to oscillator circuit.

Pin 2, XTAL1: Low-impedance output from oscillator circuit.

Connection Diagram



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Order Number INS8048, INS8048J, INS8048L, INS8049, INS8049I, INS8049L, NS8040U, NS8050I, NS8050U, NS8050U, NS87P50, NS87P50I and NS87P50U See NS Package Number D40G or N40A

Functional Description

The following paragraphs contain the functional description of the major elements of the 48-Series microcomputer/microprocessor. (Figure 1) is a block diagram of the 48-Series devices. The data paths are illustrated in simplified form

to show how the various logic elements communicate with each other to implement the instruction set common to all devices.

48-Series Block Diagram

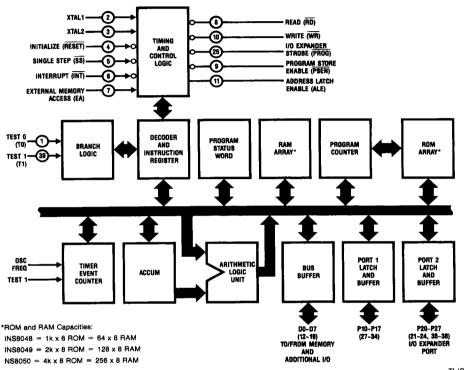


FIGURE 1. 48-Series Detailed Block Diagram

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Functional Description (Continued) PROGRAM MEMORY

The Program Memory (ROM) contained on the INS8048/ 49/50 devices is comprised of 1024, 2048 or 4096 8-bit bytes, respectively. As is seen by examining the 48-Series instruction set, these bytes may be program instructions, program data or ROM addressing data. The ROM for the above devices must be mask programmed at the National Semiconductor factory. The ROMless microcomputers, INS8035, INS8039 and INS8040, use external program memory. This makes program development straightforward using standard UV erasable PROMs to emulate a possible future single chip (using the on-board ROM) system. ROM addressing, up to a maximum of 4k, is accomplished by a 12-bit Program Counter (PC). The INS8048 and INS8049 will automatically address external memory when the boundary of their internal memories, 1k and 2k respectively, are exceeded. The binary value of the address selects one of the 8-bit bytes contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential binary count value.

With reference to the Program Memory Map (see Figure 2) there are three ROM addresses which provide for the control of the microcomputer.

- Memory Location 0000—Asserting the RESET (negative true) input to the microcomputer forces the first instruction to be fetched from address 0000.
- Memory Location 0003—Asserting the interrupt (negative true) input to the microcomputer (when interrupt is enabled) forces a jump to subroutine.
- Memory Location 0007—A Timer/Counter interrupt that results from Timer/Counter overfow (when enabled) forcing a jump to subroutine.

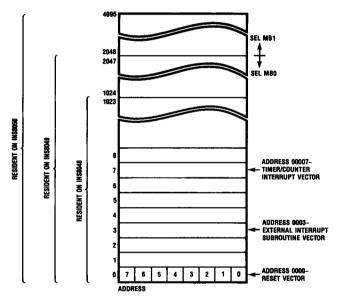


FIGURE 2. INS8048/49/50 Resident ROM Program Memory Map

TL/C/5488-17

Functional Decscription (Continued)

DATA MEMORY (RAM)

The resident RAM data memory is arranged as 64 (INS8035/8048), 128 (INS8039/8049), or 256 (NS8040/8050) bytes. RAM addressing is implemented indirectly via either of two 8-bit RAM pointer registers R0 and R1. These pointer registers are essentially the first two locations in the RAM (see *Figure 3*), addressing 00 and 01. RAM addressing may also be performed directly by 11 direct register instructions. The register area of the RAM array is made up of eight working registers that occupy either the first bank (0), locations 0 to 7, or the second bank (1), locations 24 to 31. The second bank of working registers is selected by using the Register Bank Switch instruction (SEL RB). If this bank is not used for working registers, it can be used as user RAM.

There is an 8-level stack after Bank 0 that occupies address locations 8 to 23. These RAM locations are addressed indirectly through R0, R1 or the 3-bit Stack Pointer (SP). The stack pointer keeps track of the return address and pushes each return address down into the stack. There are 8 levels of subroutine nesting possible in the stack because each address occupies 10 bits or more using two bytes in RAM. When the level of subroutine nesting is less than 8, the stacks not used may be utilized as user RAM locations.

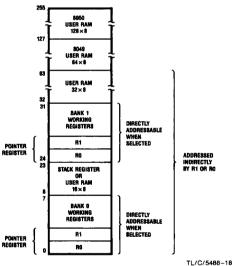


FIGURE 3. 8048-Series Resident RAM Data Memory Map

INPUT/OUTPUT

The 48-series devices have 27 lines of input/output organized as three 8-bit ports plus three test inputs. The three ports may be used as inputs, outputs or bidirectional ports. Ports 1 and 2 differ from Port 3 (Bus Port) in that they are quasi-bidirectional ports. Ports 1 and 2 can be used as input and output while being statically latched. If more I/O lines are required, Port 2 can also serve as a 4-bit I/O bus expander when used in conjunction with the INS8243 I/O Expander.

The bus port is a true bidirectional port and is either statically latched or synchronous. It can be written to using WR strobe or read from using RD strobe. During an external program memory fetch, the 8 lower-order program counter bits are present at this port. The addressed instruction appears on this bus when PSEN is low. During an external RAM data transaction, this port presents address and data under control of ALE, RD, and WR.

POWER-DOWN MODE

During the power-down mode, V_{DD} , which normally maintains the RAM cells, is the only pin that receives power. V_{CC} , which serves the CPU and ports, is dropped from a voltage of nominal 5 to 0 after the CPU is reset, so that the RAM cells are unaltered by the loss of power. When power is restored, the processor goes through the normal power-on procedure.

MICROWIRE FUNCTIONS

New functions applicable to microwire mode are as follows: The SK output frequency is selected by writing into the P27 latch as follows:

- 0 = Instruction Cycle Divided by 1
- 1 = Instruction Cycle Divided by 4

The SO output is enabled or disabled by writing into the P26 latch as follows:

- 0 = Enabled
- 1 = Disabled

The DONE flip-flop is tested with the JT0, JNT0 instructions.

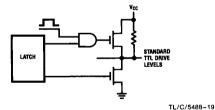


FIGURE 4. Ports 1 and 2 Input/Output Circuit

Instruction Set

Table I details the 96 instructions common to both the microcomputers and the microprocessors. The table provides the mnemonic, function, and description, instruction code, number of cycles and, where applicable, flag settings.

Managania	Eurotion	Description	Cvcles	Bytes		Fla	gs	
Mnemonic	Function	Description	Cycles	bytes	С	AC	F0	F1
CONTROL								
ENI		Enable the External Interrupt Input.	1	1				
DIS I		Disable the External Interrupt Input.	1	1				
ENTO CLK		Enable T0 as the Clock Output.	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0-2047) of Program Memory.	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048-4095) of Program Memory.	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0-7) of Data Memory.	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24-31) of Data Memory.	1	1				
DATA MOVES								
MOV A, #data	(A) ← data	Move Immediate the specified data into the Accumulator.	2	2				
MOV A, Rr	(A) ← (Rr); r = 0-7	Move the contents of the designated register into the Accumulator.	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0-1	Move Indirect the contents of data memory location into the Accumulator.	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1				
MOV Rr, #data	(Rr) ← data; r = 0-7	Move Immediate the specified data into the designated register.	2	2				
MOV Rr, A	(Rr) ← (A); r = 0-7	Move Accumulator contents into the designated register.	1	1				
MOV @ Rr, A	$((Rr)) \leftarrow (A); r = 0-1$	Move Indirect Accumulator contents into data memory location.	1	1				
MOV @ Rr, #data	((Rr)) ← data; r = 0-7	Move Immediate the specified data into data memory.	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the Program Status Word.	1	1	•	•	•	
MOVP A, @ A	(PC 0-7) ← (A) (A) ← ((PC))	Move the content of program memory location in the current page addressed by the content of Accumulator into the Accumulator.	2	1				
MOVP3 A, @ A	(PC 0-7) ← (A) (PC 8-10) ← 011 (A) ← ((PC))	Move the content of program memory location in page 3 addressed by the content of Accumulator into the Accumulator.	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0-1	Move Indirect the contents of external data memory into the Accumulator.	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0-1	Move Indirect the contents of the Accumulator into external data memory.	2	1				
XCH A, Rr	(A) \longleftrightarrow (Rr); $r = 0-7$	Exchange the Accumulator and designated register's contents.	1	1				
XCH A, @ Rr	(A) \longleftrightarrow ((Rr)); $r = 0-1$	Exchange Indirect contents of Accumulator and location in data memory.	1	1				
XCHD A, @ Rr	(A0−A3) ← (((Rr)) 0−3);	Exchange Indirect 4-bit contents of Accumulator and data memory.	1	1				

			!		I			
Mnemonic	Function	Description	Cycles	Bytes	C	AC	gs F0	F
TIMER COUNTE	ir		l			1 70		<u>. </u>
EN TCNTI		Enable Internal Interrupt Flag for Timer/ Counter output.	1	1				
DIS TONTI		Disable Internal Interrupt Flag for Timer/ Counter output.	1	1				Γ
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/ Counter.	1	1				
STOP TONT		Stop Count for Event Counter.	1	1				
STRT CNT		Start Count for Event Counter.	1	1				Г
STRT T		Start Count for Timer.	1	1				
ACCUMULATOR	?							_
ADD A, #data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	2	2	•	•		
ADD A, Rr	$(A) \leftarrow (A) + (Rr)$ for $r = 0-7$	Add contents of designated register to the Accumulator.	1	1	•	•		
ADD A, @ Rr	$(A) \leftarrow (A) + ((Rr))$ for $r = 0-1$	Add Indirect the contents of data memory location of the Accumulator.	1	1	•	•		
ADDC A, #data	(A) ← (A)(C) + data	Add Immediate with carry the specified data to the Accumulator.	2	2	•	•		
ADDC A, Rr	$(A) \leftarrow (A) + (C) + (Rr)$ for $r = 0-7$	Add with carry the contents of the designated register to the Accumulator.	1	1	•	•		
ADDC A, @ Rr	$(A) \leftarrow (A) + (C) + ((Rr))$ for $r = 0-1$	Add Indirect with carry the contents of data memory location to the Accumulator.	1	1	•	•		
ANL A, #data	(A) ← (A) AND data	Logical AND specified Immediate Data with Accumulator	2	2				
ANL A, Rr	(A) \leftarrow (A) AND (Rr) for $r = 0-7$	Logical AND contents of designated register with Accumulator	1	1				
ANL A, @ Rr	(A) \leftarrow (A) AND ((Rr)) for $r = 0-1$	Logical AND Indirect the contents of data memory with Accumulator.	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	1	1				
CLR A	A ← 0	CLEAR the contents of the Accumulator.	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator.	1	1	•			
DEC A	(A) ← (A) − 1	DECREMENT by 1 the Accumulator's contents.	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the Accumulator's contents.	1	1				
ORL A, #data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator.	2	2				
ORL A, Rr	(A) \leftarrow (A) OR (Rr) for $r = 0-7$	Logical OR contents of designated register with Accumulator.	1	1				
ORL A, @ Rr	(A) \leftarrow (A) OR ((Rr)) for $r = 0-1$	Logical OR Indirect the contents of data memory location with Accumulator.	1	1				

Mnemonic	Function	Description	Cycles	Bytes		Fla	ıgs	
Milelionic	runction	Description	Cycles	Dytes	C	AC	F0	F1
ACCUMULATO	OR (Continued)							
RLA	$(An + 1) \leftarrow (An)$ for $n = 0-6$ $(A0) \leftarrow (A7)$	Rotate Accumulator left by 1-bit without carry.	1	1				
RLC A	$(An + 1) \leftarrow (An); n = 0-6$ $(A0) \leftarrow (C)$ $(C) \leftarrow (A7)$	Rotate Accumulator left by 1-bit through carry.	1	1	•			
RR A	$(An) \leftarrow (An + 1); n = 0-6$ $(A7) \leftarrow (A0)$	Rotate Accumulator right by 1-bit without carry.	1	1				
RRC A	$(An) \leftarrow (An + 1); n + 0-6$ $(A7) \leftarrow (C)$ $(C) \leftarrow (A0)$	Rotate Accumulator right by 1-bit through carry.	1	1	•			
SWAP	(A4−A7) ←→ (A0−A3)	Swap the 2 4-bit nibbles in the Accumulator.	1	1				
XRL A, #data	(A) ← (A) XOR data	Logical XOR Immediate specified data with Accumulator.	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0-7	Logical XOR contents of designated register with Accumulator.	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0-1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1				
BRANCH								
DJNZ Rr, addr	$(Rr) \leftarrow (Rr) -; r = 0-7$ if $(Rr) \neq 0;$ $(PC 0-7) \leftarrow addr$	Decrement the specified register and test contents.	2	2				
JBb addr	$(PC 0-7) \leftarrow \text{addr if Bb} = 1$ $(PC) \leftarrow (PC) + 2 \text{ if BB} = 0$	Jump to specified address if Accumulator bit is set.	2	2				
JC addr	$(PC 0-7) \leftarrow \text{addr if } C = 1$ $(PC) \leftarrow (PC) + 2 \text{ If } C = 0$	Jump to specified address if carry flag is set.	2	2				L
JFO addr	$(PC 0-7) \leftarrow addr if F0 = 1$ $(PC) \leftarrow (PC) + 2 fF0 = 0$	Jump to specified address if Flag F0 is set.	2	2				
JFI addr	$(PC 0-7) \leftarrow \text{addr if } F1 = 1$ $(PC) \leftarrow (PC) + 2 \text{ If } F1 = 0$	Jump to specified address if Flag F1 is set.	2	2				
JMP addr	(PC 8-10) ← 8-10 (PC 0-7) ← addr 0-7 (PC 11) ← DBF	Direct Jump to specified address with the 2k address block.	2	2				
JMPP @ A	(PC 0-7) ← ((A))	Jump Indirect to specified address pointed to by the Accumulator in current page.	2	1				
JNC addr	$(PC 0-7) \leftarrow addr if C = 0$ $(PC) \leftarrow (PC) + 2 if C = 1$	Jump to specified address if carry flag is low.	2	2				
JNI addr	$(PC 0-7) \leftarrow addr if I = 0$ $(PC) \leftarrow (PC) + 2 if I = 1$	Jump to specified address if interrupt is low.	2	2				
JNT0 addr	$(PC 0-7) \leftarrow \text{addr if } T0 = 0$ $(PC) \leftarrow (PC) + 2 \text{ if } T0 = 1$	Jump to specified address if Test 0 is low.	2	2				
JNT1 addr	$(PC 0-7) \leftarrow \text{addr if } T1 = 0$ $(PC) \leftarrow (PC) + 2 \text{ if } T1 = 1$	Jump to specified address if Test 1 is low.	2	2				

INS8048/INS8049/INS8048L/INS8049L/INS8048I/INS8049I/NS8050U/NS 8040U/NS87P50U/NS8050UL/NS8050UI/NS87P50

Mnemonic	Function	Description	0	D		Fla	ıgs	
whemonic	Function	Description	Cycles	Bytes	С	AC	F0	F1
BRANCH (Continu	ued)		•					
JNZ addr	$(PC 0-7) \leftarrow addr \text{ if } A \neq 0$ $(PC) \leftarrow (PC) + 2 \text{ if } A = 0$	Jump to specified address if Accumulator is non-zero.	2	2				
JFT addr	$(PC 0-7) \leftarrow addr \text{ if } TF = 1$ $(PC) \leftarrow (PC) + 2 \text{ if } TF = 0$	Jump to specified address if Timer Flag is set to 1.	2	2				
JT0 addr	$(PC 0-7) \leftarrow \text{addr if } T0 = 1$ $(PC) \leftarrow (PC) + 2 \text{ if } T0 = 0$	Jump to specified address if Test 0 is a 1.	2	2				
JT1 addr	$(PC 0-7) \leftarrow if T1 = 1$ $(PC) \leftarrow (PC) + 2 if T1 = 0$	Jump to specified address if Test 1 is a 1.	2	2				
JZ addr	$(PC 0-7) \leftarrow addr \text{ if } A = 0$ $(PC) \leftarrow (PC) + 1 \text{ if } A = 1$	Jump to specified address if Accumulator is 0.	2	2				
INPUT/OUTPUT								
ANL BUS, #data	(BUS) ← (BUS) AND data	Logical AND Immediate specified data with contents of BUS.	2	2				
ANL Pp, #data	(Pp) ← (Pp) AND data; p = 1-2	Logical AND Immediate specified data with designated port (1 or 2).	2	2				
ANLD Pp, A	(Pp) ← (Pp) AND (A0-A3); p = 4-7	Logical AND contents of Accumulator with designated port (4-7).	2	1				
IN A, Pp	(A) ← (Pp); p = 1-2	Input data from designated port (1-2) into Accumulator.	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	2	1				
MOVD A, Pp	$(A0-A3) \leftarrow (Pp);$ $p = 4-7 (A4-A7) \leftarrow 0$	Move contents of designated port (4-7) into Accumulator.	2	1				
MOVD Pp, A	(Pp) ← (A0-A3); p = 4-7	Move contents of Accumulator to designated port (4-7).	2	1				
ORL BUS, #data	(BUS) ← (BUS) OR data	Logical OR Immediate specified data with contents of BUS.	2	2			·	
ORLD Pp, A	(Pp) ← (Pp) OR (A0-A3); p = 4-7	Logical OR contents of Accumulator with designated port (4-7).	2	1				
ORL Pp, #data	(Pp) ← (Pp) OR data; p = 1-2	Logical OR Immediate specified data with designated port (1-2).	2	2				
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto BUS.	2	1				
OUTL Pp, A	(Pp) ← (A); p = 1-2	Output contents of Accumulator to designated port (1-2).	2	1				
REGISTERS								
DEC Rr	(Rr) ← (Rr) − 1; r = 0−7	Decrement by 1 contents of designated register.	1	1				
INC Rr	(Rr) ← (Rr) + 1; r = 0-7	Increment by 1 contents of designated register.	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0-1	Increment Indirect by 1 the contents of data memory location.	1	1				

TABLE I. Instruction Set (Continued)								
Mnemonic	Function	Description	Cycles	Bytes	Flags			
					С	AC	F0	F1
SUBROUTIN	NË		,					
CALL addr	((SP)) ← (PC) ((SP)) ← (PSW 4-7) (SP) ← (SP) + 1 (PC 8-10) ← addr 8-10 (PC 0-7) ← addr 0-7 (PC 11) ← DBF	Call designated Subroutine.	2	2				
RET	(SP) ← (SP) − 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	2	1				
RETR	(SP) ← (SP) - 1 (PC) ← ((SP)) (PSW 4-7) ← ((SP))	Return from Subroutine restoring Program Status Word.	2	1	•	•		
FLAGS								
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1.	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	1				•
MISCELLAN	IEOUS							
NOP		No operation	1	1				
MICROWIRI	EINSTRUCTIONS							
XCHM	$A \longleftrightarrow SIO$	Reset DONE flip-flop, Clock counter. SK designated as an output. MICROWIRE/PLUS mode selected.						
XCHS	A ←→ SIO	Reset DONE flip-flop, Clock counter. SK designated as an input. MICROWIRE/PLUS mode selected.						

Symbol Definitions

Symbol	Description		
Α	Accumulator		
AC	Auxiliary Carry Flag		
addr	Program Memory Address (12 bits)		
b	Bit Designator (b = 0-7		
BS	Bank Switch		
Bus	Bus Port		
С	Carry Flag		
CLK	Clock Signal		
CNT	Event Counter		
D	Nibble Designator (4 bits)		
data	Number of Expression (8 bits)		
DBF	Memory Bank Flip-Flop		
F ₀ , F ₁	Flags 0, 1		
I	Interrupt		
Р	"In-Page" Operation Designator		

Symbol	Description		
р	Port Designator (p = 1, 2 or 4-7)		
PSW	Program Status Word		
r	Register Designator (r = 0, 1 or 0-7)		
SP	Stack Pointer		
Т	Timer		
TF	Timer Flag		
T0, T1	Testable Flags 0, 1		
Х	External RAM		
#	Prefix for Immediate Data		
@	Prefix for Indirect Address		
\$	Program Counter's Current Value		
(x)	Contents of Register		
((xx))	Contents of Memory Location Addressed by the Contents of Register		
	Replaced by		

Typical Applications

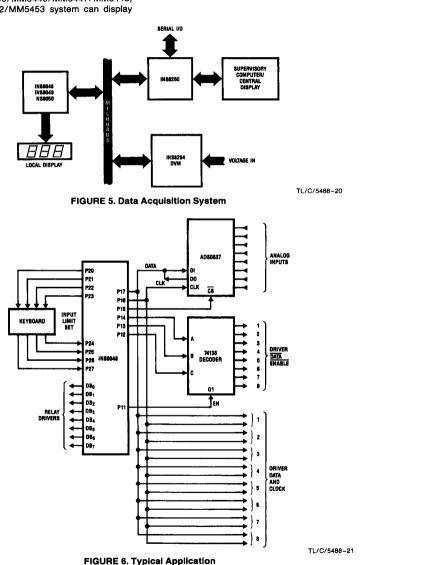
Figure 5 shows a typical remote data acquisition system with an INS8250 Programmable Asynchronous Communication System, which can receive commands or update information from a supervisory computer. The figure also shows an INS8294 CMOS DVM that receives data at V_{IN} and displays the data on the 7-segment local display unit. Data is transferred from the INS8294 to the INS8094 via National's MICROBUSTM.

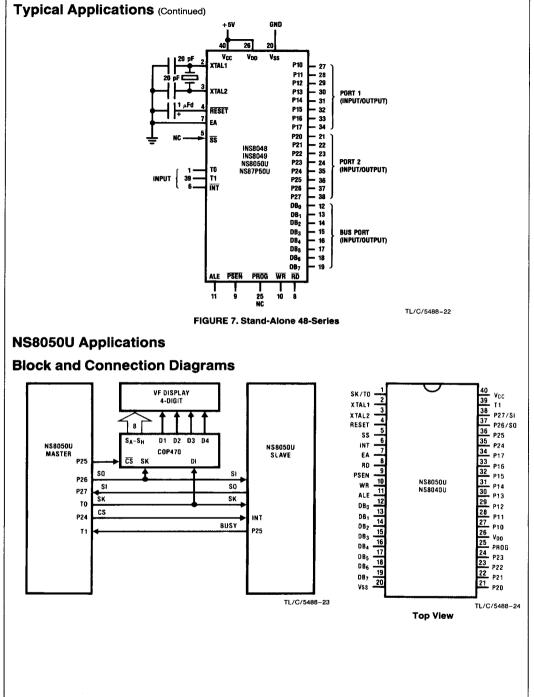
Figure 6 offers an example system that utilizes the unique capacity of these parts. With the addition of an ADC0837 serial A/D converter and a DM74LS138 3-to-8 decoder, the basic INS8048 and MM5445/MM5446/MM5447/MM5448, MM5450/MM5451/MM5452/MM5453 system can display

inputs from 8 separate I/O devices using only one of the INS8048's I/O ports. The other port and the bus can handle any number of tasks. Shown here is the use of Port 2 to control a keyboard, used to enter limits on the inputs. The bus is used to control relay drivers which will regulate the I/O devices when the limits (previously set on the keyboard) are met.

Figure 7 shows a typical way to use the 48-Series microcontrollers in a stand-alone system.

Crystal used is parallel resonant, AT cut and 1 MHz to 6 MHz. All outputs are standard TTL compatible at 5V.





NS8050U Applications (Continued)

MICROWIRE/PLUS consists of a three wire communications port with a clocked 8-bit shift register. The three lines consist of Serial Output (SO), Serial Input (SI) and Serial Clock (SK) and the Shift register is referred to as the Serial Input/Output Register. One 8050U is designated the master and it supplies the clock for the MICROWIRE/PLUS system and initiates data transfer. All transfers are between the master and one or more slaves. A slave can be any MICROWIRE/PLUS.

MICROWIRE Peripherals

DATA ACQUISITION

COP43X 8-bit A/D converters

FREQUENCY GENERATORS AND COUNTERS

COP452

Frequency generator and counter

DISPLAY DRIVERS

COP470

Four-digit vacuum fluorescent display

driver

COP472

Triplex liquid crystal display controller

MM5445, 5446, Vacuum fluorescent display driver

5447, 5448

MM5450, 5451 LED display driver MM5452, 5453 Liquid crystal display driver

MM5480, 5481 LED display driver

MM5484, 5485 16- and 11-segment LED display driver

MM58201

Multiplexed LCD driver
High-voltage display driver

MM58248

MEMORIES

MEMORIES

COP498

Low-power CMOS RAM and timer

COP499 COP494 Low-power CMOS RAM 256-bit, 5V only EEPROM

COP495

1024-bit, 5V only EEPROM

RADIO TUNING

DS890X

AM/FM digital phase-locked loop synthe-

sizer

Peripheral device information may be found in the COPS Microcontrollers Databook.