ATA Flash Disk Controller

SST55LD019M

Advance Information

FEATURES:

- **Industry Standard ATA/IDE Bus Interface**
  - Host Interface: 8- or 16-bit access
  - Supports up to PIO Mode-4
  - Supports up to Multi-word DMA Mode-2
- **Interface for standard NAND Flash Media**
  - Flash Media Interface: 8-bit or 16-bit access
    - Supports up to 8 flash media devices directly
    - Supports up to 64 flash media devices with external decoding logic
  - Supports Multi-Level Cell (MLC) and high density Single-Level Cell (SLC) flash media
    - 2 KByte program page size only
- **Low power, 3.3V core operation**
- **5.0V or 3.3V host interface through V_{DDQ} pins**
- **Low current operation:**
  - Active mode: 25 mA/35 mA (3.3V/5.0V) (typical)
  - Sleep mode: 40 µA/50 µA (3.3V/5.0V) (typical)
- **Power Management Unit**
  - Immediate disabling of unused circuitry
- **Expanded Data Protection**
  - WP_PD# pin configurable by firmware for prevention of data overwrites
- **20-byte Unique ID for Enhanced Security**
  - Factory Pre-programmed 10-byte Unique ID
  - User-Programmable 10-byte ID
- **Integrated Voltage Detector**
  - Industrial Controller requires external POR# signal
- **Pre-programmed Embedded Firmware**
  - Performs self-initialization on first system Power-on
  - Executes industry standard ATA/IDE commands
  - Implements dynamic wear-leveling algorithms to substantially increase the longevity of flash media
  - Embedded Flash File System
  - Built-in ECC corrects up to 3 random 12-bit symbols of error per 512-byte sector
- **Internal or External System Clock Option**
- **Multi-tasking Technology enables Fast Sustained Write Performance (Host to Flash)**
  - Up to 10MB/sec
- **Fast Sustained Read Performance (Flash to Host)**
  - Up to 10 MB/sec
- **Automatic Recognition and Initialization of Flash Media Devices**
  - Seamless integration into a standard SMT manufacturing process
  - 5 sec. (typical) for flash drive recognition and setup
- **Commercial and Industrial Temperature Ranges**
  - 0°C to 70°C for commercial operation
  - -40°C to +85°C for industrial operation
- **Packages Available**
  - 100-lead TQFP – 16mm x 16mm
  - 84-ball TFBGA – 9mm x 9mm
  - 85-ball VFBGA – 6mm x 6mm
- **All non-Pb (lead-free) devices are RoHS compliant**

PRODUCT DESCRIPTION

SST's ATA Flash Disk Controller is the heart of a high-performance, flash media-based data storage system. The ATA Flash Disk Controller recognizes the control, address, and data signals on the ATA/IDE bus and translates them into memory accesses to the standard NAND-type flash media. The SST55LD019M device supports Multi-Level Cell (MLC) and high density Single-Level Cell (SLC) flash media. This technology suits solid state mass storage applications offering new, expanded functionality while enabling smaller, lighter designs with lower power consumption.

The ATA/IDE interface is widely used in such products as portable and desktop computers, digital cameras, music players, handheld data collection scanners, PDAs, handy terminals, personal communicators, audio recorders, monitoring devices, and set-top boxes. SST's ATA Flash Disk Controller supports standard ATA/IDE protocol with up to PIO Mode-4 and Multi-word DMA Mode-2 interface.

Utilizing SST's proprietary SuperFlash memory technology, the ATA Flash Disk Controller is factory pre-programmed with an embedded flash file system which, upon initial Power-on, recognizes the attached flash media devices, sets up a bad block table, executes all necessary handshaking routines for flash media support, and, finally, performs the low-level format. This process typically takes about 3 sec + 0.5 sec/GByte of drive capacity, allowing a 2 GByte flash drive to be fully initialized in about 4 seconds.

This technology enables a very fast, completely seamless integration of flash drives into an embedded design. For added manufacturing flexibility, system debug, re-initialization, and user customization can be accomplished either through the ATA/IDE interface, for ATA Disk Module or flash drive products, or through the Serial Communication Interface (SCI), for fully embedded ATA Flash Disk Controller designs.

Advance Information

The SST55LD019M high-performance ATA Flash Disk Controller is optimized to achieve the highest performance from MLC flash and offers sustained read and write performance up to 10.0 MB/sec. The SST55LD019M can directly support up to 8 flash media devices or, through simple decoding logic, can support up to 64 flash media devices. Users can select either an internal or external system clock option for optimal performance vs. the supply current.

The SST55LD019M controller provides a WP_PD# pin to protect critical information stored in the flash media from unauthorized overwrites.

The ATA Flash Disk Controller comes pre-programmed with a 10-byte unique serial ID. For even greater system security, the user has the option of programming an additional 10 Bytes of ID space to create a unique, 20-byte ID.

The ATA Flash Disk Controller comes packaged in an industry-standard, 100-lead TQFP package, an 84-ball TFBGA package, or a 85-ball VFBGA package for easy integration into an SMT manufacturing process.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1.0 GENERAL DESCRIPTION

The ATA Flash Disk Controller contains a microcontroller and embedded flash file system integrated in TQFP and TFBGA packages. Refer to Figure 2-1 for the ATA Flash Disk Controller block diagram. The controller interfaces with the host system allowing data to be written to and read from the flash media.

1.1 Performance-optimized ATA Flash Disk Controller

The heart of the flash drive is the ATA Flash Disk Controller which translates standard ATA signals into flash media data and control signals. The following components contribute to the ATA Flash Disk Controller's operation.

1.1.1 Microcontroller Unit (MCU)

The MCU translates ATA/IDE commands into data and control signals required for flash media operation.

1.1.2 Internal Direct Memory Access (DMA)

The ATA Flash Disk Controller uses internal DMA allowing instant data transfer from buffer to flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

1.1.3 Power Management Unit (PMU)

The power management unit controls the power consumption of the ATA Flash Disk Controller. The PMU dramatically reduces the power consumption of the ATA Flash Disk Controller by putting the part of the circuitry that is not in operation into sleep mode.

1.1.4 SRAM Buffer

A key contributor to the ATA Flash Disk Controller performance is an SRAM buffer. The buffer optimizes the host's data transfer to and from the flash media.

1.1.5 Embedded Flash File System

The embedded flash file system is an integral part of the ATA Flash Disk Controller. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads.
2. Provides dynamic flash media wear leveling to spread the flash writes across all unused memory address space to increase the longevity of flash media.
3. Keeps track of data file structures.

1.1.6 Error Correction Code (ECC)

The ATA Flash Disk Controller utilizes 72-bit Reed-Solomon Error Detection Code (EDC) and Error Correction Code (ECC), which provides the following error immunity for each 512-byte block of data:

1. Corrects up to three random 12-bit symbol errors.
2. Corrects single bursts up to 25 bits.
3. Detects single bursts up to 61 bits and double bursts up to 15 bits.
4. Detects up to six random 12-bit symbol errors.

1.1.7 Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed to enable the user to restart the self-initialization process and to customize the drive identification information.

1.1.8 Multi-tasking Interface

The multi-tasking interface enables fast and sustained write performance by allowing concurrent Read, Program, and Erase operations to multiple flash media devices. This interface optimizes the performance of Multi-Level Cell (MLC) and high-density Single-Level Cell (SLC) flash media.

2.0 FUNCTIONAL BLOCKS

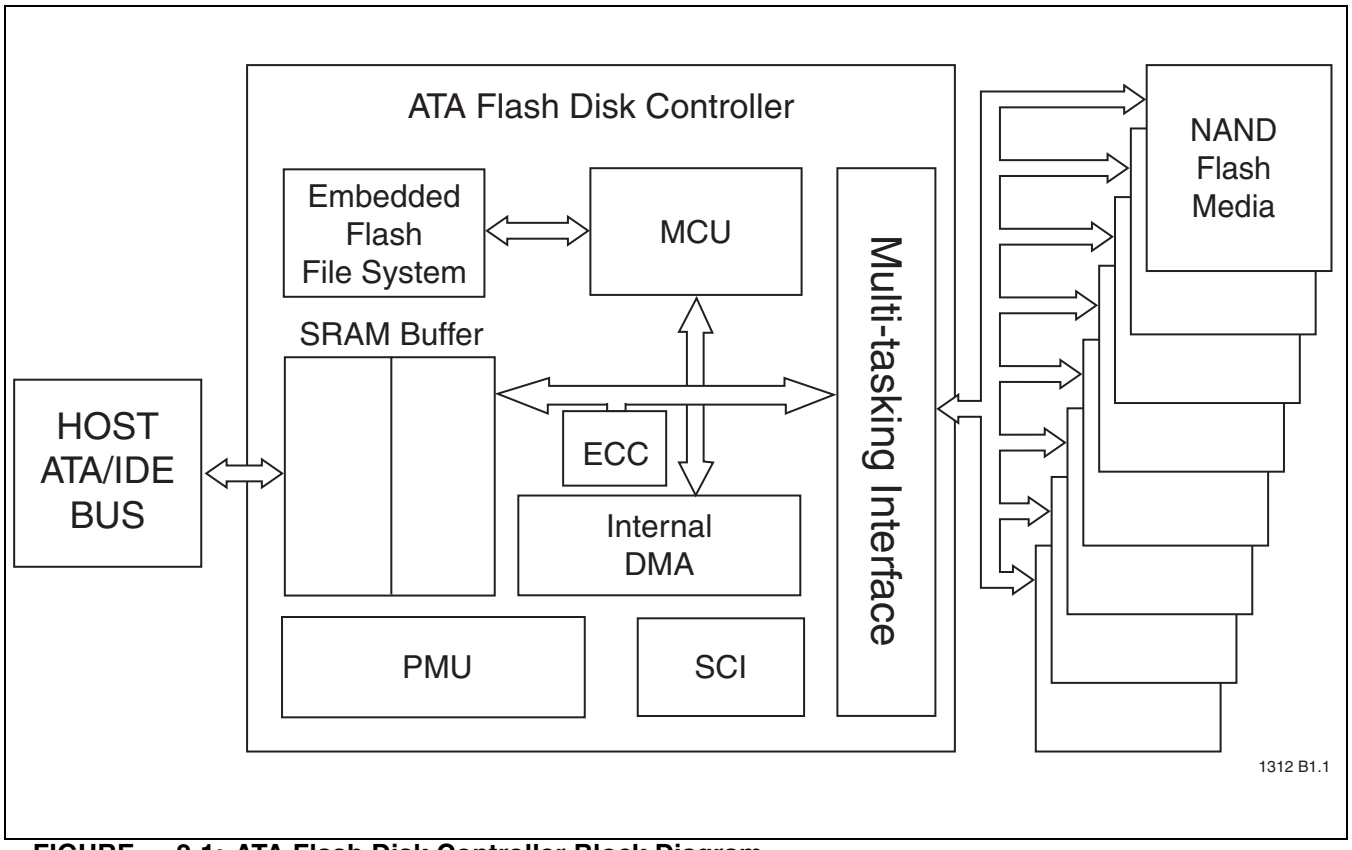


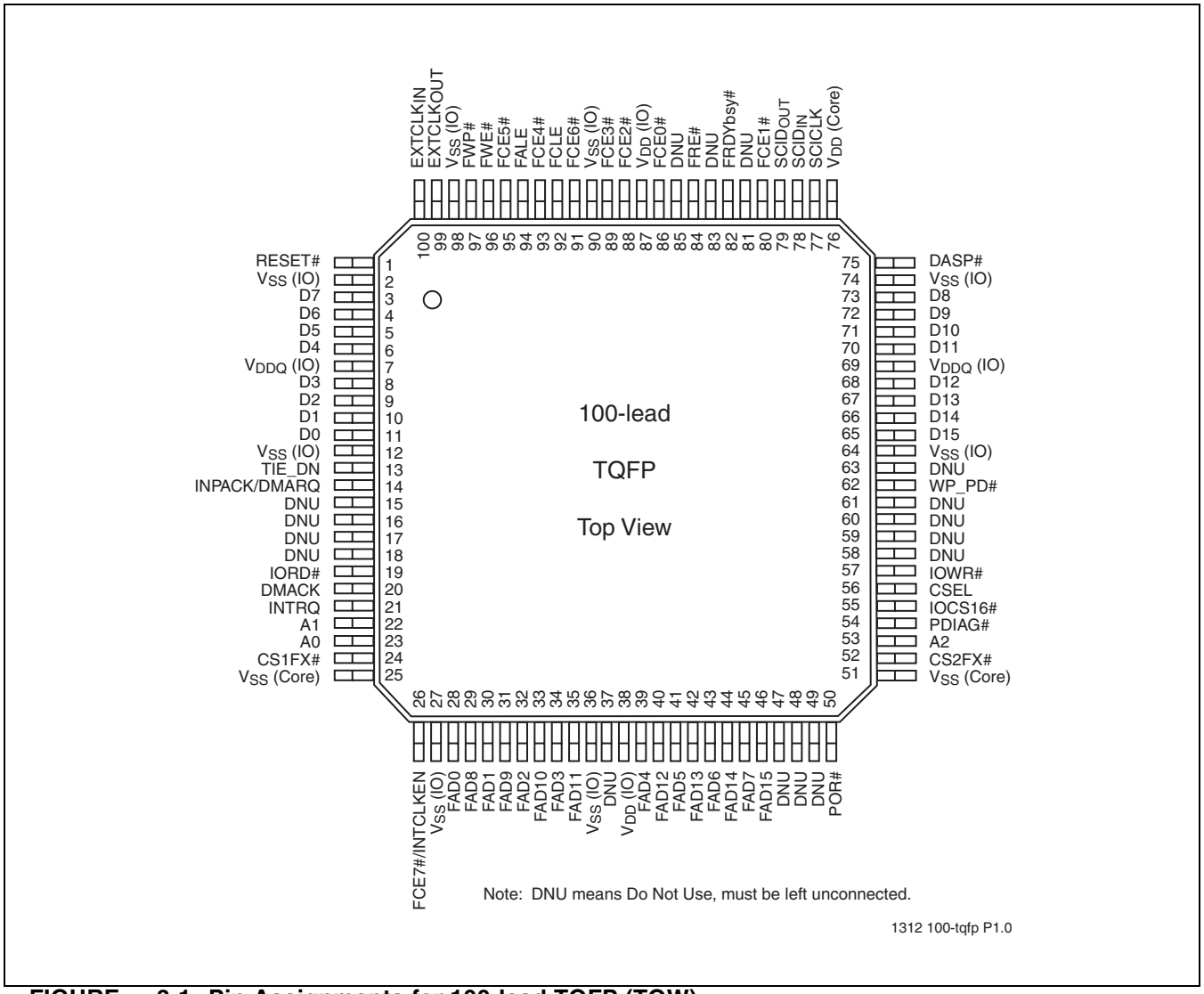
FIGURE 2-1: ATA Flash Disk Controller Block Diagram

Advance Information

3.0 PIN ASSIGNMENTS

The signal/pin assignments are listed in Table 3-1. Low active signals have a "#" suffix. Pin types are Input, Output, or Input/Output. Signals whose source is the host are designated as inputs while signals that the ATA Flash Disk Controller sources are outputs.

The ATA Flash Disk Controller functions in ATA mode, which is compatible with IDE hard disk drives.



Note: DNU means Do Not Use, must be left unconnected.

1312 100-tqfp P1.0

FIGURE 3-1: Pin Assignments for 100-lead TQFP (TQW)

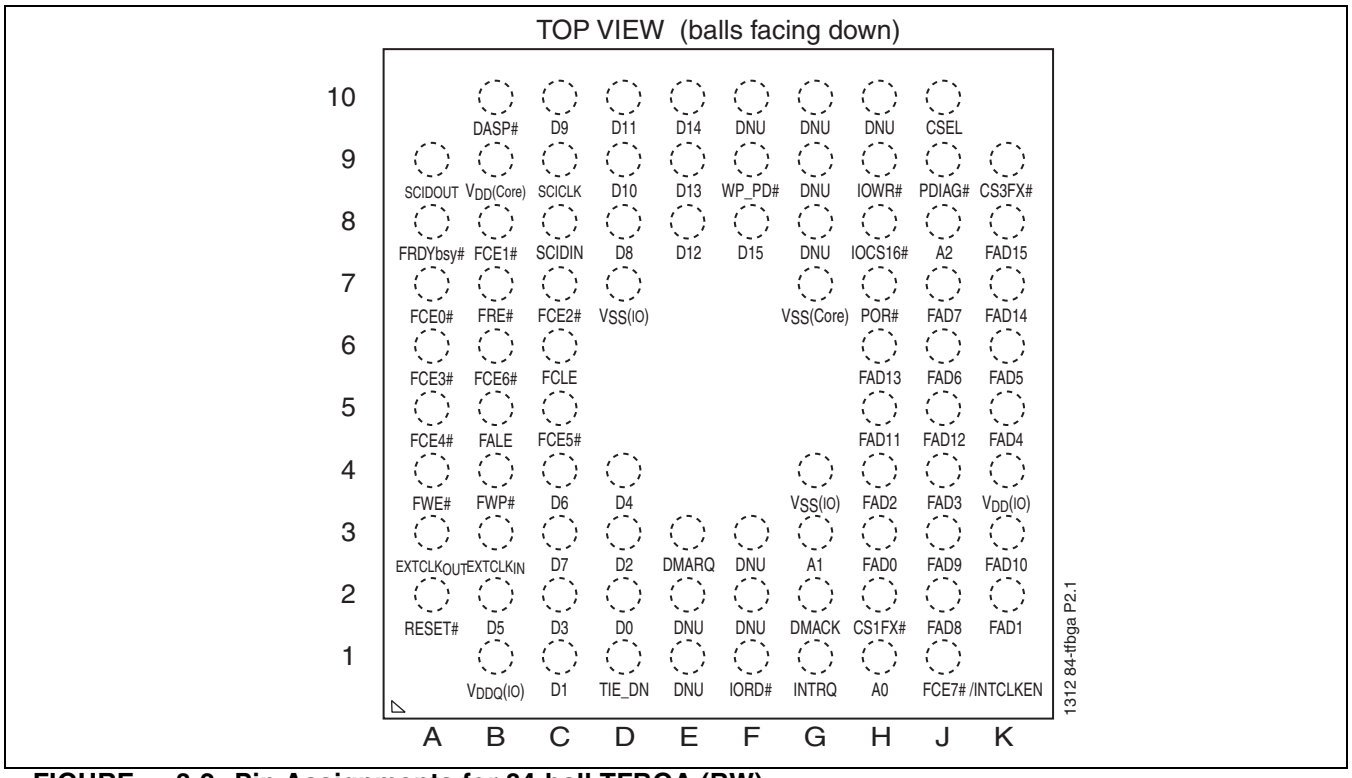


FIGURE 3-2: Pin Assignments for 84-ball TFBGA (BW)

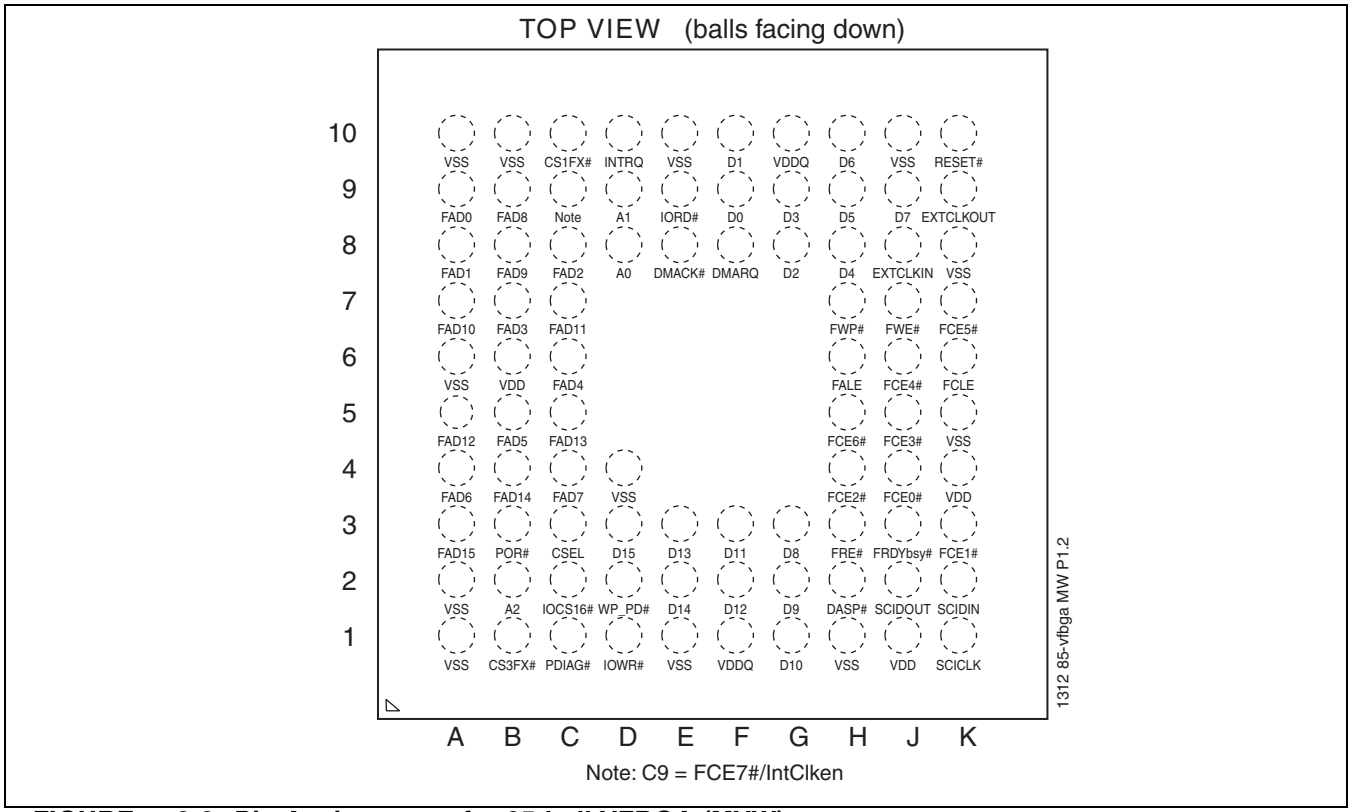


FIGURE 3-3: Pin Assignments for 85-ball VFBGA (MVW)

TABLE 3-1: Pin Assignments (1 of 4)

Symbol	Pin No. 100-TQFP	Pin No. 85-VFBGA	Pin No. 84-TFBGA	Pin Type	I/O Type[1]	Name and Functions
Host Side Interface						
A2	53	B2	J8	I	I1Z	A[2:0] are used to select one of eight registers in the Task File.
A1	22	D9	G3			
A0	23	D8	H1			
D15	65	D3	F8	I/O	I1Z/O2	D[15:0] Data bus
D14	66	E2	E10			
D13	67	E3	E9			
D12	68	F2	E8			
D11	70	F3	D10			
D10	71	G1	D9			
D9	72	G2	C10			
D8	73	G3	D8			
D7	3	J9	C3			
D6	4	H10	C4			
D5	5	H9	B2			
D4	6	H8	D4			
D3	8	G9	C2			
D2	9	G8	D3			
D1	10	F10	C1			
D0	11	F9	D2			
DMACK	20	E8	G2	I	I2U	DMA Acknowledge - input from host
DMARQ	14	F8	E3	O	O1	DMA Request to host
CS1FX#	24	C10	H2	I	I2Z	CS1FX# is the chip select for the task file registers
CS3FX#	52	B1	K9			CS3FX# is used to select the alternate status register and the Device Control register.
CSEL	56	C3	J10	I	I1U	This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave. The pin setting should remain the same from Power-on to Power-down.
IORD#	19	E9	F1	I	I2Z	This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the chip.
IOWR#	57	D1	H9			The I/O Write strobe pulse is used to clock I/O data into the chip.
IOCS16#	55	C2	H8	O	O2	This output signal is asserted low when the device is indicating a word data transfer cycle.
INTRQ	21	D10	G1	O	O1	This signal is the active high Interrupt Request to the host.
PDIAG#	54	C1	J9	I/O	I1U/O1	The Pass Diagnostic signal in the Master/Slave handshake protocol.
DASP#	75	H2	B10	I/O	I1U/O6	The Drive Active/Slave Present signal in the Master/Slave handshake protocol.
RESET#	1	K10	A2	I	I2U	This input pin is the active low hardware reset from the host.

TABLE 3-1: Pin Assignments (Continued) (2 of 4)

Symbol	Pin No. 100-TQFP	Pin No. 85-VFBGA	Pin No. 84-TFBGA	Pin Type	I/O Type[1]	Name and Functions
WP_PD#	62	D2	F9	I	I1U	The WP_PD# pin can be used for either the Write Protect mode or Power-down mode, but only one mode is active at any time. The Write Protect or Power-down modes can be selected through the host command. The Write Protect mode is the factory default setting.
Flash Media Interface						
FWP#	97	H7	B4	O	O5	Active Low Flash Media Chip Write Protect Connect this pin to the NAND flash media Write Protect pin
FRDYbsy#	82	J3	A8	I	I4U	Flash Media Chip Ready/Busy# Signal high is flash media ready signal. Low is busy.
FRE#	84	H3	B7	O	O5	Active Low Flash Media Chip Read
FWE#	96	J7	A4			Active Low Flash Media Chip Write
FCLE	92	K6	C6			Active High Flash Media Chip Command Latch Enable
FALE	94	H6	B5			Active High Flash Media Chip Address Latch Enable
FAD15	46	A3	K8	I/O	I3U/O5	Flash Media Chip High Byte Address/Data Bus pins
FAD14	44	B4	K7			
FAD13	42	C5	H6			
FAD12	40	A5	J5			
FAD11	35	C7	H5			
FAD10	33	A7	K3			
FAD9	31	B8	J3			
FAD8	29	B9	J2			
FAD7	45	C4	J7	I/O	I3U/O5	Flash Media Chip Low Byte Address/Data Bus pins
FAD6	43	A4	J6			
FAD5	41	B5	K6			
FAD4	39	C6	K5			
FAD3	34	B7	J4			
FAD2	32	C8	H4			
FAD1	30	A8	K2			
FAD0	28	A9	H3			
FCE6#	91	H5	B6	O	O4	Active Low Flash Media Chip Enable pin
FCE5#	95	K7	C5			
FCE4#	93	J6	A5			
FCE3#	89	J5	A6			
FCE2#	88	H4	C7			
FCE1#	80	K3	B8			
FCE0#	86	J4	A7			
FCE7#/ INTCLKEN	26	C9	J1	O	I3D/O4	Active Low Flash Media Chip Enable pin This pin is sensed during the Power-on Reset (POR) to select an internal clock mode. If this pin is pulled up during the Power-on Reset then the internal clock is selected.

TABLE 3-1: Pin Assignments (Continued) (3 of 4)

Symbol	Pin No. 100-TQFP	Pin No. 85-VFBGA	Pin No. 84-TFBGA	Pin Type	I/O Type[1]	Name and Functions
Serial Communication Interface (SCI)						
$SCID_{OUT}$	79	J2	A9	O	O4	SCI interface data output
$SCID_{IN}$	78	K2	C8	I	I3U	SCI interface data input
SCICLK	77	K1	C9	I	I3U	SCI interface clock
External Clock Option						
FCE7#/ INTCLKEN	26	C9	J1	I/O	I3D/O4	Active Low Flash Media Chip Enable pin This pin is sensed during the Power-on Reset (POR) to select an Internal Clock mode. If this pin is pulled up during the Power-on Reset then the Internal Clock is selected.
$EXTCLK_{IN}$	100	J8	B3	I	I4Z	External Clock source input pin
$EXTCLK_{OUT}$	99	K9	A3	O	O4	External Clock source output pin
Miscellaneous						
V_{SS} (IO)	2 12 27 36 64 74 90 98	A2 A6 A10 D4 E1 E10 H1 J10 K5 K8	D7, G4	PWR		Ground for I/O
V_{SS} (Core)	25 51	A1 B10	G7	PWR		Ground for Core
V_{DD} (IO)	38 87	B6 K4	K4	PWR		V_{DD} (3.3V)
V_{DD} (Core)	76	J1	B9	PWR		V_{DD} (3.3V)
V_{DDQ} (IO)	7 69	F1 G10	B1	PWR		V_{DDQ} (5V/3.3V) for Host interface
POR#	50	B3	H7	I	Analog Input[2]	Power-on Reset (POR). Active Low
T_{IE}_DN	13		D1			Pins need to be connected to V_{SS}.

TABLE 3-1: Pin Assignments (Continued) (4 of 4)

Symbol	Pin No. 100-TQFP	Pin No. 85-VFBGA	Pin No. 84-TFBGA	Pin Type	I/O Type[1]	Name and Functions
DNU[3]	15		E1			Do Not Use, must be left unconnected.
	16		E2			
	17		F2			
	18		F3			
	37		F10			
	47		G8			
	48		G9			
	49		G10			
	58		H10			
	59					
	60					
	61					
	63					
	81					
	83					
	85					

T3-1.3 1312

1. Please refer to Section 11.1 for details.
2. Analog input for supply voltage detection
3. All DNU pins should not be connected.

4.0 CAPACITY SPECIFICATION

Table 4-1 shows the default capacity and specific settings for heads, sectors, and cylinders. Users can change the default settings in the drive ID table (see Table 10-4) for customization. If the total number of bytes is less than the default, the remaining space could be used as spares to increase the flash drive endurance. It should also be noted that if the total flash drive capacity exceeds the total default number of bytes, the flash drive endurance will be reduced.

TABLE 4-1: Default ATA Flash Drive Settings

Capacity[1]	Total Bytes	Cylinders[2]	Heads[2]	Sectors[2]	Max LBA
128 MB	128,057,344	977	8	32	250,880
256 MB	256,901,120	980	16	32	501,760
512 MB	512,483,328	993	16	63	1,000,944
1024 MB	1,024,966,656	1986	16	63	2,001,888
2048 MB	2,048,385,024	3969	16	63	4,000,752
4096 MB	4,096,253,952	7937	16	63	8,000,496
6 GB	6,001,164,288	11628	16	63	11,721,024
8 GB	8,001,552,384	15504	16	63	15,628,032
10 GB	10,001,940,480	16383[3]	16	63	19,535,040
12 GB	12,001,296,384	16383[3]	16	63	23,440,032
14 GB	14,001,684,480	16383[3]	16	63	27,347,040
16 GB	16,001,040,384	16383[3]	16	63	31,252,032
18 GB	18,001,428,480	16383[3]	16	63	35,159,040
20 GB	20,001,816,576	16383[3]	16	63	39,066,048
22 GB	22,001,172,480	16383[3]	16	63	42,971,040
24 GB	24,001,560,576	16383[3]	16	63	46,878,048
26 GB	26,001,948,672	16383[3]	16	63	50,785,056
28 GB	28,001,304,576	16383[3]	16	63	54,690,048
30 GB	30,001,692,672	16383[3]	16	63	58,597,056
32 GB	32,001,048,576	16383[3]	16	63	62,502,048

T4-1.7 1312

1. These flash drive capacities can only be manufactured by using the specified version of the ATA Flash Disk Controller.
2. Cylinders, Heads, and Sectors can be re-configured from the default settings during the manufacturing process.
3. Cylinders, Heads, and Sectors are not applicable for these capacities. Only LBA addressing applies.

4.1 Functional Specifications

Table 4-2 shows the performance and the maximum capacity supported by the SST55LD019M controller.

TABLE 4-2: Functional Specification of SST55LD019M

Functions	SST55LD019M
ATA Controller Supported Capacity	128 MByte to 32 GB with external decoding[1] logic
ATA Controller Performance-Sustained Write speed	Up to 10.0 MB/sec
ATA Controller Performance-Sustained Read speed	Up to 10.0 MB/sec

T4-2.4 1312

1. Please refer to the reference schematics for high-capacity flash drive design.

5.0 MANUFACTURING SUPPORT

The ATA Flash Disk controller firmware contains a list of supported standard NAND flash media devices. Upon initial Power-on, the controller scans all connected flash media devices and reads their device ID. If the device ID matches the listed flash media devices in the ATA Flash Disk controller, the controller performs drive recognition based on the algorithm provided by the flash media suppliers, including setting up the bad block table, executing all the necessary handshaking routines for flash media support, and, finally, performing the low-level format. For Power-up timing specifications, please refer to Table 11-4.

Please contact SST for the most current list of supported NAND Flash media devices.

In the event that the NAND flash media device ID is not recognized by the ATA Flash Disk controller, the user has an option of adding this device to the controller device table through the manufacturing interface provided by SST. Please contact SST for the ATA Flash Disk controller manufacturing interface software. If the drive initialization fails, and a visual inspection is unable to determine the problem, the SST55LD019M ATA Flash Disk controller provides a comprehensive interface for manufacturing flow debug. This interface not only allows debug of the failure and manual reset of the initialization process, but also allows customization of user definable options.

5.1 ATA/IDE Interface

The ATA Flash Disk controller interface can be used for manufacturing support. SST provides an example of a DOS-based solution (an executable routine downloadable from SST's web site) for manufacturing debug and rework.

5.2 Serial Communication Interface (SCI)

For additional manufacturing flexibility, the SCI bus can be used for manufacturing error reporting. The SCI consists of 3 active signals: $SCID_{OUT}$, $SCID_{IN}$, and SCICLK.

6.0 EXTERNAL CLOCK INTERFACE

The external clock interface allows ATA Flash Disk controller operation from an external clock source generated by an RC circuit. Do not use a free running clock as input to the EXTCLKIN pin; an RC circuit must be used. Contact SST for reference circuit and recommended external clock settings.

While the controller has an internal clock source, the external clock source allows slowing of the system clock operation to limit the peak current and overcome additional bus loading.

The external clock interface consists of three signals: INTCLKEN, EXTCLKIN, and EXTCLKOUT. The INTCLKEN pin selects between external and internal clock sources for the ATA Flash Disk controller. If this pin is pulled high before device Power-on, then the internal clock source is selected; otherwise, the external clock source is selected. The EXTCLKIN and EXTCLKOUT signals are the input and output clock signals, respectively.

7.0 CONFIGURABLE WRITE PROTECT/POWER-DOWN MODES

The WP_PD# pin can be used for either Write Protect mode or Power-down mode, but only one mode is active at any time. Either mode can be selected through the host command, Set-WP_PD#-Mode, explained in Section 10.2.1.20.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

7.1 Write Protect Mode

When the device is configured in the Write Protect mode, the WP_PD# pin offers extended data protection. This feature can be either selected through a jumper or host logic to protect the stored data from inadvertent system writes or erases, and viruses. The Write Protect feature protects the full address space of the data stored on the flash media.

In the Write Protect mode, the WP_PD# pin should be asserted prior to issuing the destructive commands: Erase-Sector, Format-Track, Write-DMA, Write-Long-Sector, Write-Multiple, Write-Multiple-without-Erase, Write-Sector(s), Write-Sector-without-Erase, or Write-Verify. This will force the ATA Flash Disk Controller to reject any destructive commands from the ATA interface. All destructive commands will return 51H in the Status register and 04H in the Error register signifying an invalid command. All non-destructive commands will be executed normally.

7.2 Power-down Mode

When the device is configured in the Power-down mode, if the WP_PD# pin is asserted during a command, the ATA disk controller completes the current command and returns to the standby mode immediately to save power. Afterwards, the device will not accept any other commands. Only a Power-on Reset (POR) or hardware reset will bring the device to normal operation with the WP_PD# pin de-asserted.

8.0 POWER-ON AND BROWN-OUT RESET CHARACTERISTICS

Please contact SST to obtain ATA Flash Disk controller reference design schematics including the POR# circuit for commercial and industrial ATA Flash Disk controller offerings.

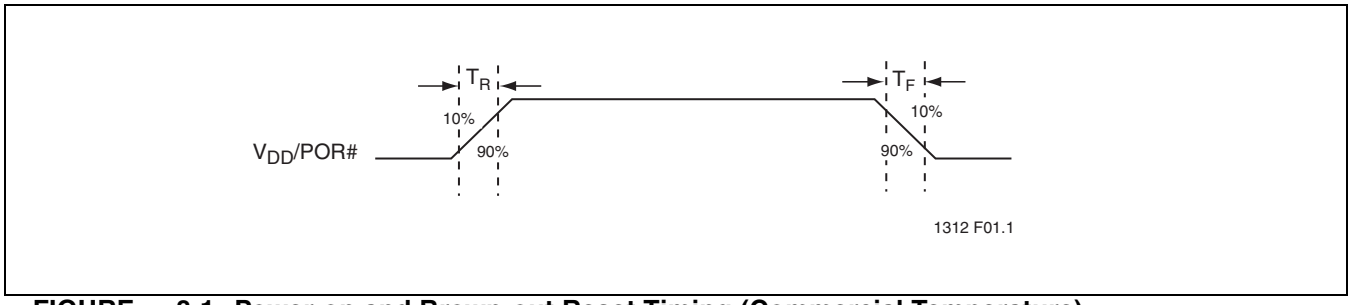


FIGURE 8-1: Power-on and Brown-out Reset Timing (Commercial Temperature)

TABLE 8-1: Power-on and Brown-out Reset Timing (Commercial Temperature)

Item	Symbol	Min	Max	Units
V_{DD}/POR# Rise Time[1]	T_R		200	ms
V_{DD}/POR# Fall Time[2]	T_F		200	ms

T8-1.0 1312

1. V_{DD} Rise Time should be greater than or equal to POR# Rise Time.
2. V_{DD} Fall Time should be slower than or equal to POR# Fall Time.

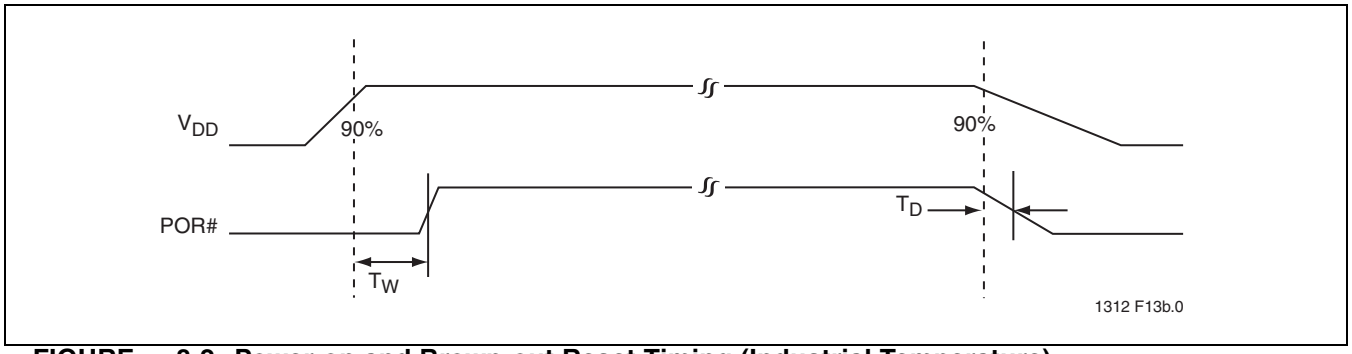


FIGURE 8-2: Power-on and Brown-out Reset Timing (Industrial Temperature)

TABLE 8-2: Power-on and Brown-out Reset Timing (Industrial Temperature)

Item	Symbol	Min	Max	Units
POR Wait Time	T_W	0.1		ms
Brown-out Delay Time	T_D		30	µs

T8-2.0 1312

9.0 I/O TRANSFER FUNCTION

The default operation for the ATA Flash Disk Controller is 16-bit. However, if the host issues a Set-Feature command to enable 8-bit mode, the ATA Flash Disk Controller permits 8-bit data access.

The following table defines the function of various operations.

TABLE 9-1: I/O Function

Function Code	CS3FX#	CS1FX#	A0-A2	IORD#	IOWR#	D15-D8	D7-D0
Invalid Mode	V_{IL}	V_{IL}	X	X	X	Undefined	Undefined
Standby Mode	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Task File Write	V_{IH}	V_{IL}	1-7H	V_{IH}	V_{IL}	X	Data In
Task File Read	V_{IH}	V_{IL}	1-7H	V_{IL}	V_{IH}	High Z	Data Out
Data Register Write	V_{IH}	V_{IL}	0	V_{IH}	V_{IL}	In[1]	In
Data Register Read	V_{IH}	V_{IL}	0	V_{IL}	V_{IH}	Out[1]	Out
Control Register Write	V_{IL}	V_{IH}	6H	V_{IH}	V_{IL}	X	Control In
Alt Status Read	V_{IL}	V_{IH}	6H	V_{IL}	V_{IH}	High Z	Status Out
Drive Address	V_{IL}	V_{IH}	7H	V_{IL}	V_{IH}	High Z	Data Out

T9-1.0 1312

1. If 8-bit data transfer mode is enabled.
In 8-bit data transfer mode, High Byte is undefined for Data Out. For Data In, X can be V_{IH} or V_{IL}, but no other value.

10.0 SOFTWARE INTERFACE

10.1 ATA Flash Disk Controller Drive Register Set Definitions and Protocol

This section defines the drive registers for the ATA Flash Disk Controller and the protocol used to address them.

10.1.1 ATA Flash Disk Controller Addressing

The I/O decoding for an ATA Flash Disk Controller is shown in Table 10-1.

TABLE 10-1: Task File Registers

					Registers	
CS3FX#	**CS1FX#**	**A2**	**A1**	**A0**	**IORD# = 0 (IOWR#=1)**	**IOWR# = 0 (IORD#=1)**
1	0	0	0	0	Data (Read)	Data (Write)
1	0	0	0	1	Error	Feature
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector Number (LBA 7-0)	Sector Number (LBA 7-0)
1	0	1	0	0	Cylinder Low (LBA 15-8)	Cylinder Low (LBA 15-8)
1	0	1	0	1	Cylinder High (LBA 23-16)	Cylinder High (LBA 23-16)
1	0	1	1	0	Drive/Head	Drive/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alternate Status	Device Control
0	1	1	1	1	Drive Address	Reserved

T10-1.0 1312

10.1.2 ATA Flash Disk Controller Registers

The following section describes the hardware registers used by the host software to issue commands to the ATA Flash Disk Controller. These registers are often collectively referred to as the Task File registers. The registers are only selectable through CS3FX#, CS1FX#, and A_2-A_0 signals.

10.1.2.1 Data Register (Read/Write)

This 16-bit register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format-Track command. Data transfer can be performed in PIO mode.

10.1.2.2 Error Register (Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
BBK	UNC	0	IDNF	0	ABRT	0	AMNF	**0000 0000b**

Symbol	**Function**
BBK	This bit is set when a Bad Block is detected.
UNC	This bit is set when an Uncorrectable Error is encountered.
IDNF	The requested sector ID is in error or cannot be found.
ABRT	This bit is set if the command has been aborted because of an ATA Flash Disk Controller status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued. It is required that the host retry any command that ends with an error condition.
AMNF	This bit is set in case of a general error.

10.1.2.3 Feature Register (Write Only)

This register provides information regarding features of the ATA Flash Disk Controller that the host can utilize.

10.1.2.4 Sector Count Register

This register contains the numbers of sectors of data requested to be transferred on a Read or Write operation between the host and the ATA Flash Disk Controller. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

10.1.2.5 Sector Number (LBA 7-0) Register

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any ATA Flash Disk Controller data access for the subsequent command.

10.1.2.6 Cylinder Low (LBA 15-8) Register

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

10.1.2.7 Cylinder High (LBA 23-16) Register

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

10.1.2.8 Drive/Head (LBA 27-24) Register

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
1	LBA	1	DRV	HS3	HS2	HS1	HS0	**1010 0000b**

Symbol	Function
LBA	LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block mode, the Logical Block Address is interpreted as follows: LBA7-LBA0: Sector Number register D7-D0. LBA15-LBA8: Cylinder Low register D7-D0. LBA23-LBA16: Cylinder High register D7-D0. LBA27-LBA24: Drive/Head register bits HS3-HS0.
DRV	DRV is the drive number. When DRV=0 (Master), Master is selected. When DRV=1 (Slave), Slave is selected.
HS3	When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.
HS2	When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.
HS1	When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.
HS0	When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

10.1.2.9 Status & Alternate Status Registers (Read Only)

These registers return the ATA Flash Disk Controller status when read by the host. Reading the Status register does clear a pending interrupt while reading the alternate Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR	**1000 0000b**

Symbol	**Function**
BUSY	The busy bit is set when the ATA Flash Disk Controller has access to the command buffer and registers and the host is locked out from accessing the Command register and buffer. No other bits in this register are valid when this bit is set to a 1.
RDY	RDY indicates whether the device is capable of performing ATA Flash Disk Controller operations. This bit is cleared at power up and remains cleared until the ATA Flash Disk Controller is ready to accept a command.
DWF	This bit, if set, indicates a write fault has occurred.
DSC	This bit is set when the ATA Flash Disk Controller is ready.
DRQ	The Data-Request bit is set when the ATA Flash Disk Controller requires that information be transferred either to or from the host through the Data register.
CORR	This bit is set when a correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector Read operation.
ERR	This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. It is required that the host retry any media access command (such as Read-Sector and Write-Sector) that ends with an error condition.

10.1.2.10 Device Control Register (Write Only)

This register is used to control the ATA Flash Disk Controller interrupt request and to issue a software reset. This register can be written to even if the device is busy. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
X	X	X	X	1	SW Rst	-IEn	0	**0000 1000b**

Symbol	**Function**
SW Rst	This bit is set to 1 in order to force the ATA Flash Disk Controller to perform a software Reset operation. The chip remains in reset until this bit is reset to ‘0.’
-IEn	0: The Interrupt Enable bit enables interrupts 1: Interrupts from the ATA Flash Disk Controller are disabled This bit is set to 0 at Power-on and Reset.

10.1.2.11 Drive Address Register (Read Only)

This register contains the inverted drive select and head select addresses of the currently selected drive. The bits in this register are as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
X	-WTG	-HS3	-HS2	-HS1	-HS0	-DS1	-DS0	**x111 1110b**

Symbol	**Function**
-WTG	This bit is 0 when a Write operation is in progress, otherwise, it is 1.
-HS3	This bit is the negation of bit 3 in the Drive/Head register.
-HS2	This bit is the negation of bit 2 in the Drive/Head register.
-HS1	This bit is the negation of bit 1 in the Drive/Head register.
-HS0	This bit is the negation of bit 0 in the Drive/Head register.
-DS1	This bit is 0 when drive 1 is active and selected.
-DS0	This bit is 0 when drive 0 is active and selected.

10.1.2.12 Command Register (Write Only)

This register contains the command code being sent to the drive. Command execution begins immediately after this register is written. The executable commands, the command codes, and the necessary parameters for each command are listed in Table 10-2.

10.2 ATA Flash Disk Controller Command Description

This section defines the software requirements and the format of the commands the host sends to the ATA Flash Disk Controller. Commands are issued to the ATA Flash Disk Controller by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register. The manner in which a command is accepted varies. There are three classes (see Table 10-2) of command acceptance, all dependent on the host not issuing commands unless the ATA Flash Disk Controller is not busy (BSY=0).

10.2.1 ATA Flash Disk Controller Command Set

Table 10-2 summarizes the ATA Flash Disk Controller command set with the paragraphs that follow describing the individual commands and the task file for each.

TABLE 10-2: ATA Flash Disk Controller Command Set

Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
Check-Power-Mode	E5H or 98H	-	-	-	-	D[8]	-
Execute-Drive-Diagnostic	90H	-	-	-	-	D	-
Flush-Cache	E7H	-	-	-	-	D	-
Format-Track	50H	-	Y[7]	-	Y	Y[8]	Y
Identify-Drive	ECH	-	-	-	-	D	-
Idle	E3H or 97H	-	Y	-	-	D	-
Idle-Immediate	E1H or 95H	-	-	-	-	D	-
Initialize-Drive-Parameters	91H	-	Y	-	-	Y	-
NOP	00H	-	-	-	-	D	-
Read-Buffer	E4H	-	-	-	-	D	-
Read-DMA	C8H or C9H	-	Y	Y	Y	Y	Y
Read-Multiple	C4H	-	Y	Y	Y	Y	Y
Read-Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
Recalibrate	1XH	-	-	-	-	D	-
Seek	7XH	-	-	Y	Y	Y	Y
Set-Features	EFH	Y	-	-	-	D	-
Set-Multiple-Mode	C6H	-	Y	-	-	D	-
Set-Sleep-Mode	E6H or 99H	-	-	-	-	D	-
Set-WP_PD#-Mode	8BH	Y	-	-	-	D	-
Standby	E2H or 96H	-	-	-	-	D	-
Standby-Immediate	E0H or 94H	-	-	-	-	D	-
Write-Buffer	E8H	-	-	-	-	D	-
Write-DMA	CAH or CBH	-	Y	Y	Y	Y	Y
Write-Multiple	C5H	-	Y	Y	Y	Y	Y
Write-Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
Write-Verify	3CH	-	Y	Y	Y	Y	Y

T10-2.1 1312

1. FR - Features register
2. SC - Sector Count register
3. SN - Sector Number register
4. CY - Cylinder registers
5. DH - Drive/Head register
6. LBA - Logical Block Address mode supported (see command descriptions for use)
7. Y - The register contains a valid parameter for this command.
8. For the Drive/Head register: Y means both the ATA Flash Disk Controller and Head parameters are used;
   D means only the ATA Flash Disk Controller parameter is valid and not the Head parameter.

10.2.1.1 Check-Power-Mode - 98H or E5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	98H or E5H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command checks the power mode. Because the ATA Flash Disk Controller can recover from sleep in 200 ns, Idle mode is never enabled. ATA Flash Disk Controller sets BSY, sets the Sector Count register to 00H, clears BSY, and generates an interrupt.

10.2.1.2 Execute-Drive-Diagnostic - 90H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command performs the internal diagnostic tests implemented by the ATA Flash Disk Controller.

If the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices.

The diagnostic codes shown in Table 10-3 are returned in the Error register at the end of the command.

TABLE10-3:Diagnostic Codes

Code	Error Type
01H	No Error Detected
02H	Formatter Device Error
03H	Sector Buffer Error
04H	ECC Circuitry Error
05H	Controlling Microprocessor Error
8XH	Slave Error

T10-3.0 1312

10.2.1.3 Flush-Cache - E7H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E7H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the ATA Flash Disk Controller to complete writing data from its cache. The ATA Flash Disk Controller then clears BSY and generates an interrupt.

10.2.1.4 Format-Track - 50H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is accepted for host backward compatibility. The ATA Flash Disk Controller expects a sector buffer of data from the host to follow the command with the same protocol as the Write-Sector(s) command although the information in the buffer is not used by the ATA Flash Disk Controller. The use of this command is not recommended.

10.2.1.5 Identify-Drive - ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify-Drive command enables the host to receive parameter information from the ATA Flash Disk Controller. This command has the same protocol as the Read-Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 10-4. All reserved bits or words are zero. Table 10-4 gives the definition for each field in the Identify-Drive information.

TABLE10-4:Identify-Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044AH	2	General configuration bit
1	bbbbH[1]	2	Default number of cylinders
2	0000H	2	Reserved
3	bbbbH[1]	2	Default number of heads
4	0000H	2	Reserved
5	0000H	2	Reserved
6	bbbbH[1]	2	Default number of sectors per track
7-8	bbbbH[2]	4	Number of sectors per device (Word 7 = MSW, Word 8 = LSW)
9	bbBFH	2	Vendor Unique
10-14	eeeeH[3]	10	User-programmable serial number in ASCII
15-19	ddddH[4]	10	SST preset, unique ID in ASCII
20	0002H	2	Buffer type
21	0200H	2	Buffer size in 512 Byte increments
22	0004H	2	# of ECC bytes passed on Read/Write-Long-Sector Commands
23-26	aaaaH[5]	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	ccccH[6]	40	User Definable Model number
47	0001H	2	Maximum number of sectors on Read/Write-Multiple command
48	0000H	2	Reserved
49	0B00H	2	Capabilities
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode
52	0000H	2	Reserved
53	0003H	2	Translation parameters are valid
54	nnnnH	2	Current numbers of cylinders
55	nnnnH	2	Current numbers of heads
56	nnnnH	2	Current sectors per track
57-58	nnnnH	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	0101H	2	Multiple sector setting
60-61	nnnnH	4	Total number of sectors addressable in LBA mode
62	0000H	2	Reserved
63	0n07H	2	DMA data transfer is supported in ATA Flash Disk Controller
64	0003H	2	Advanced PIO Transfer mode supported
65	0078H	2	120 ns cycle time support for Multi-word DMA Mode-2
66	0078H	2	120 ns cycle time support for Multi-word DMA Mode-2
67	0078H	2	PIO Mode-4 supported
68	0078H	2	PIO Mode-4 supported
69-79	0000H	22	Reserved
80	007EH	2	ATA/ATAPI major version number
81	0019H	2	ATA/ATAPI minor version number
82	7068H	2	Features/command sets supported
83	4000H	2	Features/command sets supported
84	4000H	2	Features/command sets supported
85-87	xxxxH	6	Features/command sets enabled
88-128	0000H	82	Reserved
129-159	0000H	62	Vendor unique bytes

TABLE10-4:Identify-Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
160-255	0000H	192	Reserved

T10-4.3 1312

1. bbbb - default value set by controller. The selections could be user programmable.
2. n - calculated data based on product configuration
3. eeee - the default value is 2020H
4. dddd - unique number of each device
5. aaaa - any unique SST firmware revision
6. cccc - default value is “xxxxMB/xxGB ATA Flash Disk” where xxx is the flash drive capacity. The user has an option to change the model number during manufacturing.

10.2.1.5.1 Word 0: General Configuration

This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 MByte/sec and is not MFM encoded.

10.2.1.5.2 Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

10.2.1.5.3 Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

10.2.1.5.4 Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

10.2.1.5.5 Word 7-8: Number of Sectors

This field contains the number of sectors per ATA Flash Disk Controller. This double word value is also the first invalid address in LBA translation mode. This field is only required by CF feature set support.

10.2.1.5.6 Word 10-19: Serial Number

The contents of this field are right justified and padded with spaces (20H). The right-most ten bytes are a SST preset, unique ID. The left-most ten bytes are a user-programmable value with a default value of spaces.

10.2.1.5.7 Word 20: Buffer Type

This field defines the buffer capability:

0002H: a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the ATA Flash Disk Controller.

10.2.1.5.8 Word 21: Buffer Size

This field defines the buffer capacity in 512 Byte increments. SST’s ATA Flash Disk Controller has up to 2 sector data buffer for host interface.

10.2.1.5.9 Word 22: ECC Count

This field defines the number of ECC bytes used on each sector in the Read- and Write-Long-Sector commands.

10.2.1.5.10 Word 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

10.2.1.5.11 Word 27-46: Model Number

This field is reserved for the model number for this product.

10.2.1.5.12 Word 47: Read-/Write-Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read-Multiple or Write-Multiple commands.

10.2.1.5.13 Word 49: Capabilities

Bit	Function
13	Standby Timer 0: forces sleep mode when host is inactive.
11	IORDY Support 1: ATA Flash Disk Controller supports PIO Mode-4.
9	LBA support 1: ATA Flash Disk Controller supports LBA mode addressing.
8	DMA Support 1: DMA mode is supported.

10.2.1.5.14 Word 51: PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer. ATA Flash Disk Controller supports up to PIO Mode-4.

10.2.1.5.15 Word 53: Translation Parameters Valid

Bit	Function
0	1: words 54-58 are valid and reflect the current number of cylinders, heads and sectors.
1	1: words 64-70 are valid to support PIO Mode-3 and 4.

10.2.1.5.16 Word 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

10.2.1.5.17 Word 57-58: Current Capacity

This field contains the product of the current cylinders times heads times sectors.

10.2.1.5.18 Word 59: Multiple Sector Setting

This field contains a validity flag in the Odd Byte and the current number of sectors that can be transferred per interrupt for Read/Write Multiple in the Even Byte. The Odd Byte is always 01H which indicates that the Even Byte is always valid.

The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this word by default contains a 00H which indicates that Read/Write Multiple commands are not valid.

10.2.1.5.19 Word 60-61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the ATA Flash Disk Controller in LBA mode only.

10.2.1.5.20 Word 63: Multi-word DMA Transfer Mode

This field identifies the multi-word DMA transfer modes supported by the ATA Flash Disk Controller and indicates the mode that is currently selected. Only one DMA mode can be selected at any given time.

Bit	Function
15-11	Reserved
10	Multi-word DMA mode 2 selected 1: Multi-word DMA mode 2 is selected and bits 8 and 9 are cleared to 0 0: Multi-word DMA mode 2 is not selected.
9	Multi-word DMA mode 1 selected 1: Multi-word DMA mode 1 is selected and 8 and 10 should be cleared to 0. 0: Multi-word DMA mode 1 is not selected.
8	Multi-word DMA mode 0 selected 1: Multi-word DMA mode 0 is selected and bits 9 and 10 are cleared to 0. 0: Multi-word DMA mode 0 is not selected.
7-3	Reserved
2	Multi-word DMA mode 2 supported 1: Multi-word DMA mode 2 and below are supported and Bits 0 and 1 are set to 1.
1	Multi-word DMA mode 1 supported 1: Multi-word DMA mode 1 and below are supported.
0	Multi-word DMA mode 0 supported 1: Multi-word DMA mode 0 is supported.

10.2.1.5.21 Word 64: Advanced PIO Data Transfer Mode

Bit	Function
0	1: ATA Flash Disk Controller supports PIO Mode-3.
1	1: ATA Flash Disk Controller supports PIO Mode-4.

10.2.1.5.22 Word 65: Minimum Multi-word DMA Transfer Cycle Time Per Word

This field defines the minimum Multi-word DMA transfer cycle time per word. This field defines, in nanoseconds, the minimum cycle time that the ATA Flash Disk Controller supports when performing Multi-word DMA transfers on a per word basis. SST's ATA Flash Disk Controller supports up to Multi-word DMA Mode-2, so this field is set to 120ns.

10.2.1.5.23 Word 66: Device Recommended Multi-word DMA Cycle Time

This field defines the ATA Flash Disk Controller recommended Multi-word DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command for any location on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the ATA Flash Disk Controller may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result. SST's ATA Flash Disk Controller supports up to Multi-word DMA Mode-2, so this field is set to 120 ns.

10.2.1.5.24 Word 67: Minimum PIO Transfer Cycle Time Without Flow Control

The ATA Flash Disk Controller's minimum cycle time is 120 ns.

10.2.1.5.25 Word 68: Minimum PIO Transfer Cycle Time With IORDY

The ATA Flash Disk Controller's minimum cycle time is 120 ns, e.g., PIO Mode-4.

10.2.1.5.26 Word 80: Major Version Number

If not 0000H or FFFFH, the device claims compliance with the major version(s) as indicated by bits (6:1) being set to one. Since ATA standards maintain downward compatibility, a device may set more than one bit. SST55LD019x supports ATA-1 to ATA-6.

10.2.1.5.27 Word 81: Minor Version Number

If an implementer claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to the ATA-3 standard, word 81 should be 0000H or FFFFH.

A value of 0019H reported in word 81 indicates ATA/ATAPI-6 T13 1410D revision 3a guided the implementation.

10.2.1.5.28 Words 82-84: Features/command sets supported

Words 82, 83, and 84 indicate the features and command sets supported.

Word 82

Bit	Function
15	0: Obsolete
14	1: NOP command is supported
13	1: Read Buffer command is supported
12	1: Write Buffer command is supported
11	0: Obsolete
10	0: Host Protected Area feature set is not supported
9	0: Device Reset command is not supported
8	0: Service interrupt is not supported
7	0: Release interrupt is not supported
6	1: Look-ahead is supported
5	1: Write cache is supported
4	0: Packet Command feature set is not supported
3	1: Power Management feature set is supported
2	0: Removable Media feature set is not supported
1	0: Security Mode feature set is not supported
0	0: SMART feature set is not supported

Word 83

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are not valid
14	1: Provides indication that the features/command sets supported words are valid
13-9	0: Reserved
8	0: Set-Max security extension is not supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not supported
3	0: Advanced Power Management feature set is not supported
2	0: CFA feature set is not supported
1	0: Read DMA Queued and Write DMA Queued commands are not supported
0	0: Download Microcode command is not supported

Word 84

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are valid
14	1: Provides indication that the features/command sets supported words are valid
13-0	0: Reserved

10.2.1.5.29 Words 85-87: Features/command sets enabled

Words 85, 86, and 87 indicate features/command sets enabled.

The host can enable/disable the features or command set only if they are supported in Words 82-84.

Word 85

Bit	Function
15	0: Obsolete
14	0: NOP command is not enabled 1: NOP command is enabled
13	0: Read Buffer command is not enabled 1: Read Buffer command is enabled
12	0:Write Buffer command is not enabled 1: Write Buffer command is enabled
11	0: Obsolete
10	0: Host Protected Area feature set is not enabled
9	0: Device Reset command is not enabled
8	0: Service interrupt is not enabled
7	0: Release interrupt is not enabled
6	0: Look-ahead is not enabled 1: Look-ahead is enabled
5	0: Write cache is not enabled 1: Write cache is enabled
4	0: Packet Command feature set is not enabled
3	0: Power Management feature set is not enabled 1: Power Management feature set is enabled
2	0: Removable Media feature set is not enabled
1	0: Security Mode feature set is not supported
0	0: SMART feature set is not enabled

Word 86

Bit	Function
15-9	0: Reserved
8	1: Set-Max security extension supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not enabled
3	0: Advanced Power Management feature set is not supported via the Set Features command
2	0: CFA feature set is not enabled
1	0: Read DMA Queued and Write DMA Queued commands are not enabled
0	0: Download Microcode command is not enabled

Word 87

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are valid
14	1: Provides indication that the features/command sets supported words are valid
13-0	0: Reserved

10.2.1.6 Idle - 97H or E3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97H or E3H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

This command causes the ATA Flash Disk Controller to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic Power-down mode is enabled. If the sector count is zero, the automatic Power-down mode is also enabled, the timer count is set to 3, with each count being 5 ms. Note that this time base (5 msec) is different from the ATA specification.

10.2.1.7 Idle-Immediate - 95H or E1H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	95H or E1H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the ATA Flash Disk Controller to set BSY, enter the Idle mode, clear BSY and generate an interrupt.

10.2.1.8 Initialize-Drive-Parameters - 91H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91H							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Number of Sectors							
Feature (1)	X							

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Drive/Head registers are used by this command.

10.2.1.9 NOP - 00H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	00H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command always fails with the ATA Flash Disk Controller returning command aborted.

10.2.1.10 Read-Buffer - E4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Read-Buffer command enables the host to read the current contents of the ATA Flash Disk Controller's sector buffer. This command has the same protocol as the Read-Sector(s) command

10.2.1.11 Read-DMA - C8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C8H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command executes in a similar manner to the Read-Sector(s) command except for the following:
- the host initializes the DMA channel prior to issuing the command;
- data transfers are qualified by DMARQ and are performed by the DMA channel;
- the ATA Flash Disk Controller issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the DMA transfer phase of a Read-DMA command, the ATA Flash Disk Controller will provide the status of the BSY bit or the DRQ bit until the command is completed.

10.2.1.12 Read-Multiple - C4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the ATA Flash Disk Controller can support up to a block count of 1 as indicated in the Identify-Drive Command information.

The Read-Multiple command is similar to the Read-Sector(s) command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read-Sectors operation except that the number of sectors defined by a Set Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set-Multiple-Mode command, which must be executed prior to the Read-Multiple command. When the Read-Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = remainder (sector count/block count).

If the Read-Multiple command is attempted before the Set-Multiple-Mode command has been executed or when Read-Multiple commands are disabled, the Read-Multiple operation is rejected with an

Aborted Command error. Disk errors encountered during Read-Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read-Sector(s) command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

10.2.1.13 Read-Sector(s) - 20H or 21H

Bit ->	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command (7)	20H or 21H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register. When this command is issued and after each sector of data (except the last one) has been read by the host, the ATA Flash Disk Controller sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 Bytes of data from the buffer.

At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

10.2.1.14 Read-Verify-Sector(s) - 40H or 41H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40H or 41H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is identical to the Read-Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the ATA Flash Disk Controller sets BSY.

When the requested sectors have been verified, the ATA Flash Disk Controller clears BSY and generates an interrupt. Upon command completion, the Command Block registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the verify terminates at the sector where the error occurs. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count register contains the number of sectors not yet verified.

10.2.1.15 Recalibrate - 1XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1XH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a No Operation command to the ATA Flash Disk Controller and is provided for compatibility purposes.

10.2.1.16 Seek - 7XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7XH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a No Operation command to the ATA Flash Disk Controller although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

10.2.1.17 Set-Features - EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 10-5 defines all features that are supported.

TABLE10-5:Features Supported

Feature	Operation
01H	Enable 8-bit data transfers.
02H	Enable Write cache
03H	Set transfer mode based on value in Sector Count register. Table 10-6 defines the values.
09H	Enable Extended Power Operations
0AH	Enable Power Level 1 commands
55H	Disable Read Look Ahead.
66H	Disable Power-on Reset (POR) establishment of defaults at software reset.
69H	NOP - Accepted for backward compatibility.
81H	Disable 8-bit data transfer.
82H	Disable Write Cache
89H	Disable Extended Power operations
8AH	Disable Power Level 1 commands
96H	NOP - Accepted for backward compatibility.
97H	Accepted for backward compatibility. Use of this Feature is not recommended.
9AH	Set the host current source capability Allows trade-off between current drawn and Read/Write speed
BBH	4 Bytes of data apply on Read/Write-Long-Sector commands.
AAH	Enable Read-Look-Ahead
CCH	Enable Power-on Reset (POR) establishment of defaults at software reset.

T10-5.0 1312

Features 01H and 81H are used to enable and clear 8-bit data transfer mode. If the 01H feature command is issued all data transfers will occur on the low order D_7-D_0 data bus and the IOCS16# signal will not be asserted for data register accesses.

Features 02H and 82H allow the host to enable or disable write cache in the ATA Flash Disk Controllers that implement write cache. When the subcommand Disable-Write-Cache is issued, the ATA Flash Disk Controller should initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03H allows the host to select the transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode is selected at all times. The host may change the selected modes by the Set-Features command.

Features 66H and CCH can be used to enable and disable whether the Power-on Reset (POR) Defaults will be set when a software reset occurs.

TABLE10-6:Transfer Mode Values

Mode	Bits [7:3]	Bits [2:0]
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode[1]
Multi-word DMA mode	00100b	mode[1]
Reserved	Other	N/A

T10-6.0 1312

1. Mode = transfer mode number, all other values are not valid

10.2.1.18 Set-Multiple-Mode - C6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command enables the ATA Flash Disk Controller to perform Read and Write-Multiple operations and establishes the block count for these commands. The Sector Count register is loaded with the number of sectors per block. Upon receipt of the command, the ATA Flash Disk Controller sets BSY to 1 and checks the Sector Count register.

If the Sector Count register contains a valid value (see Section 10.2.1.5.12 for details) and the block count is supported, the value is loaded for all subsequent Read-Multiple and Write-Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted Command error is posted, and Read-Multiple and Write-Multiple commands are disabled. If the Sector Count register contains 0 when the command is issued, Read and Write-Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write-Multiple disabled.

10.2.1.19 Set-Sleep-Mode - 99H or E6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99H or E6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the ATA Flash Disk Controller to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 15 milliseconds.

10.2.1.20 Set-WP_PD#-Mode - 8BH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	8BH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	6EH							
Cyl Low (4)	44H							
Sec Num (3)	72H							
Sec Cnt (2)	50H							
Feature (1)	55H or AAH							

This command configures the WP_PD# pin for either the Write Protect mode or the Power-down mode. When the host sends this command to the device with the value AAH in the feature register, the WP_PD# pin is configured for the Write Protect mode described in Section 7.1. The Write Protect mode is the factory default setting. When the host sends this command to the device with the value 55H in the feature register, WP_PD# is configured for the Power-down mode.

All values in the C/D/H register, the Cylinder Low register, the Cylinder High register, the Sector Number register, the Sector Count register, and the Feature register need to match the values shown above, otherwise, the command will be treated as an invalid command.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

10.2.1.21 Standby - 96H or E2H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	96H or E2H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the ATA Flash Disk Controller to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

10.2.1.22 Standby-Immediate - 94H or E0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	94H or E0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the ATA Flash Disk Controller to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

10.2.1.23 Write-Buffer - E8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Write-Buffer command enables the host to overwrite contents of the ATA Flash Disk Controller’s sector buffer with any data pattern desired. This command has the same protocol as the Write-Sector(s) command and transfers 512 Bytes.

10.2.1.24 Write-DMA - CAH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CAH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command executes in a similar manner to Write-Sector(s) except for the following:
- the host initializes the DMA channel prior to issuing the command;
- data transfers are qualified by DMARQ and are performed by the DMA channel;
- the ATA Flash Disk Controller issues only one interrupt per command to indicate that data transfer has terminated and status is available. During the execution of a WRITE DMA command, the ATA Flash Disk Controller will provide status of the BSY bit or the DRQ bit until the command is completed.

10.2.1.25 Write-Multiple - C5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5H							
C/D/H (6)	1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the ATA Flash Disk Controller can support up to a block count of 1 as indicated in the Identify-Drive Command information.

This command is similar to the Write-Sectors command. The ATA Flash Disk Controller sets BSY within 400 ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write-Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set-Multiple-Mode command, which must be executed prior to the Write-Multiple command.

When the Write-Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = remainder (sector count/block).

If the Write-Multiple command is attempted before the Set-Multiple-Mode command has been executed or when Write-Multiple commands are disabled, the Write-Multiple operation will be rejected with an aborted command error.

Errors encountered during Write-Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count register contains the residual number of sectors that need to be transferred for successful completion of the command e.g. each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count register contains 6 and the address is that of the third sector.

10.2.1.26 Write-Sector(s) - 30H or 31H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30H or 31H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register. When this command is accepted, the ATA Flash Disk Controller sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

10.2.1.27 Write-Verify - 3CH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3CH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is similar to the Write-Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write-Sector(s) command.

Advance Information

10.2.2 Error Posting

The following table summarizes the valid status and error values for the ATA Flash Disk Controller command set.

TABLE 10-7: Error and Status Register[1]

	Error Register					Status Register				
Command	**BBK**	**UNC**	**IDNF**	**ABRT**	**AMNF**	**RDY**	**DWF**	**DSC**	**CORR**	**ERR**
Check-Power-Mode				V		V	V	V		V
Execute-Drive-Diagnostic[2]						V		V		V
Flush-Cache				V		V	V	V		V
Format-Track			V	V	V	V	V	V		V
Identify-Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle-Immediate				V		V	V	V		V
Initialize-Drive-Parameters						V		V		V
NOP				V		V	V			V
Read-Buffer				V		V	V	V		V
Read-DMA	V	V	V	V	V	V	V	V	V	V
Read-Multiple	V	V	V	V	V	V	V	V	V	V
Read-Sector(s)	V	V	V	V	V	V	V	V	V	V
Read-Verify-Sector(s)	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Seek			V	V		V	V	V		V
Set-Features				V		V	V	V		V
Set-Multiple-Mode				V		V	V	V		V
Set-Sleep-Mode				V		V	V	V		V
Set-WP_PD#-Mode				V		V		V		V
Standby				V		V	V	V		V
Standby-Immediate				V		V	V	V		V
Write-Buffer				V		V	V	V		V
Write-DMA	V		V	V	V	V	V	V		V
Write-Multiple	V		V	V	V	V	V	V		V
Write-Sector(s)	V		V	V	V	V	V	V		V
Write-Verify	V		V	V	V	V	V	V		V
Invalid-Command-Code				V		V	V	V		V

T10-7.4 1312

1. The host is required to reissue any media access command (such as Read-Sector and Write-Sector) that ends with an error condition.
2. See Table 10-3
   V = valid on this command

11.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D.C. Voltage on Pins[1] I3, I4, O4, and O5 to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Pins[1] I3, I4, O4, and O5 to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
D.C. Voltage on Pins[1] I1, I2, O1, O2, and O6 to Ground Potential. . . . . -0.5V to V_{DDQ}+0.5V
Transient Voltage (<20 ns) on Pins[1] I1, I2, O1, O2, and O6 to Ground Potential. . . . . -2.0V to V_{DDQ}+2.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds). . . . . 300°C
Surface Mount Solder Reflow Temperature . . . . . 260°C for 10 seconds
Output Short Circuit Current[2] . . . . . 50 mA

1. Please refer to Table 3-1 for pin assignment information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

TABLE 11-1: Absolute Maximum Power Pin Stress Ratings

Parameter	Symbol	Conditions
Input Power	V_{DDQ} V_{DD}	-0.3V min to 6.5V max -0.3V min to 4.0V max
Voltage on any flash media interface pin with respect to V_{SS}		-0.5V min to V_{DD} + 0.5V max
Voltage on all other pins with respect to V_{SS}		-0.5V min to V_{DDQ} + 0.5V max

T11-1.0 1312

TABLE 11-2: Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.135-3.465V	4.5-5.5V; 3.135-3.465V
Industrial	-40°C to +85°C	3.135-3.465V	4.75-5.25V; 3.135-3.465V

TABLE 11-3: AC Conditions of Test

Input Rise/Fall Time	10 ns
Output Load	C_L = 100 pF
See Figure 11-1	

Note: All AC specifications are guaranteed by design.

TABLE 11-4: Recommended System Power-on Timing

Symbol	Parameter	Typical	Maximum	Units
$T_{PU-INITIAL}$	Drive Initialization to Ready	3 sec + (0.5 sec/GByte)	100	sec
$T_{PU-READY1}$[1]	Host Power-on/Reset to Ready Operation	400	1000	ms
$T_{PU-WRITE1}$[1]	Host Power-on/Reset to Write Operation	400	1000	ms

T11-4.1 1312

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 11-5: Capacitance (Ta = 25°C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	15 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	9 pF

T11-5.0 1312

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 11-6: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T11-6.0 1312

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

11.1 DC Characteristics

TABLE 11-7: DC Characteristics for Media Interface

Symbol	Type	Parameter	Min	Max	Units	Conditions
V_{IH3}	I3	Input Voltage	2.0		V	V_{DD}=V_{DD} Max
V_{IL3}				0.8		V_{DD}=V_{DD} Min
I_{IL3}	I3Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} Max
I_{U3}	I3U	Input Pull-Up Current	-8	-50	uA	V_{IN} = GND, V_{DD} = V_{DD} Max
I_{D3}	I3D	Input Pull-Down Current	30	200	uA	V_{IN} = V_{DD}, V_{DD} = V_{DD} Max
V_{T+4}	I4	Input Voltage Schmitt Trigger		2.5	V	V_{DD} = V_{DD} Max
V_{T-4}			0.75			V_{DD} = V_{DD} Min
I_{IL4}	I4Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} Max
I_{U4}	I4U	Input Pull-Up Current	-8	-50	uA	V_{IN} = GND, V_{DD} = V_{DD} Max
V_{OH4}	O4	Output Voltage	2.4		V	I_{OH4}=I_{OH4} Min
V_{OL4}				0.4		I_{OL4}=I_{OL4} Max
I_{OH4}		Output Current	-1.5		mA	V_{DD}=V_{DD} Min
I_{OL4}		Output Current		1.5	mA	V_{DD}=V_{DD} Min
V_{OH5}	O5	Output Voltage	2.4		V	I_{OH5}=I_{OH5} Min
V_{OL5}				0.4		I_{OL5}=I_{OL5} Max
I_{OH5}		Output Current	-3		mA	V_{DD}=V_{DD} Min
I_{OL5}		Output Current		3	mA	V_{DD}=V_{DD} Min

T11-7.1 1312

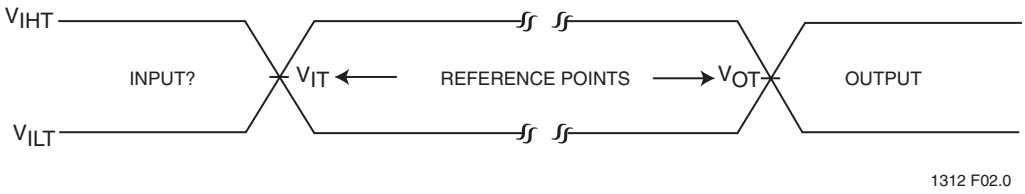
TABLE 11-8: DC Characteristics for Host Interface

Symbol	Type	Parameter	Min	Max	Units	Conditions
V_{IH1}	I1	Input Voltage	2.0V		V	V_{DDQ}=V_{DDQ} Max
V_{IL1}				0.8V		V_{DDQ}=V_{DDQ} Min
I_{IL1}	I1Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DDQ}, V_{DDQ} = V_{DDQ} Max
I_{U1}	I1U	Input Pull-Up Current	-110	-1	uA	V_{OUT} = GND, V_{DDQ} = V_{DDQ} Max
V_{T+2}	I2	Input Voltage Schmitt Trigger		2.0	V	V_{DDQ}=V_{DDQ} Max
V_{T-2}			0.8			V_{DDQ}=V_{DDQ} Min
I_{IL2}	I2Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DDQ}, V_{DDQ} = V_{DDQ} Max
I_{U2}	I2U	Input Pull-Up Current	-110	-1	uA	V_{OUT} = GND, V_{DDQ} = V_{DDQ} Max
V_{OH1}	O1	Output Voltage	2.4		V	I_{OH1}=I_{OH1} Min
V_{OL1}				0.4		I_{OL1}=I_{OL1} Max
I_{OH1}		Output Current	-4		mA	V_{DDQ}=V_{DDQ} Min
I_{OL1}		Output Current		4	mA	V_{DDQ}=V_{DDQ} Min
V_{OH2}	O2	Output Voltage	2.4		V	I_{OH2}=I_{OH2} Min
V_{OL2}				0.4		I_{OL2}=I_{OL2} Max
I_{OH2}		Output Current	-6		mA	V_{DDQ}=3.135V-3.465V
I_{OL2}		Output Current		6	mA	V_{DDQ}=3.135V-3.465V
I_{OH2}		Output Current	-8		mA	V_{DDQ}=4.5V-5.5V
I_{OL2}		Output Current		8	mA	V_{DDQ}=4.5V-5.5V
V_{OH6}	O6	Output Voltage for DASP# pin	2.4		V	I_{OH6}=I_{OH6} Min
V_{OL6}				0.4		I_{OL6}=I_{OL6} Max
I_{OH6}		Output Current for DASP# pin	-3		mA	V_{DDQ}=3.135V-3.465V
I_{OL6}		Output Current for DASP# pin		8	mA	V_{DDQ}=3.135V-3.465V
I_{OH6}		Output Current for DASP# pin	-3		mA	V_{DDQ}=4.5V-5.5V
I_{OL6}		Output Current for DASP# pin		12	mA	V_{DDQ}=4.5V-5.5V
I_{DD}[1,2]	PWR	Power supply current (T_A = 0°C to +70°C)		50	mA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max
I_{DD}[1,2]	PWR	Power supply current (T_A = -40°C to +85°C)		100	mA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max
I_{SP}	PWR	Sleep/Standby/Idle current (T_A = 0°C to +70°C)		100	µA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max
I_{SP}	PWR	Sleep/Standby/Idle current (T_A = -40°C to +85°C)		200	µA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max

T11-8.1 1312

1. Sequential data transfer for 1 sector read data from host interface and write data to media.
2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

11.2 AC Characteristics



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 11-1: AC Input/Output Reference Waveforms

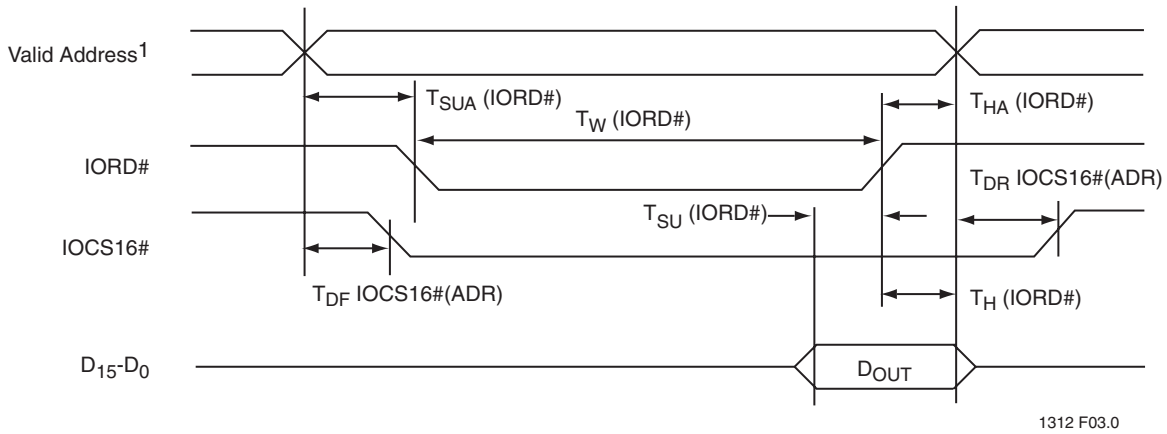
11.2.1 Host Side Interface I/O Input (Read) Timing Specification

TABLE 11-9: Host Side Interface I/O Read Timing

Symbol	Parameter	Min	Max	Units
T_{SU} (IORD#)	Data Setup before IORD#	20	-	ns
T_H (IORD#)	Data Hold following IORD#	5	-	ns
T_W (IORD#)	IORD# Width Time	70	-	ns
T_{SUA} (IORD#)	Address Setup before IORD#	25	-	ns
T_{HA} (IORD#)	Address Hold following IORD#	10	-	ns
T_{DF} IOCS16#(ADR)	IOCS16# Delay Falling from Address	-	20	ns
T_{DR} IOCS16#(ADR)	IOCS16# Delay Rising from Address	-	20	ns

T11-9.0 1312

Note: The maximum load on IOCS16# is 1 LSTTL with 50pF total load.
All AC specifications are guaranteed by design.



1. Valid Address consists of signals CS1FX#, CS3FX# and A_2-A_0.

FIGURE 11-2: Host Side Interface I/O Read Timing Diagram

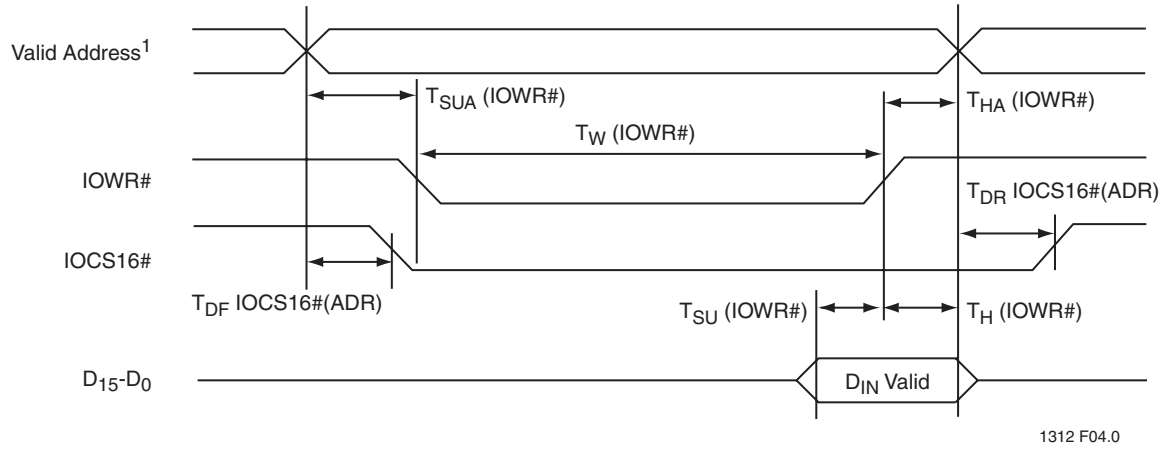
11.2.2 Host Side Interface I/O Output (Write) Timing Specification

TABLE 11-10: Host Side Interface I/O Write Timing Specification

Symbol	Parameter	Min	Max	Units
T_{SU} (IOWR#)	Data Setup before IOWR#	20	-	ns
T_H (IOWR#)	Data Hold following IOWR#	10	-	ns
T_W (IOWR#)	IOWR# Width Time	70	-	ns
T_{SUA} (IOWR#)	Address Setup before IOWR#	25	-	ns
T_{HA} (IOWR#)	Address Hold following IOWR#	10	-	ns
T_{DF} IOCS16#(ADR)	IOCS16# Delay Falling from Address	-	20	ns
T_{DR} IOCS16#(ADR)	IOCS16# Delay Rising from Address	-	20	ns

T11-10.0 1312

Note: The maximum load on IOCS16# is 1 LSTTL with 50pF total load.
All AC specifications are guaranteed by design.



1. Valid Address consists of signals CS1FX#, CS3FX# and A_2-A_0.

FIGURE 11-3: Host Side Interface I/O Write Timing Diagram

11.2.3 Multi-word DMA Data Transfer

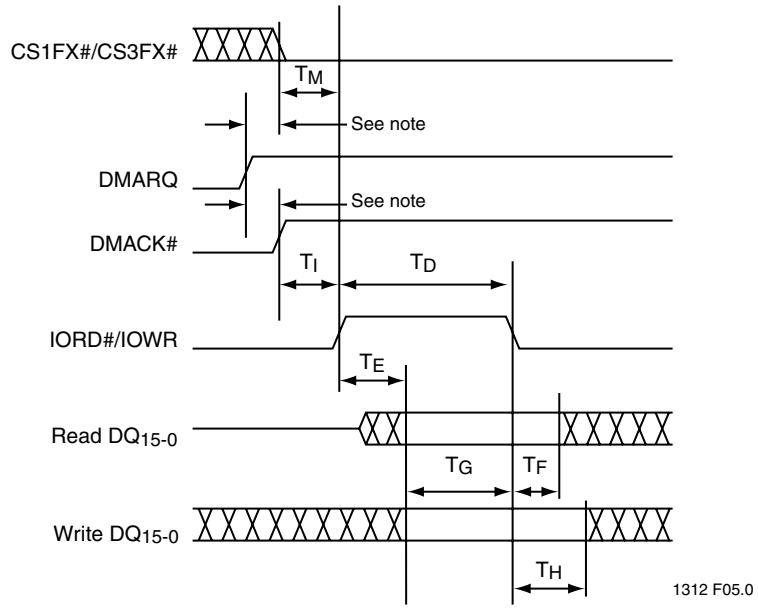
TABLE 11-11: Multi-word DMA Timing Parameters - Mode 2

Symbol	Parameter	Min	Max	Units
T_0[1]	Cycle Time	120		ns
T_D	IORD#/IOWD# Asserted Pulse Width	70		ns
T_E	IORD# Data Access		50	ns
T_F	IORD# Data Hold	5		ns
T_G	IORD#/IOWD# Data Setup	20		ns
T_H	IOWD# Data Hold	10		ns
T_I	DMACK# to IORD#/IOWR# Setup	0		ns
T_J	IORD#/IOWD# to DMACK Hold	5		ns
T_{KR}	IORD# Negated Pulse Width	25		ns
T_{KW}	IOWD# Negated Pulse Width	25		ns
T_{LR}	IORD# to DMARQ Delay		35	ns
T_{LW}	IOWD# to DMARQ Delay		35	ns
T_M	CS(1:0) Valid to IORD#/IOWD#	25		ns
T_N	CS(1:0) Hold	10		ns
T_Z	DMACK# to Read Data Released		25	ns

T11-11.0 1312

1. T_0 is the minimum total cycle time, T_D is the minimum IORD#/IOWD# assertion time, and T_K (T_{KR} or T_{KW}, as appropriate) is the minimum IORD#/IOWD# negation time. A host should lengthen T_D and/or T_K to ensure that T_0 is equal to the value reported in the device ID.

Note: All AC specifications are guaranteed by design.



Note: The host should not assert DMACK# or negate both CS1FX# and CS3FX# until the assertion of DMARQ is detected. The maximum time from the assertion of DMARQ to the assertion of DMACK# or the negation of both CS0 and CS1 is not defined.

FIGURE 11-4: Initiating a Multi-word DMA Data Transfer

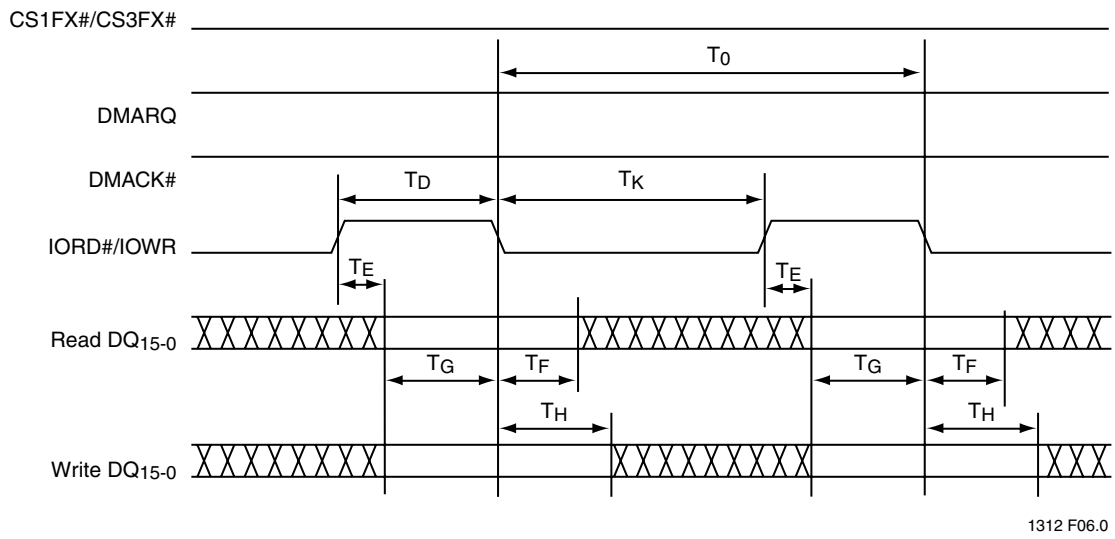
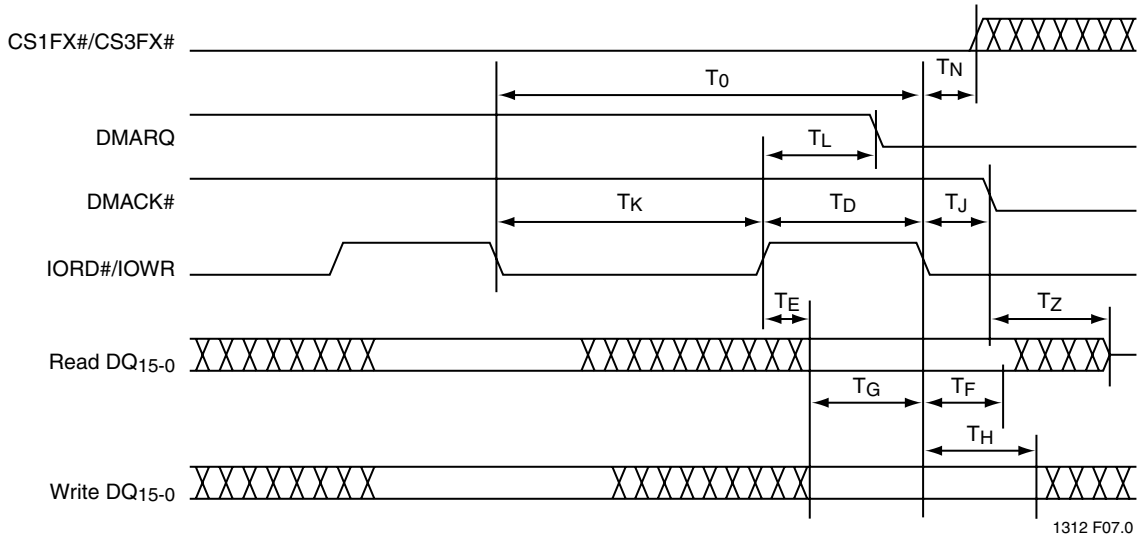
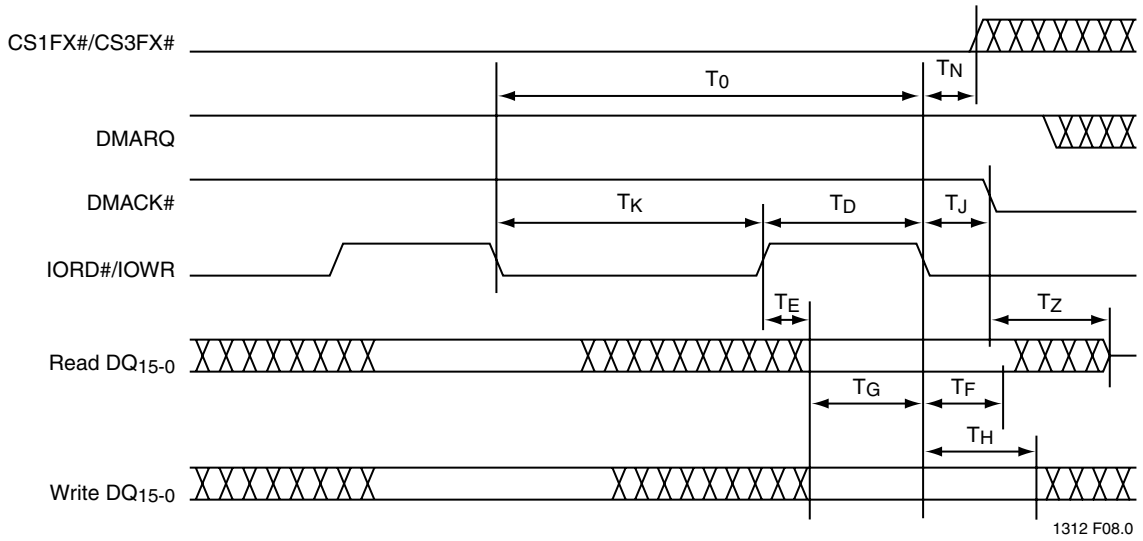


FIGURE 11-5: Sustaining a Multi-word DMA Data Transfer



Note: To terminate the data burst, the Device shall negate DMARQ within the T_L of the assertion of the current IORD# or IOWR# pulse. The last data word for the burst should be transferred by the negation of the current IORD# or IOWR# pulse. If all data for the command has not been transferred, the device shall reassert DMARQ again at any later time to resume the DMA operation.

FIGURE 11-6: Device Terminates a Multi-word DMA Data Transfer



Note: 1. To terminate the transmission of a data burst, the host should negate DMACK# within the specified time after a IORD# or IOWR# pulse. No further IORD# or IOWR# pulses shall be asserted for this burst.
2. If the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK# or may negate DMARQ at any time after detecting that DMACK# has been negated.

FIGURE 11-7: Host Terminates a Multi-word DMA Data Transfer

11.2.4 Media Side Interface I/O Timing Specifications

TABLE 11-12: SST55LD019M Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{CLS}	FCLE Setup Time	20	-	ns
T_{CLH}	FCLE Hold Time	40	-	ns
T_{CS}	FCE# Setup Time	40	-	ns
T_{CH}	FCE# Hold Time for Command/Data Write Cycle	40	-	ns
T_{CHR}	FCE# Hold Time for Sequential Read Last Cycle	-	40	ns
T_{WP}	FWE# Pulse Width	20	-	ns
T_{WH}	FWE# High Hold Time	20	-	ns
T_{WC}	Write Cycle Time	40	-	ns
T_{ALS}	FALE Setup Time	20	-	ns
T_{ALH}	FALE Hold Time	40	-	ns
T_{DS}	FAD[15:0] Setup Time	20	-	ns
T_{DH}	FAD[15:0] Hold Time	20	-	ns
T_{RP}	FRE# Pulse Width	20	-	ns
T_{RR}	Ready to FRE# Low	40	-	ns
T_{REA}	FRE# Data Setup Access Time	20	-	ns
T_{RC}	Read Cycle Time	40	-	ns
T_{REH}	FRE# High Hold Time	30	-	ns
T_{RHZ}	FRE# High to Data Hi-Z	5	-	ns

T11-12.0 1312

Note: All AC specifications are guaranteed by design.

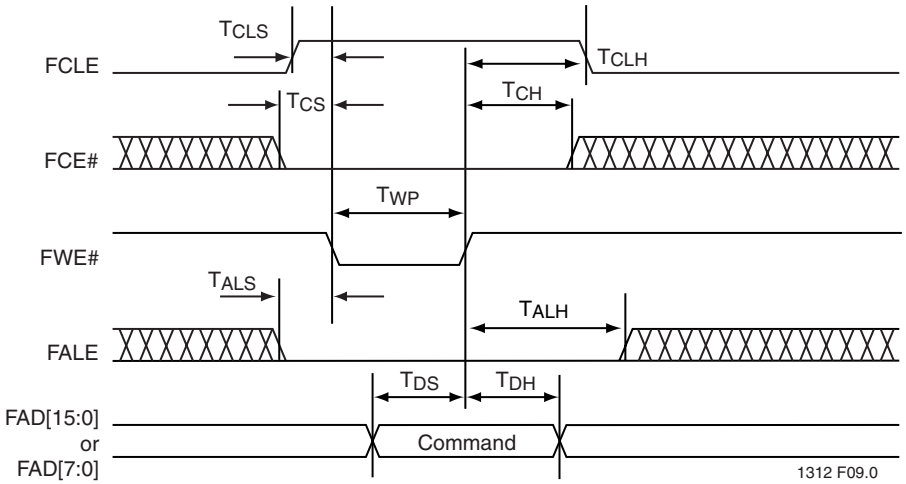


FIGURE 11-8: Media Command Latch Cycle

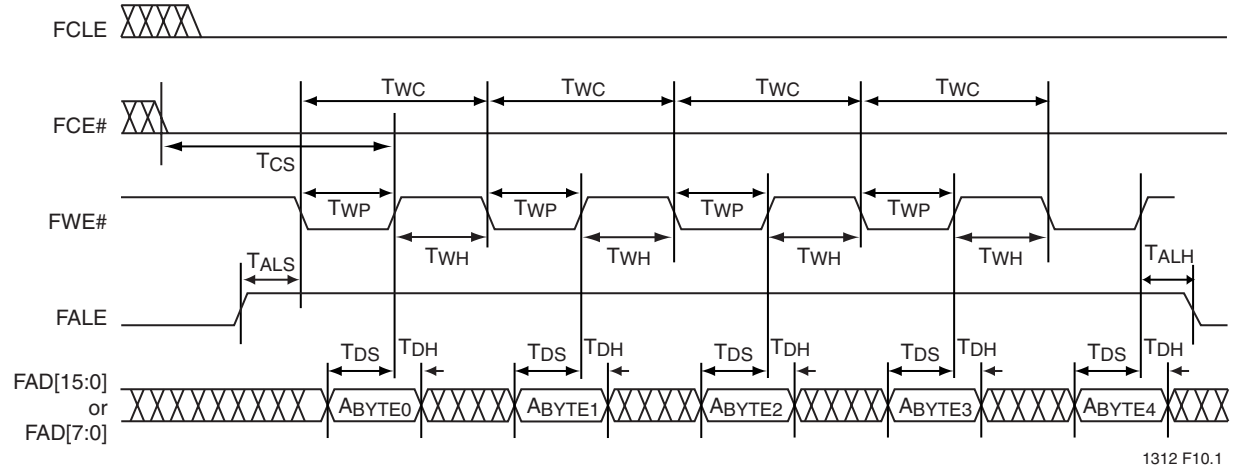


FIGURE 11-9: Media Address Latch Cycle

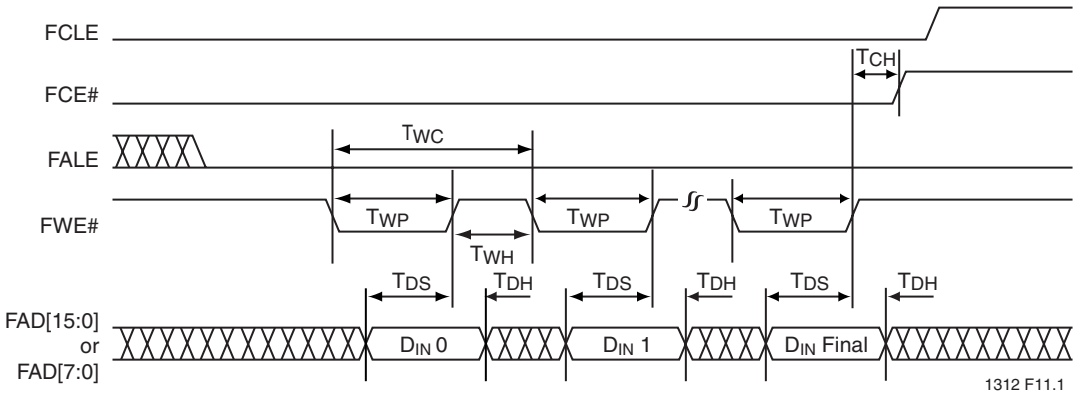


FIGURE 11-10: Media Data Loading Latch Cycle

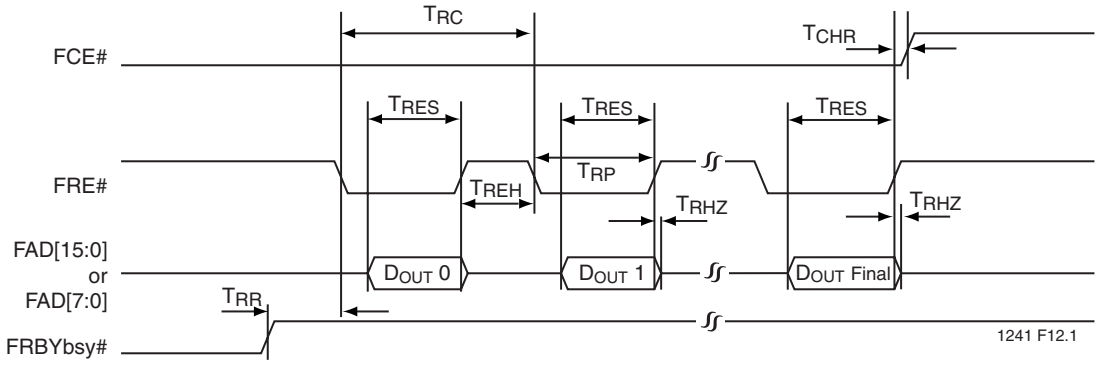


FIGURE 11-11: Media Data Read Cycle

12.0 APPENDIX

12.1 Differences between SST's ATA Flash Disk Controller and ATA/ATAPI-5 Specifications

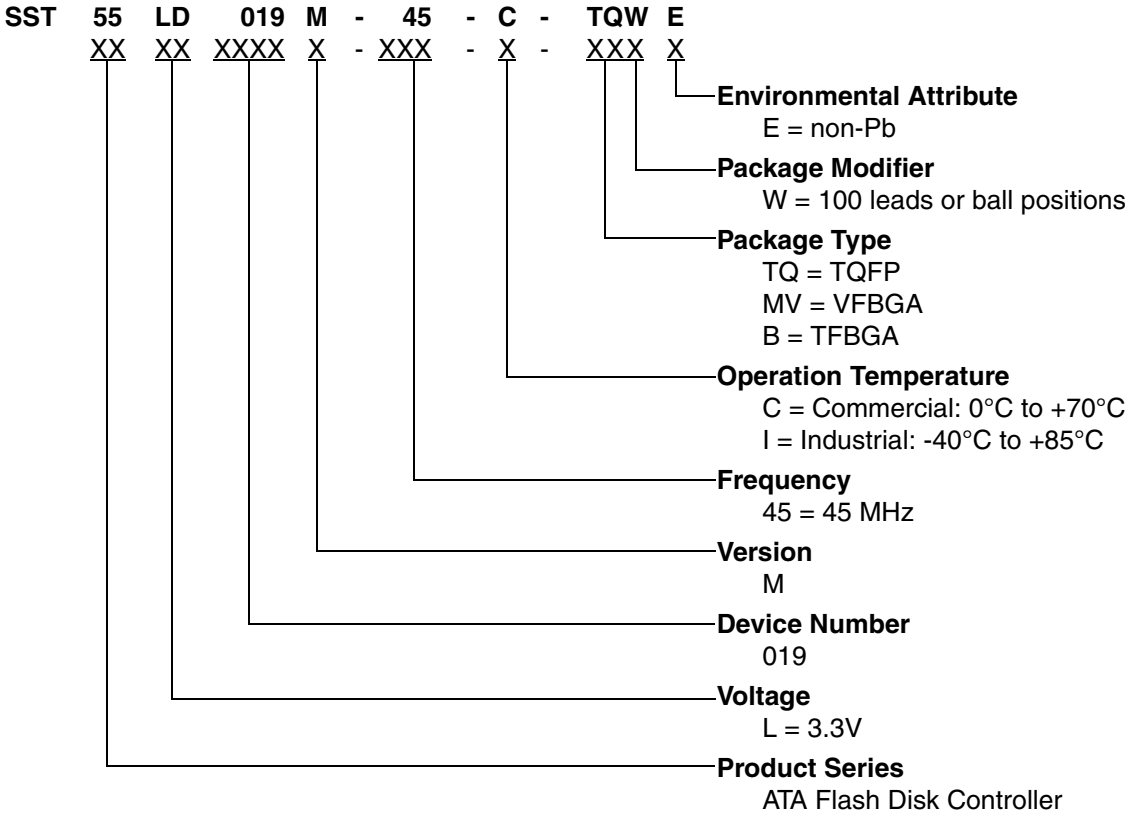
12.1.1 Idle Timer

The Idle timer uses an incremental value of 5 ms, rather than the 5 sec minimum increment value specified in ATA specifications.

12.1.2 Recovery from Sleep Mode

For ATA Flash Disk Controller devices, recovery from sleep mode is accomplished by simply issuing another command to the device. A hardware or software reset is not required.

13.0 PRODUCT ORDERING INFORMATION



13.1 Valid Combinations

Valid combinations for SST55LD019M

SST55LD019M-45-C-TQWE	SST55LD019M-45-C-BWE	SST55LD019M-45-C-MVWE
SST55LD019M-45-I-TQWE	SST55LD019M-45-I-BWE	SST55LD019M-45-I-MVWE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

14.0 PACKAGING DIAGRAM

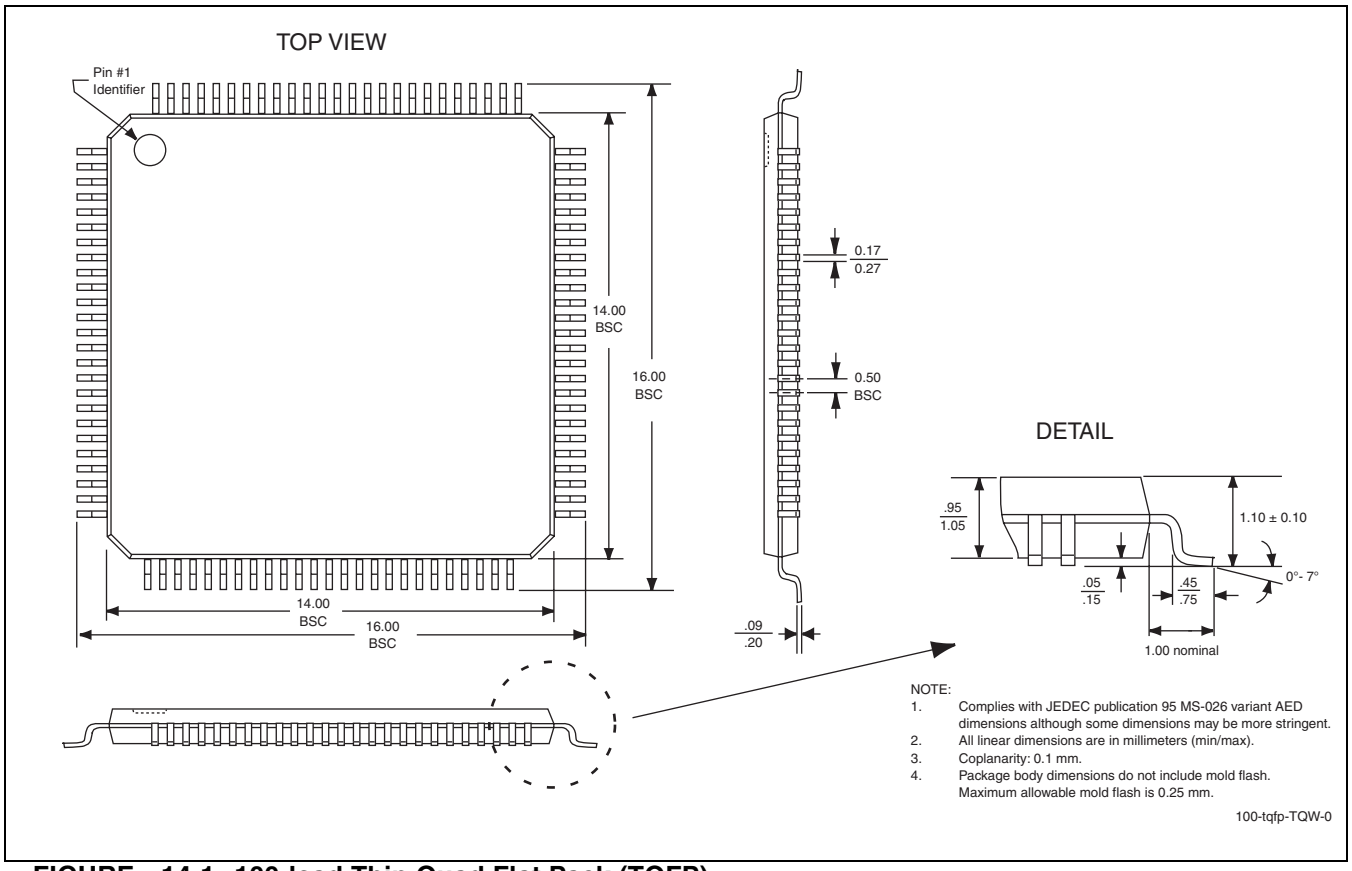
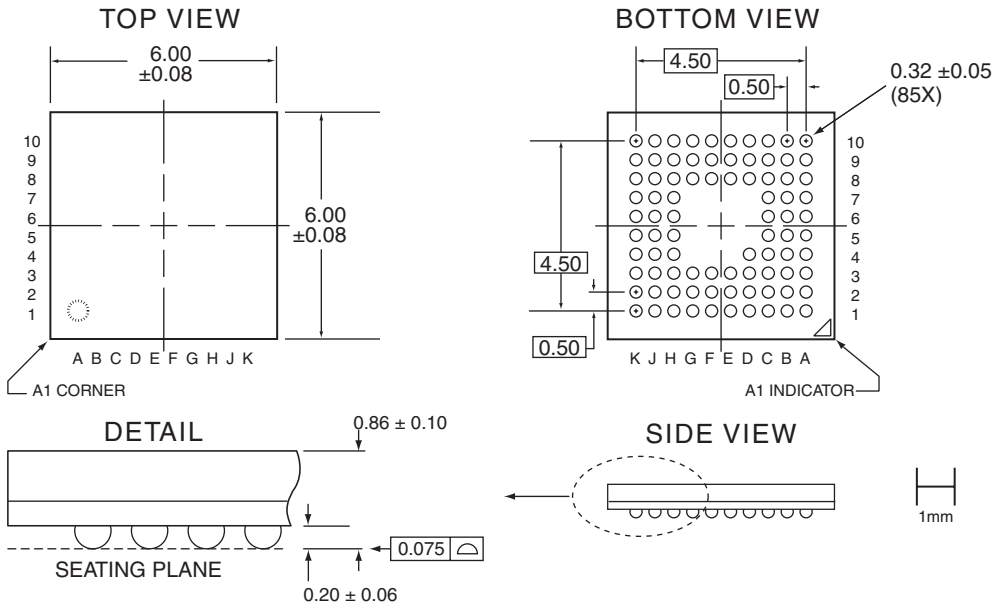


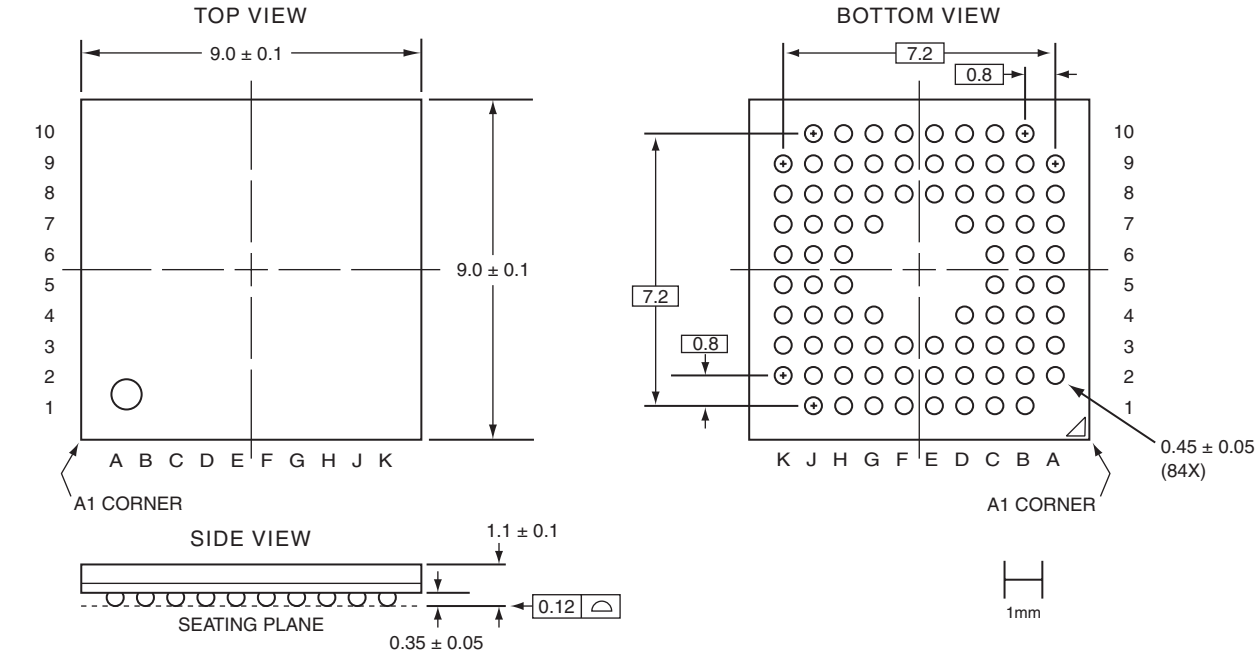
FIGURE 14-1: 100-lead Thin Quad Flat Pack (TQFP)
SST Package Code: TQW



Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-225, this specific package is not registered
2. All linear dimensions are in millimeters
3. Coplanarity: 0.075 mm
4. Ball opening size is 0.29 mm (± 0.05 mm)

85-vfbga-MVW-6x6-32mic-0.0

FIGURE 14-2: 85-ball Very-Thin, Fine-Pitch, Ball Grid Array (VFBGA)
SST Package Code: MVW



Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-210, this specific package is not registered.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. Ball opening size is 0.38 mm (± 0.05 mm)

84-tfbga-BW-9x9-450mic-2

FIGURE 14-3: 84-ball Thin, Fine-pitch, Ball Grid Array (TFBGA)
SST Package Code: BW

TABLE 14-1: Revision History

Number	Description	Date
00	• S71312: Initial release of the Data Sheet	Feb 2006
01	• Updated V_{DD} and V_{DDQ} in Table 11-2 on page 45	Dec 2006