Preliminary TOSHIBA CMOS Digital Integrated Circuits Silicon Monolithic

JBT6K47-AS

Source Driver for TFT LCD Panels

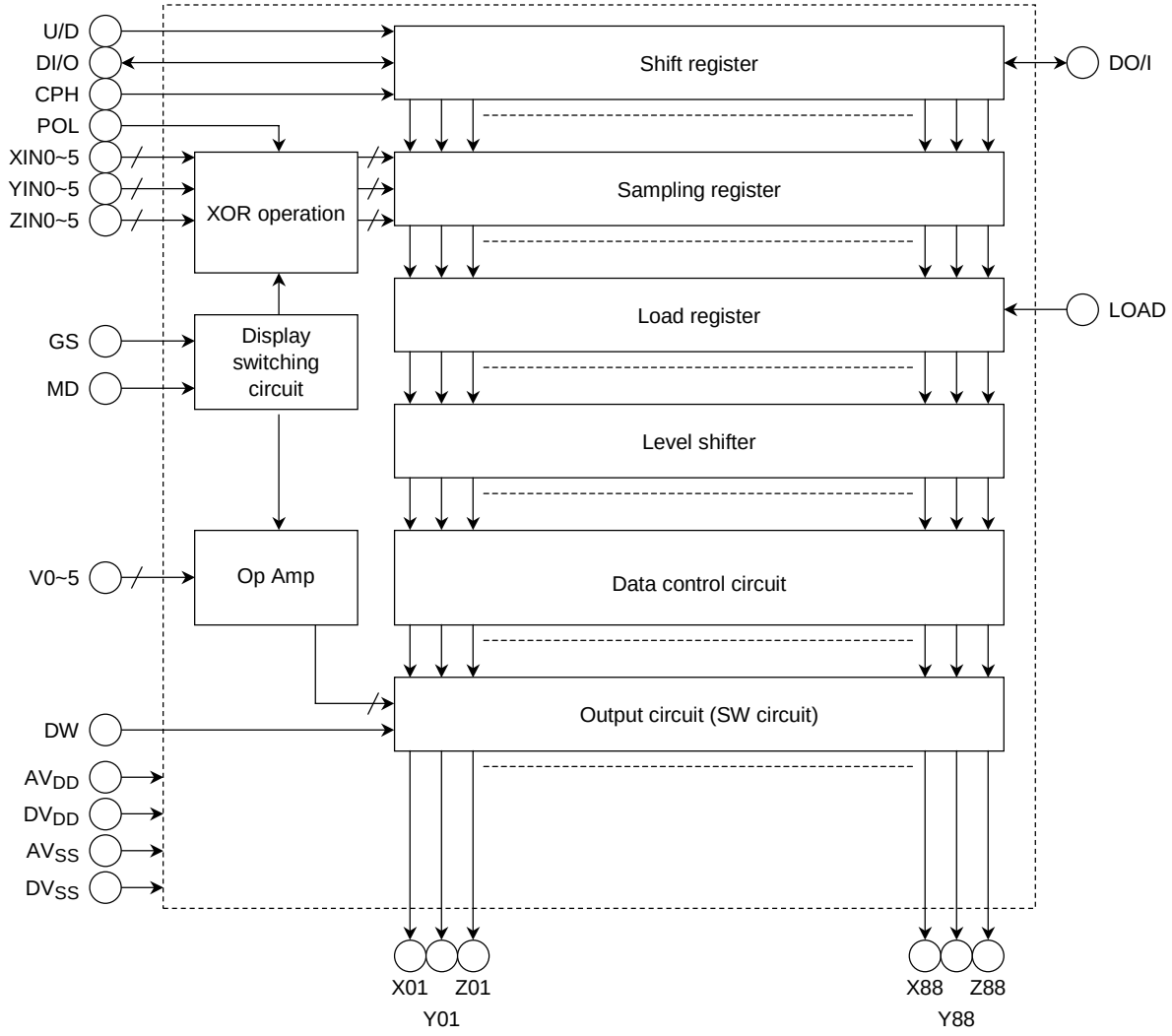
The JBT6K47-AS is a 64 gray-level, 240-channel-output source driver for TFT LCD panels. 6-bit digital input enable to display colors using internal DA converter and five external power supplies. Also, JBT6K47-AS incorporates power saving function to control recognition of the grayscale data input. When display performance is not necessary, such as in a portable device, JBT6K47-AS ignores the grayscale input data.

Based on high-speed CMOS, the JBT6K47-AS offers both low power consumption and high-speed operation.

Features

- Grayscale data: 18-bit digital (3 outputs × 6 bits) parallel transfer method, selectable write direction
- Panel drive outputs: 240 outputs
- Grayscale levels: Capable of switching 2-grayscale mode and 16 grayscale/64 grayscale mode, and capable of reference analog voltage inputs.
- High-speed operation: 5 MHz (max)
- Display mode: Normal display mode
- Power supply voltage: Digital power supply voltage (DV_{DD}) .....2.5 to 3.6 V
  Analog power supply voltage (AV_{DD}).....4.5 to 5.6 V
- Operating temperature: −20 to 75°C
- Package: Gold bump chip
- CMOS process
- Cascading multiple devices

Block Diagram



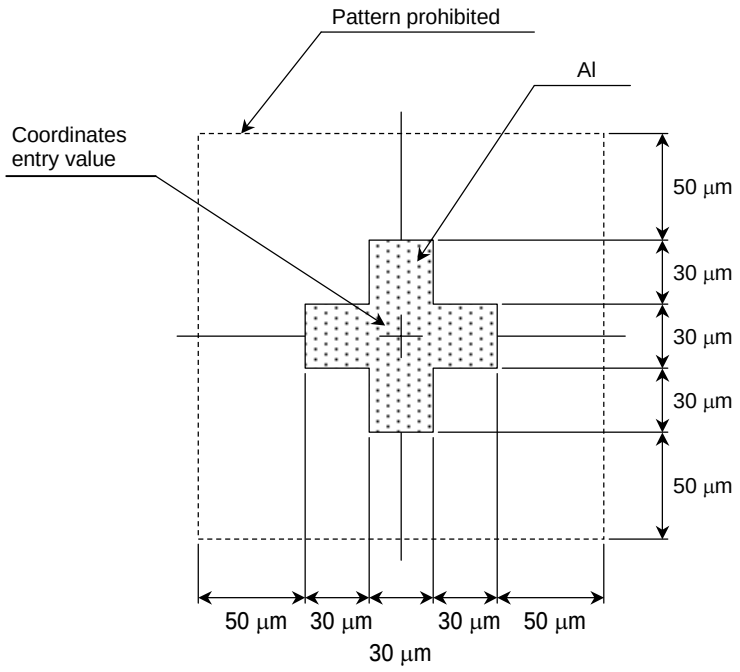
PAD Coordinates

Item		Size	Unit
Chip size		12600 × 2350	μm
Chip end coordinates	(1)	−6300, 1175	μm
	(2)	−6300, −1175	
	(3)	6300, −1175	
	(4)	6300, 1175	
Bump pitch		43	μm
Bump height		(15)	μm

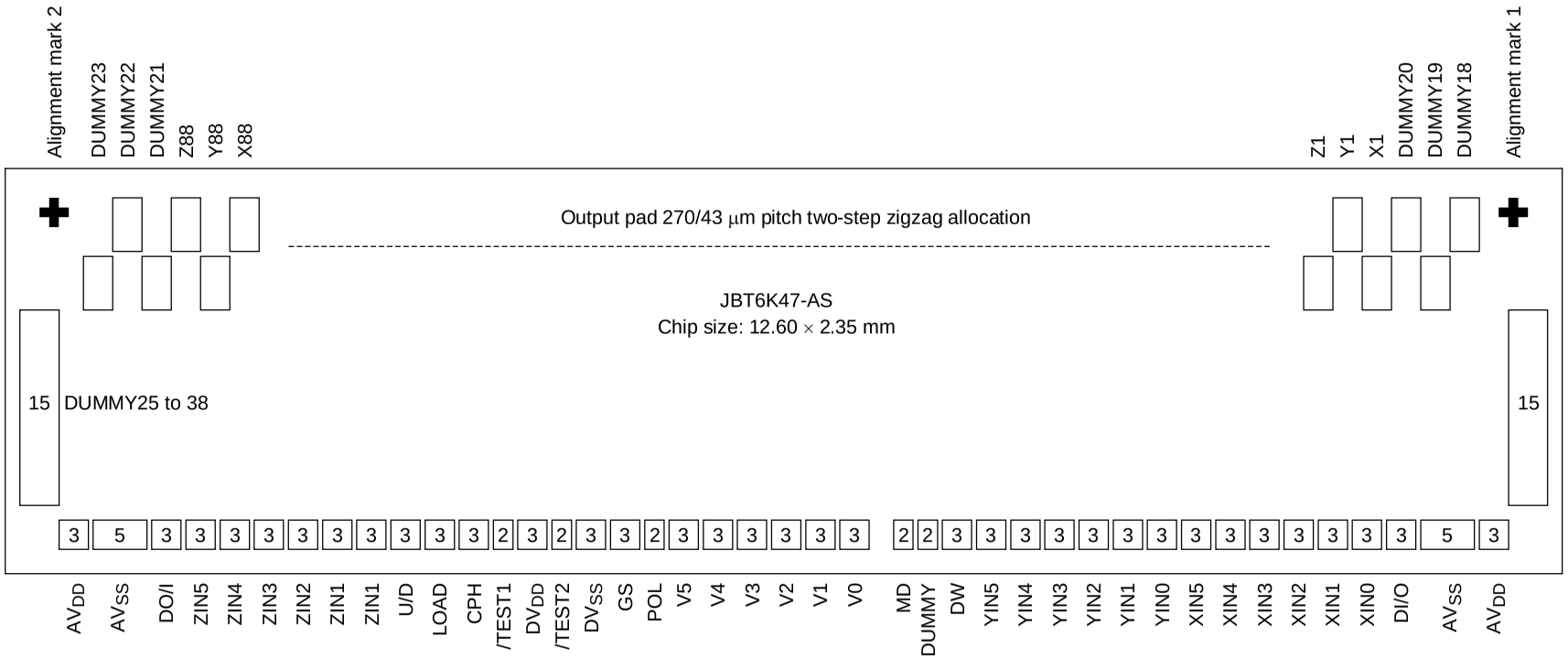
Pin Name	Numbers of Pin
Input pin	123 (Except dummy pins)
Output pin	264 (Except dummy pins)
TEG pin	8
DUMMY pin	38
Alignment mark	2

Note 1: The TEG pin is a test pin reserved for electrical characteristics measurements and must be left open.

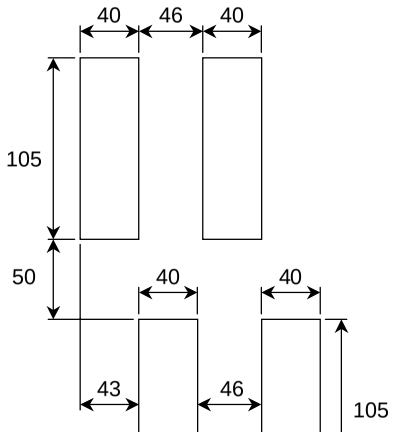
Alignment mark



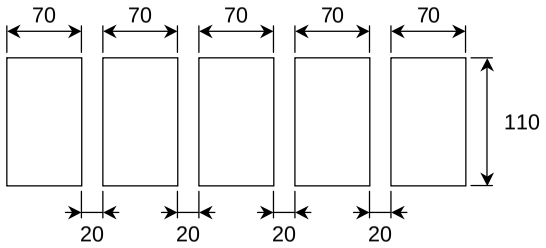
PAD Layout



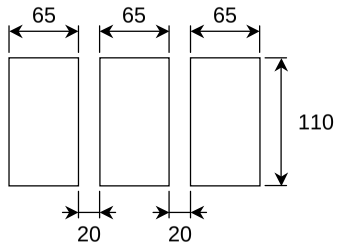
- Output pins (X1~Z88)



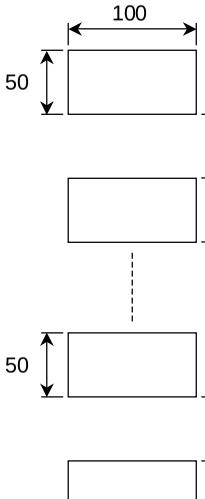
- Power supply pins (AV_{SS})



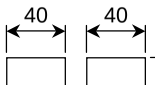
- Power supply pins (AV_{DD}, DV_{DD}, DV_{SS}, V0-V5)



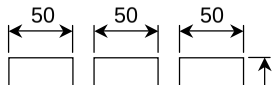
- Short-side dummy pins



- Input pins (/TEST1, /TEST2, POL, MD)



- Input pins (others)



PAD Coordinates (1)

[Unit: μm]

No.	Name	X POINT	Y POINT
1	AV_{DD}	−5994	−996
2	AV_{DD}	−5909	−996
3	AV_{DD}	−5824	−996
4	AV_{SS}	−5679	−996
5	AV_{SS}	−5589	−996
6	AV_{SS}	−5499	−996
7	AV_{SS}	−5409	−996
8	AV_{SS}	−5319	−996
9	DO/I	−5171	−996
10	DO/I	−5101	−996
11	DO/I	−5031	−996
12	ZIN5	−4911	−996
13	ZIN5	−4841	−996
14	ZIN5	−4771	−996
15	ZIN4	−4621	−996
16	ZIN4	−4551	−996
17	ZIN4	−4481	−996
18	ZIN3	−4361	−996
19	ZIN3	−4291	−996
20	ZIN3	−4221	−996
21	ZIN2	−4071	−996
22	ZIN2	−4001	−996
23	ZIN2	−3931	−996
24	ZIN1	−3811	−996
25	ZIN1	−3741	−996
26	ZIN1	−3671	−996
27	ZIN0	−3521	−996
28	ZIN0	−3451	−996
29	ZIN0	−3381	−996
30	U/D	−3261	−996
31	U/D	−3191	−996
32	U/D	−3121	−996
33	LOAD	−2971	−996
34	LOAD	−2901	−996
35	LOAD	−2831	−996
36	CPH	−2711	−996
37	CPH	−2641	−996
38	CPH	−2571	−996
39	/TEST1	−2404	−996
40	/TEST1	−2344	−996
41	DV_{DD}	−2221	−996
42	DV_{DD}	−2136	−996
43	DV_{DD}	−2051	−996
44	/TEST2	−1920	−996
45	/TEST2	−1860	−996
46	DV_{SS}	−1737	−996
47	DV_{SS}	−1652	−996
48	DV_{SS}	−1567	−996
49	GS	−1409	−996
50	GS	−1339	−996
51	GS	−1269	−996
52	POL	−1154	−996
53	POL	−1094	−996
54	V5	−873	−996
55	V5	−788	−996
56	V5	−703	−996
57	V4	−568	−996
58	V4	−483	−996
59	V4	−398	−996
60	V3	−233	−996
61	V3	−148	−996
62	V3	−63	−996
63	V2	72	−996
64	V2	157	−996
65	V2	242	−996
66	V1	407	−996
67	V1	492	−996
68	V1	577	−996
69	V0	712	−996
70	V0	797	−996
71	V0	882	−996
72	MD	1103	−996
73	MD	1163	−996
74	DUMMY1	1278	−996
75	DUMMY2	1348	−996
76	DW	1472	−996
77	DW	1542	−996
78	DW	1612	−996
79	YIN5	1732	−996
80	YIN5	1802	−996
81	YIN5	1872	−996
82	YIN4	2022	−996
83	YIN4	2092	−996
84	YIN4	2162	−996
85	YIN3	2282	−996
86	YIN3	2352	−996
87	YIN3	2422	−996
88	YIN2	2572	−996
89	YIN2	2642	−996
90	YIN2	2712	−996
91	YIN1	2832	−996
92	YIN1	2902	−996
93	YIN1	2972	−996
94	YIN0	3122	−996
95	YIN0	3192	−996
96	YIN0	3262	−996
97	XIN5	3382	−996
98	XIN5	3452	−996
99	XIN5	3522	−996
100	XIN4	3672	−996
101	XIN4	3742	−996
102	XIN4	3812	−996
103	XIN3	3932	−996
104	XIN3	4002	−996
105	XIN3	4072	−996
106	XIN2	4222	−996
107	XIN2	4292	−996
108	XIN2	4362	−996
109	XIN1	4482	−996
110	XIN1	4552	−996
111	XIN1	4622	−996
112	XIN0	4772	−996
113	XIN0	4842	−996
114	XIN0	4912	−996
115	DI/O	5032	−996
116	DI/O	5102	−996
117	DI/O	5172	−996
118	AV_{SS}	5321	−996
119	AV_{SS}	5411	−996
120	AV_{SS}	5501	−996
121	AV_{SS}	5591	−996
122	AV_{SS}	5681	−996
123	AV_{DD}	5824	−996
124	AV_{DD}	5909	−996
125	AV_{DD}	5994	−996
126	DUMMY3	6146	−785
127	DUMMY4	6146	−685
128	DUMMY5	6146	−585
129	DUMMY6	6146	−485

PAD Coordinates (2)

[Unit: μm]

No.	Name	X POINT	Y POINT
130	DUMMY7	6146	−385
131	DUMMY8	6146	−285
132	DUMMY9	6146	−185
133	DUMMY10	6146	−85
134	DUMMY11	6146	15
135	DUMMY12	6146	115
136	DUMMY13	6146	215
137	DUMMY14	6146	315
138	DUMMY15	6146	415
139	DUMMY16	6146	515
140	DUMMY17	6146	615
141	DUMMY18	5784	1015
142	DUMMY19	5741	860
143	DUMMY20	5698	1015
144	X1	5655	860
145	Y1	5612	1015
146	Z1	5569	860
147	X2	5526	1015
148	Y2	5483	860
149	Z2	5440	1015
150	X3	5397	860
151	Y3	5354	1015
152	Z3	5311	860
153	X4	5268	1015
154	Y4	5225	860
155	Z4	5182	1015
156	X5	5139	860
157	Y5	5096	1015
158	Z5	5053	860
159	X6	5010	1015
160	Y6	4967	860
161	Z6	4924	1015
162	X7	4881	860
163	Y7	4838	1015
164	Z7	4795	860
165	X8	4752	1015
166	Y8	4709	860
167	Z8	4666	1015
168	X9	4623	860
169	Y9	4580	1015
170	Z9	4537	860
171	X10	4494	1015
172	Y10	4451	860
173	Z10	4408	1015
174	X11	4365	860
175	Y11	4322	1015
176	Z11	4279	860
177	X12	4236	1015
178	Y12	4193	860
179	Z12	4150	1015
180	X13	4107	860
181	Y13	4064	1015
182	Z13	4021	860
183	X14	3978	1015
184	Y14	3935	860
185	Z14	3892	1015
186	X15	3849	860
187	Y15	3806	1015
188	Z15	3763	860
189	X16	3720	1015
190	Y16	3677	860
191	Z16	3634	1015
192	X17	3591	860
193	Y17	3548	1015
194	Z17	3505	860
195	X18	3462	1015
196	Y18	3419	860
197	Z18	3376	1015
198	X19	3333	860
199	Y19	3290	1015
200	Z19	3247	860
201	X20	3204	1015
202	Y20	3161	860
203	Z20	3118	1015
204	X21	3075	860
205	Y21	3032	1015
206	Z21	2989	860
207	X22	2946	1015
208	Y22	2903	860
209	Z22	2860	1015
210	X23	2817	860
211	Y23	2774	1015
212	Z23	2731	860
213	X24	2688	1015
214	Y24	2645	860
215	Z24	2602	1015
216	X25	2559	860
217	Y25	2516	1015
218	Z25	2473	860
219	X26	2430	1015
220	Y26	2387	860
221	Z26	2344	1015
222	X27	2301	860
223	Y27	2258	1015
224	Z27	2215	860
225	X28	2172	1015
226	Y28	2129	860
227	Z28	2086	1015
228	X29	2043	860
229	Y29	2000	1015
230	Z29	1957	860
231	X30	1914	1015
232	Y30	1871	860
233	Z30	1828	1015
234	X31	1785	860
235	Y31	1742	1015
236	Z31	1699	860
237	X32	1656	1015
238	Y32	1613	860
239	Z32	1570	1015
240	X33	1527	860
241	Y33	1484	1015
242	Z33	1441	860
243	X34	1398	1015
244	Y34	1355	860
245	Z34	1312	1015
246	X35	1269	860
247	Y35	1226	1015
248	Z35	1183	860
249	X36	1140	1015
250	Y36	1097	860
251	Z36	1054	1015
252	X37	1011	860
253	Y37	968	1015
254	Z37	925	860
255	X38	882	1015
256	Y38	839	860
257	Z38	796	1015
258	X39	753	860

PAD Coordinates (3)

[Unit: μm]

No.	Name	X POINT	Y POINT
259	Y39	710	1015
260	Z39	667	860
261	X40	624	1015
262	Y40	581	860
263	Z40	538	1015
264	X41	495	860
265	Y41	452	1015
266	Z41	409	860
267	X42	366	1015
268	Y42	323	860
269	Z42	280	1015
270	X43	237	860
271	Y43	194	1015
272	Z43	151	860
273	X44	108	1015
274	Y44	65	860
275	Z44	22	1015
276	X45	−21	860
277	Y45	−64	1015
278	Z45	−107	860
279	X46	−150	1015
280	Y46	−193	860
281	Z46	−236	1015
282	X47	−279	860
283	Y47	−322	1015
284	Z47	−365	860
285	X48	−408	1015
286	Y48	−451	860
287	Z48	−494	1015
288	X49	−537	860
289	Y49	−580	1015
290	Z49	−623	860
291	X50	−666	1015
292	Y50	−709	860
293	Z50	−752	1015
294	X51	−795	860
295	Y51	−838	1015
296	Z51	−881	860
297	X52	−924	1015
298	Y52	−967	860
299	Z52	−1010	1015
300	X53	−1053	860
301	Y53	−1096	1015
302	Z53	−1139	860
303	X54	−1182	1015
304	Y54	−1225	860
305	Z54	−1268	1015
306	X55	−1311	860
307	Y55	−1354	1015
308	Z55	−1397	860
309	X56	−1440	1015
310	Y56	−1483	860
311	Z56	−1526	1015
312	X57	−1569	860
313	Y57	−1612	1015
314	Z57	−1655	860
315	X58	−1698	1015
316	Y58	−1741	860
317	Z58	−1784	1015
318	X59	−1827	860
319	Y59	−1870	1015
320	Z59	−1913	860
321	X60	−1956	1015
322	Y60	−1999	860
323	Z60	−2042	1015
324	X61	−2085	860
325	Y61	−2128	1015
326	Z61	−2171	860
327	X62	−2214	1015
328	Y62	−2257	860
329	Z62	−2300	1015
330	X63	−2343	860
331	Y63	−2386	1015
332	Z63	−2429	860
333	X64	−2472	1015
334	Y64	−2515	860
335	Z64	−2558	1015
336	X65	−2601	860
337	Y65	−2644	1015
338	Z65	−2687	860
339	X66	−2730	1015
340	Y66	−2773	860
341	Z66	−2816	1015
342	X67	−2859	860
343	Y67	−2902	1015
344	Z67	−2945	860
345	X68	−2988	1015
346	Y68	−3031	860
347	Z68	−3074	1015
348	X69	−3117	860
349	Y69	−3160	1015
350	Z69	−3203	860
351	X70	−3246	1015
352	Y70	−3289	860
353	Z70	−3332	1015
354	X71	−3375	860
355	Y71	−3418	1015
356	Z71	−3461	860
357	X72	−3504	1015
358	Y72	−3547	860
359	Z72	−3590	1015
360	X73	−3633	860
361	Y73	−3676	1015
362	Z73	−3719	860
363	X74	−3762	1015
364	Y74	−3805	860
365	Z74	−3848	1015
366	X75	−3891	860
367	Y75	−3934	1015
368	Z75	−3977	860
369	X76	−4020	1015
370	Y76	−4063	860
371	Z76	−4106	1015
372	X77	−4149	860
373	Y77	−4192	1015
374	Z77	−4235	860
375	X78	−4278	1015
376	Y78	−4321	860
377	Z78	−4364	1015
378	X79	−4407	860
379	Y79	−4450	1015
380	Z79	−4493	860
381	X80	−4536	1015
382	Y80	−4579	860
383	Z80	−4622	1015
384	X81	−4665	860
385	Y81	−4708	1015
386	Z81	−4751	860
387	X82	−4794	1015

PAD Coordinates (4) [Unit: μm]

No.	Name	X POINT	Y POINT
388	Y82	−4837	860
389	Z82	−4880	1015
390	X83	−4923	860
391	Y83	−4966	1015
392	Z83	−5009	860
393	X84	−5052	1015
394	Y84	−5095	860
395	Z84	−5138	1015
396	X85	−5181	860
397	Y85	−5224	1015
398	Z85	−5267	860
399	X86	−5310	1015
400	Y86	−5353	860
401	Z86	−5396	1015
402	X87	−5439	860
403	Y87	−5482	1015
404	Z87	−5525	860
405	X88	−5568	1015
406	Y88	−5611	860
407	Z88	−5654	1015
408	DUMMY21	−5697	860
409	DUMMY22	−5740	1015
410	DUMMY23	−5783	860
411	DUMMY24	−6146	615
412	DUMMY25	−6146	515
413	DUMMY26	−6146	415
414	DUMMY27	−6146	315
415	DUMMY28	−6146	215
416	DUMMY29	−6146	115
417	DUMMY30	−6146	15
418	DUMMY31	−6146	−85
419	DUMMY32	−6146	−185
420	DUMMY33	−6146	−285
421	DUMMY34	−6146	−385
422	DUMMY35	−6146	−485
423	DUMMY36	−6146	−585
424	DUMMY37	−6146	−685
425	DUMMY38	−6146	−785
—	Alignment mark 1	6054	940
—	Alignment mark 2	−6054	940

Pin Function

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>X01 to X88
Y01 to Y88
Z01 to Z88</td><td>O</td><td>LCD panel drive pins</td></tr>
<tr><td>DI/O
DO/I</td><td>I/O</td><td>Data transfer enable pin
These pins indicate the input, starting to transfer the grayscale data, and the output, ending to transfer the data. The U/D pin as shown below determines the function.
<table><tr><th>U/D</th><th>DI/O</th><th>DO/I</th></tr><tr><td>H</td><td>Input</td><td>Output</td></tr><tr><td>L</td><td>Output</td><td>Input</td></tr></table>When set for input
A high on DI/O or DO/I is latched into the internal logic synchronously with the rising edge of CPH. When the internal circuit is in standby state, the device is ready to transfer data.
The grayscale data is latched in sequentially, starting at the next rise of CPH. Also, regardless how many rising edges are existed, DI/O or DO/I recognizes the first rising edge, and the grayscale data is latched at the next rising edge.
When set for output
The pin is used to transfer the enable signal to the JBT6K47-AS at the next stage of the LCD driver.
The pin enters standby state after outputting a high.</td></tr>
<tr><td>U/D</td><td>I</td><td>Transfer direction select pin
This pin specifys the directions of transfering the grayscale data.
Data is transferred synchronously with each rising edge of CPH in one of the following sequences:
When U/D is High: X01 to Z01, X02 to Y02, Z03 to Z03, ……
When U/D is Low: X88 to Z88, X87 to Z87, X86 to Z86, ……
The voltage applied to this pin must be a DC-level voltage that is either high or low.</td></tr>
<tr><td>CPH</td><td>I</td><td>Data transfer clock pin (Can be stopped except the sampling period)
This clock input is used to transfer grayscale data.
In sync with the rising edge of CPH, writes grayscale data bus data to the sampling register.</td></tr>
<tr><td>XIN0 to XIN5
YIN0 to YIN5
ZIN0 to ZIN5</td><td>I</td><td>Grayscale data input pin
An output data consists of six bits, and three output data are latched into the devise simultaneously in one transfer. The POL pin and the result of the operation are written in this data bus. Weighted data bit is shown below.
Grayscale data = (32 × wIN5) + (16 × wIN4) + (8 × wIN3) + (4 × wIN2) + (2 × wIN1) + wIN0
w = X, Y, Z</td></tr>
<tr><td>LOAD</td><td>I</td><td>Data load input pin
This pin recognizes the High level. The data is transferred from the Sampling register to the Load register asynchronously at the rising edge of CPH, and outputs the corresponded voltage to the grayscale data.</td></tr>
<tr><td>POL</td><td>I</td><td>Data polarity reversal pin
This pin is used to select reversing the grayscale data or not.
When POL is High: Reversing the grayscale data.
When POL is Low: Not reversing the grayscale data. The data is transferred to the internal logic from the timing generator.
The grayscale data bus and the operation result of this pin are latched into the internal logic synchronously with the rising edge of CPH.</td></tr>
<tr><td>DW</td><td>I</td><td>Data control pin
This pin is used to forcibly make the grayscale data to High level.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>GS
MD</td><td>I</td><td>Grayscale data bus switching pin (Switching display mode)
This pin enables to choose the display colors by switching numbers of valid data bus of the grayscale consisted of 6 bits/out.

<table>
<tr><th>MD</th><th>GS</th><th>Numbers of Valid Bus</th><th>Gradation Levels</th><th>Display Colors</th></tr>
<tr><td>L</td><td>H</td><td>6/out</td><td>64 levels</td><td>26 thousand colors</td></tr>
<tr><td>L</td><td>L</td><td>4/out</td><td>16 levels</td><td>4096 colors</td></tr>
<tr><td>H</td><td>L</td><td>1/out</td><td>2 levels</td><td>8 colors</td></tr>
</table>
Note 2: When MD = “1”, GS = “1”, select 4-bit mode (4096 colors)</td></tr>
<tr><td>/TEST1
/TEST2</td><td>I</td><td>Test pin
The pull up resistor is connected to this pin, and must be left open.</td></tr>
<tr><td>V0 to V5</td><td>I</td><td>Power supply pin for grayscale reference voltage (For reference analog voltage inputs)
$V_{SS} \leqq V0 \leqq V1 \leqq V2 \leqq V3 \leqq V4 \leqq V5 \leqq AV_{DD}$ or
$V_{SS} \leqq V5 \leqq V4 \leqq V3 \leqq V2 \leqq V1 \leqq V0 \leqq AV_{DD}$</td></tr>
<tr><td>DV_{DD}</td><td>—</td><td>Digital circuit power supply pin</td></tr>
<tr><td>AV_{DD}</td><td>—</td><td>Analog circuit power supply pin</td></tr>
<tr><td>DV_{SS}</td><td>—</td><td>Digital circuit GND pin</td></tr>
<tr><td>AV_{SS}</td><td>—</td><td>Analog circuit GND pin</td></tr>
</table>

Device Operation

- Starting data transfer

  A high input to the data transfer enable pin (DI/O or DO/I) is latched into the internal logic synchronously with the rising edge of CPH, setting the device ready to transfer data. Data transfer starts at the next rise of CPH.
  Also, regardless how many rising edges are existed, DI/O or DO/I recognizes the first rising edge, and the grayscale data is latched at the next rising edge.

- Data transfer method

  The data is latched in from the grayscale bus to the sampling register synchronously with each rising edge of CPH.
  Grayscale data for three outputs are latched into the device simultaneously in one transfer.
  Grayscale data are written as three outputs in parallel during one transfer. Data transfer completes after 88 transfers. Then the device enters Standby mode.
  Data written to the sampling register are the operation result of the grayscale data bus.

- Terminating data transfer

  The data transfer enable pin (DO/I or DI/O) output goes high synchronously with the rising edge of CPH one clock period before the last data is latched in.
  The output from this pin can be connected directly as input to the data transfer enable pin (DI/O or DO/I) of the next stage LCD driver. In this way, multiple devices can be easily cascaded to drive a large screen.

- Panel drive output

  After finishing transferring the grayscale data, the data is latched into the devise when Load is at High level. The grayscale data of the sampling register is transferred to the load register, and the LCD panel drive output is switched to the corresponded output to the grayscale data. The load signal recognizes the data asynchronously with the CPH.

- The grayscale data bus

  JBT6K47-AS is capable to determine the valid grayscale data bus by controlling MD pin and GS pin. The relationship between the MD pin or the GS pin and the valid grayscale data bus is shown below. Input Low or High for the invalid grayscale data bus.

MD	GS	Grayscale Data Bus	Colors	Valid Grayscale Data Bus					
				nIN5	nIN4	nIN3	nIN2	nIN1	nIN0
L	H	6-bit mode	26 thousand colors	Valid					
	L	4-bit mode	4096 colors	Valid				L/H	L/H
H	L	1 bit mode	8 colors	Valid	L/H	L/H	L/H	L/H	L/H

n = X, Y, Z

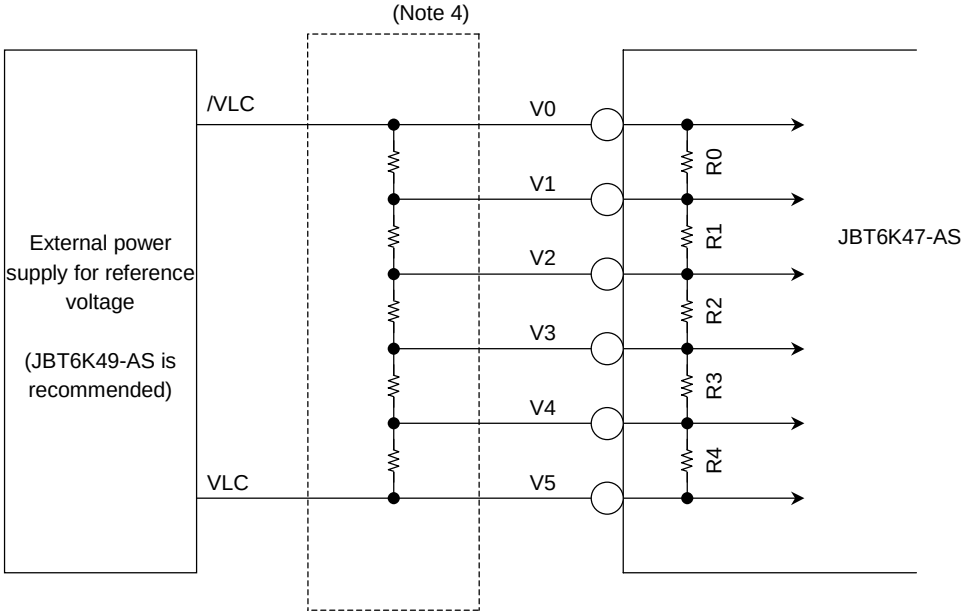
Note 3: L/H indicates V_{DD} level or V_{SS} level.

: When MD = High, GS = High, the grayscale data bus is set to 4-bit mode.

- Reference power supply circuit

  The connection between the device and the reference power supply for reference analog voltage inputs is configured with the resistors in series. The reference power supply circuit is capable of impedance transforming the corrected voltage using the Op amp, and the voltage is used for the grayscale level power supply of the internal circuit.

  (Total of 32 resistor ladders)



Note 4: When correction is needed, connect the correction resistor between VLC terminal and /VLC terminal of JBT6K49-AS, and apply bias on V0 to V5 pins of JBT6K47-AS.

- Grayscale data and output voltages

  The output voltage is determined by the grayscale data value and six reference analog voltage inputs (V0 to V5). It equally divides γ correction voltage using 6 bits grayscale data and converting D/A.

wIN5 (MSB)	wIN4	wIN3	wIN2	wIN1	wIN0 (LSB)

W = X, Y, Z

Grayscale Data	Function
00H to 0CH	Divide V0-V1 equally into 40, and output voltage.
0DH to 14H	Divide V1-V2 equally into 8, and output voltage.
15H to 2DH	Divide V2-V3 equally into 25, and output voltage.
2EH to 36H	Divide V3-V4 equally into 9, and output voltage.
37H to 3FH	Divide V4-V5 equally into 38, and output voltage.

- Grayscale data and output voltages (At 6-bit mode)

Grayscale Data	GDn5	GDn4	GDn3	GDn2	GDn1	GDn0	Output Voltage
00H	0	0	0	0	0	0	V0
01H	0	0	0	0	0	1	V1 + (V0 − V1) × 17/40
02H	0	0	0	0	1	0	V1 + (V0 − V1) × 23/40
03H	0	0	0	0	1	1	V1 + (V0 − V1) × 27/40
04H	0	0	0	1	0	0	V1 + (V0 − V1) × 30/40
05H	0	0	0	1	0	1	V1 + (V0 − V1) × 31/40
06H	0	0	0	1	1	0	V1 + (V0 − V1) × 33/40
07H	0	0	0	1	1	1	V1 + (V0 − V1) × 34/40
08H	0	0	1	0	0	0	V1 + (V0 − V1) × 35/40
09H	0	0	1	0	0	1	V1 + (V0 − V1) × 36/40
0AH	0	0	1	0	1	0	V1 + (V0 − V1) × 37/40
0BH	0	0	1	0	1	1	V1 + (V0 − V1) × 38/40
0CH	0	0	1	1	0	0	V1 + (V0 − V1) × 39/40
0DH	0	0	1	1	0	1	V1
0EH	0	0	1	1	1	0	V2 + (V1 − V2) × 1/8
0FH	0	0	1	1	1	1	V2 + (V1 − V2) × 2/8
10H	0	1	0	0	0	0	V2 + (V1 − V2) × 3/8
11H	0	1	0	0	0	1	V2 + (V1 − V2) × 4/8
12H	0	1	0	0	1	0	V2 + (V1 − V2) × 5/8
13H	0	1	0	0	1	1	V2 + (V1 − V2) × 6/8
14H	0	1	0	1	0	0	V2 + (V1 − V2) × 7/8
15H	0	1	0	1	0	1	V2
16H	0	1	0	1	1	0	V3 + (V2 − V3) × 1/25
17H	0	1	0	1	1	1	V3 + (V2 − V3) × 2/25
18H	0	1	1	0	0	0	V3 + (V2 − V3) × 3/25
19H	0	1	1	0	0	1	V3 + (V2 − V3) × 4/25
1AH	0	1	1	0	1	0	V3 + (V2 − V3) × 5/25
1BH	0	1	1	0	1	1	V3 + (V2 − V3) × 6/25
1CH	0	1	1	1	0	0	V3 + (V2 − V3) × 7/25
1DH	0	1	1	1	0	1	V3 + (V2 − V3) × 8/25
1EH	0	1	1	1	1	0	V3 + (V2 − V3) × 9/25
1FH	0	1	1	1	1	1	V3 + (V2 − V3) × 10/25

n = R, G, B

Grayscale Data	GDn5	GDn4	GDn3	GDn2	GDn1	GDn0	Output Voltage
20H	1	0	0	0	0	0	V3 + (V2 − V3) × 11/25
21H	1	0	0	0	0	1	V3 + (V2 − V3) × 12/25
22H	1	0	0	0	1	0	V3 + (V2 − V3) × 13/25
23H	1	0	0	0	1	1	V3 + (V2 − V3) × 14/25
24H	1	0	0	1	0	0	V3 + (V2 − V3) × 15/25
25H	1	0	0	1	0	1	V3 + (V2 − V3) × 16/25
26H	1	0	0	1	1	0	V3 + (V2 − V3) × 17/25
27H	1	0	0	1	1	1	V3 + (V2 − V3) × 18/25
28H	1	0	1	0	0	0	V3 + (V2 − V3) × 19/25
29H	1	0	1	0	0	1	V3 + (V2 − V3) × 20/25
2AH	1	0	1	0	1	0	V3 + (V2 − V3) × 21/25
2BH	1	0	1	0	1	1	V3 + (V2 − V3) × 22/25
2CH	1	0	1	1	0	0	V3 + (V2 − V3) × 23/25
2DH	1	0	1	1	0	1	V3 + (V2 − V3) × 24/25
2EH	1	0	1	1	1	0	V3
2FH	1	0	1	1	1	1	V4 + (V3 − V2) × 1/9
30H	1	1	0	0	0	0	V4 + (V3 − V2) × 2/9
31H	1	1	0	0	0	1	V4 + (V3 − V2) × 3/9
32H	1	1	0	0	1	0	V4 + (V3 − V2) × 4/9
33H	1	1	0	0	1	1	V4 + (V3 − V2) × 5/9
34H	1	1	0	1	0	0	V4 + (V3 − V2) × 6/9
35H	1	1	0	1	0	1	V4 + (V3 − V2) × 7/9
36H	1	1	0	1	1	0	V4 + (V3 − V2) × 8/9
37H	1	1	0	1	1	1	V4
38H	1	1	1	0	0	0	V5 + (V4 − V5) × 1/38
39H	1	1	1	0	0	1	V5 + (V4 − V5) × 2/38
3AH	1	1	1	0	1	0	V5 + (V4 − V5) × 3/38
3BH	1	1	1	0	1	1	V5 + (V4 − V5) × 4/38
3CH	1	1	1	1	0	0	V5 + (V4 − V5) × 6/38
3DH	1	1	1	1	0	1	V5 + (V4 − V5) × 7/38
3EH	1	1	1	1	1	0	V5 + (V4 − V5) × 10/38
3FH	1	1	1	1	1	1	V5

n = R, G, B

- Grayscale data and output voltages (At 4-bit mode)

Grayscale Data	GDn 5	GDn 4	GDn 3	GDn 2	Output Voltage
00H	0	0	0	0	V0
01H	0	0	0	1	V1 + (V0 – V1) × 30/40
02H	0	0	1	0	V1 + (V0 – V1) × 35/40
03H	0	0	1	1	V1 + (V0 – V1) × 39/40
04H	0	1	0	0	V2 + (V1 – V2) × 4/8
05H	0	1	0	1	V2
06H	0	1	1	0	V3 + (V2 – V3) × 4/25
07H	0	1	1	1	V3 + (V2 – V3) × 8/25

Grayscale Data	GDn 5	GDn 4	GDn 3	GDn 2	Output Voltage
08H	1	0	0	0	V3 + (V2 – V3) × 13/25
09H	1	0	0	1	V3 + (V2 – V3) × 17/25
0AH	1	0	1	0	V3 + (V2 – V3) × 21/25
0BH	1	0	1	1	V3
0CH	1	1	0	0	V4 + (V3 – V4) × 5/9
0DH	1	1	0	1	V4
0EH	1	1	1	0	V5 + (V4 – V5) × 4/38
0FH	1	1	1	1	V5

n = R, G, B

GDn1~0 = “L”

- Grayscale data and output voltages (At 1 bit mode)

Grayscale Data	GDn 5	Output Voltage
00H	0	V0
01H	1	V5

n = R, G, B

GDn4 to 0 = “L”

- Reference analog voltage inputs resistance ratio (R0 = 91.7 kΩ)

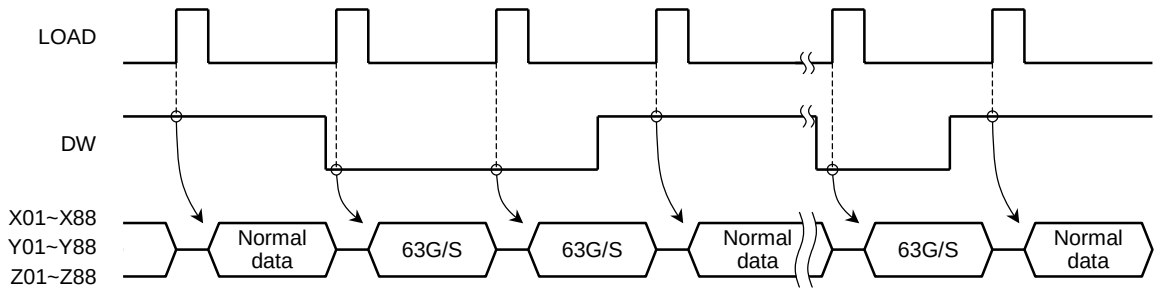
R0	R1	R2	R3	R4
1.00	0.11	0.24	0.10	0.72

Note 5: Total resistance value is about 200 kΩ.

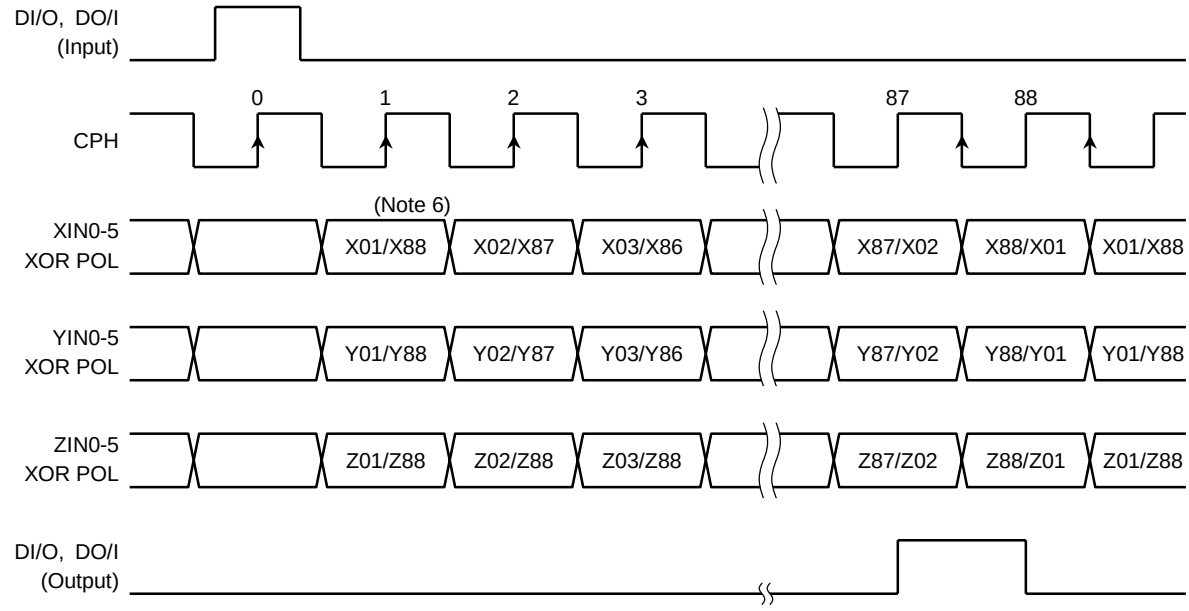
- How to fix the grayscale data forcibly

JBT6K47-AS is able to fix all the grayscale data to 63G/S despite the grayscale input by controlling the DW pin.

The DW signal and output data timing is shown below.

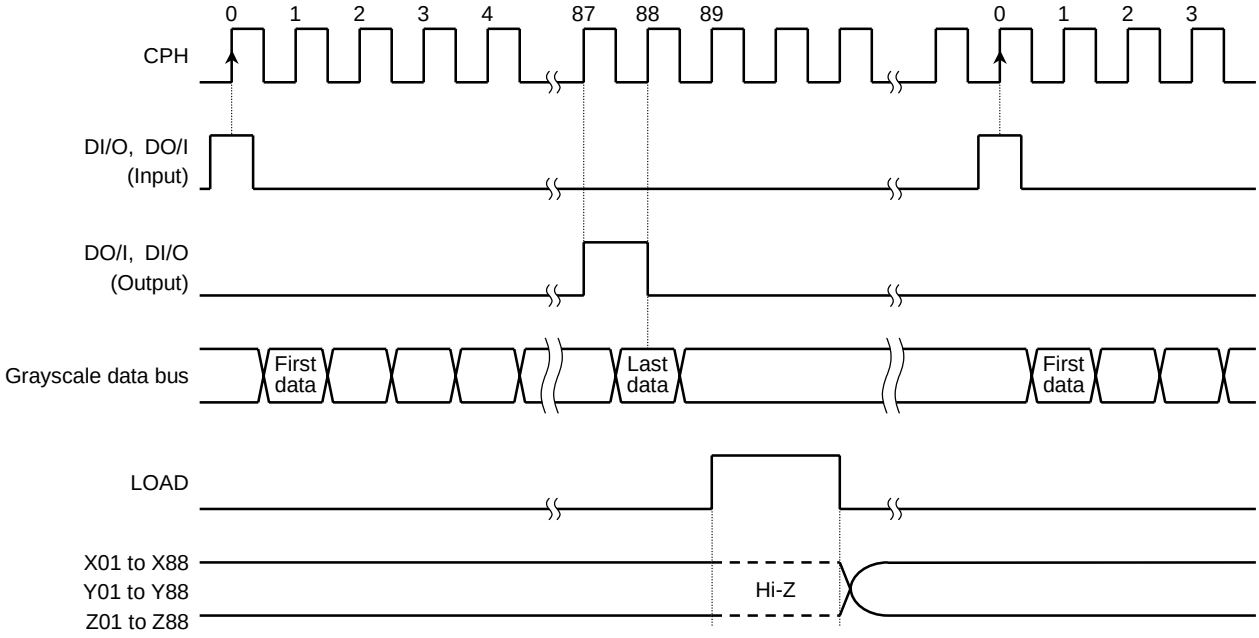


Timing Diagrams (1)



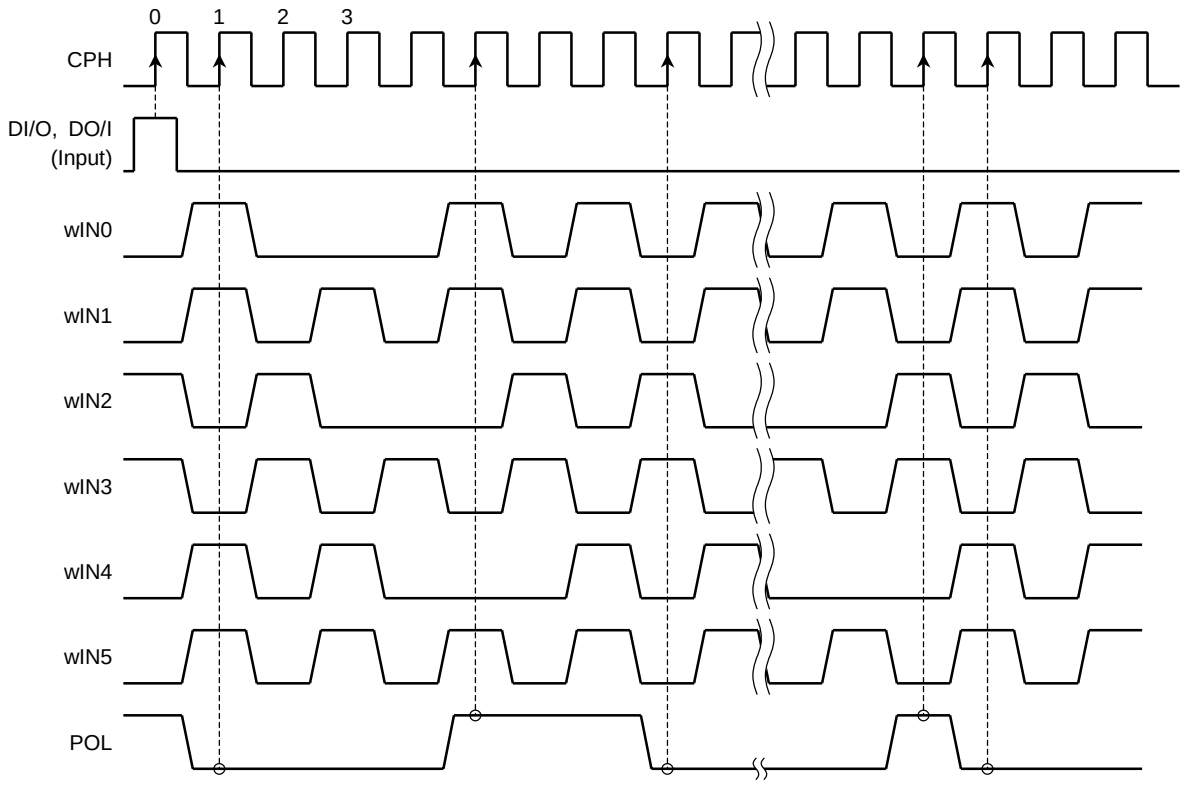
Note 6: Upper stage: X01 → U/D = High
Lower stage: X88 → U/D = Low

Timing Diagrams (2)



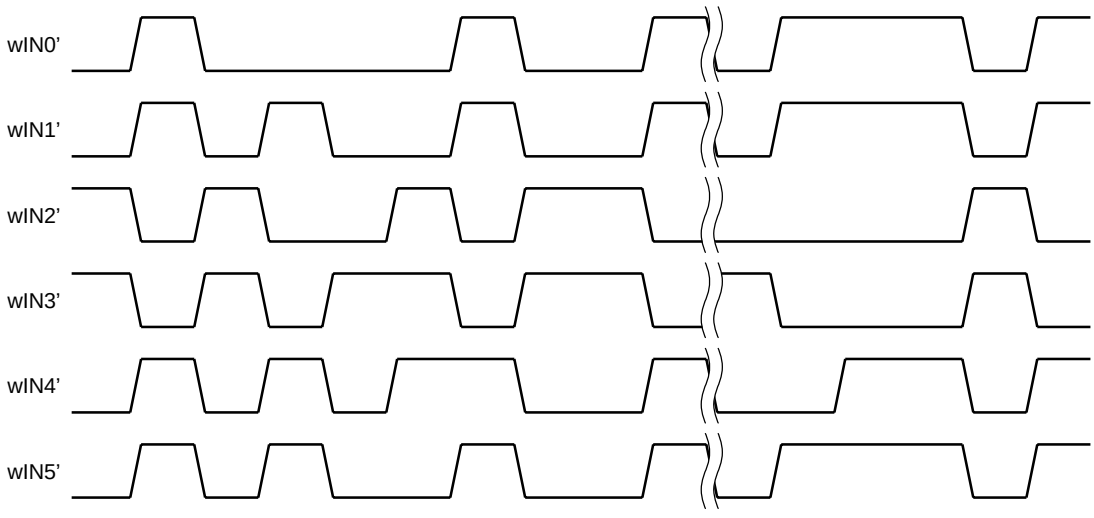
Timing Diagrams (3)

ex) Grayscale data and POL pins



w = X, Y, Z

Importing the grayscale data



w = X, Y, Z

Absolute Maximum Ratings (unless otherwise specified, V_{SS} = 0 V, Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Supply voltage	Digital	DV_{DD}	−0.3 to 6.5	V
	Analog	AV_{DD}	−0.3 to 6.5	
Input voltage	Digital	V_{IND}	−0.3 to DV_{DD} + 0.3	V
	Analog	V_{INA}	−0.3 to AV_{DD} + 0.3	
Reference analog voltage inputs voltage		V0~V5	−0.3 to AV_{DD} + 0.3	V
Output voltage	I/O	V_{OUT1}	−0.3 to DV_{DD} + 0.3	V
	OUT	V_{OUT2}	−0.3 to AV_{DD} + 0.3	
Operating temperature		T_{opr}	−20 to 75	°C
Storage temperature		T_{stg}	−55 to 125	°C

Note 7: The following shows the relative magnitude of each reference analog voltage:
V0 ≦ V1 ≦ V2 ≦ V3 ≦ V4 ≦ V5 or V5 ≦ V4 ≦ V3 ≦ V2 ≦ V1 ≦ V0. V0 ≠ V5

Electrical Characteristics

DC Characteristics (unless otherwise specified, AV_{DD} = 4.5 to 5.6 V, DV_{DD} = 2.5 to 3.6 V, Ta = –20 to 75°C; Typical value is AV_{DD} = 5.0 V, DV_{DD} = 3.0 V, f_{CPH} = 5 MHz, Ta = 25°C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Relevant Pin
Operating voltage (1)		DV_{DD}	—	—	2.5	—	3.6	V	DV_{DD}
Operating voltage (2)		AV_{DD}	—	—	4.5	—	5.6	V	AV_{DD}
Reference analog voltage inputs voltage		V0 to V5	—	(Note 11)	0	—	AV_{DD}	V	V0 to V5
Input current	Low level	I_{IL}	—	—			1	μA	(Note 9)
	High level	I_{IH}					1		
Input voltage	Low level	V_{IL}	—	—	0		0.2 DV_{DD}	V	(Note 10)
	High level	V_{IH}			0.8 DV_{DD}		DV_{DD}		
Output voltage	Low level	V_{OL}	—	I_{OL} = 0.1 mA	0		0.5	V	DI/O, DO/I
	High level	V_{OH}		I_{OH} = −0.1 mA	DV_{DD} − 0.5		DV_{DD}		
Output off current		I_{OFF}	—	(Note 12)			1	μA	X01 to X88 Y01 to Y88 Z01 to Z88
Output voltage range		V_{OUT1}	—	Output VG1 to VG62	0.1		AV_{DD} − 0.1	V	
		V_{OUT2}		Output VG0, VG63	0		AV_{DD}		
Output voltage deviation		V_{DO}	—	C_L = 30 pF	−20		20	mV	
Operating frequency		f_{CPH}	—	—	DC		5	MHz	CPH
Output load capacity		C_{L1}	—	—			30	pF/pin	X01 to X88 Y01 to Y88 Z01 to Z88
		C_{L2}	—	(Note 8)	30			pF	

Note 8: 30 pF (min) must be connected to the selected grayscale level (incorporated amplifier)

DC Characteristics (**unless otherwise specified, AV_{DD} = 4.5 to 5.6 V, DV_{DD} = 2.5 to 3.6 V, Ta = –20 to 75°C**
Typical value is AV_{DD} = 5.0 V, DV_{DD} = 3.0 V, f_{CPH} = 5 MHz, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Relevant Pin
Current consumption (1)	AI_{DD1}	—	(Note 13)		620	TBD	μA	AV_{DD}
	AI_{DD2}		(Note 14)		210	TBD		
	AI_{DD3}		(Note 15)		80	TBD		
	AI_{DDS}		(Note 16)		580	TBD		
Current consumption (2)	DI_{DD1}	—	(Note 13)		390	TBD	μA	DV_{DD}
	DI_{DD2}		(Note 14)		300	TBD		
	DI_{DD3}		(Note 15)		170	TBD		
	DI_{DDS}		(Note 16)		1	TBD		
Standby current	IDSTB	—	—		1	TBD	μA	

Note 9: XIN0-3, YIN0-3, ZIN0-3, DI/O, DO/I, CPH, LOAD, MD, GS, DW, U/D, Except test pins.

Note 10: XIN0-3, YIN0-3, ZIN0-3, DI/O, DO/I, CPH, LOAD, MD, GS, DW, U/D, Except test pins.

Note 11: $V0 \leqq V1 \leqq V2 \leqq V3 \leqq V4 \leqq V5$ or $V5 \leqq V4 \leqq V3 \leqq V2 \leqq V1 \leqq V0$. $V0 \neq V5$

Note 12: AV_{DD} = 5.5 V, f_{CPH} = 5 MHz, 1 H = 64 μs, DI/O = “L”

Note 13: DV_{DD} = 3.3 V, AV_{DD} = 5.5 V, f_{CPH} = 5 MHz, 1 H = 64 μs, no load, checkerboard pattern, 6-bit mode

Note 14: DV_{DD} = 3.3 V, AV_{DD} = 5.5 V, f_{CPH} = 5 MHz, 1 H = 64 μs, no load, checkerboard pattern, 4-bit mode

Note 15: DV_{DD} = 3.3 V, AV_{DD} = 5.5 V, f_{CPH} = 5 MHz, 1 H = 64 μs, no load, checkerboard pattern, 1 bit mode

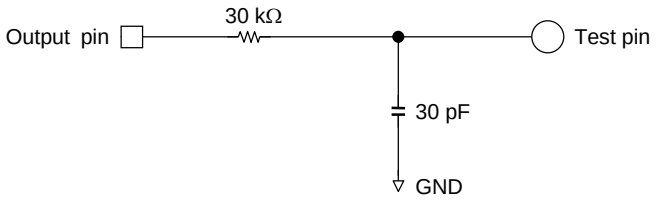
Note 16: DV_{DD} = 3.3 V, AV_{DD} = 5.5 V, f_{CPH} = 5 MHz, 1 H = 64 μs, no load, 6-bit mode, DI/O = “L”

AC Characteristics (1) **(unless otherwise specified, AV_{DD} = 4.5 to 5.6 V, DV_{DD} = 2.5 to 3.6 V, Ta = –20 to 75°C Typical vale is AV_{DD} = 5.0 V, DV_{DD} = 3.0 V, Ta = 25°C)**

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
CPH Pulse width	H	t_{CWH}	—	—	20			ns
	L	t_{CWL}	—	—	20			
Enable setup time		t_{sDI}	—	—	15			ns
Enable hold time		t_{hDI}	—	—	0			ns
Enable high period		t_{DIWH}	—	—			1	CPH
Data setup time		t_{sDD}	—	—	8			ns
Data hold time		t_{hDD}	—	—	0			ns
LOAD setup time		t_{sLD}	—	—	1			CPH
LOAD hold time		t_{hLD}	—	—	1			CPH
LOAD High period		t_{LWH}	—	—	200			ns
Output delay time	1	t_{pdDO1}	—	C_L = 10 pF (Note 18)			12	ns
		t_{pdDO2}	—	C_L = 10 pF (Note 18)			12	
	2	t_{pdDX}	—	C_L = 30 pF (Note 17, 18)		5	8	μs
	3	t_{ptdDX2}	—	C_L = 30 pF × 264 (Note 17, 18)		30	45	

Note 17: Test circuit (1)

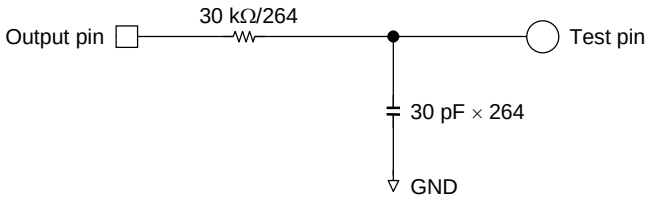
When 1 output is selected:



Note: Volume of probe and jig is included.

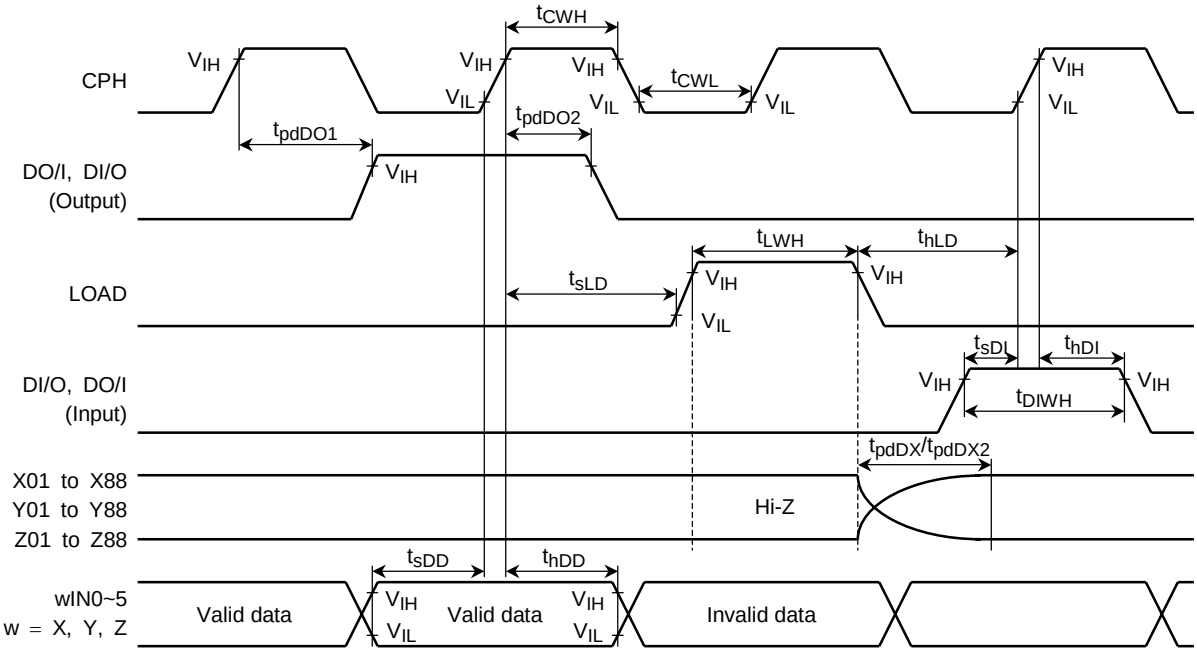
Test circuit (2)

When 264 output is selected:



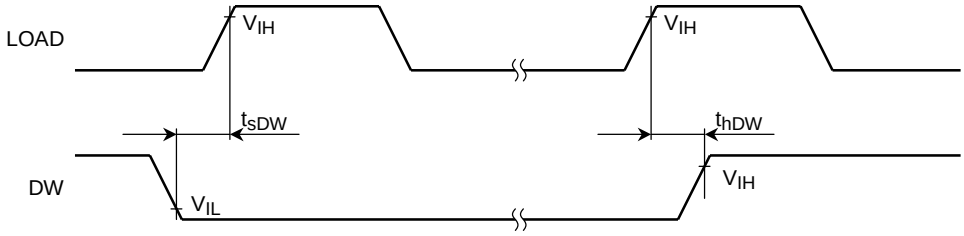
Note: Volume of probe and jig is included.

Note 18: When the amplitude is 4 V and it reached at 90% level.



AC Characteristics (2) (**unless otherwise specified, AV_{DD} = 4.5 to 5.6 V, DV_{DD} = 2.5 to 3.6 V, Ta = −20 to 75°C**
Typical value is AV_{DD} = 5.0 V, DV_{DD} = 3.0 V, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
DW setup time	t_{sDW}	—	—	5			ns
DW hold time	t_{hDW}	—	—	5			ns



RESTRICTIONS ON PRODUCT USE

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- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer’s own risk.
- Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.
  This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
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