

# NM93C86AU

## 16K-Bit MICROWIRE™ Interface

### Serial EEPROM

#### General Description

The NM93C86AU is a 16K (16,384) bit serial interface CMOS EEPROM (Electrically Erasable Programmable Read-Only Memory). This device fully conforms to the MICROWIRE™ 4-wire protocol which uses Chip Select (CS), Clock (SK), Data-in (DI) and Data-out (DO) pins to synchronously control the EEPROM data transfer and the ORG pin, which allows configuring the part for an 8-bit or 16-bit data format. In addition, the serial interface allows a minimal pin count, packaging designed to simplify PC board layout requirements and offers the designer a variety of low voltage and low power options.

The NM93C86AU MICROWIRE EEPROM offers the user the ability to configure the EEPROM as a 16-bit dataword (ORG pin =  $V_{CC}$ ; 16 bits x 1,024 addresses) or an 8-bit data byte (ORG pin =  $V_{SS}$ ; 8 bits x 2,048 addresses).

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability, and low power consumption for a continuously reliable non-volatile solution for all markets.

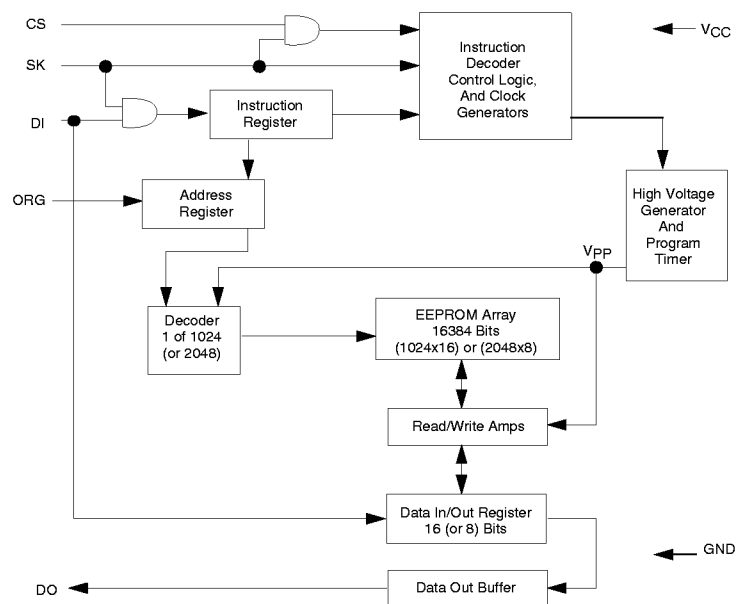
#### Functions

- MICROWIRE™ 4-wire interface
- 16K bits organized as 8 x 2,048 or 16 x 1,024 organization (ORG pin control)
- Extended 2.7V to 5.5V operating voltage
- 1MHz operation
- Self-timed programming cycle (6ms typical)
- "Programming complete" indicated by DO Ready/Busy polling

#### Features

- The MICROWIRE interface offers the greatest ease of use vs. clock rate of serial data transfer methods
- Bulk mode programming to allow simultaneous programming of all addresses
- Low  $V_{CC}$  Programming Lockout (3.8V)
  - "H" option (Standard  $V_{CC}$  range) parts only
- Schmitt trigger (hysteresis) on all inputs
- Typical 200 $\mu$ A active current ( $I_{CCA}$ )
- Typical 1 $\mu$ A standby current ( $I_{SB}$ ) for "L" devices and 0.1 $\mu$ A standby current for "LZ" devices
- Endurance: Up to 1,000,000 data changes
- Data retention greater than 40 years

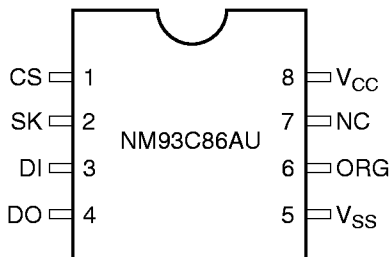
#### Block Diagram



DS800021-12

## Connection Diagram

**Dual-In-Line Package (N)  
and 8-Pin SO Package (M8)**



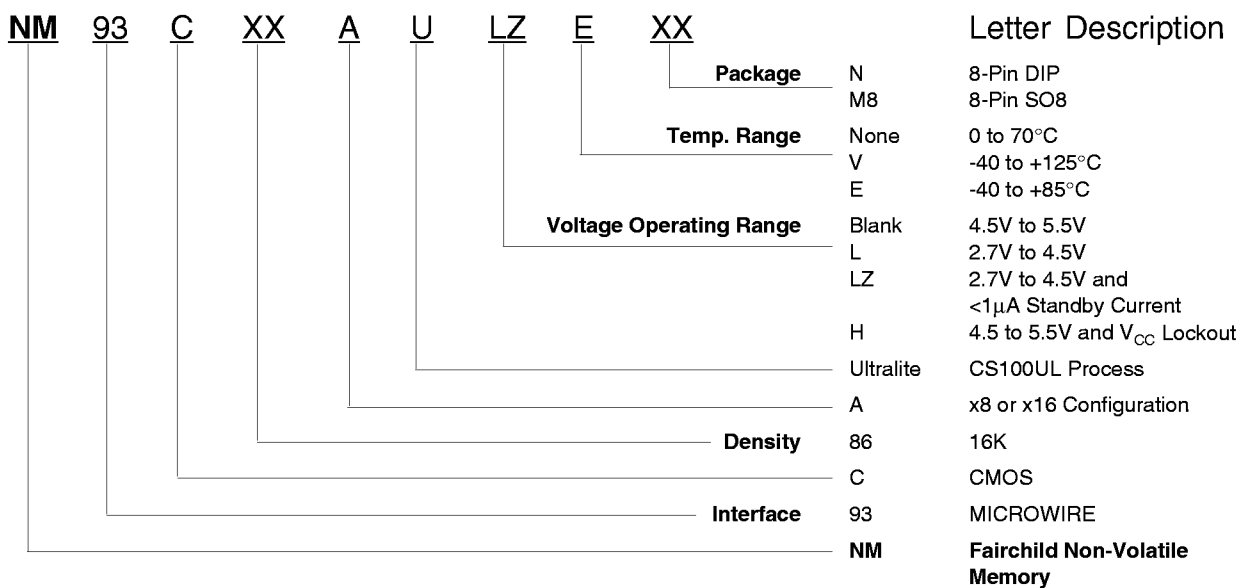
DS800021-14

**Top View**  
**See Package Number**  
**N08E and M08A**

## Pin Names

Pin	Description
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V <sub>SS</sub>	Ground
ORG	Memory Organization Select
NC	No Connect
V <sub>CC</sub>	Positive Power Supply

## Ordering Information



### Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	$V_{CC} + 1$ to $-0.3V$
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V

### Operating Range

Ambient Operating Temperature	NM93C86AU	0°C to +70°C
	NM93C86AUE	-40°C to +85°C
	NM93C86AUV	-40°C to +125°C
Power Supply ( $V_{CC}$ ) Range	NM93C86AU/NM93C86AUH	4.5V to 5.5V

### DC and AC Electrical Characteristics $4.5V \leq V_{CC} \leq 5.5V$

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
$I_{CCA}$	Operating Current		$CS = V_{IH}$ , $SK=1$ MHz		1	mA
$I_{CCS}$	Standby Current		$CS = 0V$ $ORG = V_{CC}$ or $NC$		50	$\mu A$
$I_{IL}$	Input Leakage		$V_{IN} = 0V$ to $V_{CC}$ (Note 2)	-1	1	$\mu A$
$I_{ILO}$	Input Leakage ORG Pin		ORG tied to $V_{CC}$ ORG tied to $V_{SS}$ (Note 3)	-1 -2.5	1 2.5	$\mu A$
$I_{OL}$	Output Leakage		$V_{IN} = 0V$ to $V_{CC}$	-1	1	$\mu A$
$V_{IL}$	Input Low Voltage			-0.1	0.8	V
$V_{IH}$	Input High Voltage			2	$V_{CC} + 1$	V
$V_{OL1}$	Output Low Voltage		$I_{OL} = 2.1$ mA		0.4	V
$V_{OH1}$	Output High Voltage		$I_{OH} = -400$ $\mu A$	2.4		V
$V_{OL2}$	Output Low Voltage		$I_{OL} = 10$ $\mu A$		0.2	V
$V_{OH2}$	Output High Voltage		$I_{OL} = -10$ $\mu A$	$V_{CC} - 0.2$		V
$f_{SK}$	SK Clock Frequency		(Note 4)	0	1	MHz
$t_{SKH}$	SK High Time	NM93C86AU NM93C86AUE/V		250 300		ns
$t_{SKL}$	SK Low Time			250		ns
$t_{SKS}$	SK Setup Time		SK must be at $V_{IL}$ for $t_{SKS}$ before CS goes high	50		ns
$t_{CS}$	Minimum CS Low Time		(Note 5)	250		ns
$t_{CSS}$	CS Set-up Time			50		ns
$t_{DH}$	DO Hold Time			70		ns
$t_{DIS}$	DI Set-up Time	NM93C86AU NM93C86AUE/V		100 200		ns
$t_{CSH}$	CS Hold Time			0		ns
$t_{DIH}$	DI Hold Time			20		ns
$t_{PD1}$	Output Delay to "1"				500	ns
$t_{PD0}$	Output Delay to "0"				500	ns
$t_{SV}$	CS to Status Valid				500	ns
$t_{DF}$	CS to DO in TRI-STATE®				100	ns
$t_{WP}$	Write Cycle Time				10	ms

### Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

### Operating Range

Ambient Operating Temperature	0°C to +70°C
NM93C86AUL/LZ	-40°C to +85°C
NM93C86AULE/LZE	-40°C to +125°C
NM93C86AULV/LZV	
Power Supply (V <sub>CC</sub> )	2.7V to 4.5V

### Low V<sub>CC</sub> (2.7V to 4.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I <sub>CCA</sub>	Operating Current		CS = V <sub>IH</sub> , SK = 250KHz		1	mA
I <sub>CCS</sub>	Standby Current		CS = V <sub>IL</sub>		10	μA
	L				1	μA
	LZ				1	μA
I <sub>IL</sub>	Input Leakage		V <sub>IN</sub> = 0V to V <sub>CC</sub> (Note 2)		±1	μA
I <sub>ILO</sub>	Input Leakage		ORG tied to V <sub>CC</sub>	-1	1	μA
	ORG Pin		ORG tied to V <sub>SS</sub> (Note 3)	-2.5	2.5	μA
I <sub>OL</sub>	Output Leakage		V <sub>IN</sub> = 0V to V <sub>CC</sub>		±1	μA
V <sub>IL</sub>	Input Low Voltage			-0.1	0.15 V <sub>CC</sub>	V
V <sub>IH</sub>	Input High Voltage			0.8 V <sub>CC</sub>	V <sub>CC</sub> + 1	V
V <sub>OL</sub>	Output Low Voltage		I <sub>OL</sub> = 10 μA		0.1 V <sub>CC</sub>	V
V <sub>OH</sub>	Output High Voltage		I <sub>OH</sub> = -10 μA	0.9 V <sub>CC</sub>		V
f <sub>SK</sub>	SK Clock Frequency		(Note 4)	0	250	KHz
t <sub>SKH</sub>	SK High Time			1		μs
t <sub>SKL</sub>	SK Low Time			1		μs
t <sub>SKS</sub>	SK Setup Time		SK must be at V <sub>IL</sub> for t <sub>SKS</sub> before CS goes high	0.2		μs
t <sub>CS</sub>	Minimum CS Low Time		(Note 5)	1		μs
t <sub>CSS</sub>	CS Setup Time			0.2		μs
t <sub>DH</sub>	DO Hold Time			70		ns
t <sub>DIS</sub>	DI Setup Time			0.4		μs
t <sub>CSSH</sub>	CS Hold Time			0		ns
t <sub>DIH</sub>	DI Hold Time			0.4		μs
t <sub>PD1</sub>	Output Delay to "1"				2	μs
t <sub>PD0</sub>	Output Delay to "0"				2	μs
t <sub>SV</sub>	CS to Status Valid				1	μs
t <sub>DF</sub>	CS to DO in TRI-STATE		CS = V <sub>IL</sub>		0.4	μs
t <sub>WP</sub>	Write Cycle Time				15	ms

### Capacitance T<sub>A</sub> = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C <sub>OUT</sub>	Output Capacitance		5	pF
C <sub>IN</sub>	Input Capacitance		5	pF

**Note 1:** Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** Typical leakage values are in the 20 nA range.

**Note 3:** The ORG pin may draw > 1 μA when in the x8 mode due to an internal pull-up transistor.

**Note 4:** The shortest allowable SK clock period = 1/f<sub>SK</sub> (as shown under the f<sub>SK</sub> parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t<sub>SKH</sub> and t<sub>SKL</sub> limits must be observed. Therefore, it is not allowable to set 1/f<sub>SK</sub> = t<sub>SKH</sub>minimum + t<sub>SKL</sub>minimum for shorter SK cycle time operation.

**Note 5:** CS (Chip Select) must be brought low (to V<sub>IL</sub>) for an interval of t<sub>CS</sub> in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagrams in the following pages.)

### AC Test Conditions

V <sub>CC</sub> Range	V <sub>IL</sub> /V <sub>IH</sub> Input Levels	V <sub>IL</sub> /V <sub>IH</sub> Timing Level	V <sub>OL</sub> /V <sub>OH</sub> Timing Level	I <sub>OL</sub> /I <sub>OH</sub>
2.7V ≤ V <sub>CC</sub> ≤ 5.5V (Extended Voltage Levels)	.03V/1.8V	1.0V	0.8V/1.5V	±10μA
4.5V ≤ V <sub>CC</sub> ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	-2.1mA/0.4mA

Output Load: 1 TTL Gate (C<sub>L</sub> = 100 pF)

## MICROWIRE I/O Pin Description

### Chip Select (CS):

This pin enables and disables the MICROWIRE device and performs 2 general functions:

1. When in the low state, the MICROWIRE device is disabled and the output tri-stated (high impedance). If this pin is brought high (rising edge active), all internal registers are reset and the device is enabled, allowing MICROWIRE communication via DI/DO pins. To restate, the CS pin must be held high during all device communication and opcode functions. If the CS pin is brought low, all functions will be disabled and reset when CS is brought high again. The exception to this is when a programming cycle is initiated. Again, all activity on the CS, DI and DO pins is ignored until CS is brought high.
2. When programming is in progress, the Data-Out pin will display the programming status as either BUSY (DO low) or READY (DO high) when CS is brought high. (Again, the output will be tri-stated when CS is low.) To restate, during programming, the CS pin may be brought high and low any number of times to view the programming status without affect the programming operation. Once programming is completed (Output in READY state), the output is 'cleared' (returned to normal tri-state condition) by clocking in a Start Bit. After the Start Bit is clocked in, the output will return to a tri-stated condition. When clocked in, this Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits.

Unlike the lower density members of the Microwire product family (NM93C06, NM93C46, NM93C56, NM93C66) programming is not initiated by bringing CS low.

### Serial Clock (SK):

This pin is the clock input (rising edge active) for clocking in all opcodes and data on the DI pin and clocking out all data on the DO pin. However, this pin has no effect on the asynchronous programming cycle (see the CD pin section) as the BUSY/READY status is a function of the CD pin only.

### Data-In (DI):

All serial communication into the device is performed using this input pin (rising edge active). In order to avoid false Start Bits, or related issues, it is advised to keep the DI pin in the low state unless actually clocking in data bits (Start Bit, Opcode, Address or incoming data bits to be programmed). Please note that the first '1' clocked into the device (after CS is brought high) is seen as a Start Bit and the beginning of a serial command string, so caution must be observed when bringing CS high.

### Data-Out (DO):

All serial communication out of the device (READ opcode) is performed using this output pin (rising edge active) as well as indicating the READY/BUSY status during the asynchronous programming cycle. Note that, during READ operations, the output data is clocked out after the last address bit (A0) is clocked in. If a 3-wire application is required (where DI and DO are tied together), sections in AN-758, or related application notes, must be followed for correct operation.

### Organization (ORG):

This pin controls the device architecture (8-bit data word vs. 16-bit data word). If the ORG pin is brought to  $V_{CC}$ , the device is configured with a 16-bit data word and if the ORG pin is brought to  $V_{SS}$  (Ground), the device is configured with an 8-bit data word (refer to other sections for details of both configurations). If the ORG pin is left floating, the device will default to a 16-bit data word.

## Instruction Set for the NM93C86AU

ORG Pin Logic	Memory	
	Configuration	# of Address Bits
0	2048 x 8	11 Bits
1	1024 x 16	10 Bits

### 1024 by 16-Bit Organization (NM93C86AU when ORG = V<sub>CC</sub> or NC)

Instruction	SB	Op Code 2 Bits	Address 10 Bits	Data 16 Bits	Function
READ	1	10	A9–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXXXX		Disables all programming modes.
ERASE	1	11	A9–A0		Erases selected register.
WRITE	1	01	A9–A0	D15–D0	Writes data pattern D15–D0 into selected register.
ERAL	1	00	10XXXXXXXX		Erases all registers.
WRAL	1	00	01XXXXXXXX	D15–D0	Writes data pattern D15–D0 into all registers.

### 2048 by 8-Bit Organization (NM93C86AU when ORG = GND)

Instruction	SB	Op Code 2 Bits	Address 11 Bits	Data 8 Bits	Function
READ	1	10	A10–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXXXXXX		Disables all programming modes.
ERASE	1	11	A10–A0		Erases selected register.
WRITE	1	01	A10–A0	D7–D0	Writes data pattern D7–D0 into selected register.
ERAL	1	00	10XXXXXXXXXX		Erases all registers.
WRAL	1	00	01XXXXXXXXXX	D7–D0	Writes data pattern D7–D0 into all registers.

## Functional Description

### Programming

The programming cycle is automatically started after entering the LAST bit of the programming instruction string (unlike other Microwire family members which use CS to initiate programming). This feature, counting the number of instruction bits, decreases the likelihood of inadvertent programming and allows the programming to be cancelled before sending out the last bit in the string (be bringing CS low).

Programming Instruction	Last Bit in String
WRITE	D0
WRAL	D0
ERASE	A0
ERAL	A0

Note that, in the ERASE/ERAL instructions, the A0 bit is the last bit in the string and clocking in that bit will initiate programming. In order to maintain compatibility, **CS may be brought low after clocking in the last bit, but it is not necessary.**

In all programming modes the READY/BUSY status of the device can be determined by polling the DO pin. After clocking in the last bit of the instruction sequence and with the CS held "high", the DO pin will exit the high impedance state and indicate the READY/BUSY status of the device. DO = logical "0" indicates that programming is still in progress and no other instruction can be executed.

DO = logical "1" indicates that the device is READY for another instruction. If CS is forced "low" the DO pin will return to the high impedance state. After the programming cycle has been completed and DO = logical "1", the DO pin can be reset back to the high impedance state by clocking a logical "1" into the DI pin. (This is also performed with the start bit on all op codes, thus clocking an instruction has the same effect.)

### Read (READ)

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a serial-out shift register. A dummy bit (logical 0) precedes the serial data output string. Output data changes are initiated by a low to high transition of SK clock after the last address bit (A0) is clocked in.

### Erase/Write Enable (EWEN)

When V<sub>CC</sub> is applied to the part, it "powers up" in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V<sub>CC</sub> is removed from the part.

## Functional Description (Continued)

### Erase/Write Disable (EWDS)

To protect against accidental data overwrites, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

### Erase (ERASE)

The ERASE instruction will program all bits in the specified register to the logical "1" state. The self-timed programming cycle is initiated on the rising edge of the SK clock as the last address bit (A0) is clocked in. At this point CS, SK and DI become don't care states. After starting an Erase cycle the DO pin indicates the READY/BUSY status of the chip if CS is held "high". DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased.

### Write (WRITE)

The WRITE instruction is followed by 16 bits of data (or 8 bits of data when using the NM93C86AU in the x8 organization) to be written into the specified address. Note that if the CS is brought "low" before clocking in all of the data bits, then the WRITE instruction will be aborted. The self-timed programming cycle is initiated on the rising edge of the SK clock as the last data bit (D0) is clocked in. At this point, CS, SK and DI become don't care states. No separate ERASE cycle is required before a WRITE instruction.

As in the ERASE instruction, after starting a WRITE cycle, the DO pin indicates the READY/BUSY status of the chip if CS is held "high". DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been written and that the part is ready for another instruction.

### Erase All (ERAL)

The ERAL instruction will simultaneously program all registers in the memory array to the logical "1" state.

### Write All (WRAL)

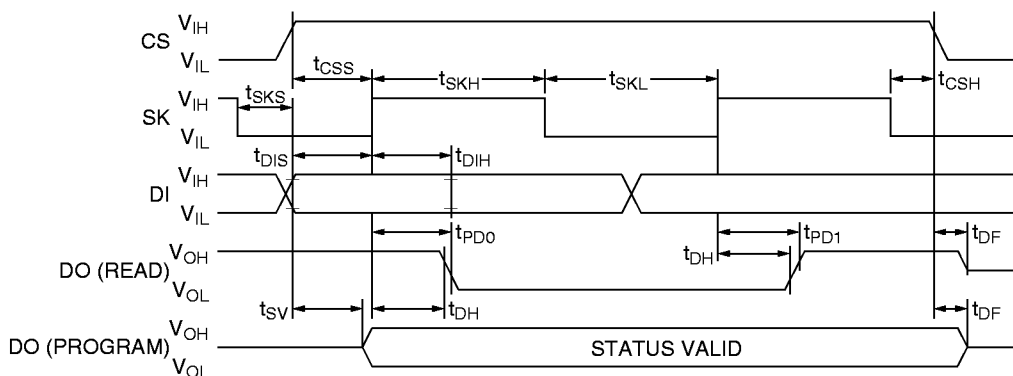
The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction.

### Low V<sub>CC</sub> Lockout

The NM93C86AxHx ("H" option) protects against data corruption during programming by preventing any programming operations if V<sub>CC</sub> drops below approximately 3.8V (V<sub>CC</sub> Lockout trip level). This is accomplished by continually monitoring the CS (Chip Select) pin and, when active (high), preventing programming if the V<sub>CC</sub> drops below the Lockout trip level. After any programming opcode is fully clocked in and the V<sub>PP</sub> internal high voltage has been turned on, the lockout is disabled. The lockout is inactive if any opcode is entered **except** a programming opcode. **Disabled programming is indicated by no BUSY signal appearing at the output (the output remains tri-stated).** To restate, the V<sub>CC</sub> Lockout feature is active from the time CS goes high up to the time that the V<sub>PP</sub> internal high voltage is turned on. (The Low V<sub>CC</sub> Lockout feature is not enabled for any non-programming opcodes.) **Once programming has begun, the programming cycle cannot be interrupted except by removal of V<sub>CC</sub>, which could result in data corruption.**

## Timing Diagrams for the NM93C86AU

### Synchronous Data Timing

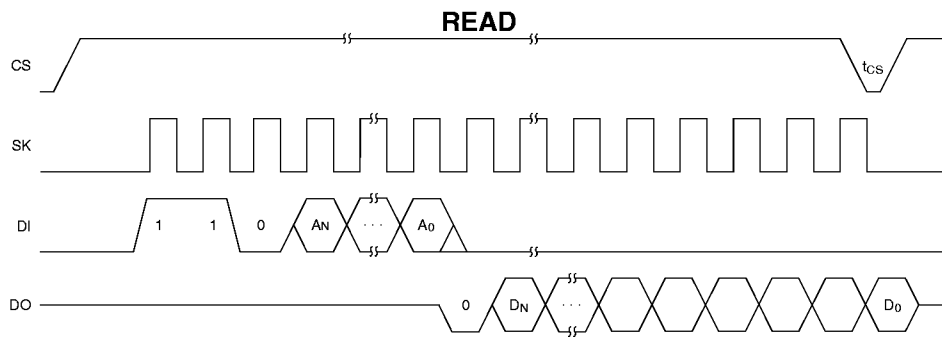


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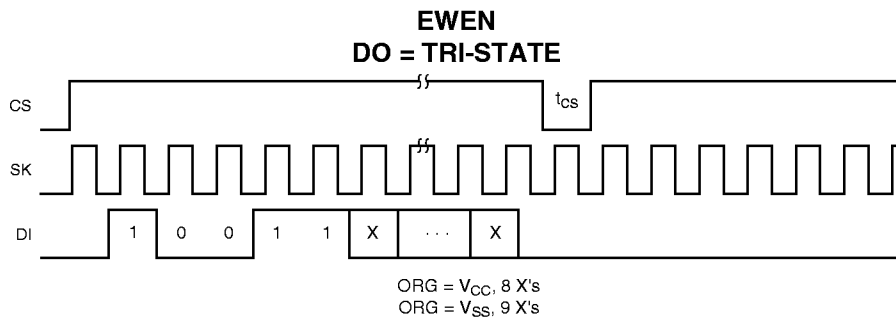
### Timing Diagrams for the NM93C86AU (Continued)

#### Key for Timing Diagrams Organization of Address and Data Fields for the NM93C86AU

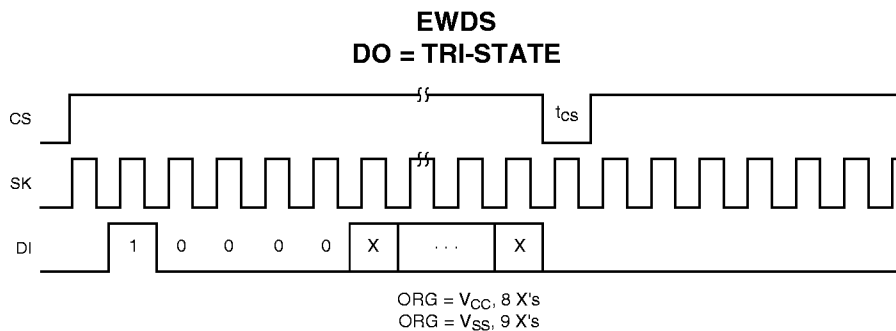
ORG	Organization	A <sub>N</sub>	D <sub>N</sub>
V <sub>CC</sub> or NC	1024 x 16	A9	D15
V <sub>SS</sub>	2048 x 8	A10	D7



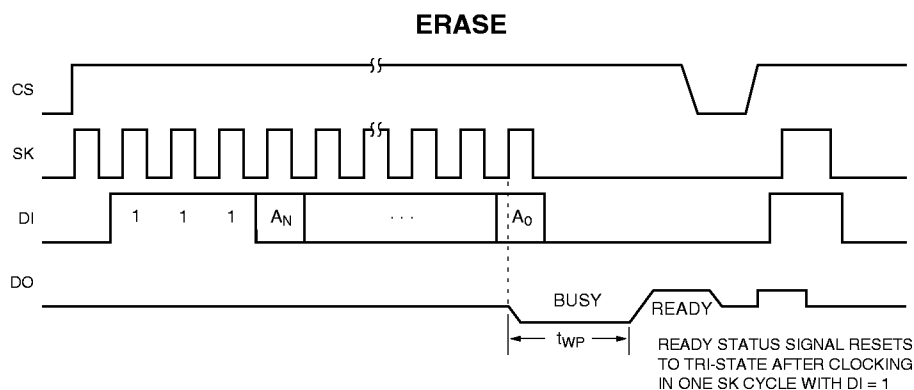
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DS800021-5



DS800021-6

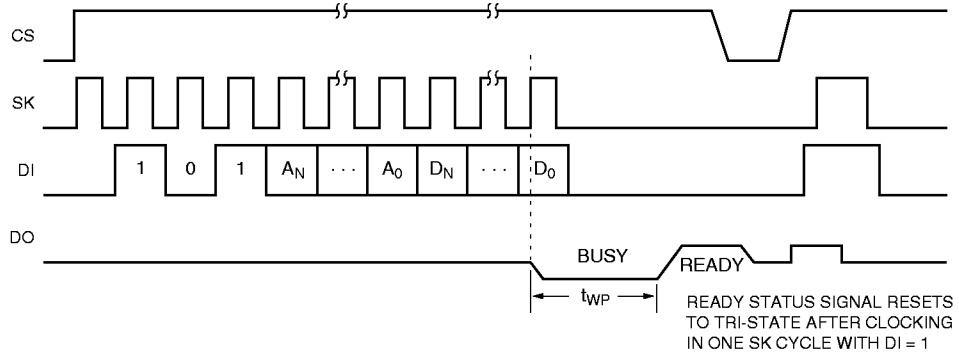


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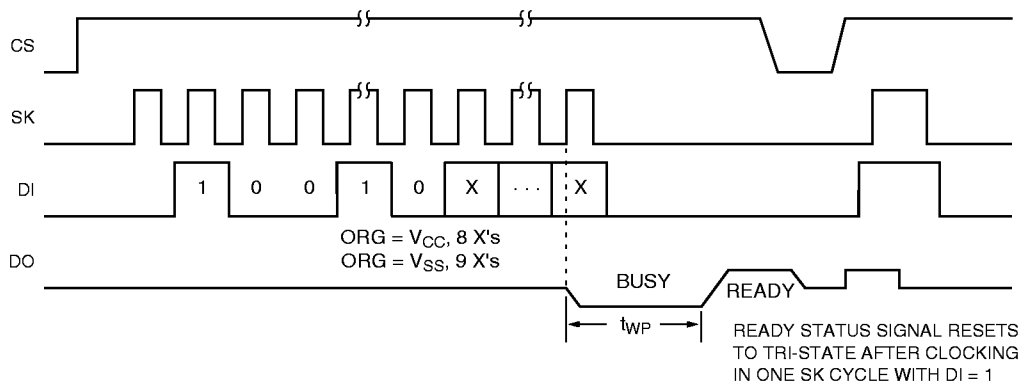
Timing Diagrams for the NM93C86AU (Continued)

WRITE



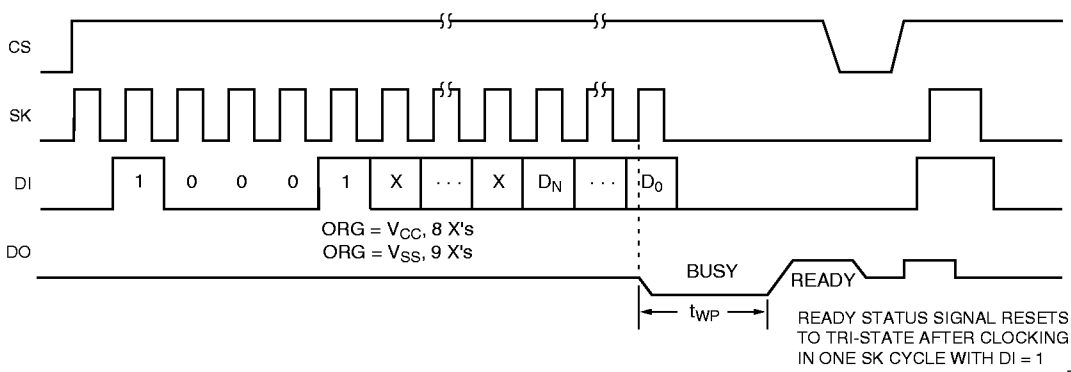
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ERAL



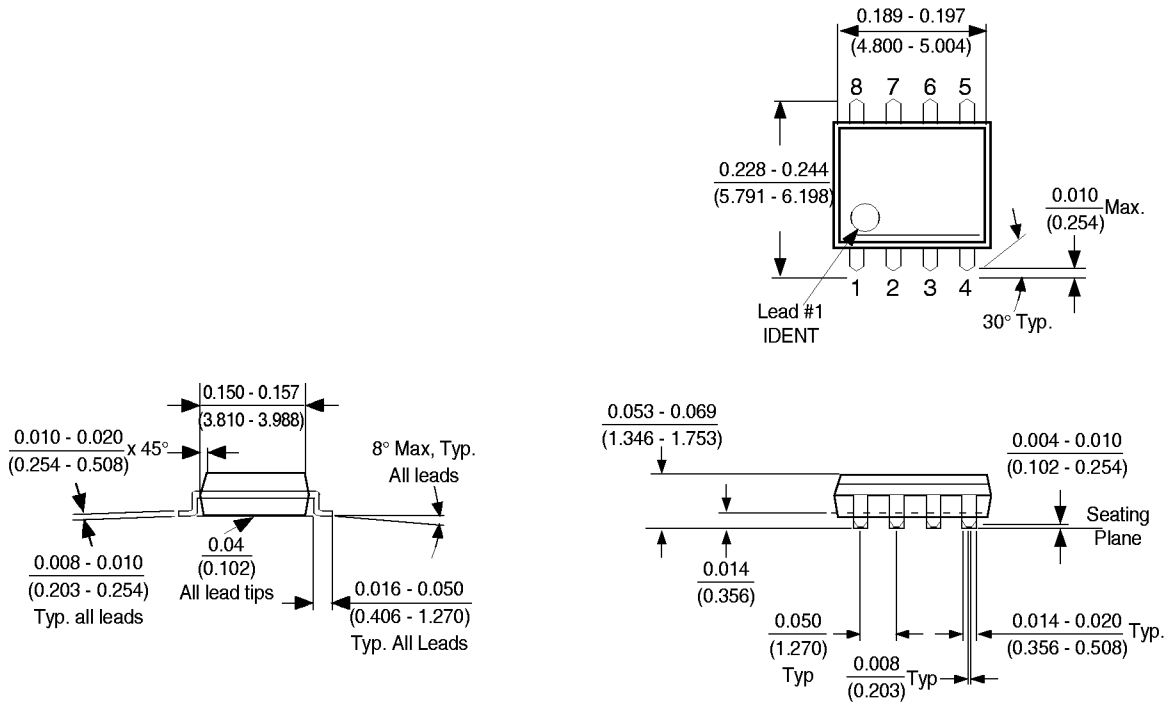
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WRAL



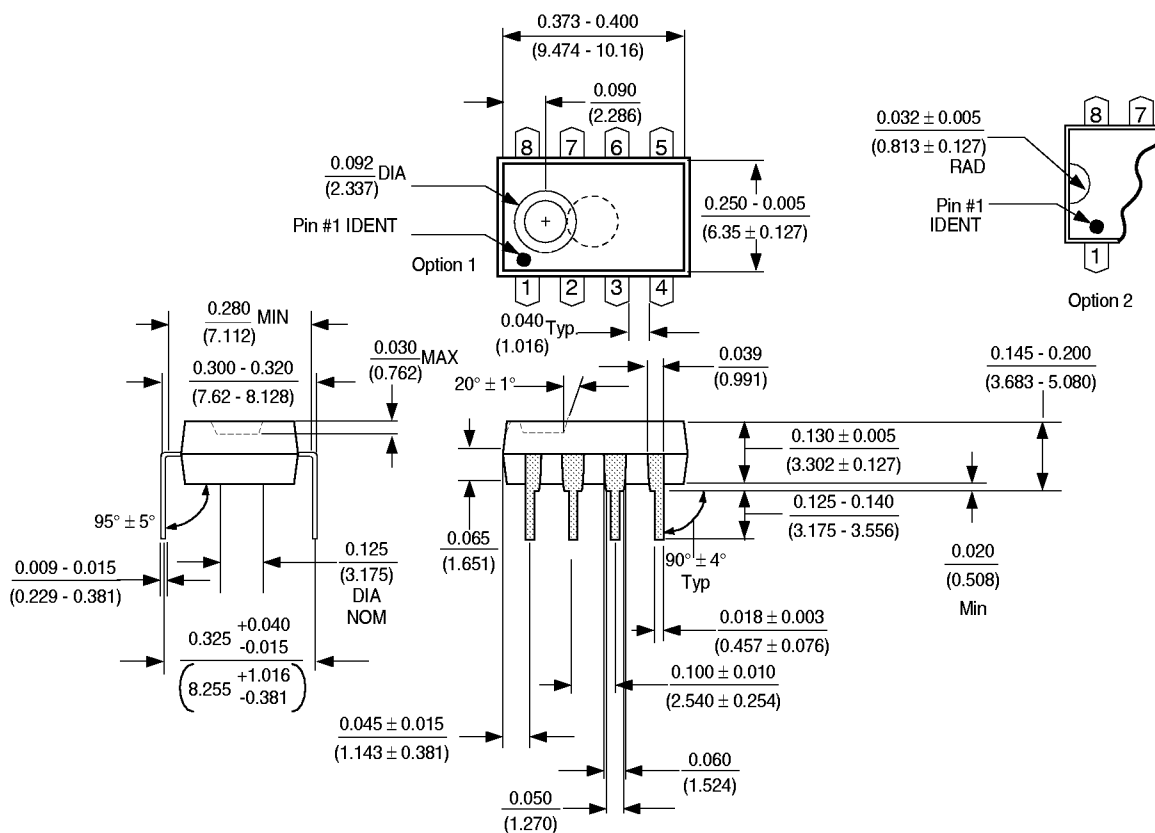
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**Physical Dimensions** inches (millimeters) unless otherwise noted



**Molded Small Outline Package (M8)  
Package Number M08A**

**Physical Dimensions** inches (millimeters) unless otherwise noted



**Molded Dual-in-Line Package (N)  
Package Number N08E**

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