

## Radiation Hardened Dual-D Flip-Flop with Set and Reset

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HCTS74T is a Radiation Hardened positive edge triggered flip-flop with set and reset.

### Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

**Detailed Electrical Specifications for the HCTS74T are contained in SMD 5962-95763.** A "hot-link" is provided from our website for downloading.

[www.intersil.com/spacedefense/newsafclasst.asp](http://www.intersil.com/spacedefense/newsafclasst.asp)

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.

[www.intersil.com/quality/manuals.asp](http://www.intersil.com/quality/manuals.asp)

### Ordering Information

| ORDERING NUMBER | PART NUMBER | TEMP. RANGE (°C) |
|-----------------|-------------|------------------|
| 5962R9576301TCC | HCTS74DTR   | -55 to 125       |
| 5962R9576301TXC | HCTS74KTR   | -55 to 125       |

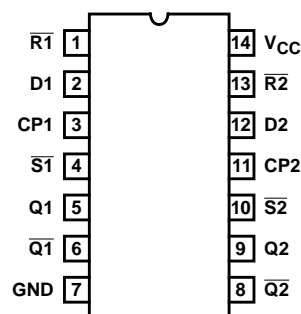
NOTE: **Minimum order quantity for -T is 150 units through distribution, or 450 units direct.**

### Features

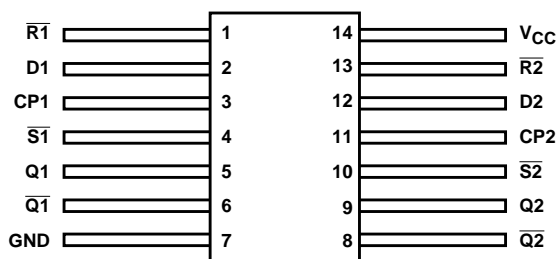
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose ( $\gamma$ )  $1 \times 10^5$  RAD(Si)
  - Latch-Up Free Under Any Conditions
  - SEP Effective LET No Upsets:  $>100$  MEV-cm<sup>2</sup>/mg
  - Single Event Upset (SEU) Immunity  $< 2 \times 10^{-9}$  Errors/Bit-Day (Typ)
- 3 Micron Radiation Hardened SOS CMOS
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - $V_{IL} = 0.8V$  Max
  - $V_{IH} = V_{CC}/2$  Min
- Input Current Levels  $I_i \leq 5mA$  at  $V_{OL}$ ,  $V_{OH}$

### Pinouts

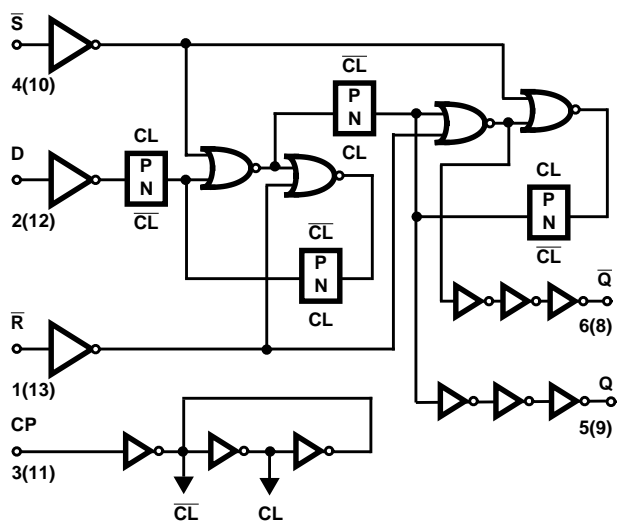
**HCTS74T (SBDIP), CDIP2-T14**  
TOP VIEW



**HCTS74T (FLATPACK), CDFP3-F14**  
TOP VIEW



Functional Diagram



TRUTH TABLE

| INPUTS |       |    |   | OUTPUTS        |                |
|--------|-------|----|---|----------------|----------------|
| SET    | RESET | CP | D | Q              | $\bar{Q}$      |
| L      | H     | X  | X | H              | L              |
| H      | L     | X  | X | L              | H              |
| L      | L     | X  | X | H <sup>†</sup> | H <sup>†</sup> |
| H      | H     |    | H | H              | L              |
| H      | H     |    | L | L              | H              |
| H      | H     | L  | X | Q <sub>0</sub> | $\bar{Q}_0$    |

NOTE: L = Logic Level Low, H = Logic Level High, X = Don't Care  
 = Transition from Low to High Level.

Q<sub>0</sub> = The level of Q before the indicated input conditions were established.

<sup>†</sup> This configuration is non-stable, that is, it will not persist when set and reset inputs return to their inactive (High) level.

# HCTS74T

## Die Characteristics

### DIE DIMENSIONS:

(2261 $\mu\text{m}$  x 2235 $\mu\text{m}$  x 533 $\mu\text{m}$   $\pm$ 51 $\mu\text{m}$ )  
89 x 88 x 21mils  $\pm$ 2mil

### METALLIZATION:

Type: Al Si  
Thickness: 11k $\text{\AA}$   $\pm$ 1k $\text{\AA}$

### SUBSTRATE POTENTIAL:

Unbiased (Silicon on Sapphire)

### BACKSIDE FINISH:

Sapphire

### PASSIVATION:

Type: Silox ( $\text{SiO}_2$ )  
Thickness: 13k $\text{\AA}$   $\pm$ 2.6k $\text{\AA}$

### WORST CASE CURRENT DENSITY:

$< 2.0\text{e}5 \text{ A/cm}^2$

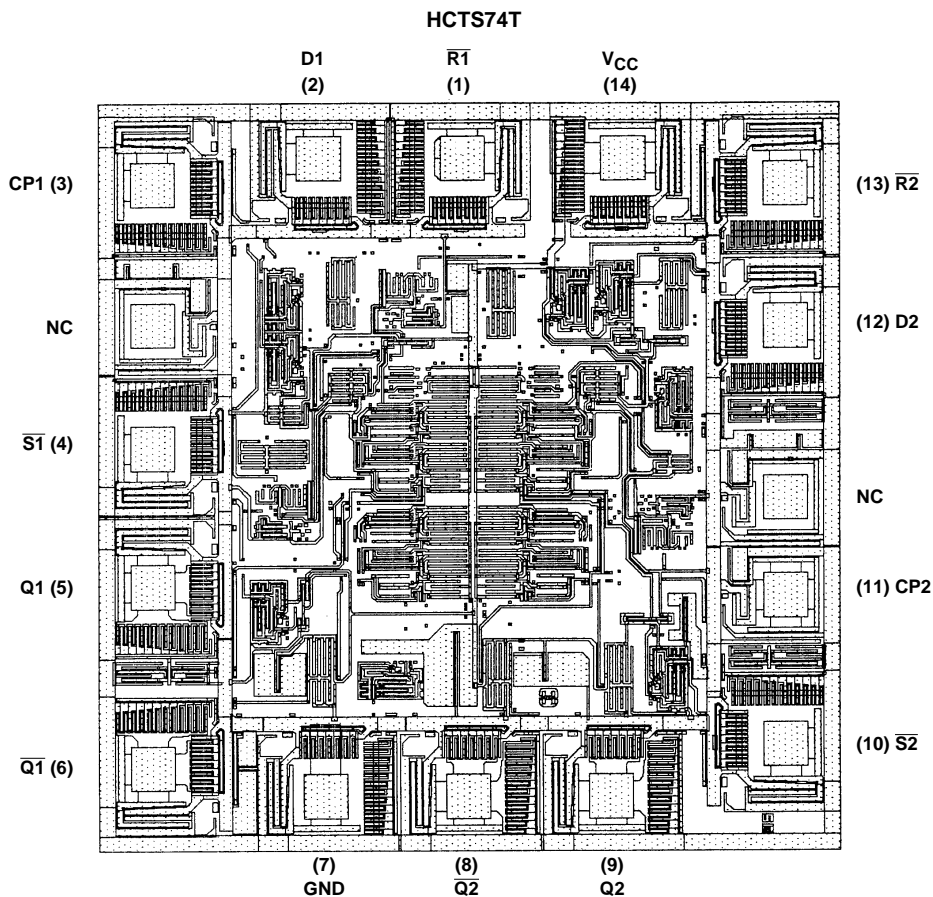
### TRANSISTOR COUNT:

200

### PROCESS:

CMOS SOS

## Metallization Mask Layout



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCTS74 is TA14438A.

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