Data Sheet

C-3e NETWORK PROCESSOR

SILICON REVISION A1

C3ENPA1-DS/D
Rev 03 PRELIMINARY

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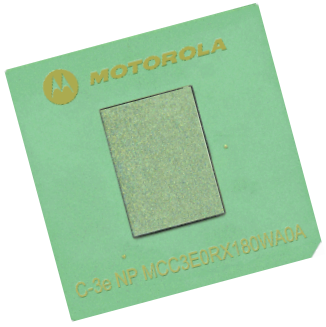

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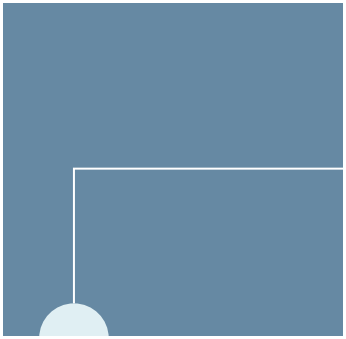
Rev 03

CONTENTS

LIST OF FIGURES

LIST OF TABLES



ABOUT THIS GUIDE

Guide Overview

The C-3e Network Processor Data Sheet describes the hardware layout specifications including pinouts, memory configuration guidelines, timing diagrams, power and power sequencing guidelines, thermal design guidelines, and mechanical specifications. This document contains information on a pre-production product. Specifications and information herein are subject to change without notice.

This guide assumes a good understanding of the C-3e™ Network Processor (NP) architecture. See the *C-5e/C3e Network Processor Architecture GuidE (part number C5EC3EARCH-RM/D)* for more detail about how the hardware works.

This guide also assumes good working knowledge of the C-Ware Software Toolset.

This guide covers the following topics:

- Functional Description
- Signal Descriptions
- Electrical Specifications
- Mechanical Specifications

Data Sheet Classifications

Table 1 describes the Data Sheet classifications of Advance, Preliminary, and Production.

Table 1 Data Sheet Classifications

CLASSIFICATION	DESCRIPTION
Advance Information	Used to advise customers of the proposed addition to the product line. This document will typically contain some useful information including interfacing with the user's system and some specifications. The goal of this document is to allow customers to begin designs but with expectation of changes. Specification details may be changed later without notice.
Preliminary Information	Describes pre-production or first production devices and is usually indicative of production stage performance. Minor changes should be expected as characteristic spreads become better controlled. Specification details may be changed slightly without notice, but the customer can design their product based on this data sheet.
Production Data	Defines the long-term specified production limits based on fully characterized data. It includes a disclaimer to allow improvements in specifications and modifications that do not affect form, fit or function in original applications; if absolute maximum ratings are changed, they should improve rather than downgrade.

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PDF files offer several ways for moving among the document's pages, as follows:

- To move quickly from section to section within the document, use the *Acrobat bookmarks* that appear on the left side of the Acrobat Reader window. The bookmarks provide an expandable outline view of the document's contents. To display the document's Acrobat bookmarks, press the "Display both bookmarks and page" button on the Acrobat Reader tool bar.
- To move to the referenced page of an entry in the document's Contents or Index, click on the entry itself, each of which is hyperlinked.
- To follow a cross-reference to a heading, figure, or table, click the blue text.

- To move to the beginning or end of the document, to move page by page within the document, or to navigate among the pages you displayed by clicking on hyperlinks, use the Acrobat Reader navigation buttons shown in this figure:

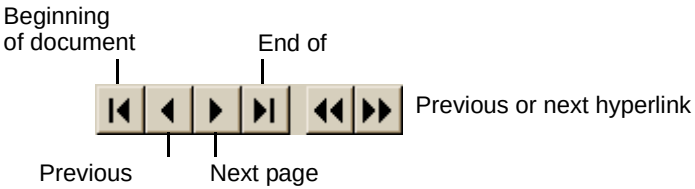


Table 2 summarizes how to navigate within an electronic document.

Table 2 Navigating Within a PDF Document

TO NAVIGATE THIS WAY	CLICK THIS
Move from section to section within the document.	A bookmark on the left side of the Acrobat Reader window
Move to an entry in the Table of Contents.	The entry itself
Move to an entry in the Index.	The page number
Move to an entry in the List of Figures or List of Tables.	The Figure or Table number
Follow a cross-reference (highlighted in blue text).	The cross-reference text
Move page by page.	The appropriate Acrobat Reader navigation buttons
Move to the beginning or end of the document.	The appropriate Acrobat Reader navigation buttons
Move backward or forward among a series of hyperlinks you have selected.	The appropriate Acrobat Reader navigation buttons

Guide Conventions

The following visual elements are used throughout this guide, where applicable:

This icon and text designates information of special note.

Warning: *This icon and text indicate a potentially dangerous procedure. Instructions contained in the warnings must be followed.*

Warning: *This icon and text indicate a procedure where the reader must take precautions regarding laser light.*

This icon and text indicate the possibility of electrostatic discharge (ESD) in a procedure that requires the reader to take the proper ESD precautions.

Revision History

Table 3 provides details about changes made for each revision of this guide.

Table 3 *C-3e Network Processor Data Sheet* Revision History

REVISION DATE	CST REVISION	CDS REVISION	CHANGES
November 8, 2002	2.2	2.0	• Added information about optional capacitors, nominal values for recommended operating conditions, and updated package measurement values. • Pin number typographical correction in Table 28, pin AF12 corrected to FIN4 (instead of FIN14), and pin AE5 corrected to PAD23 (instead of PAD27). • Typographic corrections throughout.

Related Product Documentation

Table 4 lists the user and reference documentation for Motorola 's C-Port silicon documentation set.

Table 4 C-Port Silicon Documentation Set

DOCUMENT SUBJECT	DOCUMENT NAME	PURPOSE	DOCUMENT ID
Processor Information	*C-5 Network Processor Architecture Guide*	Describes the full architecture of the C-5 network processor.	C5NPARCH-RM/D
	C-5 Network Processor Data Sheet	Describes hardware design specifications for the C-5 network processor.	C5NPDATA-DS/D
	C-5e/C-3e Network Processor Architecture Guide	Describes the full architecture of the C-5e and C-3e network processors.	C5EC3EARCH-RM/D
	C-5e Network Processor Data Sheet	Describes hardware design specifications for the C-5e network processor.	C5ENPA1-DS/D
	C-3e Network Processor Data Sheet	Describes hardware design specifications for the C-3e network processor.	C3ENPA1-DS/D
	C-5 Network Processor to C-5e Network Processor Comparison Delta Document	Describes key architectural features of the C-5e, and highlights main differences between C-5 and C-5e.	C5C5EDELTA-RM/D
	M-5 Channel Adapter Architecture Guide	Describes the full architecture of the M-5 channel adapter.	M5CAARCH-RM/D
	M-5 Channel Adapter Data Sheet	Describes hardware design specifications for the M-5 channel adapter.	M5CA0-DS/D
	Q-5/Q-3 Traffic Management Coprocessor Architecture Guide	Describes the full architecture of the Q-5 and Q-3 traffic management coprocessor.	Q5Q3ARCH-RM/D
	Q-5 Traffic Management Coprocessor Data Sheet	Describes hardware design specifications for the Q-5 traffic management coprocessor.	Q5TMCA0-DS/D

Chapter 1

FUNCTIONAL DESCRIPTION

Features

Key features of the C-3e™ Network Processor (NP) are its massive processing capabilities and its high level of functional integration on one chip.

Massive Processing Power

- Operating frequencies: up to 180MHz
- 3Gbps of bandwidth (for non-blocking throughput)
- More than 3,000MIPS of computing power (for adding services throughout the protocol stack)
- Up to 9 million packets per second transmitted at wire speed
- 17 programmable RISC Cores (for cell/packet forwarding)
- 32 programmable Serial Data Processors (for processing bit streams)
- Up to 133 million table lookups per second
- Three internal buses for 46Gbs of aggregate bandwidth

High Functional Integration

- 728 pin Ball Grid Array (BGA) package
- 16 Channel Processors (8 CP's with full functionality configurable for full I/O or recirculation, and 8 CP's with limited functionality configurable only for bit and byte level recirculation) including:
  - Embedded OC-3c, OC-12, OC-12c SONET framers
  - Programmable MAC interface
  - RISC Cores
  - Programmable pin PHY interfaces
- Embedded coprocessors for table lookup (classification), buffer management (payload control), and queue management (QoS implementation)

- Dedicated Fabric Processor and port
- Embedded RISC Executive Processor
- Integrated 32bit 33/66MHz PCI bus interface

Block Diagram

The C-3e™ NP, has an architecture specifically designed for networking applications. The following sections describe each component of the C-3e NP.

The main components of the C-3e NP are:

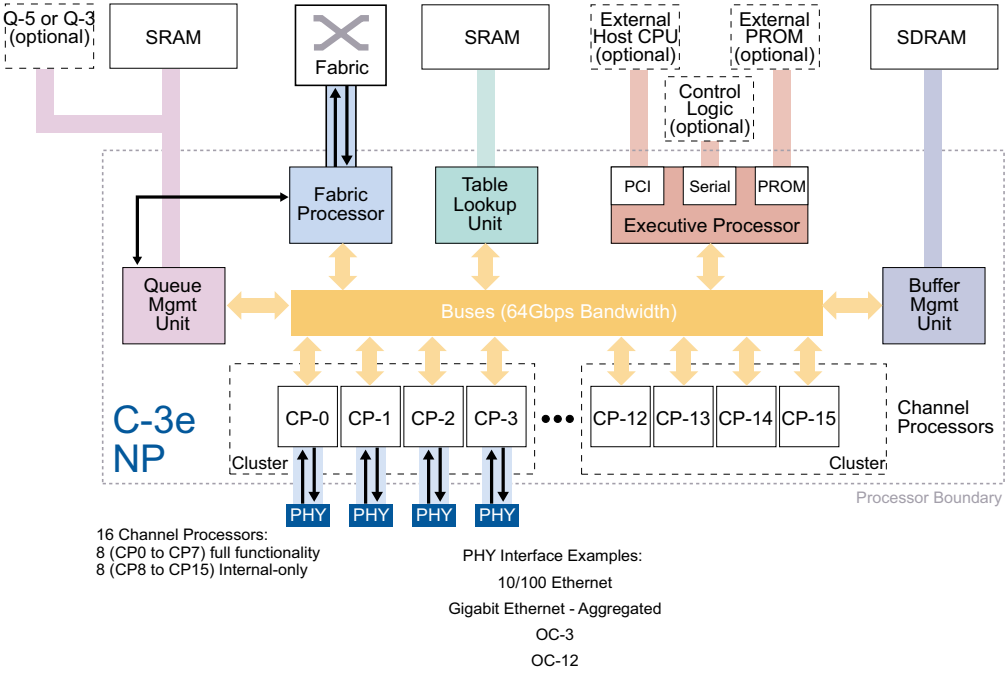
- Channel Processors
- Executive Processor
- Fabric Processor
- Buffer Management Unit
- Table Lookup Unit
- Queue Management Unit

The C-3e NP conforms with both SONET and SDH. Therefore, OC-3(STS-3/STM-1), and OC-12 (STS-12/STM-4).

Figure 1 shows a block diagram of the C-3e NP, including its potential external interfaces.

For more information about the architecture of the C-3e NP, see the *C-5e/C-3e Network Processor Architecture Guide (part number C5EC3EARCH-RM/D)*.

Figure 1 C-3e Network Processor Block Diagram



Channel Processors

The C-3e NP contains eight programmable external Channel Processors (CPs) that receive, process, and transmit network data, plus an additional eight internal CPs that process data. Typically one CP is assigned to each port for medium bandwidth applications (Fast Ethernet to OC-3). Multiple CPs can be assigned to a port in a configuration called *channel aggregation* in high bandwidth applications (greater than OC-3). Multiple logical ports can be assigned to a single CP, with the addition of an external multiplexor, for low bandwidth applications, such as DS1 to DS3.

The C-3e NP's architecture supports a variety of industry-standard serial and parallel protocols and individual port data rates including:

- 10/100Mb Ethernet (RMII)
- 1Gb Ethernet (GMII and TBI)
- OC-3c
- OC-12
- 100Mbit FibreChannel
- DS1/DS3, supported through the use of external framers/multiplexors

The C-3e NP's programmability can also support a variety of special interfaces, such as various xDSL encapsulations and proprietary protocols.

Key components of each CP are a RISC Core (CPRC) that orchestrates cell/packet processing and a set of microprogrammable, special-purpose processors, called Serial Data Processors (SDPs), that provide features such as Ethernet MAC and SONET/SDH framing, multichannel HDLC, and ATM cell delineation. This means you usually only need to include PHYs to complete the system.

Executive Processor

The Executive Processor (XP) serves as a centralized computing resource for the C-3e NP and manages the system interfaces.

The XP performs conventional supervisory tasks in the C-3e NP, including:

- Reset and initialization of the C-3e NP
- Program loading and control of CPs
- Centralized exception handling
- Management of a host interface through the PCI
- Management of system interfaces (PCI, Serial Bus, PROM)

System Interfaces

The system interfaces to the XP are:

- **PCI** — Provides an industry standard 32bit 33/66MHz PCI channel used for chip-level shared resources. The PCI has both *initiator* and *target* capabilities. The PCI interface is typically connected to a host processor.
- **Serial Bus Interface** — Provides a general purpose bi-directional, two-wire serial bus and I/O port that allows the C-3e NP to control external logic with either of two standard protocols:
  - The **MDIO (high-speed) protocol**: uses a 16bit data format with 10bits of addressing and supports transfers up to 25MHz.
  - The **low-speed protocol**: uses an 8bit data format followed by an acknowledge bit and supports transfers up to 400kbps.

  Software is used to select which protocol to use, by setting the appropriate bits in the Serial Bus Configuration Register. When a serial bus transfer is active, an external pin is driven by the C-3e NP to indicate which protocol is being used (SPLD=0 indicates MDIO protocol; SPLD=1 indicates low-speed protocol).

  Both SIDA and SICL are bi-directional lines that are connected, via an external pull-up resistor, to a positive supply voltage. When the bus is free, both lines are HIGH because of the pull-up resistor. The output stages of the devices connected to the bus must have either an open-drain or open-collector in order to perform the wired-AND function required for its arbitration mechanism.

- **PROM Interface** — Allows the XP to boot from nonvolatile, flash memory. The PROM interface is a low-speed, serial I/O port that runs at $^1/_2$ to $^1/_{16}$ the core clock rate. The maximum PROM size addressable is 4MBytes, and must use a "by 16" part. External board logic is required to perform serial-to-parallel conversion for PROM address outputs and parallel-to-serial conversion for PROM data inputs.

Fabric Processor

The Fabric Processor (FP) acts as a high-speed network interface port with advanced functionality. It allows the C-3e NP to interface to an application-specific switching solution internal to your design. The FP port supports the bidirectional transfer of segments from the C-3e NP to a hardware interface that provides connectivity to other network processors or other similar line processing hardware. There are numerous parameters that can be configured within the FP to allow the interface to be adapted to different fabric protocols. The FP can be configured to conform to three (3) different fabric interfaces that include: UTOPIA-1, -2, -3.

The FP can be configured to run at any frequency up to 125MHz, with the receive and transmit data buses up to 16 bits wide. This allows a wide range of supported bandwidths to and from the switching fabric, all the way up to 2000 Mbps full duplex bandwidth.

Buffer Management Unit

The Buffer Management Unit (BMU) interfaces the C-3e NP to external pipeline architecture, Single Data Rate Synchronous DRAM. The external memory is partitioned and used as buffers for receiving and transmitting data between CPs, the FP, and the XP. It is also used as second level storage in the XP memory hierarchy.

The interface to an array of SDRAM chips is 139bits wide, composed of 128 data bits, two internal control bits, and nine SECDED (single error correction-double error detection) ECC (error correction code) bits. The interface is compliant with the PC100 standard and operates at up to 125MHz with 3.3V LVTTL-compatible inputs and outputs. The refresh period, Trcd, Tcas, Trp, Tmrd, and Trc are configurable via boot time configuration (see the *C-5e/C-3e Network Processor Architecture Guide (part number C5EC3EARCH-RM/D)* for more details).

The C-3e NP non-configurable interface transfers four beats of data for each read and write using a sequential burst type. In addition, the C-3e NP uses an auto-refresh mode for the RAM's.

Some of these parameters are programmed into the SDRAMs' mode register and can be applied only once per power cycle. The ECC functionality can be enabled or disabled via configuration register writes.

If needed, the interface can narrowed to 128bits by disabling ECC and providing board pull-ups for the two control bits and nine ECC bits. This is useful if DIMMs are used in the board design. If individual SDRAM parts are used, x16 and x32 are supported. The BMU supports SDRAM devices that use 12 address lines. Internal address calculation paths limit the maximum memory size to 128MBytes. Only one physical bank of SDRAM is supported.

Table Lookup Unit

The Table Lookup Unit (TLU) performs table lookups in external SRAM. It can also be used for statistics accumulation and retrieval and as general data storage. The TLU simultaneously supports multiple application-defined tables and multiple search strategies, such as those needed for routing, circuit switching, and QoS lookup tasks.

The C-3e NP uses external 64bit wide ZBT Pipelined Bursting Static RAM (SRAM) modules (at frequencies up to 125MHz) for storage of its tables. These modules allow implementation of tables with 2^{25} x 64bit entries using 8Mbit SRAM technology. The maximum amount of memory supported by the TLU is 128MBytes in four banks, when SRAM technology supports 4M x 18pins parts.

Table 5 TLU SRAM Configurations

SRAM TECHNOLOGY	MIN TABLE SIZE (ONE BANK)	MAXIMUM TABLE SIZE (FOUR BANKS)
1Mbit (32k x 32pins)	256kBytes	1MBytes
2Mbit (64k x 32pins)	512kBytes	2MBytes
4Mbit (256k x 18pins)	2MBytes	8MBytes
8Mbit (512k x 18pins)	4MBytes	16MBytes
16Mbit (1M x 18pins)	8MBytes	32MBytes
32Mbit (2M x 18pins)	16MBytes	64MBytes
64Mbit (4M x 18pins)	32MBytes	128MBytes

Queue Management Unit

The Queue Management Unit (QMU) autonomously manages a number of application-defined descriptor queues. It handles inter-CP and inter-C-3e NP descriptor flows by providing switching and buffering. It also performs descriptor replication for multicast applications. A number of up to 128 queues can be assigned to each CPRC for QoS-based services.

The QMU provides a queuing engine internal to the chip and uses external SRAM to store the descriptors. Scheduling is done by the CPs. The QMU supports up to 512 queues and 16, 384 descriptor buffers. A descriptor buffer holds an application-defined "descriptor", which is a structure that defines the payload buffer handle and other attributes of the forwarded cell or packet.

The QMU's external SRAM interface uses ZBT synchronous SRAMs organized in a single bank of up to 128k, 32bit words. This interface runs at up to 150MHz frequency.

The C-3e provides two modes for managing queues. They consist of:

- Internal Mode (using the internal QMU only)
- External Mode (using the internal QMU and the external Q-5 Traffic Management Coprocessor, or using the internal QMU and the external Q-3 Traffic Management Coprocessor)**.**

See the *C-5e/C-3e Network Processor Architecture Guide (part number C5EC3EARCH-RM/D),* as well as, the *Q-5/Q-3 Traffic Management Coprocessor Architecture Guide (part number Q5Q3ARCH-RM/D)* for more details.

Chapter 2

SIGNAL DESCRIPTIONS

Signal Summary

There are nine (9) functional groupings of signals in the C-3e Network Processor:

- Clock — 7 pins
- Channel Processors (CP0 - CP7) — 8x7 = 56 pins
- Executive Processor (XP) — 57 pins
  - PCI Interface — 50 pins
  - PROM Interface — 4 pins
  - Serial Bus Interface — 2 pins
  - General System Interface — 1 pin
- Fabric Processor (FP) — 42 pins
- Buffer Management Unit (BMU) — 160 pins
- Table Lookup Unit (TLU) — 99 pins
- Queue Management Unit (QMU) — 59 pins
- Power — 234 pins
- Test — 14 pins

Two (2) of the sections (CPs and FP) are configurable, depending on the type of device being implemented.

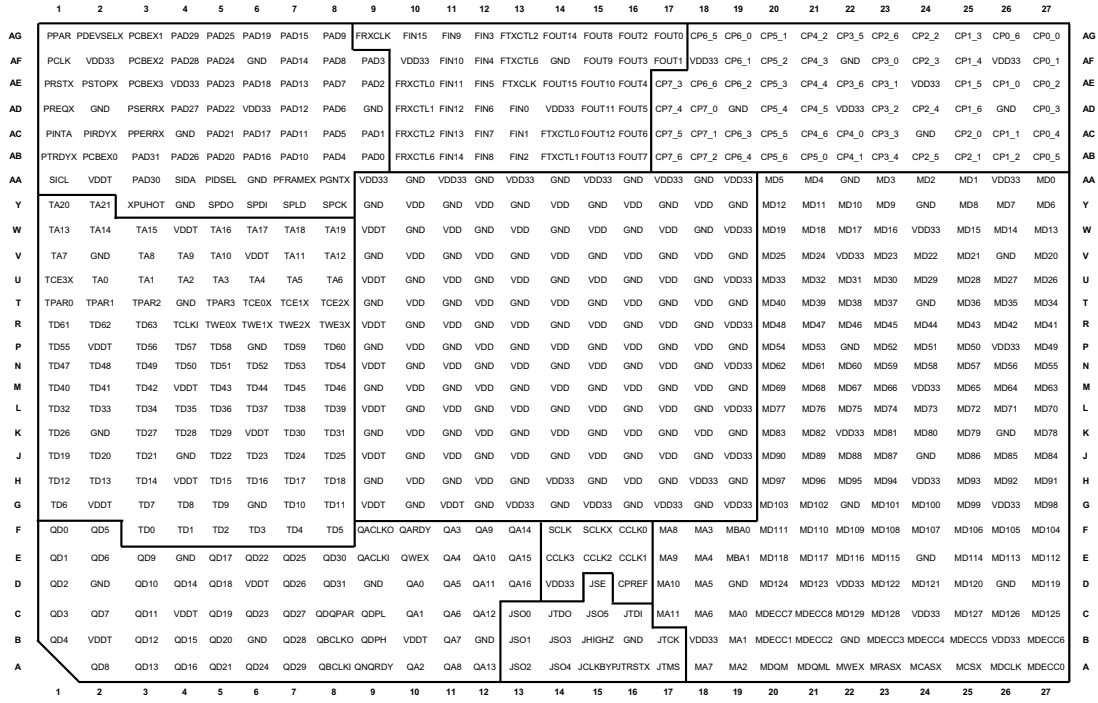
Pinout Diagram

The C-3e NP contains 728 pins. These pin numbers are referenced throughout the remaining chapter. Figure 2 shows the pin locations from the top view. In contrast, Figure 3 shows the pin locations from the bottom view.

Figure 2 Pin Locations (Top View)

	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
AG	CP0_0	CP0_6	CP1_3	CP2_2	CP2_6	CP3_5	CP4_2	CP5_1	CP6_0	CP6_5	FOUT0	FOUT2	FOUT8	FOUT14	FTXCTL2	FIN3	FIN9	FIN15	FRXCLK	PAD9	PAD15	PAD19	PAD25	PAD29	PCBEX1	PDEVSELX	PPAR	AG
AF	CP0_1	VDD33	CP1_4	CP2_3	CP3_0	GND	CP4_3	CP5_2	CP6_1	VDD33	FOUT1	FOUT3	FOUT9	GND	FTXCTL6	FIN4	FIN10	VDD33	PAD3	PAD8	PAD14	GND	PAD24	PAD28	PCBEX2	VDD33	PCLK	AF
AE	CP0_2	CP1_0	CP1_5	VDD33	CP3_1	CP3_6	CP4_4	CP5_3	CP6_2	CP6_6	CP7_3	FOUT4	FOUT10	FOUT15	FTXCLK	FIN5	FIN11	FRXCTL0	PAD2	PAD7	PAD13	PAD18	PAD23	VDD33	PCBEX3	PSTOPX	PRSTX	AE
AD	CP0_3	GND	CP1_6	CP2_4	CP3_2	VDD33	CP4_5	CP5_4	GND	CP7_0	CP7_4	FOUT5	FOUT11	VDD33	FIN0	FIN6	FIN12	FRXCTL1	GND	PAD6	PAD12	VDD33	PAD22	PAD27	PSERRX	GND	PREQX	AD
AC	CP0_4	CP1_1	CP2_0	GND	CP3_3	CP4_0	CP4_6	CP5_5	CP6_3	CP7_1	CP7_5	FOUT6	FOUT12	FTXCTL0	FIN1	FIN7	FIN13	FRXCTL2	PAD1	PAD5	PAD11	PAD17	PAD21	GND	PPERRX	PIRDYX	PINTA	AC
AB	CP0_5	CP1_2	CP2_1	CP2_5	CP3_4	CP4_1	CP5_0	CP5_6	CP6_4	CP7_2	CP7_6	FOUT7	FOUT13	FTXCTL1	FIN2	FIN8	FIN14	FRXCTL6	PAD0	PAD4	PAD10	PAD16	PAD20	PAD26	PAD31	PCBEX0	PTRDYX	AB
AA	MD0	VDD33	MD1	MD2	MD3	GND	MD4	MD5	VDD33	GND	VDD33	GND	VDD33	GND	VDD33	GND	VDD33	GND	VDD33	PGNTX	PFRAMEX	GND	PIDSEL	SIDA	PAD30	VDDT	SICL	AA
Y	MD6	MD7	MD8	GND	MD9	MD10	MD11	MD12	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	SPCK	SPLD	SPDI	SPDO	GND	XPUHOT	TA21	TA20	Y
W	MD13	MD14	MD15	VDD33	MD16	MD17	MD18	MD19	VDD33	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDDT	TA19	TA18	TA17	TA16	VDDT	TA15	TA14	TA13	W
V	MD20	GND	MD21	MD22	MD23	VDD33	MD24	MD25	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	TA12	TA11	VDDT	TA10	TA9	TA8	GND	TA7	V
U	MD26	MD27	MD28	MD29	MD30	MD31	MD32	MD33	VDD33	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDDT	TA6	TA5	TA4	TA3	TA2	TA1	TA0	TCE3X	U
T	MD34	MD35	MD36	GND	MD37	MD38	MD39	MD40	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	TCE2X	TCE1X	TCE0X	TPAR3	GND	TPAR2	TPAR1	TPAR0	T
R	MD41	MD42	MD43	MD44	MD45	MD46	MD47	MD48	VDD33	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDDT	TWE3X	TWE2X	TWE1X	TWE0X	TCLKI	TD63	TD62	TD61	R
P	MD49	VDD33	MD50	MD51	MD52	GND	MD53	MD54	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	TD60	TD59	GND	TD58	TD57	TD56	VDDT	TD55	P
N	MD55	MD56	MD57	MD58	MD59	MD60	MD61	MD62	VDD33	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDDT	TD54	TD53	TD52	TD51	TD50	TD49	TD48	TD47	N
M	MD63	MD64	MD65	VDD33	MD66	MD67	MD68	MD69	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	TD46	TD45	TD44	TD43	VDDT	TD42	TD41	TD40	M
L	MD70	MD71	MD72	MD73	MD74	MD75	MD76	MD77	VDD33	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDDT	TD39	TD38	TD37	TD36	TD35	TD34	TD33	TD32	L
K	MD78	GND	MD79	MD80	MD81	VDD33	MD82	MD83	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	TD31	TD30	VDDT	TD29	TD28	TD27	GND	TD26	K
J	MD84	MD85	MD86	GND	MD87	MD88	MD89	MD90	VDD33	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDDT	TD25	TD24	TD23	TD22	GND	TD21	TD20	TD19	J
H	MD91	MD92	MD93	VDD33	MD94	MD95	MD96	MD97	GND	VDD33	GND	VDD	GND	VDD33	GND	VDD	GND	VDD	GND	TD18	TD17	TD16	TD15	VDDT	TD14	TD13	TD12	H
G	MD98	VDD33	MD99	MD100	MD101	GND	MD102	MD103	VDD33	GND	VDD33	GND	VDD33	GND	VDD33	GND	VDDT	GND	VDDT	TD11	TD10	GND	TD9	TD8	TD7	VDDT	TD6	G
F	MD104	MD105	MD106	MD107	MD108	MD109	MD110	MD111	MBA0	MA3	MA8	CCLK0	SCLKX	SCLK	QA14	QA9	QA3	QARDY	QACLKO	TD5	TD4	TD3	TD2	TD1	TD0	QD5	QD0	F
E	MD112	MD113	MD114	GND	MD115	MD116	MD117	MD118	MBA1	MA4	MA9	CCLK1	CCLK2	CCLK3	QA15	QA10	QA4	QWEX	QACLKI	QD30	QD25	QD22	QD17	GND	QD9	QD6	QD1	E
D	MD119	GND	MD120	MD121	MD122	VDD33	MD123	MD124	GND	MA5	MA10	CPREF	JSE	VDD33	QA16	QA11	QA5	QA0	GND	QD31	QD26	VDDT	QD18	QD14	QD10	GND	QD2	D
C	MD125	MD126	MD127	VDD33	MD128	MD129	MDECC8	MDECC7	MA0	MA6	MA11	JTDI	JSO5	JTDO	JSO0	QA12	QA6	QA1	QDPL	QDQPAR	QD27	QD23	QD19	VDDT	QD11	QD7	QD3	C
B	MDECC6	VDD33	MDECC5	MDECC4	MDECC3	GND	MDECC2	MDECC1	MA1	VDD33	JTCK	GND	JHIGHZ	JSO3	JSO1	GND	QA7	VDDT	QDPH	QBCLKO	QD28	GND	QD20	QD15	QD12	VDDT	QD4	B
A	MDECC0	MDCLK	MCSX	MCASX	MRASX	MWEX	MDQML	MDQM	MA2	MA7	JTMS	JTRSTX	JCLKBYP	JSO4	JSO2	QA13	QA8	QA2	QNQRDY	QBCLKI	QD29	QD24	QD21	QD16	QD13	QD8		A
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 3 Pin Locations (Bottom View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
AG	PPAR	PDEVSELX	PCBEX1	PAD29	PAD25	PAD19	PAD15	PAD9	FRXCLK	FIN15	FIN9	FIN3	FTXCTL2	FOUT14	FOUT8	FOUT2	FOUT0	CP6_5	CP6_0	CP5_1	CP4_2	CP3_5	CP2_6	CP2_2	CP1_3	CP0_6	CP0_0	AG
AF	PCLK	VDD33	PCBEX2	PAD28	PAD24	GND	PAD14	PAD8	PAD3	VDD33	FIN10	FIN4	FTXCTL6	GND	FOUT9	FOUT3	FOUT1	VDD33	CP6_1	CP5_2	CP4_3	GND	CP3_0	CP2_3	CP1_4	VDD33	CP0_1	AF
AE	PRSTX	PSTOPX	PCBEX3	VDD33	PAD23	PAD18	PAD13	PAD7	PAD2	FRXCTL0	FIN11	FIN5	FTXCLK	FOUT15	FOUT10	FOUT4	CP7_3	CP6_6	CP6_2	CP5_3	CP4_4	CP3_6	CP3_1	VDD33	CP1_5	CP1_0	CP0_2	AE
AD	PREQX	GND	PSERRX	PAD27	PAD22	VDD33	PAD12	PAD6	GND	FRXCTL1	FIN12	FIN6	FIN0	VDD33	FOUT11	FOUT5	CP7_4	CP7_0	GND	CP5_4	CP4_5	VDD33	CP3_2	CP2_4	CP1_6	GND	CP0_3	AD
AC	PINTA	PIRDYX	PPERRX	GND	PAD21	PAD17	PAD11	PAD5	PAD1	FRXCTL2	FIN13	FIN7	FIN1	FTXCTL0	FOUT12	FOUT6	CP7_5	CP7_1	CP6_3	CP5_5	CP4_6	CP4_0	CP3_3	GND	CP2_0	CP1_1	CP0_4	AC
AB	PTRDYX	PCBEX0	PAD31	PAD26	PAD20	PAD16	PAD10	PAD4	PAD0	FRXCTL6	FIN14	FIN8	FIN2	FTXCTL1	FOUT13	FOUT7	CP7_6	CP7_2	CP6_4	CP5_6	CP5_0	CP4_1	CP3_4	CP2_5	CP2_1	CP1_2	CP0_5	AB
AA	SICL	VDDT	PAD30	SIDA	PIDSEL	GND	PFRAMEX	PGNTX	VDD33	GND	VDD33	GND	VDD33	GND	VDD33	GND	VDD33	GND	VDD33	MD5	MD4	GND	MD3	MD2	MD1	VDD33	MD0	AA
Y	TA20	TA21	XPUHOT	GND	SPDO	SPDI	SPLD	SPCK	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	MD12	MD11	MD10	MD9	GND	MD8	MD7	MD6	Y
W	TA13	TA14	TA15	VDDT	TA16	TA17	TA18	TA19	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	MD19	MD18	MD17	MD16	VDD33	MD15	MD14	MD13	W
V	TA7	GND	TA8	TA9	TA10	VDDT	TA11	TA12	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	MD25	MD24	VDD33	MD23	MD22	MD21	GND	MD20	V
U	TCE3X	TA0	TA1	TA2	TA3	TA4	TA5	TA6	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	MD33	MD32	MD31	MD30	MD29	MD28	MD27	MD26	U
T	TPAR0	TPAR1	TPAR2	GND	TPAR3	TCE0X	TCE1X	TCE2X	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	MD40	MD39	MD38	MD37	GND	MD36	MD35	MD34	T
R	TD61	TD62	TD63	TCLKI	TWE0X	TWE1X	TWE2X	TWE3X	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	MD48	MD47	MD46	MD45	MD44	MD43	MD42	MD41	R
P	TD55	VDDT	TD56	TD57	TD58	GND	TD59	TD60	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	MD54	MD53	GND	MD52	MD51	MD50	VDD33	MD49	P
N	TD47	TD48	TD49	TD50	TD51	TD52	TD53	TD54	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	MD62	MD61	MD60	MD59	MD58	MD57	MD56	MD55	N
M	TD40	TD41	TD42	VDDT	TD43	TD44	TD45	TD46	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	MD69	MD68	MD67	MD66	VDD33	MD65	MD64	MD63	M
L	TD32	TD33	TD34	TD35	TD36	TD37	TD38	TD39	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	MD77	MD76	MD75	MD74	MD73	MD72	MD71	MD70	L
K	TD26	GND	TD27	TD28	TD29	VDDT	TD30	TD31	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	MD83	MD82	VDD33	MD81	MD80	MD79	GND	MD78	K
J	TD19	TD20	TD21	GND	TD22	TD23	TD24	TD25	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	MD90	MD89	MD88	MD87	GND	MD86	MD85	MD84	J
H	TD12	TD13	TD14	VDDT	TD15	TD16	TD17	TD18	GND	VDD	GND	VDD	GND	VDD33	GND	VDD	GND	VDD33	GND	MD97	MD96	MD95	MD94	VDD33	MD93	MD92	MD91	H
G	TD6	VDDT	TD7	TD8	TD9	GND	TD10	TD11	VDDT	GND	VDDT	GND	VDD33	GND	VDD33	GND	VDD33	GND	VDD33	MD103	MD102	GND	MD101	MD100	MD99	VDD33	MD98	G
F	QD0	QD5	TD0	TD1	TD2	TD3	TD4	TD5	QACLKO	QARDY	QA3	QA9	QA14	SCLK	SCLKX	CCLK0	MA8	MA3	MBA0	MD111	MD110	MD109	MD108	MD107	MD106	MD105	MD104	F
E	QD1	QD6	QD9	GND	QD17	QD22	QD25	QD30	QACLKI	QWEX	QA4	QA10	QA15	CCLK3	CCLK2	CCLK1	MA9	MA4	MBA1	MD118	MD117	MD116	MD115	GND	MD114	MD113	MD112	E
D	QD2	GND	QD10	QD14	QD18	VDDT	QD26	QD31	GND	QA0	QA5	QA11	QA16	VDD33	JSE	CPREF	MA10	MA5	GND	MD124	MD123	VDD33	MD122	MD121	MD120	GND	MD119	D
C	QD3	QD7	QD11	VDDT	QD19	QD23	QD27	QDQPAR	QDPL	QA1	QA6	QA12	JSO0	JTDO	JSO5	JTDI	MA11	MA6	MA0	MDECC7	MDECC8	MD129	MD128	VDD33	MD127	MD126	MD125	C
B	QD4	VDDT	QD12	QD15	QD20	GND	QD28	QBCLKO	QDPH	VDDT	QA7	GND	JSO1	JSO3	JHIGHZ	GND	JTCK	VDD33	MA1	MDECC1	MDECC2	GND	MDECC3	MDECC4	MDECC5	VDD33	MDECC6	B
A		QD8	QD13	QD16	QD21	QD24	QD29	QBCLKI	QNQRDY	QA2	QA8	QA13	JSO2	JSO4	JCLKBYPJ	TRSTX	JTMS	MA7	MA2	MDQM	MDQML	MWEX	MRASX	MCASX	MCSX	MDCLK	MDECC0	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	

Pin Descriptions Grouped by Function

The C-3e NP pins are categorized in groups, reflecting interfaces to the chip:

- Clock Signals
- CP Interface Signals
- Executive Processor System Interface Signals
- Fabric Processor Interface Signals
- BMU SDRAM Interface Signals
- TLU SRAM Interface Signals
- QMU SRAM (Internal Mode) Interface Signals
- QMU to Q-5/Q-3 (External Mode) Interface Signals
- Power Supply Signals
- Test Signals

Pins conform to Joint Electronic Devices Engineering Council (JEDEC) standards.

LVTTL and LVPECL Specifications

C-3e NP pins are the following types:

- Low Voltage TTL-Compatible (LVTTL). The C-3e NP's LVTTL pins conform to the JEDEC JESD8-B specification.
- Low Voltage Positive Emitter Coupled Logic (LVPECL).

All of the signals in the following tables in this chapter denote whether the individual signal is an Input (I), Output (O), both Input and Output (I/O), or power (P). In addition, a PU, PD, and nc are used. The PU indicates that an internal resistor will pullup the pad if left unconnected. PD indicates an internal pulldown resistor. NC means the pad is to be left unconnected.

Clock Signals

Table 6 describes the C-3e NP clock signals.

Table 6 Clock and Reference Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
SCLK* SCLKX*	F14 F15	1 1	LVPECL LVPECL	I I	Core Clock Rate (Differential)
CCLK0	F16	1	LVTTL	I_{PD}	Programmable CP Clock Input
CCLK1	E16	1	LVTTL	I_{PD}	Programmable CP Clock Input
CCLK2	E15	1	LVTTL	I_{PD}	Programmable CP Clock Input
CCLK3	E14	1	LVTTL	I_{PD}	Programmable CP Clock Input
CPREF†	D16	1	LVPECL	I_{PD}	Reference
TOTAL		**7**			

* SCLK and SCLKX must not be AC-coupled.

† If any of the CPs are configured for LVPECL operation (OC3) using the pin mode registers, then CPREF must be wired to an external reference, as specified in Table 34 on page 73. If none of the CPs are configured for LVPECL operation, then the CPREF pin can be left unconnected.

CP Interface Signals

The C-3e NP's 8 external CPs support various network physical interfaces, providing a serial interface to the PHY layer. Interfaces are configured via bits in the C-3e NP register set. Many interfaces are possible by programming the configuration registers. CPs can be used individually or in a cluster (four CPs) to implement the various interfaces.

Table 7 provides a quick reference of all the CP pins organized by clusters. There are seven physical I/O pins associated with each CP. All pins are capable of receiving data, with some configurable to be input clocks, output clocks, or data drivers. In addition, pairs of pins can be configured as differential pairs for LVPECL compatibility.

In the case of RMII, OC-3, DS1, and DS3, the drivers and receivers at the pin are locally configured to match the relevant PHY or Framer chip. OC-12 uses the aggregation of four CPs (one cluster), while GMII and Ten Bit Interface (TBI) can use either eight CPs (four for receive and four for transmit) or four CPs that share the transmit and receive functions for non-wire speed applications.

During CP aggregation, all 28 pins associated with a cluster are routed to all of the Serial Data Processors (SDPs) in that cluster. This allows round-robin usage of portions of the SDPs, with each getting access to the necessary I/O pins.

The signals for the following CP physical interfaces are included in this section:

- DS1/T1 Framer Interface Configuration
- 10/100 Ethernet (RMII) Configuration
- Gigabit Ethernet (GMII) Configuration
- Gigabit Ethernet and Fibre Channel TBI Configuration
- SONET OC-3 Transceiver Interface Configuration
- SONET OC-12 Transceiver Interface Configuration

Table 7 CP Physical Interface Signals and Pins (Grouped by Clusters)

CP CLUSTER 1		CP CLUSTER 2	
SIGNAL	**PIN #**	**SIGNAL**	**PIN #**
CP0_0	AG27	CP4_0	AC22
CP0_1	AF27	CP4_1	AB22
CP0_2	AE27	CP4_2	AG21
CP0_3	AD27	CP4_3	AF21
CP0_4	AC27	CP4_4	AE21
CP0_5	AB27	CP4_5	AD21
CP0_6	AG26	CP4_6	AC21
CP1_0	AE26	CP5_0	AB21
CP1_1	AC26	CP5_1	AG20
CP1_2	AB26	CP5_2	AF20
CP1_3	AG25	CP5_3	AE20
CP1_4	AF25	CP5_4	AD20
CP1_5	AE25	CP5_5	AC20
CP1_6	AD25	CP5_6	AB20
CP2_0	AC25	CP6_0	AG19
CP2_1	AB25	CP6_1	AF19
CP2_2	AG24	CP6_2	AE19
CP2_3	AF24	CP6_3	AC19
CP2_4	AD24	CP6_4	AB19
CP2_5	AB24	CP6_5	AG18
CP2_6	AG23	CP6_6	AE18
CP3_0	AF23	CP7_0	AD18
CP3_1	AE23	CP7_1	AC18
CP3_2	AD23	CP7_2	AB18
CP3_3	AC23	CP7_3	AE17
CP3_4	AB23	CP7_4	AD17

Table 7 CP Physical Interface Signals and Pins (Grouped by Clusters) (continued)

CP CLUSTER 1		CP CLUSTER 2	
SIGNAL	**PIN #**	**SIGNAL**	**PIN #**
CP3_5	AG22	CP7_5	AC17
CP3_6	AE22	CP7_6	AB17

DS1/T1 Framer Interface Configuration

Table 8 describes the serial framer interface signals. For each CP (0-7), you can implement one serial Framer interface.

Table 8 DS1/T1 Framer Interface Signals

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n*_0	Table 7	1	LVTTL	O_{PD}	TCLK	Transmit Clock (1.544MHz)
CP*n*_1	Table 7	1	LVTTL	I_{PU}	RCLK	Receive Clock (1.544MHz)
CP*n*_2	Table 7	1	LVTTL	O_{PD}	TData	Transmit Data
CP*n*_3	Table 7	1	LVTTL	O_{PU}	TFrame	Transmit Frame Synchronization
CP*n*_4	Table 7	1	LVTTL	I_{PD}	RData	Receive Data
CP*n*_5	Table 7	1	LVTTL	I_{PU}	RFrame	Receive Frame Synchronization
CP*n*_6	Table 7	1	nc	nc_{PU}	nc	nc
TOTAL PINS		**7**				

* *n* can be from 0 to 7. See Table 7.

† Reference Table 7 for pin numbers for the actual cluster(s) you are configuring.

10/100 Ethernet (RMII) Configuration

Table 9 describes the 10/100BASE-T Ethernet Reduced Media Independent Interface (RMII) signals. For each CP (0-15), you can implement one 10/100 Ethernet interface.

Table 9 10/100 Ethernet Signals

SIGNAL NAME*	PIN #	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n*_0	Table 7	1	LVTTL	O_{PD}	REF_CLK	Transmit and Receive Clock (50MHz)
CP*n*_1	Table 7	1	LVTTL	I_{PU}	CRS_DV	Carrier Sense (CRS)/ Receive Data Valid (RX_DV). CRS indicates that traffic is on the link, and is asserted if the signal is a 1 or an alternating 1010... RX_DV indicates that a receive frame is in progress and the data present on the RXD pins is valid. It is asserted if this signal is a 1 for more than one cycle.
CP*n*_2	Table 7	1	LVTTL	O_{PD}	TXD(0)	Transmit Data 0 (first on wire)
CP*n*_3	Table 7	1	LVTTL	O_{PU}	TXD(1)	Transmit Data 1 (second on wire)
CP*n*_4	Table 7	1	LVTTL	I_{PD}	RXD(0)	Receive Data 0 (first on wire)
CP*n*_5	Table 7	1	LVTTL	I_{PU}	RXD(1)	Receive Data 1 (second on wire)
CP*n*_6	Table 7	1	LVTTL	O_{PU}	TX_EN	Transmit Enable. When asserted, the data on TXD is encoded and transmitted on the twisted pair cable.
TOTAL PINS		**7**				

* *n* can be from 0 to 7. See Table 7.

Gigabit Ethernet (GMII) Configuration

Gigabit Ethernet Media Independent Interface (GMII) is configured in one of two ways:

- Use one CP cluster when density is more important than wire-speed performance because you can then implement up to four Gigabit Ethernet ports per C-3e NP.
- Use two CP clusters for wire-speed performance and additional processing power. You can implement up to two Gigabit Ethernet ports per C-3e NP.

Table 10 lists the possible CP cluster combinations you can use and Figure 4 shows receive and transmit pin configurations by cluster. Table 11 lists the signals and pinouts for Gigabit Ethernet (GMII).

Table 10 Transmit and Receive Pin Combinations for Gigabit Ethernet and Fibre Channel

CLUSTER	SINGLE CLUSTER MODE (TBI OR GMII)	TWO CLUSTER MODE (GMII)*
0	Port 1 Tx and Rx	Port 1 Tx
1	Port 2 Tx and Rx	Port 1 Rx

* The Two Cluster Mode column lists typical configurations. Any cluster can be set up to either receive or transmit. So you could configure a dual cluster mode where cluster 0 receives and cluster 3 transmits.

Figure 4 GMII/TBI Transmit and Receive Pin Configurations

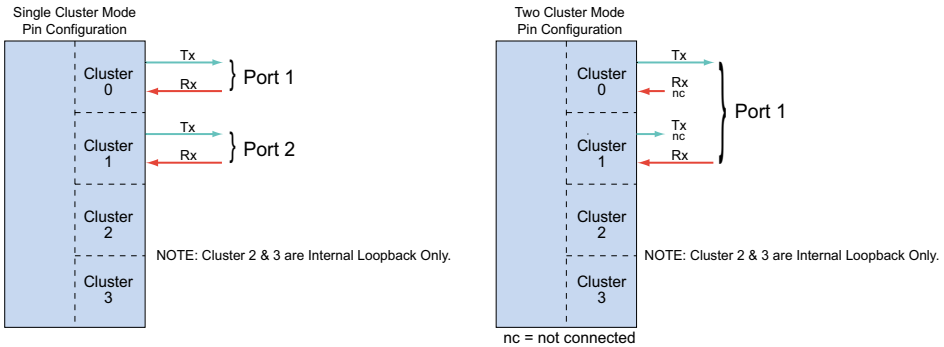


Table 11 Gigabit Ethernet (GMII/MII) Signals One Cluster Example

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n*_0	Table 7	1	LVTTL	O_{PD}	T_CLK	GMII Transmit Clock (125MHz). This clock is used to synchronize the transmit data.
CP*n*_1	Table 7	1	LVTTL	I_{PU}	TCLKI	MII transmit clock. Transmit data aligned to this clock input from phy in MII mode. 25 Mhz in 100BaseT, 2.5 in Mhz in 10BaseT
CP*n*_2	Table 7	1	LVTTL	O_{PD}	TXD(0)	Transmit Data (byte-wide data, least significant bit)
CP*n*_3	Table 7	1	LVTTL	O_{PU}	TXD(1)	Transmit Data
CP*n*_4	Table 7	1	LVTTL	O_{PD}	TXD(2)	Transmit Data
CP*n*_5	Table 7	1	LVTTL	O_{PU}	TXD(3)	Transmit Data
CP*n*_6	Table 7	1	LVTTL	O_{PU}	TX_EN	Transmit Enable. When asserted, the data on TXD is encoded and transmitted on the twisted pair cable.
CP*n+1*_0	Table 7	1	nc	nc_{PD}	nc	nc
CP*n+1*_1	Table 7	1	LVTTL	I_{PU}	COL	Collision. Asserted when both RX_DV and TX_EN are valid during half duplex operation.
CP*n+1*_2	Table 7	1	LVTTL	O_{PD}	TXD(4)	Transmit Data
CP*n+1*_3	Table 7	1	LVTTL	O_{PU}	TXD(5)	Transmit Data
CP*n+1*_4	Table 7	1	LVTTL	O_{PD}	TXD(6)	Transmit Data
CP*n+1*_5	Table 7	1	LVTTL	O_{PU}	TXD(7)	Transmit Data (byte-wide receive data, most significant bit)
CP*n+1*_6	Table 7	1	LVTTL	O_{PU}	TX_ER	Transmit Error. Asserting TX_ER when TX_EN is a 1 causes transmission of the designated “bad code” in lieu of the normal encoded data on the twisted pair data.
CP*n+2*_0	Table 7	1	nc	nc_{PD}	nc	nc
CP*n+2*_1	Table 7	1	LVTTL	I_{PU}	RCLK	Receive Clock (125MHz)
CP*n+2*_2	Table 7	1	LVTTL	I_{PD}	RXD(0)	Receive Data (byte-wide receive data, least significant bit)
CP*n+2*_3	Table 7	1	LVTTL	I_{PU}	RXD(1)	Receive Data
CP*n+2*_4	Table 7	1	LVTTL	I_{PD}	RXD(2)	Receive Data
CP*n+2*_5	Table 7	1	LVTTL	I_{PU}	RXD(3)	Receive Data
CP*n+2*_6	Table 7	1	LVTTL	I_{PU}	RX_DV	Receive Data Valid. Indicates that there is a receive frame in progress and that the data present on the RXD signals is valid.
CP*n+3*_0	Table 7	1	nc	nc_{PD}	nc	nc
CP*n+3*_1	Table 7	1	LVTTL	I_{PU}	CRS	Carrier Sense. Indicates traffic is on the link. CRS is asserted when a non-idle condition is detected on the receive data stream. CRS is deasserted when an end of frame or idle condition is detected.

Table 11 Gigabit Ethernet (GMII/MII) Signals One Cluster Example (continued)

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n+3*_2	Table 7	1	LVTTL	I_{PD}	RXD(4)	Receive Data
CP*n+3*_3	Table 7	1	LVTTL	I_{PU}	RXD(5)	Receive Data
CP*n+3*_4	Table 7	1	LVTTL	I_{PD}	RXD(6)	Receive Data
CP*n+3*_5	Table 7	1	LVTTL	I_{PU}	RXD(7)	Receive Data (most significant bit)
CP*n+3*_6	Table 7	1	LVTTL	I_{PU}	RX_ER	Receive Error Detected. Indicates that there has been an error received in the receive frame.
TOTAL PINS		**28**				

* n can be 0, or 4.
† Reference Table 7 for pin numbers for the actual cluster(s) you are configuring.

Gigabit Ethernet and Fibre Channel TBI Configuration

1000BASE-T Gigabit Ethernet and Fibre Channel TBI is implemented in much the same way as Gigabit Ethernet (GMII). Table 10 shows the possible CP pin combinations you can use and Figure 4 shows receive and transmit pin configurations by cluster. Table 12 shows the signals and pinouts for a single cluster for Gigabit Ethernet and Fibre Channel TBI.

The unused pins for the two cluster configurations should be wired down using a resistor.

Table 12 Gigabit Ethernet and Fibre Channel TBI Signals Example

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n*_0	Table 7	1	LVTTL	O_{PD}	TCLK	Transmit Clock (125MHz). This clock is used to synchronize the transmit data.
CP*n*_1	Table 7	1	nc	nc_{PU}	nc	nc
CP*n*_2	Table 7	1	LVTTL	O_{PD}	TXD(9)	Transmit Data (ten bits wide, last on wire)
CP*n*_3	Table 7	1	LVTTL	O_{PU}	TXD(8)	Transmit Data
CP*n*_4	Table 7	1	LVTTL	O_{PD}	TXD(7)	Transmit Data
CP*n*_5	Table 7	1	LVTTL	O_{PU}	TXD(6)	Transmit Data
CP*n*_6	Table 7	1	LVTTL	O_{PU}	TXD(1)	Transmit Data
CP*n+1*_0	Table 7	1	nc	nc_{PD}	nc	nc
CP*n+1*_1	Table 7	1	nc	nc_{PU}	nc	nc
CP*n+1*_2	Table 7	1	LVTTL	O_{PD}	TXD(5)	Transmit Data

Table 12 Gigabit Ethernet and Fibre Channel TBI Signals Example (continued)

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n+1*_3	Table 7	1	LVTTL	O_{PU}	TXD(4)	Transmit Data
CP*n+1*_4	Table 7	1	LVTTL	O_{PD}	TXD(3)	Transmit Data
CP*n+1*_5	Table 7	1	LVTTL	O_{PU}	TXD(2)	Transmit Data
CP*n+1*_6	Table 7	1	LVTTL	O_{PU}	TXD(0)	Transmit Data (ten bits wide, first on wire)
CP*n+2*_0	Table 7	1	nc	nc_{PD}	nc	nc
CP*n+2*_1	Table 7	1	LVTTL	I_{PU}	RCLK	Receive Clock (62.5 MHz)
CP*n+2*_2	Table 7	1	LVTTL	I_{PD}	RXD(9)	Receive Data (ten bits wide, last on wire)
CP*n+2*_3	Table 7	1	LVTTL	I_{PU}	RXD(8)	Receive Data
CP*n+2*_4	Table 7	1	LVTTL	I_{PD}	RXD(7)	Receive Data
CP*n+2*_5	Table 7	1	LVTTL	I_{PU}	RXD(6)	Receive Data
CP*n+2*_6	Table 7	1	LVTTL	I_{PU}	RXD(1)	Receive Data
CP*n+3*_0	Table 7	1	nc	nc_{PD}	nc	nc
CP*n+3*_1	Table 7	1	LVTTL	I_{PU}	RCLKN	Receive Clock Inverted
CP*n+3*_2	Table 7	1	LVTTL	I_{PD}	RXD(5)	Receive Data
CP*n+3*_3	Table 7	1	LVTTL	I_{PU}	RXD(4)	Receive Data
CP*n+3*_4	Table 7	1	LVTTL	I_{PD}	RXD(3)	Receive Data
CP*n+3*_5	Table 7	1	LVTTL	I_{PU}	RXD(2)	Receive Data
CP*n+3*_6	Table 7	1	LVTTL	I_{PU}	RXD(0)	Receive Data (ten bits wide, first on wire)
TOTAL PINS		**28**				

* n can be 0, or 4.

† Reference Table 7 for pin numbers for the actual cluster(s) you are configuring.

SONET OC-3 Transceiver Interface Configuration

Table 13 describes the SONET Optical Carrier (OC) 3 transceiver interface signals. For each CP (0-15), you can implement a single OC-3 interface.

Table 13 OC-3 Signals

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n*_0	Table 7	1	LVPECL	I_{PD}	RCLK_H	Receive Clock noninverted side of pair (155.52MHz)
CP*n*_1	Table 7	1	LVPECL	I_{PU}	RCLK_L	Receive Clock inverted side of pair (155.52MHz)
CP*n*_2	Table 7	1	LVPECL	O_{PD}	TXD_H	Transmit Data noninverted side of pair
CP*n*_3	Table 7	1	LVPECL	I_{PU}	TXD_L	Transmit Data inverted side of pair
CP*n*_4	Table 7	1	LVPECL	I_{PD}	RXD_H	Receive Data noninverted side of pair
CP*n*_5	Table 7	1	LVPECL	I_{PU}	RXD_L	Receive Data inverted side of pair
CP*n*_6	Table 7	1	LVPECL	I_{PU}	SIGNAL_DET	A light level above a certain threshold is present at the optical receiver - single ended LVPECL.
TOTAL PINS		**7**				

* *n* can be from 0 to 7.

† Reference Table 7 for pin numbers for the actual cluster(s) you are configuring.

SONET OC-12 Transceiver Interface Configuration

SONET Optical Carrier (OC) 12 is implemented by using one cluster of CPs. At any time, a CP within a cluster spends half its time performing receive functions, and the other half performing transmit functions. Table 14 shows a CP Cluster configured for one OC-12 interface.

Table 14 OC-12 Signals Example

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n*_0	Table 7	1	LVTTL	O_{PD}	TCLK	Deskewed Transmit Clock (77.76MHz). This clock is used to synchronize the transmit data.
CP*n*_1	Table 7	1	LVTTL	I_{PU}	TCLKI	Transceiver Transmit Clock. This clock sets the frequency of the transmit data and is typically sourced by the PHY chip.
CP*n*_2	Table 7	1	LVTTL	O_{PD}	TXD(0)	Transmit Data (byte-wide data, least significant bit)
CP*n*_3	Table 7	1	LVTTL	O_{PU}	TXD(1)	Transmit Data
CP*n*_4	Table 7	1	LVTTL	O_{PD}	TXD(2)	Transmit Data
CP*n*_5	Table 7	1	LVTTL	O_{PU}	TXD(3)	Transmit Data
CP*n*_6	Table 7	1	LVTTL	O_{PU}	00F	Out of Frame
CP*n+1*_0	Table 7	1	nc	nc_{PD}	nc	nc
CP*n+1*_1	Table 7	1	nc	nc_{PU}	nc	nc
CP*n+1*_2	Table 7	1	LVTTL	O_{PD}	TXD(4)	Transmit Data
CP*n+1*_3	Table 7	1	LVTTL	O_{PU}	TXD(5)	Transmit Data
CP*n+1*_4	Table 7	1	LVTTL	O_{PD}	TXD(6)	Transmit Data
CP*n+1*_5	Table 7	1	LVTTL	O_{PU}	TXD(7)	Transmit Data (byte-wide data, most significant bit)
CP*n+1*_6	Table 7	1	nc	nc_{PU}	nc	nc
CP*n+2*_0	Table 7	1	nc	nc_{PD}	nc	nc
CP*n+2*_1	Table 7	1	LVTTL	I_{PU}	RCLK	Receive Clock (77.76MHz)
CP*n+2*_2	Table 7	1	LVTTL	I_{PD}	RXD(0)	Receive Data (byte-wide receive data, least significant bit)
CP*n+2*_3	Table 7	1	LVTTL	I_{PU}	RXD(1)	Receive Data
CP*n+2*_4	Table 7	1	LVTTL	I_{PD}	RXD(2)	Receive Data
CP*n+2*_5	Table 7	1	LVTTL	I_{PU}	RXD(3)	Receive Data
CP*n+2*_6	Table 7	1	LVTTL	I_{PU}	FP	Frame Synchronization Pulse. This is valid during the third A2 of the receive SONET frame.
CP*n+3*_0	Table 7	1	nc	nc_{PD}	nc	nc

Table 14 OC-12 Signals Example (continued)

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n+3*_1	Table 7	1	nc	nc_{PU}	nc	nc
CP*n+3*_2	Table 7	1	LVTTL	I_{PD}	RXD(4)	Receive Data
CP*n+3*_3	Table 7	1	LVTTL	I_{PU}	RXD(5)	Receive Data
CP*n+3*_4	Table 7	1	LVTTL	I_{PD}	RXD(6)	Receive Data
CP*n+3*_5	Table 7	1	LVTTL	I_{PU}	RXD(7)	Receive Data (most significant bit)
CP*n+3*_6	Table 7	1	nc	nc_{PU}	nc	nc
TOTAL PINS		**28**				

* n can be 0, or 4.

† Reference Table 7 for pin numbers for a different cluster.

Executive Processor System Interface Signals

The XP's system interface manages the supervisory controls for the network interfaces, as well as the set of pins that provide interfaces to other components in the system that are not memories or network interfaces. It is also the primary interface used for initializing the C-3e NP after reset. The XP signals include PCI signals, Serial interface signals, and PROM interface signals.

PCI Signals

The PCI can be configured to support a 32bit PCI capable of operating at either 33MHz or 66MHz. The PCI is fully compliant with PCI Specification revision 2.1. Table 15 describes the PCI signals.

Table 15 PCI Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
PAD0 - PAD31	AB9, AC9, AE9, AF9, AB8, AC8, AD8, AE8, AF8, AG8, AB7, AC7, AD7, AE7, AF7, AG7, AB6, AC6, AE6, AG6, AB5, AC5, AD5, AE5, AF5, AG5, AB4, AD4, AF4, AG4, AA3, AB3,	32	PCI	I/O	Multiplexed Address/Data Bus. These signals are multiplexed address and data bits. The C-3e NP receives addresses as target and drives addresses as master. It drives the data and receives read data as master.
PCBEX0 - PCBEX3	AB2, AG3, AF3, AE3	4	PCI	I/O	Command byte enables. These signals are multiplexed command and byte enabled signals. The C-3e NP receives byte enables as target and drives byte enables as master.
PPAR	AG1	1	PCI	I/O	Parity. This signal carries even parity for AD and CBE# pins. It has the same receive and drive characteristics as the address and data bus, except that it is one PCI cycle later.
PFRAMEX	AA7	1	PCI	I/O	Cycle frame
PTRDYX	AB1	1	PCI	I/O	Target ready for data transfer
PIRDYX	AC2	1	PCI	I/O	Initiator ready for data transfer
PSTOPX	AE2	1	PCI	I/O	Target transaction stop request
PDEVSELX	AG2	1	PCI	I/O	Target device selected
PPERRX	AC3	1	PCI	I/O	Bus parity error
PSERRX	AD3	1	PCI	I/O	System error
PCLK	AF1	1	I_{PD}	I	Bus clock
PRSTX	AE1	1	PCI	I	Bus reset
PREQX	AD1	1	PCI	O	Initiator bus request (arbitration)

Table 15 PCI Signals (continued)

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
PGNTX	AA8	1	I_{PD}	I	Initiator bus grant (arbitration)
PIDSEL	AA5	1	PCI	I	Initialization device select
PINTA	AC1	1	PCI	O	Interrupt
TOTAL PINS		**50**			

Serial Interface Signals

The Serial interface is a bidirectional two-wire serial bus. It can use one of the following formats:

- An 8bit data format followed by an acknowledge bit, which supports transfers at up to 400kbps (low speed).
- a 16bit IEEE 802.3 MDIO data format with 10bits of addressing, which supports transfers up to 25MHz (high speed).

The signals and pins are identical for both the high and low speed protocols.

Which of the two data rates used is selected by the state of the PROM interface's SPLD signal that is asserted while the PROM interface is idle. When SPLD is asserted HI *the low speed serial bus protocol is selected and when SPLD is asserted* LOW *the MDIO protocol is selected.*

The bus only supports a single master hierarchy that can operate as either a receiver or a transmitter.

Both SIDA and SICL are bidirectional lines that are connected, through a pull-up resistor, to a positive supply voltage. When the bus is free, both lines are HIGH. The output stages of the devices connected to the bus must have either an open-drain or open-collector in order to perform the wired-AND function required for its arbitration mechanism.

Table 16 Serial Interface Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
SICL	AA1	1	LVTTL	I_{PD}/O	Serial Clock line
SIDA	AA4	1	LVTTL	I_{PD}/O	Serial Data line
TOTAL PINS		**2**			

PROM Interface Signals

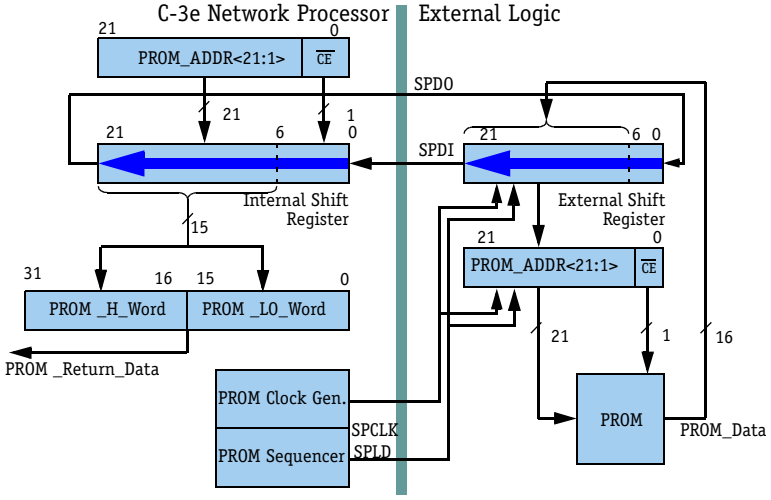
The PROM interface is a low speed I/O port that allows the C-3e NP to communicate through external logic to PROM. The PROM clock is $^1/_2$ to $^1/_{16}$ the core clock rate.The maximum PROM size addressable is 4MBytes, and must use a “by 16” part. The PROM signals are listed in Table 17.

Table 17 PROM Interface Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
SPDO	Y5	1	LVTTL	O	Serial Data Out
SPDI	Y6	1	LVTTL	I_{PD}	Serial Data In
SPLD	Y7	1	LVTTL	O	When load is asserted on a positive clock edge, the external logic performs a parallel load. On each positive clock edge when load is de-asserted, the shift registers shift. When the PROM interface is idle: • if SPLD is asserted HI it indicates low speed serial protocol, • if asserted LOW it indicates MDIO serial protocol.
SPCK	Y8	1	LVTTL	O	Clock
TOTAL PINS		**4**			

Figure 5 shows the connections between the PROM Interface and external board logic. The application is required to provide an external shift register with parallel-in and parallel-out capabilities, and a parallel load register. Both devices should be positive-edge-triggered and perform a parallel load whenever SPLD is asserted. When SPLD is deasserted the shift register shifts.

Figure 5 PROM Interface Diagram



The PROM interface operates in the following manner (Note that two accesses are piplined together to execute one 32-bit fetch). The steps are shown in Figure 6.

1 The PROM_ADDR is loaded into the network processor internal shift register.

2 The PROM_ADDR is shifted into the external shift register for 22 SPCLK cycles.

3 SPLD is asserted for one SPCLK cycle, loading the PROM_ADDR into the external presentation register.

4 SPLD is deasserted for 22 SPCLK cycles. The PROM presents the first 16bit PROM_DATA. At the same time, the next PROM_ADDR is shifted into the external shift register.

5 SPLD is asserted for one SPCLK cycle, loading the PROM_ADDR into the external presentation register and the first PROM_DATA into the external shift register.

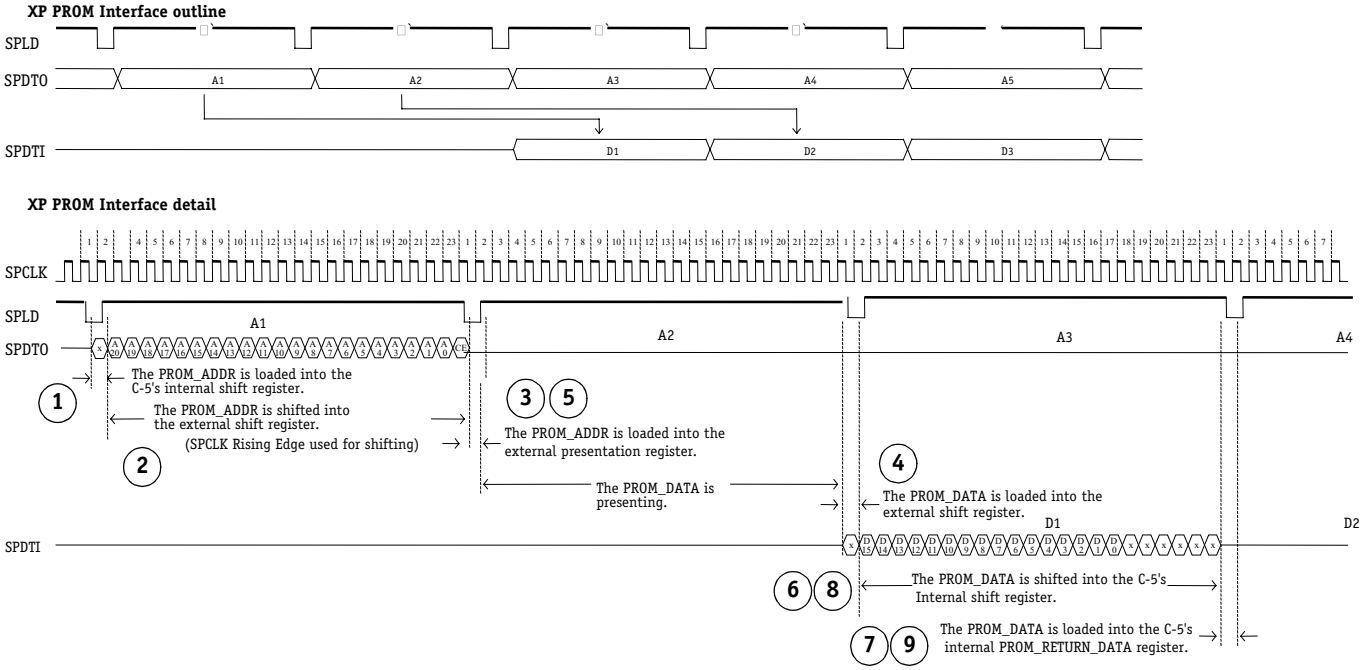
6 SPLD is deasserted for 22 SPCLK cycles, shifting the first PROM_DATA into the network processor internal shift register.

7 SPLD is asserted for one SPCLK cycle, loading the first PROM_DATA into the network processor PROM_RETURN_DATA register and the second PROM_DATA into the external shift register.

8 SPLD is deasserted for 22 SPCLK cycles, shifting the second PROM_DATA into the network processor internal shift register.

9 SPLD is asserted for one SPCLK cycle, loading the second PROM_DATA into the network processor PROM_RETURN_DATA register.

Figure 6 PROM Interface Timing Outline



General System Interface Signal

Table 18 provides the signal for the Executive Processor reset power status and I/O clock. The C-3e NP can be powered up with the XP either running or with the XP in reset mode similar to the CPs. When the XP remains in reset mode, an external host can be used to control the initialization of the C-3e NP.

Table 18 General System Interface Signal

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
XPUHOT	Y3	1	LVTTL	I_{PD}	Sample at Power On Reset determines if the XP RISC Core is held in reset. Low equals reset and High equals active. During normal operation, this is an external interrupt.
TOTAL PINS		**1**			

Fabric Processor Interface Signals

The FP has logical signal interfaces: a receive data interface and a transmit data interface, each with its own control, data, and clock signals. The interface has the following characteristic:

The interface clocks FRXCLK and FTXCLK can have a different frequency from the core C-3e NP clock frequency. The FP supports a fabric interface frequency from 10MHz to 125MHz.

FRXCLK and FTXCLK can be independent of each other; typically they have the same frequency, but are allowed to be skewed relative to each other.

Each data bus can be configured for widths of 8 (data bits 7:0 are used), or 16 (bits 15:0). In 8bit mode, data bits 15:8 are unused.

Table 19 Fabric Interface Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
FIN0 - FIN15	AD13, AC13, AB13, AG12, AF12, AE12, AD12, AC12, AB12, AG11, AF11, AE11, AD11, AC11, AB11, AG10	16	LVTTL	I_{PD}	Fabric Data Bus In
FOUT0 - FOUT15	AG17, AF17, AG16, AF16, AE16, AD16, AC16, AB16, AG15, AF15, AE15, AD15, AC15, AB15, AG14, AE14	16	LVTTL	O	Fabric Data Bus Out
FRXCLK	AG9	1	LVTTL	I_{PD}	Receive Clock
FTXCLK	AE13	1	LVTTL	I_{PD}	Transmit Clock
FRXCTL0 - FRXCTL2 & FRXCTL6	AE10, AD10, AC10, AB10	4	LVTTL	I_{PD}, O	Receive Control Signals
FTXCTL0 - FRXCTL2 & FTXCTL6	AC14, AB14, AG13, AF13	4	LVTTL	I_{PD}, O	Transmit Control Signals
TOTAL PINS		**42**			

The following tables list the Fabric Interface pin mappings:

- Utopia1, Utopia2, Utopia3 ATM Mode mappings are listed in Table 20
- Utopia1, Utopia2, Utopia3 PHY Mode mappings are listed in Table 21

Table 20 Utopia1*, 2*, 3 ATM Mode, C-3e Network Processor to Fabric Interface Pin Mapping

RECEIVE SIGNALS				TRANSMIT SIGNALS			
C-3E NETWORK PROCESSOR	**I/O**	**UTOPIA**	**NOTE**	**C-3E NETWORK PROCESSOR**	**I/O**	**UTOPIA**	**NOTE**
FRXCTL0	Output	RxEnb*	Pullup or No Connection	FTXCTL0	Output	TxEnb*	Pullup or No Connection
FRXCTL1	Input	RxClav		FTXCTL1	Input	TxClav	
FRXCTL2	Input	RxSOC		FTXCTL2	Output	TxSOC	
FRXCTL6	Input	RxPrty		FTXCTL6	Output	TxPrty	

* Cell size must be 4Byte aligned. Both RxEnb and TxEnb are Active Low.

Table 21 Utopia1*, 2*, 3 PHY Mode, C-3e Network Processor to Fabric Interface Pin Mapping

RECEIVE SIGNALS				TRANSMIT SIGNALS			
C-3E NETWORK PROCESSOR	**I/O**	**UTOPIA**	**NOTE**	**C-3E NETWORK PROCESSOR**	**I/O**	**UTOPIA**	**NOTE**
FRXCTL0	Input	TxEnb*	Pullup	FTXCTL0	Input	RxEnb*	Pullup
FRXCTL1	Output	TxClav	No Connection	FTXCTL1	Output	RxClav	No Connection
FRXCTL2	Input	TxSOC		FTXCTL2	Output	RxSOC	
FRXCTL6	Input	TxPrty		FTXCTL6	Output	RxPrty	

* Cell size must be 4Byte aligned. Both TxEnb and RxEnb are Active Low.

When configuring two C-3e network processors back-to-back using the Fabric Port, set up the transmit side of each C-3e network processor in Utopia ATM mode and the receive side of each C-3e network processor in Utopia PHY mode.

BMU SDRAM Interface Signals

The BMU and SDRAM interface signals are described in Table 22.

The BMU is designed to support SDRAM devices with 12 address lines. All 139 data lines and all 12 address lines must be connected to the SDRAM in order for the BMU to be able to read and write external SDRAM properly.

Table 22 BMU SDRAM Interface Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
MD0 - MD129	AA27, AA25, AA24, AA23, AA21, AA20, Y27, Y26, Y25, Y23, Y22, Y21, Y20, W27, W26, W25, W23, W22, W21, W20, V27, V25, V24, V23, V21, V20, U27, U26, U25, U24, U23, U22, U21, U20, T27, T26, T25, T23, T22, T21, T20, R27, R26, R25, R24, R23, R22, R21, R20, P27, P25, P24, P23, P21, P20, N27, N26, N25, N24, N23, N22, N21, N20, M27, M26, M25, M23, M22, M21, M20, L27, L26, L25, L24, L23, L22, L21, L20, K27, K25, K24, K23, K21, K20, J27, J26, J25, J23, J22, J21, J20, H27, H26, H25, H23, H22, H21, H20, G27, G25, G24, G23, G21, G20, F27, F26, F25, F24, F23, F22, F21, F20, E27, E26, E25, E23, E22, E21, E20, D27, D25, D24, D23, D21, D20, C27, C26, C25, C23, C22	130	LVTTL	I_{PD}/O	Data Lines In
MDECC0 - MDECC8	A27, B20, B21, B23, B24, B25, B27, C20, C21	9	LVTTL	I_{PD}/O	Stored as data, ECC bits
MA0 - MA11	C19, B19, A19, F18, E18, D18, C18, A18, F17, E17, D17, C17	12	LVTTL	O_{PD}	Address Outputs: A0-A11 are sampled during the ACTIVE command and READ/WRITE to select one location out of the memory array in the respective bank. The address inputs also provide the op-code during a LOAD MODE REGISTER command
MBA0 - MBA1	F19, E19	2	LVTTL	O_{PD}	Bank Address Outputs: BA0 and BA1 define which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied
MCASX	A24	1	LVTTL	O_{PD}	Command Outputs: MRASX, MCASX, MWEX and MCSX define the command being entered. *NOTE: MCSX is considered part of the command code.*

Table 22 BMU SDRAM Interface Signals (continued)

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
MRASX	A23	1	LVTTL	O_{PD}	Command Outputs: MRASX, MCASX, MWEX and MCSX define the command being entered. MCSX is considered part of the command code.
MWEX	A22	1	LVTTL	O_{PD}	Command Outputs: MRASX, MCASX, MWEX and MCSX define the command being entered. MCSX is considered part of the command code.
MCSX	A25	1	LVTTL	O_{PD}	Chip Select: MCSX enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when MCSX is registered HIGH. MCSX provides the external bank selection on systems with multiple banks. MCSX is considered part of the command code.
MDQM MDQML	A20 A21	1 1	LVTTL LVTTL	O_{PD} O_{PD}	Input/Output Mask: MDQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when MDQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a high Z state (two-clock latency) when MDQM is sampled HIGH during the READ cycle. *NOTE: MDQML is an identical copy of MDQM used to drive the loading on SDRAM configurations with 2 DQM pins.*
MDCLK	A26	1	LVTTL	I_{PD}	Clock: MDCLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of the MDCLK. MDCLK also increments the internal burst counter and controls the output registers.
TOTAL PINS		**160**			

TLU SRAM Interface Signals

The TLU SRAM interface supports up to 128MBytes of SRAM at frequencies to 125MHz using LVTTL signaling levels (in single bank-mode only) and SRAM technologies up to 64Mbits. The TLU SRAM interface signals are described in Table 23.

Table 23 TLU SRAM Interface Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
TD0 - TD63	F3, F4, F5, F6, F7, F8, G1, G3, G4, G5, G7, G8, H1, H2, H3, H5, H6, H7, H8, J1, J2, J3, J5, J6, J7, J8, K1, K3, K4, K5, K7, K8, L1, L2, L3, L4, L5, L6, L7, L8, M1, M2, M3, M5, M6, M7, M8, N1, N2, N3, N4, N5, N6, N7, N8, P1, P3, P4, P5, P7, P8, R1, R2, R3	64	LVTTL	I_{PD}/O	TLU Memory Data
TA0 - TA21	U2, U3, U4, U5, U6, U7, U8, V1, V3, V4, V5, V7, V8, W1, W2, W3, W5, W6, W7, W8, Y1, Y2	22	LVTTL	O_{PD}	TLU Memory Address
TPAR0 - TPAR3	T1, T2, T3, T5	4	LVTTL	I_{PD}/O	Word Data Parity (i.e. TPAR0 across TD15:0)
TCE0X - TCE3X	T6, T7, T8, U1	4	LVTTL	O_{PD}	TLU Memory Chip Enable
TWE0X - TWE3X	R5, R6, R7, R8	4	LVTTL	O_{PD}	TLU Memory Write Enable
TCLKI	R4	1	LVTTL	I_{PD}	TLU Clock Input
TOTAL PINS		**99**			

QMU SRAM (Internal Mode) Interface Signals

The QMU signals are described in Table 24.

Table 24 QMU SRAM (Internal Mode) Interface Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
QA0 - QA16	D10, C10, A10, F11, E11, D11, C11, B11, A11, F12, E12, D12, C12, A12, F13, E13, D13	17	LVTTL	O	Address [16:0]
QD0 - QD31	F1, E1, D1, C1, B1, F2, E2, C2, A2, E3, D3, C3, B3, A3, D4, B4, A4, E5, D5, C5, B5, A5, E6, C6, A6, E7, D7, C7, B7, A7, E8, D8	32	LVTTL	I_{PD}/O	Data
QDQPAR	C8	1	LVTTL	I_{PD}	nc
QARDY	F10	1	LVTTL	I_{PD}	nc
QNQRDY	A9	1	LVTTL	I_{PD}	nc
QWEX	E10	1	LVTTL	O	Write Enable
QBCLKO	B8	1	LVTTL	O	nc
QBCLKI	A8	1	LVTTL	I_{PD}	nc
QACLKO	F9	1	LVTTL	O	nc
QACLKI	E9	1	LVTTL	I_{PD}	Input Clock
QDPL	C9	1	LVTTL	I_{PD}/O	Data Parity Low
QDPH	B9	1	LVTTL	I_{PD}/O	Data Parity High
TOTAL PINS		**59**			

QMU to Q-5/Q-3 (External Mode) Interface Signals

The QMU to Q-5/Q-3 signals are described in Table 25.

Table 25 QMU to Q-5/Q-3 (External Mode) Interface Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
QA0 - QA15	D10, C10, A10, F11, E11, D11, C11, B11, A11, F12, E12, D12, C12, A12, F13, E13	16	LVTTL	O	Enqueue Data [8:23]
QA16	D13	1	LVTTL	O	Enqueue Parity
QD0 - QD23	F1, E1, D1, C1, B1, F2, E2, C2, A2, E3, D3, C3, B3, A3, D4, B4, A4, E5, D5, C5, B5, A5, E6, C6	24	LVTTL	I_{PD}	Dequeue Data [0:23]
QD24 - QD31	A6, E7, D7, C7, B7, A7, E8, D8	8	LVTTL	I_{PD}	Enqueue Data [0:7]
QDQPAR	C8	1	LVTTL	I_{PD}	Dequeue Parity
QARDY	F10	1	LVTTL	I_{PD}	Dequeue Ack Ready
QNQRDY	A9	1	LVTTL	O	Enqueue Ready
QWEX	E10	1	LVTTL	O	Dequeue Ready
QBCLKO	B8	1	LVTTL	O	Output ClockB
QBCLKI	A8	1	LVTTL	I_{PD}	Input ClockB
QACLKO	F9	1	LVTTL	O	Output ClockA
QACLKI	E9	1	LVTTL	I_{PD}	Input ClockA
QDPL	C9	1	LVTTL	O	Dequeue Ack [0]
QDPH	B9	1	LVTTL	O	Dequeue Ack [1]
TOTAL PINS		**59**			

Power Supply Signals Power supply, and ground signals are described in Table 26.

Table 26 Power Supply Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	SIGNAL DESCRIPTION
VDD	H10, H12, H16, J11, J13, J15, J17, K10, K12, K14, K16, K18, L11, L13, L15, L17, M10, M12, M14, M16, M18, N11, N13, N15, N17, P10, P12, P14, P16, P18, R11, R13, R15, R17, T10, T12, T14, T16, T18, U11, U13, U15, U17, V10, V12, V14, V16, V18, W11, W13, W15, W17, Y10, Y12, Y14, Y16, Y18	57	P	Core Supply Voltage (1.1V Input)
VDD33	B18, B26, C24, D14, D22, G13, G15, G17, G19, G26, H14, H18, H24, J19, K22, L19, M24, N19, P26, R19, U19, V22, W19, W24, AA9, AA11, AA13, AA15, AA17, AA19, AA26, AD6, AD14, AD22, AE4, AE24, AF2, AF10, AF18, AF26	40	P	I/O Supply Voltage (3.3V Input)
GND	B6, B12, B16, B22, D2, D9, D19, D26, E4, E24, G6, G10, G12, G14, G16, G18, G22, H9, H11, H13, H15, H17, H19, J4, J10, J12, J14, J16, J18, J24, K2, K9, K11, K13, K15, K17, K19, K26, L10, L12, L14, L16, L18, M9, M11, M13, M15, M17, M19, N10, N12, N14, N16, N18, P6, P9, P11, P13, P15, P17, P19, P22, R10, R12, R14, R16, R18, T4, T9, T11, T13, T15, T17, T19, T24, U10, U12, U14, U16, U18, V2, V9, V11, V13, V15, V17, V19, V26, W10, W12, W14, W16, W18, Y4, Y9, Y11, Y13, Y15, Y17, Y19, Y24, AA6, AA10, AA12, AA14, AA16, AA18, AA22, AC4, AC24, AD2, AD9, AD19, AD26, AF6, AF14, AF22	117	P	Ground
VDDT	B2, B10, C4, D6, G2, G9, G11, H4, J9, K6, L9, M4, N9, P2, R9, U9, V6, W4, W9, AA2	20	P	TLU and QMU I/O supply (3.3V)
TOTAL PINS		**234**		

Test Signals Test signals are described in Table 27.

Table 27 Miscellaneous Test Signals For JTAG, Scan, and Internal Test Routines

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
JTCK	B17	1	LVTTL	I_{PD}	Test Clock
JTMS	A17	1	LVTTL	I_{PD}	Test Mode Select. High selects modes as defined in the IEEE 1149.1 JTAG specification.
JTRSTX	A16	1	LVTTL	I_{PD}	Test Reset (low active)
JTDI	C16	1	LVTTL	I_{PD}	Test Data In
JTDO	C14	1	LVTTL	O	Test Data Out
JHIGHZ	B15	1	LVTTL	I_{PD}	Turns off all output drivers when High
JCLKBYP	A15	1	LVTTL	I_{PD}	1X or 2X Clock Mode Select. Low selects 1X, High selects 2X.
JSE	D15	1	LVTTL	I_{PD}	Scan Enable. High enables scan test.
JS00-JS05	C13, B13, A13, B14, A14, C15	6	LVTTL	O	Scan Out Pins
TOTAL PINS		**14**			

During JTAG, SCLK and SCLKX must remain as differential inputs.

Signals Grouped by Pin Number

The C-3e NP signals are listed by pin number in Table 28.

Table 28 Signals Listed by Pin Number

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A 1-27							
A1	Not present	A9	QNQRDY	A17	JTMS	A25	MCSX
A2	QD8	A10	QA2	A18	MA7	A26	MDCLK
A3	QD13	A11	QA8	A19	MA2	A27	MDECC0
A4	QD16	A12	QA13	A20	MDQM		
A5	QD21	A13	JS02	A21	MDQML		
A6	QD24	A14	JS04	A22	MWEX		
A7	QD29	A15	JCLKBYP	A23	MRASX		
A8	QBCLKI	A16	JTRSTX	A24	MCASX		
B 1-27							
B1	QD4	B9	QDPH	B17	JTCK	B25	MDECC5
B2	VDDT	B10	VDDT	B18	VDD33	B26	VDD33
B3	QD12	B11	QA7	B19	MA1	B27	MDECC6
B4	QD15	B12	GND	B20	MDECC1		
B5	QD20	B13	JS01	B21	MDECC2		
B6	GND	B14	JS03	B22	GND		
B7	QD28	B15	JHIGHZ	B23	MDECC3		
B8	QBCLKO	B16	GND	B24	MDECC4		
C 1-27							
C1	QD3	C9	QDPL	C17	MA11	C25	MD127
C2	QD7	C10	QA1	C18	MA6	C26	MD126
C3	QD11	C11	QA6	C19	MA0	C27	MD125
C4	VDDT	C12	QA12	C20	MDECC7		
C5	QD19	C13	JS00	C21	MDECC8		
C6	QD23	C14	JTDO	C22	MD129		

Table 28 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
C7	QD27	C15	JS05	C23	MD128		
C8	QDQPAR	C16	JTDI	C24	VDD33		
D 1-27							
D1	QD2	D9	GND	D17	MA10	D25	MD120
D2	GND	D10	QA0	D18	MA5	D26	GND
D3	QD10	D11	QA5	D19	GND	D27	MD119
D4	QD14	D12	QA11	D20	MD124		
D5	QD18	D13	QA16	D21	MD123		
D6	VDDT	D14	VDD33	D22	VDD33		
D7	QD26	D15	JSE	D23	MD122		
D8	QD31	D16	CPREF	D24	MD121		
E 1-27							
E1	QD1	E9	QACLKI	E17	MA9	E25	MD114
E2	QD6	E10	QWEX	E18	MA4	E26	MD113
E3	QD9	E11	QA4	E19	MBA1	E27	MD112
E4	GND	E12	QA10	E20	MD118		
E5	QD17	E13	QA15	E21	MD117		
E6	QD22	E14	CCLK3	E22	MD116		
E7	QD25	E15	CCLK2	E23	MD115		
E8	QD30	E16	CCLK1	E24	GND		
F 1-27							
F1	QD0	F9	QACLKO	F17	MA8	F25	MD106
F2	QD5	F10	QARDY	F18	MA3	F26	MD105
F3	TD0	F11	QA3	F19	MBA0	F27	MD104
F4	TD1	F12	QA9	F20	MD111		
F5	TD2	F13	QA14	F21	MD110		
F6	TD3	F14	SCLK	F22	MD109		

Table 28 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
F7	TD4	F15	SCLKX	F23	MD108		
F8	TD5	F16	CCLK0	F24	MD107		
G 1-27							
G1	TD6	G9	VDDT	G17	VDD33	G25	MD99
G2	VDDT	G10	GND	G18	GND	G26	VDD33
G3	TD7	G11	VDDT	G19	VDD33	G27	MD98
G4	TD8	G12	GND	G20	MD103		
G5	TD9	G13	VDD33	G21	MD102		
G6	GND	G14	GND	G22	GND		
G7	TD10	G15	VDD33	G23	MD101		
G8	TD11	G16	GND	G24	MD100		
H 1-27							
H1	TD12	H9	GND	H17	GND	H25	MD93
H2	TD13	H10	VDD	H18	VDD33	H26	MD92
H3	TD14	H11	GND	H19	GND	H27	MD91
H4	VDDT	H12	VDD	H20	MD97		
H5	TD15	H13	GND	H21	MD96		
H6	TD16	H14	VDD33	H22	MD95		
H7	TD17	H15	GND	H23	MD94		
H8	TD18	H16	VDD	H24	VDD33		
J 1-27							
J1	TD19	J9	VDDT	J17	VDD	J25	MD86
J2	TD20	J10	GND	J18	GND	J26	MD85
J3	TD21	J11	VDD	J19	VDD33	J27	MD84
J4	GND	J12	GND	J20	MD90		
J5	TD22	J13	VDD	J21	MD89		
J6	TD23	J14	GND	J22	MD88		

Table 28 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
J7	TD24	J15	VDD	J23	MD87		
J8	TD25	J16	GND	J24	GND		
K 1-27							
K1	TD26	K9	GND	K17	GND	K25	MD79
K2	GND	K10	VDD	K18	VDD	K26	GND
K3	TD27	K11	GND	K19	GND	K27	MD78
K4	TD28	K12	VDD	K20	MD83		
K5	TD29	K13	GND	K21	MD82		
K6	VDDT	K14	VDD	K22	VDD33		
K7	TD30	K15	GND	K23	MD81		
K8	TD31	K16	VDD	K24	MD80		
L 1-27							
L1	TD32	L9	VDDT	L17	VDD	L25	MD72
L2	TD33	L10	GND	L18	GND	L26	MD71
L3	TD34	L11	VDD	L19	VDD33	L27	MD70
L4	TD35	L12	GND	L20	MD77		
L5	TD36	L13	VDD	L21	MD76		
L6	TD37	L14	GND	L22	MD75		
L7	TD38	L15	VDD	L23	MD74		
L8	TD39	L16	GND	L24	MD73		
M 1-27							
M1	TD40	M9	GND	M17	GND	M25	MD65
M2	TD41	M10	VDD	M18	VDD	M26	MD64
M3	TD42	M11	GND	M19	GND	M27	MD63
M4	VDDT	M12	VDD	M20	MD69		
M5	TD43	M13	GND	M21	MD68		
M6	TD44	M14	VDD	M22	MD67		
M7	TD45	M15	GND	M23	MD66		

Table 28 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
M8	TD46	M16	VDD	M24	VDD33		
N 1-27							
N1	TD47	N9	VDDT	N17	VDD	N25	MD57
N2	TD48	N10	GND	N18	GND	N26	MD56
N3	TD49	N11	VDD	N19	VDD33	N27	MD55
N4	TD50	N12	GND	N20	MD62		
N5	TD51	N13	VDD	N21	MD61		
N6	TD52	N14	GND	N22	MD60		
N7	TD53	N15	VDD	N23	MD59		
N8	TD54	N16	GND	N24	MD58		
P 1-27							
P1	TD55	P9	GND	P17	GND	P25	MD50
P2	VDDT	P10	VDD	P18	VDD	P26	VDD33
P3	TD56	P11	GND	P19	GND	P27	MD49
P4	TD57	P12	VDD	P20	MD54		
P5	TD58	P13	GND	P21	MD53		
P6	GND	P14	VDD	P22	GND		
P7	TD59	P15	GND	P23	MD52		
P8	TD60	P16	VDD	P24	MD51		
R 1-27							
R1	TD61	R9	VDDT	R17	VDD	R25	MD43
R2	TD62	R10	GND	R18	GND	R26	MD42
R3	TD63	R11	VDD	R19	VDD33	R27	MD41
R4	TCLKI	R12	GND	R20	MD48		
R5	TWE0X	R13	VDD	R21	MD47		
R6	TWE1X	R14	GND	R22	MD46		
R7	TWE2X	R15	VDD	R23	MD45		

Table 28 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
R8	TWE3X	R16	GND	R24	MD44		
T 1-27							
T1	TPAR0	T9	GND	T17	GND	T25	MD36
T2	TPAR1	T10	VDD	T18	VDD	T26	MD35
T3	TPAR2	T11	GND	T19	GND	T27	MD34
T4	GND	T12	VDD	T20	MD40		
T5	TPAR3	T13	GND	T21	MD39		
T6	TCE0X	T14	VDD	T22	MD38		
T7	TCE1X	T15	GND	T23	MD37		
T8	TCE2X	T16	VDD	T24	GND		
U 1-27							
U1	TCE3X	U9	VDDT	U17	VDD	U25	MD28
U2	TA0	U10	GND	U18	GND	U26	MD27
U3	TA1	U11	VDD	U19	VDD33	U27	MD26
U4	TA2	U12	GND	U20	MD33		
U5	TA3	U13	VDD	U21	MD32		
U6	TA4	U14	GND	U22	MD31		
U7	TA5	U15	VDD	U23	MD30		
U8	TA6	U16	GND	U24	MD29		
V 1-27							
V1	TA7	V9	GND	V17	GND	V25	MD21
V2	GND	V10	VDD	V18	VDD	V26	GND
V3	TA8	V11	GND	V19	GND	V27	MD20
V4	TA9	V12	VDD	V20	MD25		
V5	TA10	V13	GND	V21	MD24		
V6	VDDT	V14	VDD	V22	VDD33		
V7	TA11	V15	GND	V23	MD23		
V8	TA12	V16	VDD	V24	MD22		

Table 28 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
W 1-27							
W1	TA13	W9	VDDT	W17	VDD	W25	MD15
W2	TA14	W10	GND	W18	GND	W26	MD14
W3	TA15	W11	VDD	W19	VDD33	W27	MD13
W4	VDDT	W12	GND	W20	MD19		
W5	TA16	W13	VDD	W21	MD18		
W6	TA17	W14	GND	W22	MD17		
W7	TA18	W15	VDD	W23	MD16		
W8	TA19	W16	GND	W24	VDD33		
Y 1-27							
Y1	TA20	Y9	GND	Y17	GND	Y25	MD8
Y2	TA21	Y10	VDD	Y18	VDD	Y26	MD7
Y3	XPUHOT	Y11	GND	Y19	GND	Y27	MD6
Y4	GND	Y12	VDD	Y20	MD12		
Y5	SPDO	Y13	GND	Y21	MD11		
Y6	SPDI	Y14	VDD	Y22	MD10		
Y7	SPLD	Y15	GND	Y23	MD9		
Y8	SPCK	Y16	VDD	Y24	GND		
AA 1-27							
AA1	SICL	AA9	VDD33	AA17	VDD33	AA25	MD1
AA2	VDDT	AA10	GND	AA18	GND	AA26	VDD33
AA3	PAD30	AA11	VDD33	AA19	VDD33	AA27	MD0
AA4	SIDA	AA12	GND	AA20	MD5		
AA5	PIDSEL	AA13	VDD33	AA21	MD4		
AA6	GND	AA14	GND	AA22	GND		
AA7	PFRAMEX	AA15	VDD33	AA23	MD3		
AA8	PGNTX	AA16	GND	AA24	MD2		

Table 28 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
AB 1-27							
AB1	PTRDYX	AB9	PAD0	AB17	CP7_6	AB25	CP2_1
AB2	PCBEX0	AB10	FRXCTL6	AB18	CP7_2	AB26	CP1_2
AB3	PAD31	AB11	FIN14	AB19	CP6_4	AB27	CP0_5
AB4	PAD26	AB12	FIN8	AB20	CP5_6		
AB5	PAD20	AB13	FIN2	AB21	CP5_0		
AB6	PAD16	AB14	FTXCTL1	AB22	CP4_1		
AB7	PAD10	AB15	FOUT13	AB23	CP3_4		
AB8	PAD4	AB16	FOUT7	AB24	CP2_5		
AC 1-27							
AC1	PINTA	AC9	PAD1	AC17	CP7_5	AC25	CP2_0
AC2	PIRDYX	AC10	FRXCTL2	AC18	CP7_1	AC26	CP1_1
AC3	PPERRX	AC11	FIN13	AC19	CP6_3	AC27	CP0_4
AC4	GND	AC12	FIN7	AC20	CP5_5		
AC5	PAD21	AC13	FIN1	AC21	CP4_6		
AC6	PAD17	AC14	FTXCTL0	AC22	CP4_0		
AC7	PAD11	AC15	FOUT12	AC23	CP3_3		
AC8	PAD5	AC16	FOUT6	AC24	GND		
AD 1-27							
AD1	PREQX	AD9	GND	AD17	CP7_4	AD25	CP1_6
AD2	GND	AD10	FRXCTL1	AD18	CP7_0	AD26	GND
AD3	PSERRX	AD11	FIN12	AD19	GND	AD27	CP0_3
AD4	PAD27	AD12	FIN6	AD20	CP5_4		
AD5	PAD22	AD13	FIN0	AD21	CP4_5		
AD6	VDD33	AD14	VDD33	AD22	VDD33		
AD7	PAD12	AD15	FOUT11	AD23	CP3_2		
AD8	PAD6	AD16	FOUT5	AD24	CP2_4		

Table 28 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
AE 1-27							
AE1	PRSTX	AE9	PAD2	AE17	CP7_3	AE25	CP1_5
AE2	PSTOPX	AE10	FRXCTL0	AE18	CP6_6	AE26	CP1_0
AE3	PCBEX3	AE11	FIN11	AE19	CP6_2	AE27	CP0_2
AE4	VDD33	AE12	FIN5	AE20	CP5_3		
AE5	PAD23	AE13	FTXCLK	AE21	CP4_4		
AE6	PAD18	AE14	FOUT15	AE22	CP3_6		
AE7	PAD13	AE15	FOUT10	AE23	CP3_1		
AE8	PAD7	AE16	FOUT4	AE24	VDD33		
AF 1-27							
AF1	PCLK	AF9	PAD3	AF17	FOUT1	AF25	CP1_4
AF2	VDD33	AF10	VDD33	AF18	VDD33	AF26	VDD33
AF3	PCBEX2	AF11	FIN10	AF19	CP6_1	AF27	CP0_1
AF4	PAD28	AF12	FIN4	AF20	CP5_2		
AF5	PAD24	AF13	FTXCTL6	AF21	CP4_3		
AF6	GND	AF14	GND	AF22	GND		
AF7	PAD14	AF15	FOUT9	AF23	CP3_0		
AF8	PAD8	AF16	FOUT3	AF24	CP2_3		
AG 1-27							
AG1	PPAR	AG9	FRXCLK	AG17	FOUT0	AG25	CP1_3
AG2	PDEVSELX	AG10	FIN15	AG18	CP6_5	AG26	CP0_6
AG3	PCBEX1	AG11	FIN9	AG19	CP6_0	AG27	CP0_0
AG4	PAD29	AG12	FIN3	AG20	CP5_1		
AG5	PAD25	AG13	FTXCTL2	AG21	CP4_2		
AG6	PAD19	AG14	FOUT14	AG22	CP3_5		
AG7	PAD15	AG15	FOUT8	AG23	CP2_6		
AG8	PAD9	AG16	FOUT2	AG24	CP2_2		

JTAG Support

The C-3e NP contains JTAG test logic compliant with the IEEE 1149.1 specification. All required public instructions are implemented, as well as some optional instructions. This section contains information regarding the pinout, instructions, identification codes, and boundary scan cell types.

Pinout

The C-3e NP uses the standard JTAG pins including the optional test reset pin. Table 27 describes the pins and their functions.

JTAG Data Registers

The C-3e NP contains the standard internal registers as specified in IEEE 1149.1. These registers are described in Table 29.

Table 29 JTAG Internal Register Descriptions

REGISTER NAME	REGISTER LENGTH	DESCRIPTION
Bypass	1	Standard JTAG bypass register
Boundary	1549	Boundary Scan Register
Device Identification	32	Standard JTAG IDCODE Register

Boundary Scan Restriction

SCLK/SCLKX inputs must not toggle when exercising the boundary scan function for JTAG.

Boundary Scan Cell Types

The C-3e NP boundary scan register contains only two cell types. All input cells are *observe only* cells of type BC_4. All enable and output cells are standard cells of type BC_1. In IEEE 1149.1-1990 specification, the BC_4 cell is shown in Figure 7 and the BC_1 cell is shown in Figure 8.

Figure 7 Observe-Only Cell

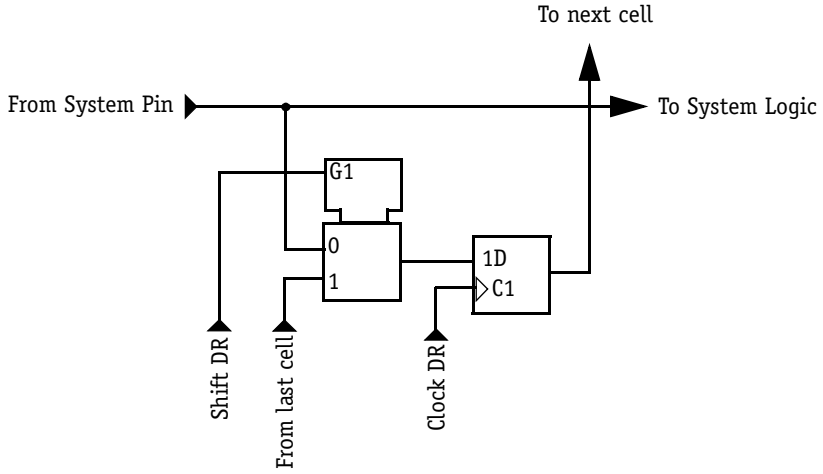
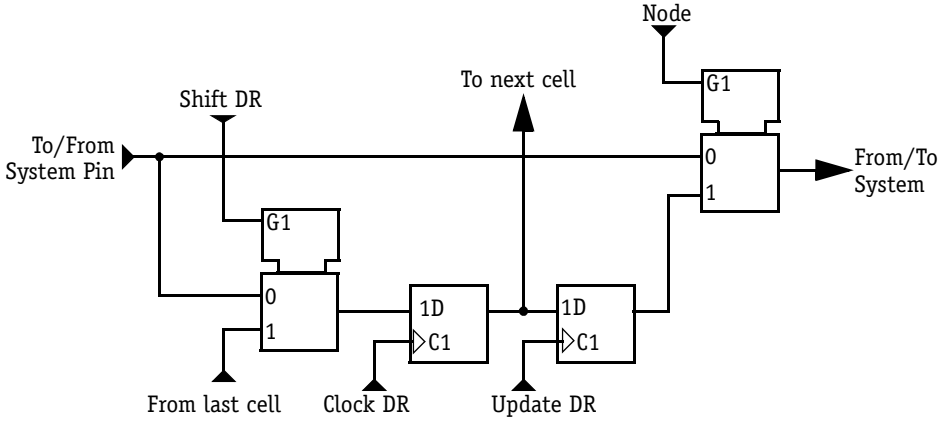


Figure 8 Cell Design That Can Be Used for Both Input and Output Pins



IDcode Register

The C-3e NP implements a standard 32bit JTAG identification register. Table 30 lists the value of the code for full identification and its sub-components.

Table 30 JTAG Identification Code and Its Sub-components

FIELD NAME	WIDTH	BIT POSITIONS	BINARY VALUE
Version	4	31-28	0000
Part Number	16	27-12	0000_0000_0010_0001
Manufacturer Identity	11	11-1	001_1001_0110
LSB	1	0	1

The concatenated 32bit value is hexidecimal 0002132d.

JTAG Instruction Register

The C-3e NP contains a 4bit instruction register. Table 31 lists the instructions that are supported.

Table 31 Instruction Register Instructions

INSTRUCTION MNEMONIC	SELECTED REGISTER	INSTRUCTION OPCODE
Extest	Boundary Scan	0000
Idcode	Identification Register	0001
Sample/Preload	Boundary Scan	0010
Highz	Bypass Register	0011
Clamp	Bypass Register	0100
Bypass	Bypass Register	0101
Reserved*	Bypass Register	0110
Reserved*	Bypass Register	0111
Bypass	Bypass Register	1000
Bypass	Bypass Register	1001
Bypass	Bypass Register	1010
Bypass	Bypass Register	1011
Bypass	Bypass Register	1100
Bypass	Bypass Register	1101

Table 31 Instruction Register Instructions (continued)

INSTRUCTION MNEMONIC	SELECTED REGISTER	INSTRUCTION OPCODE
Bypass	Bypass Register	1110
Bypass	Bypass Register	1111

* There are two reserved instructions intended for Motorola Corporation's internal use. These should not be programmed by users.

Boundary Scan Description Language

In order to simplify board test, Motorola Corporation has provided a boundary scan description language (BSDL) file (c3e.bsdl) in the Motorola web site that describes the complete set of instructions, boundary scan order, and identification code value in an industry standard format.

http://www.motorola.com/networkprocessors

Chapter 3

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 32 lists the absolute maximum ratings for the C-3e network processor. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under "Recommended Operating Conditions" (Table 33) is possible.

Exposure to conditions beyond Table 32 can:

- Reduce device reliability
- Result in premature device failure, even with no immediate sign of failure

Prolonged exposure to conditions at or near the absolute maximum ratings could also result in reduced useful life and reliability of the C-3e NP.

Table 32 C-3e Network Processor Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNIT
$V_{DD33/VDDT}$ Supply Voltage (3.3V input)*	-0.5	+5	V
V_{DD} Supply Voltage (1.1V input)*	-0.5	+2.2	V
Voltage on any pin	-0.5	V_{DD33} + 0.5	V
Static Discharge Voltage	2000/500		V
Storage Temperature	-40	+125	°C
Absolute Maximum Junction Temperature	-40	+125	°C

* Voltages are relative to Ground

Recommended Operating Conditions

The recommended operating conditions describe an environment the C-3e NP network processor is expected to encounter during normal operation. Table 33 delineates the recommended operating parameters for the C-3e NP.

Table 33 C-3e Network Processor Recommended Operating Conditions

PARAMETER	MIN	NOMINAL	MAX	UNIT
V_{DD33} Supply Voltage	3.135	3.3	3.465	V
V_{DDT} Supply Voltage	3.135	3.3	3.465	V
V_{DD} Supply Voltage	1.04	1.2	1.16	V
I_{DD33} - V_{DD33} Supply Current			0.6	A
I_{DD} - V_{DD} Supply Current			5.0	A
T_j Junction Temperature	-40		125	°C

DC Characteristics

The DC electrical characteristics define the input operating conditions for proper operation and the output responses to applied DC signals and switch characteristics over specified voltage and temperature ranges. The DC electrical characteristics are specified within the *recommended operating conditions* including operating temperature and power supply range as stated in this data sheet. Table 34 outlines the C-3e NP DC characteristics.

Table 34 C-3e Network Processor DC Characteristics

PARAMETER*	MIN	MAX	UNIT	NOTES
LVTTL Input High Voltage	2.0	V_{DD33}+.3	V	
LVTTL Input Low Voltage	-0.3	0.8	V	
LVTTL Output High Voltage	2.4		V	@I_{OH} = -2mA
LVTTL Output Low Voltage		0.4	V	@I_{OL} = +2mA
LVTTL Input Current	-100	+100	µA	V_{IN} = 0V or V_{DD33}
LVPECL Input High Voltage	V_{DD33} -1.165	V_{DD33}+.3V	V	
LVPECL Input Low Voltage	-0.3	V_{DD33} -1.475	V	
LVPECL Output High Voltage	V_{DD33} -1.025	V_{DD33} -0.60	V	Load = 50ohm to V_{DD33} - 2V
LVPECL Output Low Voltage	V_{DD33} -2.20	V_{DD33} -1.620	V	Load = 50ohm to V_{DD33} - 2V
LVPECL Input Current	-100	+100	µA	
CPREF	V_{DD33} -1.38	V_{DD33} -1.26	V	Single-ended LVPECL reference

* All voltages are relative to Ground unless otherwise indicated.

Each control input pin has a capacitance associated with it. The capacitance at the control input is due to the package and the input circuitry connected to the pin. Capacitance is based on these conditions: T_A = 25°C; V_{DD33} = 3.3V; f = 1MHz. Table 35 provides capacitance data.

Table 35 C-3e Network Processor Capacitance Data

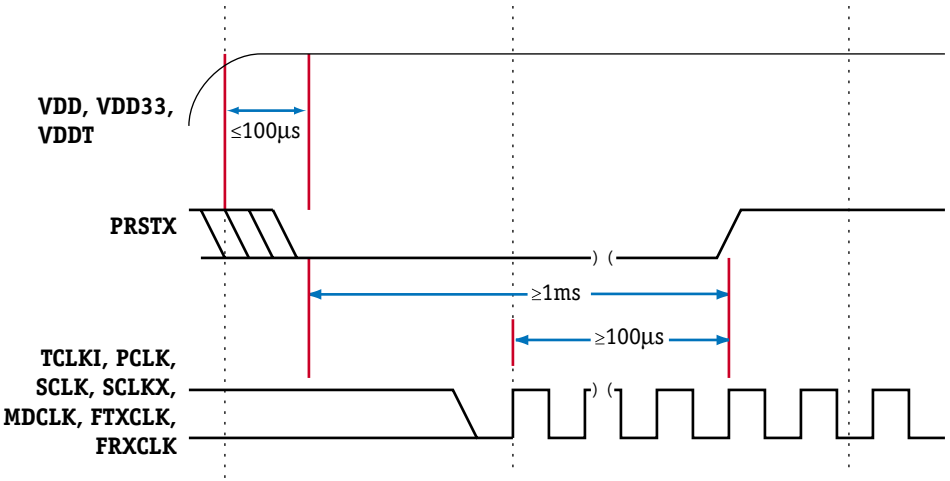
PARAMETER	TYPICAL	UNIT
All Pins	5	pF

Power Sequencing

It is intended that the VDD33/VDDT and VDD rails are sequenced to their final value together for most applications. VDD33 and VDDT must be above VDD at all times. VDD must be brought to its final value within 100ms of sequencing on VDD33 and VDDT.

It is also required that SCLK, SCLKX, TCLKI, PCLK, MDCLK, FTXCLK, and FRXCLK be running or begin running during power sequencing to propagate reset inside the C-3e NP. Figure 9 indicates the relationship between the clocks and PRSTX. There is no requirement that the asserting and deasserting edges of PRSTX be synchronous to the clocks. Reset must be asserted within 100µs of power initiation. Typically, reset is held low during power initiation.

Figure 9 Bringup Clock Timing Diagram



Power and Thermal Characteristics

Table 36 provides the derived power and thermal characteristics for the production version of the C-3e NP.

Table 36 C-3e Network Processor Power and Thermal Characteristics

PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Power Dissipation, P_D	2.5	5.5	7.5	W	180MHz core clock See Note below
Maximum Junction Temperature, T_J			125	°C	See Note below
Thermal Resistance, junction to case, θ_{JC}		<0.1		°C/W	See Note below
Thermal Resistance, junction to printed circuit board, θ_{JB}		5.5		°C/W	See Note below

Table 36 *note: Power dissipation values assume the following conditions:*

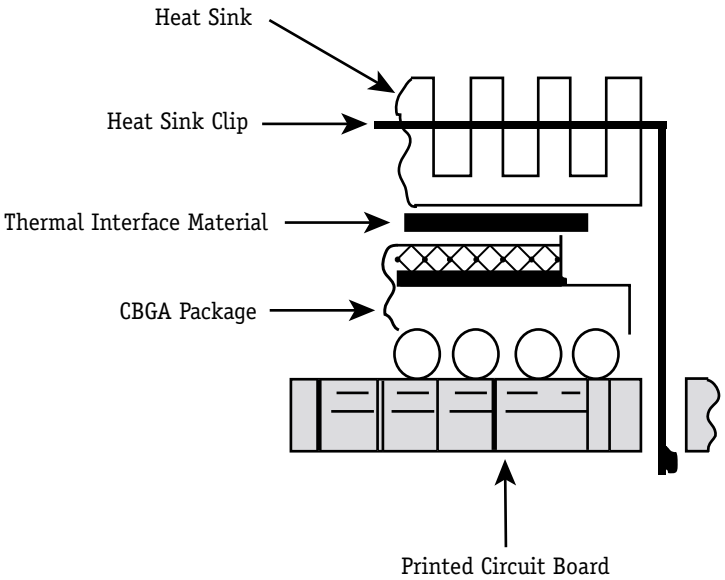
- *BMU memory operating at 125MHz*
- *TLU memory operating at 125MHz*
- *QMU operating at 150MHz*
- *VDD = 1.1V, VDD33/VDDT = 3.3V, TJ at approximately 50°C for typical values. VDD and VDD33/VDDT are 5% higher for maximum values*
- *"Minimum" PD based on idle condition (clocks running and no programs executing)*
- *"Typical" PD based on test application that implements Fast Ethernet forwarding actively running on all CPs*
- *"Maximum" PD based on maximum consumption for any high-bandwidth communications application executing on all CPs, FP, and XP*

Thermal Management Information

This section provides thermal management information for the ceramic ball grid array (CBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (refer to Figure 10); however, due to the potential

large mass of the heat sink, attachment through the printed circuit board is suggested. If a spring clip is used, the spring force should not exceed 5.5 pounds.

Figure 10 Package Cross Section View with Serveral Heat Sink Options



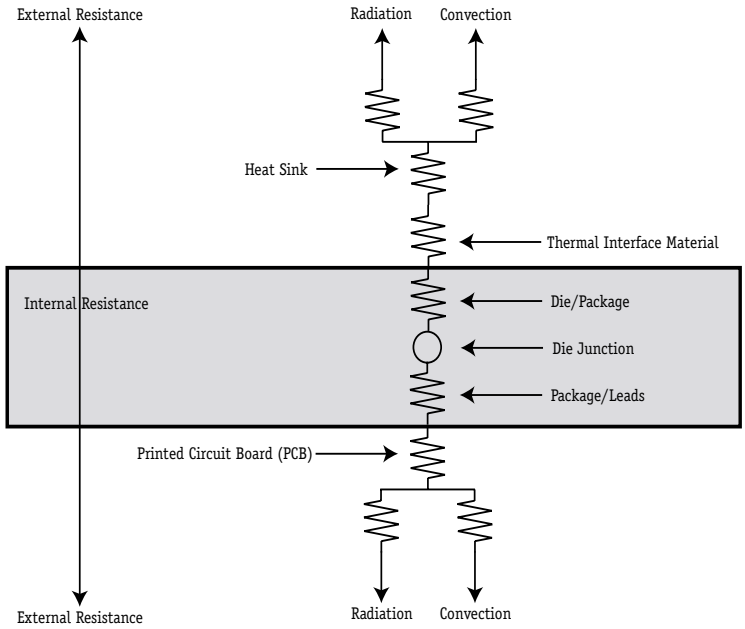
Internal Package Conduction Resistance

For the exposed-die packaging technology the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 11 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 11 Package with Heat Sink Mounted to the Printed Circuit Board



Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by convection.

Because the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

T_j is the die-junction temperature

T_a is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

θ_{jc} is the junction-to-case thermal resistance

θ_{int} is the adhesive or interface material thermal resistance

θ_{sa} is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 36. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1.5°C/W. For example, assuming a T_a of 30°C, a T_r of 5°C, a CBGA package $\theta_{jc} = 0.1$, and a maximum power consumption (P_d) of 7.5 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.5°C/W + \theta_{sa}) \times 7.5\ W$

For this example, a θ_{sa} value of 10.4°C/W or less is required to maintain the die junction temperature below the maximum value of Table 36.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

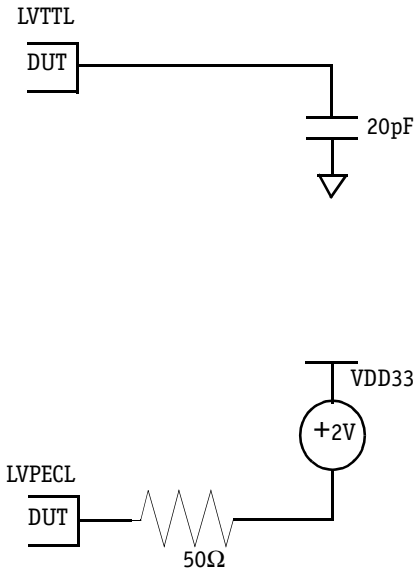
Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection,and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as system-level designs.

AC Timing Specifications

AC timing specifications consist of input requirements and output responses. The input requirements include setup and hold times, pulse widths, and high and low times. The output responses include delays from clock to signal. The AC timing specifications are defined separately for each interface to the C-3e NP.

See Figure 12. *Output timing specifications for LVTTL pins are given with a 20pF load on the output. Other loads can be simulated with the IBIS model available from Motorola. The LVPECL driver is specified into a 50Ω load terminated to a (VDD33 - 2V) reference.*

Figure 12 Test Loading Conditions



Clock Timing Specifications

The system clock timing is shown in Figure 13 and described in Table 37.

Figure 13 System Clock Timing Diagram

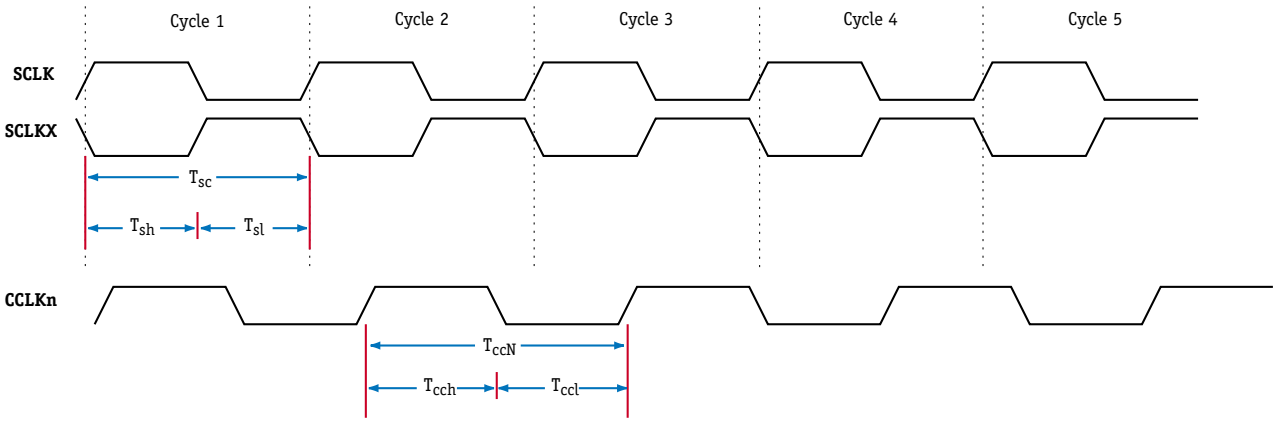


Table 37 System Clock Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	COMMENT
Tsc	System Cycle Time	3.76			ns	180MHz core clock
Tsh	Sys Clk High Pulse	45		55		Duty cycle*
Tsl	Sys Clk Low Pulse	45		55		Duty cycle*
Tcc0	CCLK0 Cycle Time		6.43		ns	†
Tcc1	CCLK1 Cycle Time		6.43		ns	†
Tcc2	CCLK2 Cycle Time		6.43		ns	†
Tcc3	CCLK3 Cycle Time		6.43		ns	†
Tcch	CCLKm High Time	40%		60%		% cycle pulse is high
Tccl	CCLKm Low Time	40%		60%		% cycle pulse is low

* Pulse duty cycle measured at crossing voltage of SCLK/SCLKX

† The frequencies specified for CCLK0 - CCLK3 allow full flexibility for the C-3e NP. It is also possible to use one or more CCLK*n* inputs for other frequencies; contact your Motorola representative for more information.

CP Timing Specifications

This section describes the timing for the following CP interfaces:

- DS1/DS3
- 10/100 Ethernet
- Gigabit Ethernet
- OC-3
- OC-12

DS1/DS3 Timing Specifications

The DS1/DS3 interface timing is shown in Figure 14 and described in Table 38.

Figure 14 DS1/DS3 Ethernet Timing Diagram

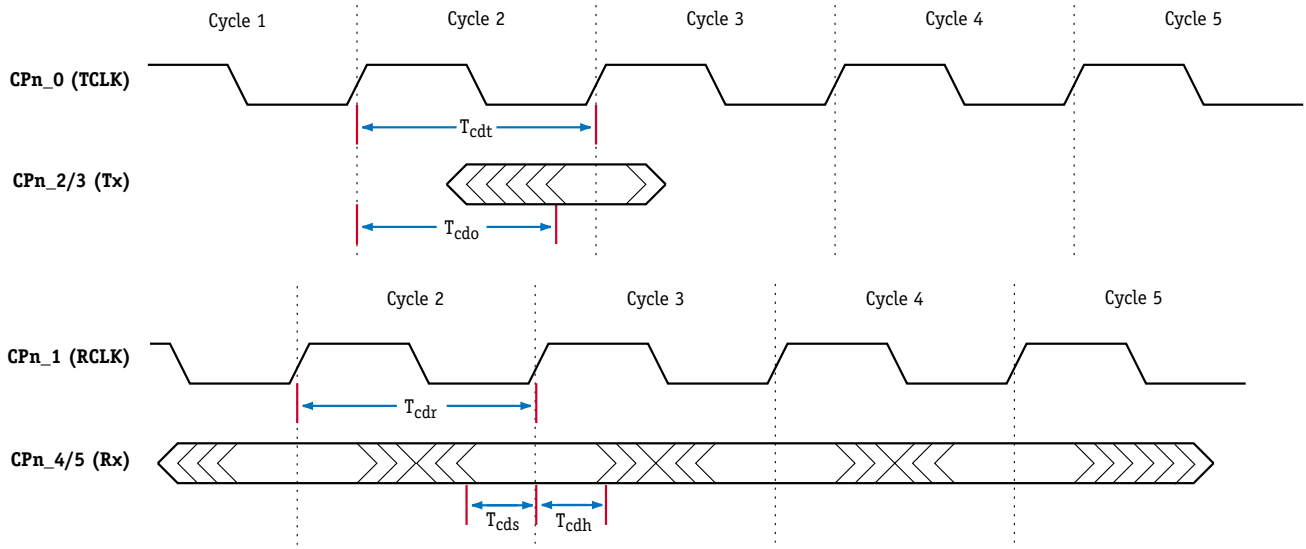


Table 38 DS1/DS3 Ethernet Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tcdt	DS1/DS3 Transmit Cycle Time		647/22.4		ns
Tcdo	DS1/DS3 Output Time	3.0/3.0		400/15.0	ns
Tcdr	DS1/DS3 Receive Cycle Time		647/22.4		ns

Table 38 DS1/DS3 Ethernet Timing Description (continued)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tcds	DS1/DS3 Setup Time	2.0			ns
Tcdh	DS1/DS3 Hold Time	0			ns

10/100 Ethernet Timing Specifications

The 10/100 Ethernet interface timing is shown in Figure 15 and described in Table 39.

Figure 15 10/100 Ethernet Timing Diagram

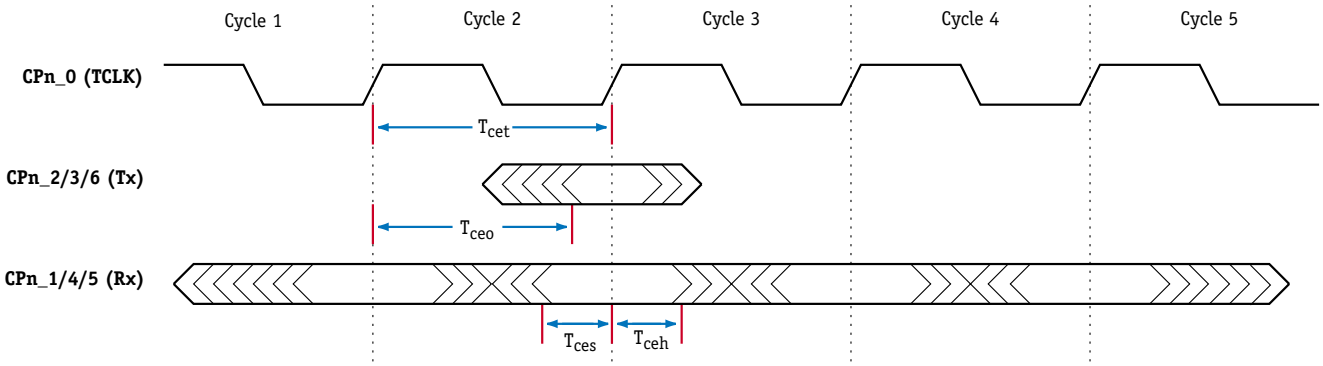


Table 39 10/100 Ethernet Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tcet	Transmit Cycle Time*		20		ns
Tceo	Output Time	3.0		15.0	ns
Tces	Setup Time	2.0			ns
Tceh	Hold Time	0			ns

* STD/Fast Ethernet

Gigabit GMII Ethernet, TBI and MII Interface Timing Specifications

The Gigabit GMII Ethernet interface timing is shown in Figure 16 and described in Table 40. The TBI interface timing is shown in Figure 16 and described in Table 41.

Figure 16 Gigabit Ethernet and TBI Interface Timing Diagram

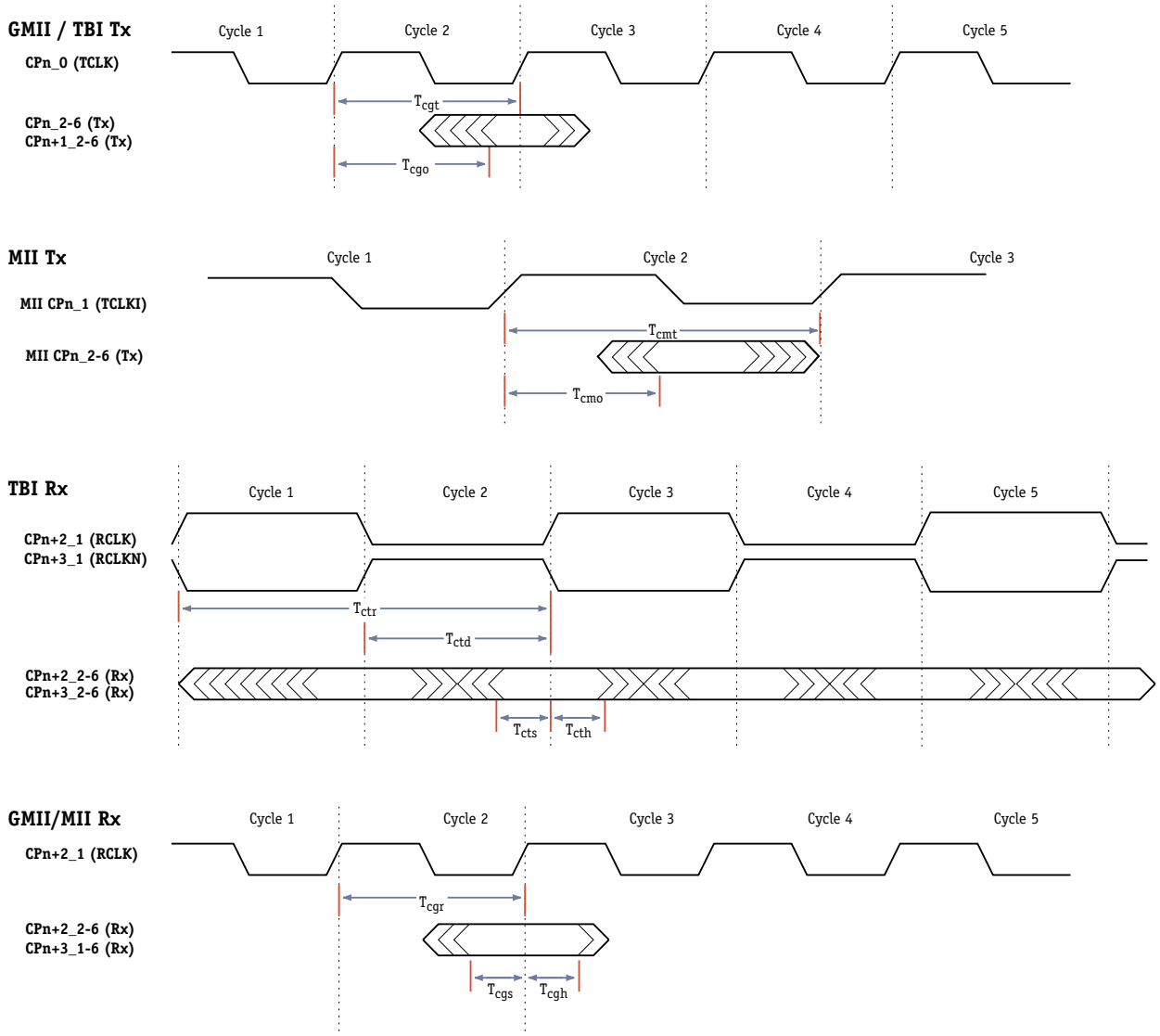


Table 40 Gigabit GMII/MII Ethernet Interface Timing Description

SYMBOL GIGABIT	PARAMETER	MIN	TYP	MAX	UNIT	COMMENT
Tcgt	Transmit Cycle Time, GMII		8.0		ns	
Tcgo	Output Time, GMII	3.0		6.0	ns	
Tcgr	Receive Cycle Time		8.0		ns	
Tcgs	Setup Time	2.0			ns	
Tcgh	Hold Time	0.0			ns	
Tcmt	Transmit Cycle Time, MII		40/400		ns	100BaseT/10BaseT
Tcmo	Output Time, MII	2		12	ns	

Table 41 Gigabit TBI Interface Timing Description

SYMBOL TBI	PARAMETER	MIN	TYP	MAX	TOL	UNIT
Tctt	Transmit Cycle Time		8.0			ns
Tcto	Output Time	3.0		6.0*		ns
Tctr	Receive Cycle Time		16.0			ns
Tctd	Rclk/Rclkn Deviation				1.0	ns
Tcts	Setup Time	2.0				ns
Tcth	Hold Time	0.0				ns

* For Fibre Channel applications this value is 7.0ns for a transmit cycle time of 9.4ns.

OC-3 Timing Specifications

The OC-3 interface timing is shown in Figure 17 and described in Table 42.

Figure 17 OC-3 Timing Diagram

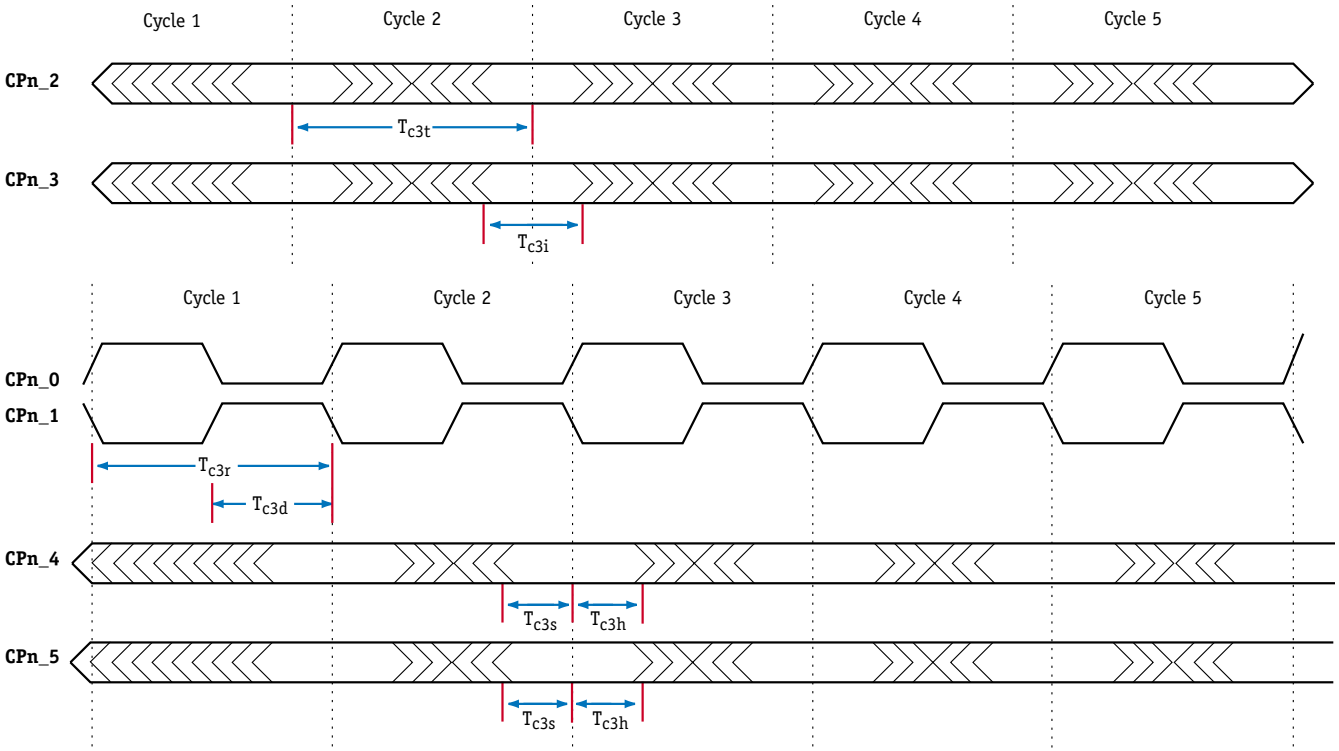


Table 42 OC-3 Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tc3t	OC-3 Transmit Cycle Time		6.43		ns
Tc3i	OC-3 Pulse Width	2.0			ns
Tc3r	OC-3 Receive Cycle Time*	6.0			ns
Tc3d	OC-3 Clock Duty Cycle	40		60	%
Tc3s	OC-3 Setup Time	2.0			ns
Tc3h	OC-3 Hold Time	0.0			ns

* 155.52MHz

OC-12 Timing Specifications

The OC-12 interface timing is shown in Figure 18 and described in Table 43.

Figure 18 OC-12 Timing Diagram

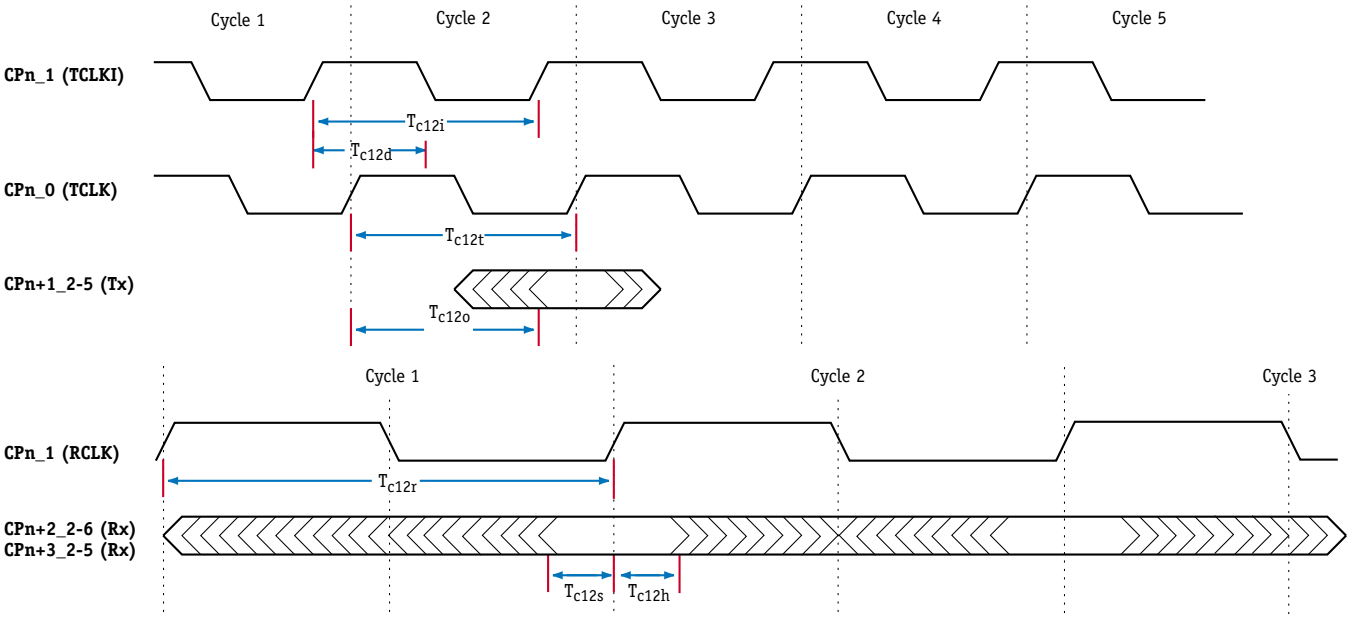


Table 43 OC-12 Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tc12i	OC-12 Transmit Cycle Time*		12.86		ns
Tc12d	OC-3 Clock Duty Cycle	40		60	%
Tc12t	OC-12 Transmit Cycle Time†		12.86		ns
Tc12o	OC-12 Output Time‡	3.0		10.0	ns
Tc12r	OC-12 Receive Cycle Time	12.0	12.86		ns
Tc12s	OC-12 Setup Time	2.0			ns
Tc12h	OC-12 Hold Time	0.0			ns

* Input from PHY
† Output from C-3e NP
‡ Aligned to TCLK

Executive Processor Timing Specifications

The XP timing specifications include:

- PCI Timing Specifications
- MDIO Serial Interface Timing Specifications
- Low Speed Serial Interface Timing Specifications
- PROM Interface Timing Specifications

PCI Timing Specifications

The PCI timing is shown in Figure 19 and described in Table 44.

Figure 19 PCI Timing Diagram

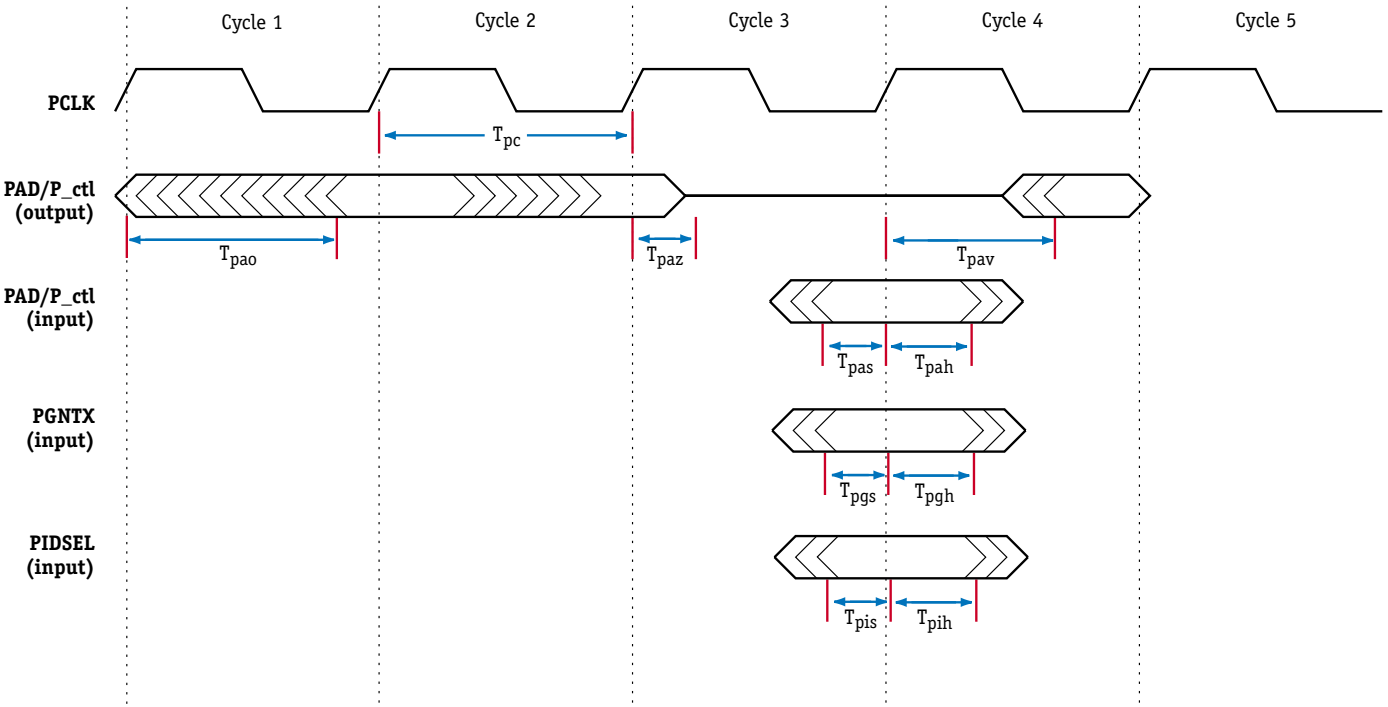


Table 44 PCI Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tpc	PCI Cycle Time*	15.0			ns
Tpas	PAD/P_ctl† Setup	3.0			ns
Tpah	PAD/P_ctl Hold	0.0			ns
Tpao	PAD/P_ctl Output	2.0		6.0	ns
Tpaz	PAD/P_ctl Clk to Tri‡	2.0		6.0	ns
Tpav	PAD/P_ctl Clk to Driven‡	2.0		6.0	ns
Tpgs	PGNTX Setup	5.1			ns
Tpgh	PGNTX Hold	0.0			ns
Tpis	PIDSEL Setup	3.0			ns
Tpih	PIDSEL Hold	0.0			ns
	PRSTX**				ns
	PINTA**				ns

* 66MHz PCI

† P_ctl includes all PCI control parameters including: PPAR, PFRAMEX, PTRDYX, PIRDYX, PSTOPX, PDEVSELX, PPERRX, PSERRX

‡ Not fully tested, values based on design/characterization.

** Asynchronous

MDIO Serial Interface Timing Specifications

The MDIO serial interface timing is shown in Figure 20 and described in Table 45.

Figure 20 MDIO Serial Interface Timing Diagram

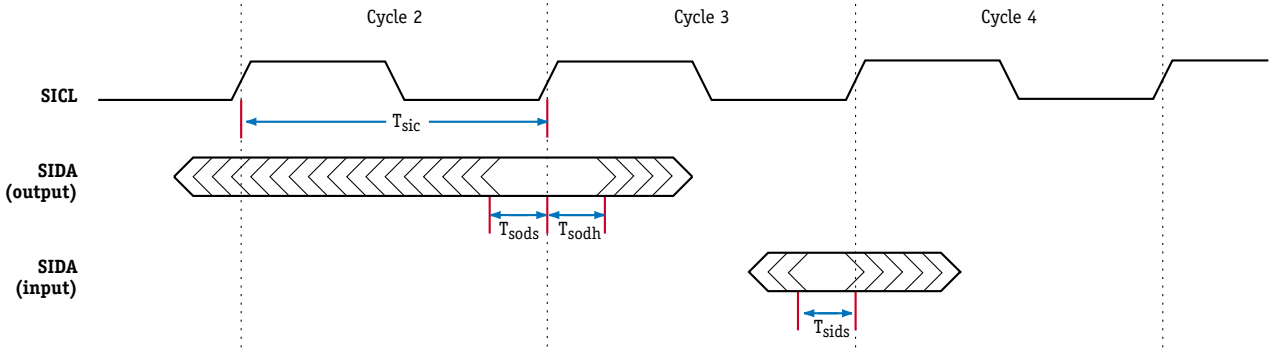


Table 45 MDIO Serial Interface Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tsic	SICL Cycle Time	40			ns
Tsids	SIDA Input Setup	10			ns
Tsidh	SIDA Input Hold	0.0			ns
Tsods	SIDA Output Setup	10			ns
Tsodh	SIDA Output Hold	10			ns

Low Speed Serial Interface Timing Specifications

The low speed serial interface timing is shown in Figure 21 and described in Table 46.

Figure 21 Low Speed Serial Interface Timing Diagram

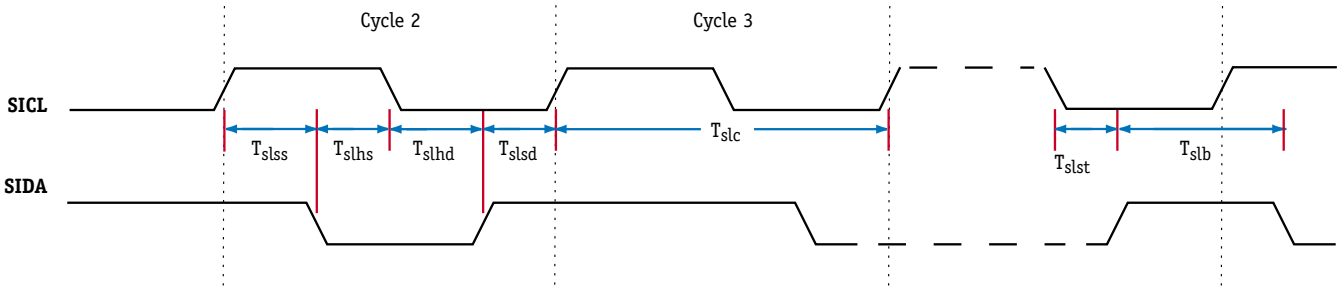


Table 46 Low Speed Serial Interface Timing Description

SYMBOL	PARAMETER	MIN	MAX	UNIT
Tslc	SICL Cycle Time	2500		ns
Tslss	Set-up Time for Repeated START Condition	600		ns
Tslhs	Hold Time START Condition	600		ns
Tslsd	Data Set-up Time	250		ns
Tslhd	Data Hold Time	0.0		ns
Tslst	Set-up Time for STOP Condition	600		ns
Tslb	Bus Free Time Between a STOP and START Condition	1250		ns
Cmax	Capacitive load for each line of the bus		400	pF

PROM Interface Timing Specifications

The PROM interface timing is shown in Figure 22 and described in Table 47.

Figure 22 PROM Interface Timing Diagram

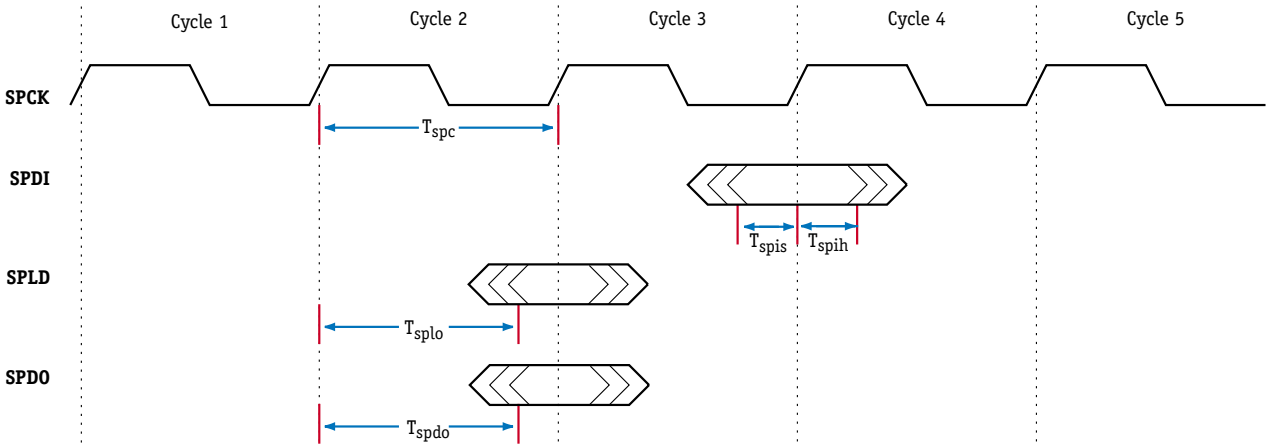


Table 47 PROM Interface Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tspc	SPCK Cycle Time	40.0			ns
Tspis	SPDI Setup	10.0			ns
Tspih	SPDI Hold	0.0			ns
Tsplo	SPLD Output	Tsc		Tsc + 3.0	ns
Tspdo	SPDO Output	Tsc		Tsc + 3.0	ns

Fabric Processor Timing Specifications

The FP timing specifications are shown in Figure 23 and described in Table 48.

Figure 23 Fabric Processor Timing Diagram

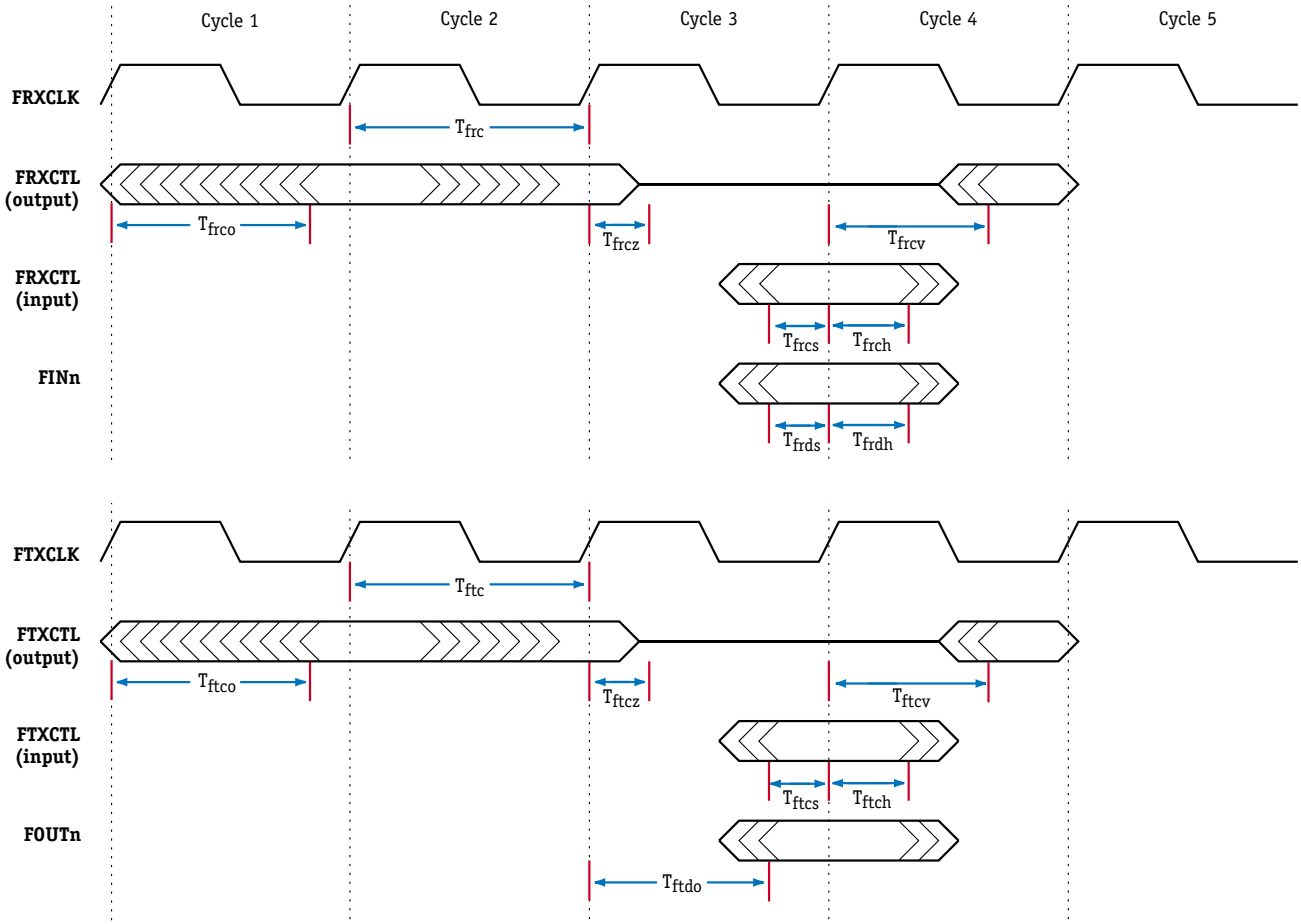


Table 48 Fabric Processor Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	COMMENT
Tfrc	FRX Cycle Time	8.0			ns	
Tfrcs	FRXCTL Setup	4.0 1.5			ns	Utopia2 Mode All other modes
Tfrch	FRXCTL Hold	0.0			ns	
Tfrco	FRXCTL Output	1.0		4.0	ns	
Tfrcz	FRXCTL Clk to Tri*	1.0		4.0	ns	
Tfrcv	FRXCTL Clk to Driven*	1.0		4.0	ns	
Tfrds	FIN Setup	4.0 1.5			ns	Utopia2 Mode All other modes
Tfrdh	FIN Hold	0.0			ns	
Tftc	FTX Cycle Time	8.0			ns	
Tftcs	FTXCTL Setup	4.0 1.5			ns	Utopia2 Mode All other modes
Tftch	FTXCTL Hold	0.0			ns	
Tftco	FTXCTL Output	1.0		4.0	ns	
Tftcz	FTXCTL Clk to Tri*	1.0		4.0	ns	
Tftcv	FTXCTL Tri to Driven*	1.0		4.0	ns	
Tftdo	FOUT Output	1.0		4.0	ns	

* Not fully tested, values based on design/characterization.

BMU Timing Specifications

The BMU timing specifications are shown in Figure 24 and described in Table 49.

The BMU synchronous DRAM interface is PC100-compliant and designed to work with industry standard SDRAM components with 12 or fewer address lines. The information below is intended to provide the output, setup, and hold data required to design this interface without duplicating the transaction waveform diagrams in SDRAM data sheets.

Figure 24 BMU Timing Diagram

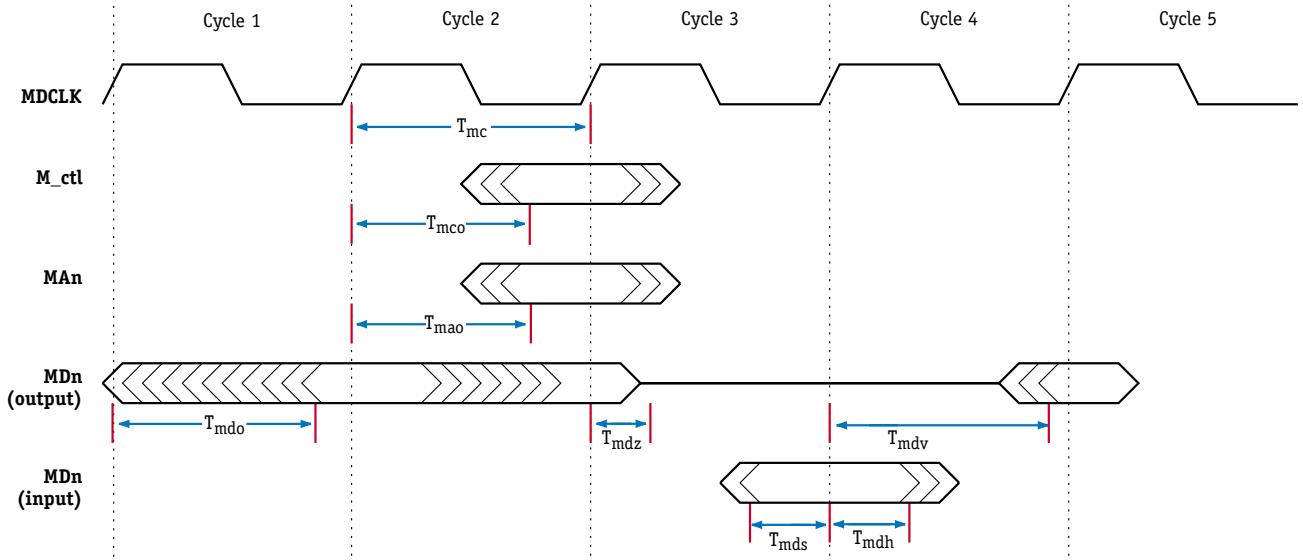


Table 49 BMU Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tmc	BMU Cycle Time	8.0			ns
Tmco	BMU Ctrl Output	0.8		3.9	ns
Tmao	BMU Addr Output	0.8		3.9	ns
Tmds	BMU Data Setup	0.5			ns
Tmdh	BMU Data Hold	1.1			ns
Tmdo	BMU Data Output	0.8		4.5	ns
Tmdz	BMU Data Clk to Tri*	0.8		4.5	ns
Tmdv	BMU Data Clk to Driven*	0.8		4.5	ns

* Not fully tested, values based on design/characterization.

Table 50 Signal Groups in BMU Timing Diagrams

SIGNAL GROUP	INCLUDED SIGNALS
Control (M_ctl)	MBA0, MBA1, MCASX, MRASX, MWEX, MCSX, MDQM, MDQML
Address (MAn)	MA0 - MA11
Data (MDn)	MD0 - MD129, MDECC0 - MDECC8

TLU Timing Specifications

The TLU timing specifications are shown in Figure 25 and described in Table 51.

Figure 25 TLU Timing Diagram

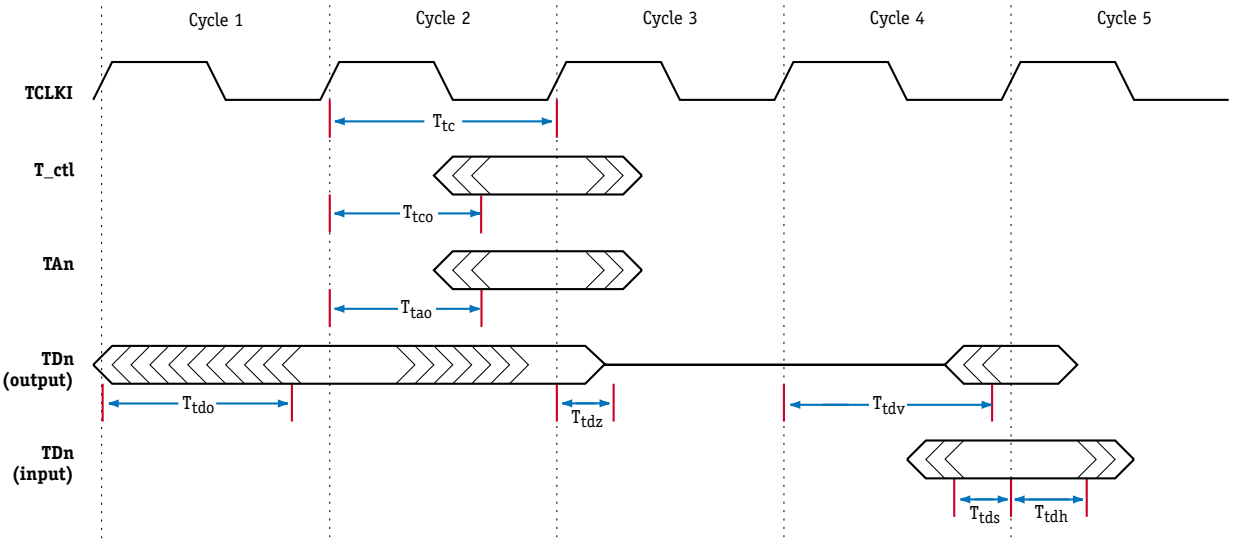


Table 51 TLU Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Ttc	TLU Cycle Time	8.0			ns
Ttco	TLU Ctrl Output	0.8		3.9	ns
Ttao	TLU Addr Output	0.8		3.9	ns
Ttds	TLU Data Setup	1.0			ns
Ttdh	TLU Data Hold	1.2			ns
Ttdo	TLU Data Output	0.8		4.2	ns
Ttdz	TLU Data Clk to Tri*	0.8		4.2	ns
Ttdv	TLU Data Clk to Driven*	0.8		4.2	ns

* Not fully tested, values based on design/characterization.

Table 52 Signal Groups in TLU Timing Diagrams

SIGNAL GROUP	INCLUDED SIGNALS
Control (T_ctl)	TCE0X - TCE3X, TWE0X - TWE3X
Address (TAn)	TA0 - TA21
Data (TDn)	TD0 - TD63, TPAR0-3

QMU SRAM (Internal Mode) Timing Specifications

The QMU SRAM (Internal Mode) timing specifications are shown in Figure 26 and described in Table 53.

Figure 26 QMU SRAM (Internal Mode) Timing Diagram

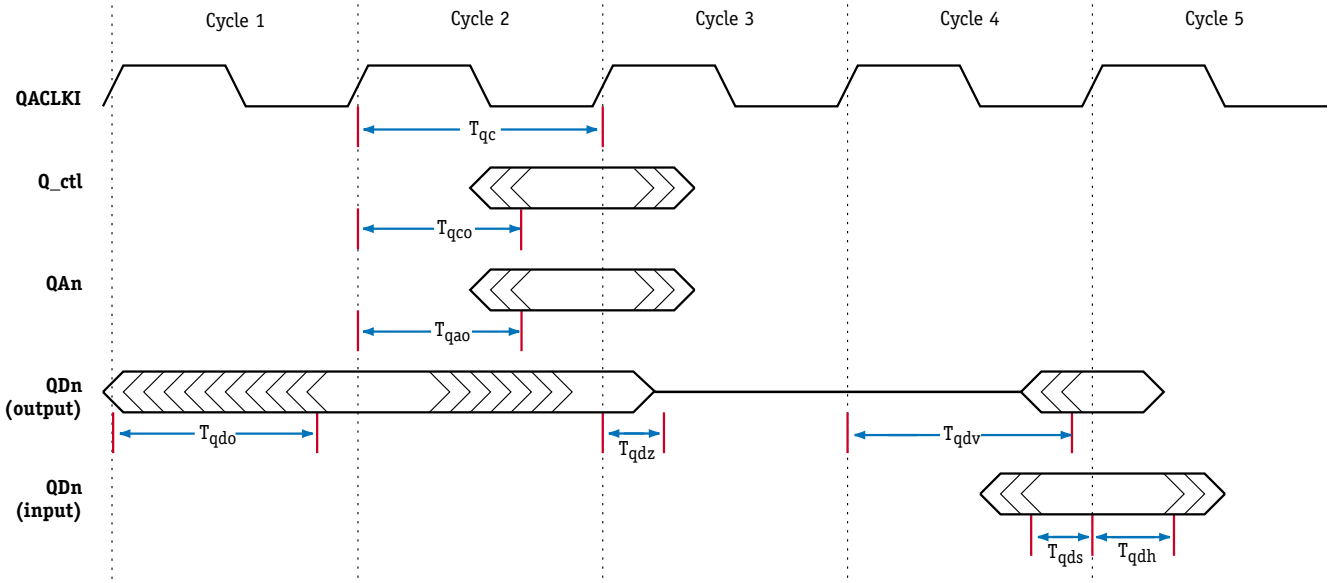


Table 53 QMU SRAM (Internal Mode) Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	COMMENT
Tqc	QMU Cycle Time	6.7			ns	
Tqco	QMU Ctrl Output	0.8		4.4	ns	Loading is 50Ω transmission line.
Tqao	QMU Addr Output	0.8		4.4	ns	Loading is 50Ω transmission line.
Tqds	QMU Data Setup	0.8			ns	
Tqdh	QMU Data Hold	0.8			ns	
Tqdo	QMU Data Output	0.9		4.4	ns	Loading is 50Ω transmission line.

Table 53 QMU SRAM (Internal Mode) Timing Description (continued)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	COMMENT
Tqdz	QMU Data Clk to Tri*	0.9		4.4	ns	
Tqdv	QMU Data Clk to Driven*	0.9		4.4	ns	

* Not fully tested, values based on design/characterization.

Table 54 Signal Groups in QMU SRAM (Internal Mode) Timing Diagrams

SIGNAL GROUP	INCLUDED SIGNALS
Control (Q_ctl)	QWEX
Address (QAn)	QA0-QA16
Data (QDn)	QD0-QD31, QDPL, QDPH

QMU to Q-5/Q-3 (External Mode) Timing Specifications

The QMU to Q-5/Q-3 (External Mode) timing specifications are shown in Figure 27 and described in Table 55.

Figure 27 QMU to Q-5/Q-3 (External Mode) Timing Diagram

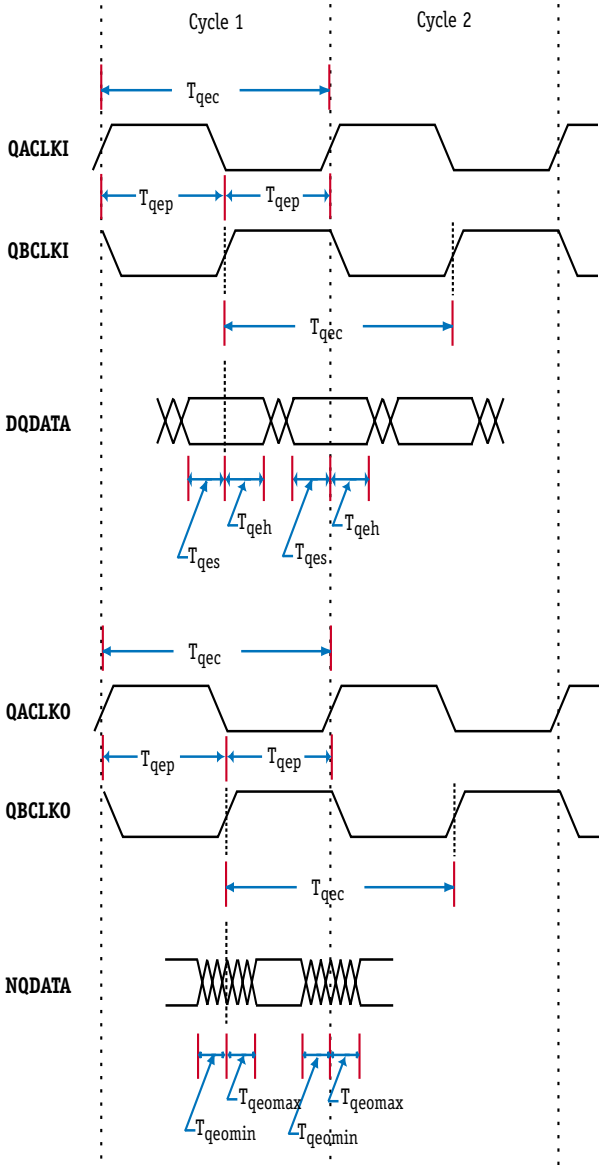


Table 55 QMU to Q-5/Q-3 (External Mode) Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	COMMENT
Tqec	QMU External Cycle Time	10.0			ns	QACLKO/QBCLKO derived from QACLKI/QBCLKI
Tqep	QMU CLKA-CLKB delta between rising edges	4.8			ns	
Tqes	QMU Input Data Setup	0.6			ns	
Tqeh	QMU Input Data Hold	0.8			ns	
Tqeo	QMU Data Output	-.85		1.3	ns	Determines valid time for data from each clock rising edge

Table 56 Signal Groups in QMU to Q-5/Q-3 (External Mode) Timimg Diagrams

SIGNAL GROUP	INCLUDED SIGNALS
Input Clocks (QnCLKI)	QACLKI, QBCLKI
Output Clocks (QnCLKO)	QACLKO, QBCLKO
Input Data (DQDATA)	QD0-23, QARDY, QDPL, QDPH, QNQRDY, QDQPAR
Output Data (NQDATA)	QA0-16, QWEX, QD24-31

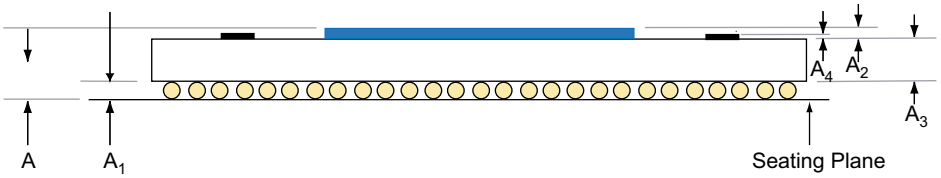
Chapter 4

MECHANICAL SPECIFICATIONS

Package Views

The C-3e network processor is an 728 pin (27 pins x 27 pins) Ball Grid Array (BGA) package as shown in the following illustrations. Table 57 defines the package measurements.

Figure 28 C-3e Network Processor BGA Package Side View



HiTCE: Green ceramic is thermally matched to FR4 circuit board.

Figure 29 C-3e Network Processor BGA Package (Bottom View)

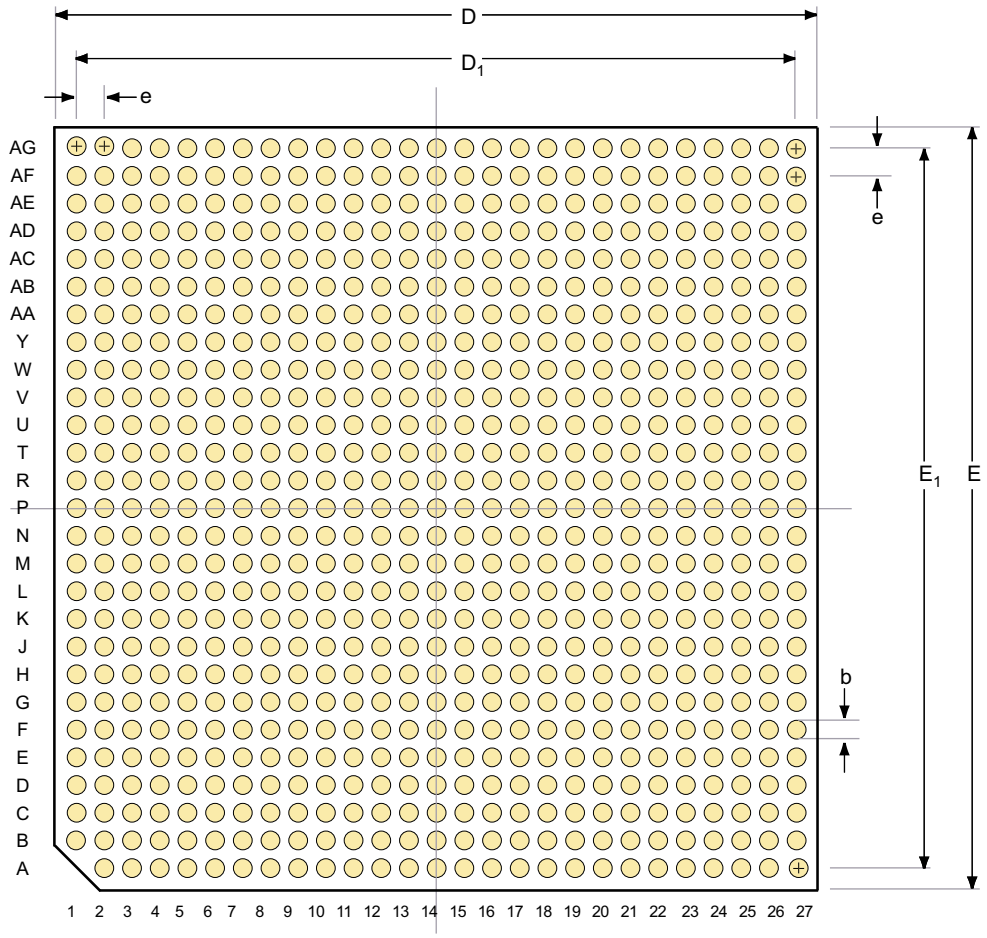
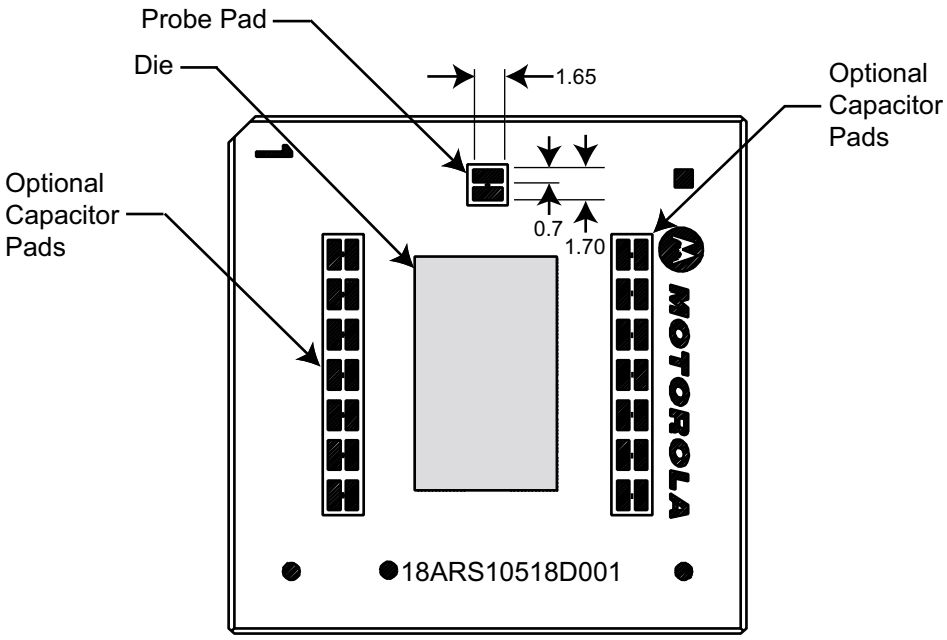


Figure 30 C-3e Network Processor BGA (Top View)



Package Measurements

Table 57 defines the C-3e NP package measurements, providing nominal, minimum, and maximum sizes where appropriate.

Table 57 Package Measurements (Reference Figure 28, Figure 29 and Figure 30 for Symbols)

SYMBOL	DEFINITION	NOM. (MM)	MIN. (MM)	MAX. (MM)
A	Overall	3.11	2.83	3.39
A_1	Ball height	0.70	0.6	0.8
A_2	C4 and Die	0.86		
A_3	Body thickness	1.55	1.41	1.69
A_4	Capacitor pad			0.6
D	Body size	29.00	28.80	29.20
D_1	Ball footprint (X)	26.00		
E	Body size	29.00	28.80	29.20
E_1	Ball footprint (Y)	26.00		
e	Ball pitch	1.00		
b	Ball diameter	0.70		

At Motorola's discretion up to fourteen (14) capacitors may or may not be attached on the top of the package.

Marking Codes

Table 58 explains the marking on the C-3e NP.

Table 58 C-3e Network Processor Marking Codes

MARKING (EXPLANATION OF CODES)	
Top	Logo/Part#/Date Code
Bottom	N/A
Pin 1 Marking	Chamfered Corner

Reflow

Typical Reflow Profile for the C-3e Switch Module comprises:

1 Follow the guidelines recommended by your solder paste supplier.

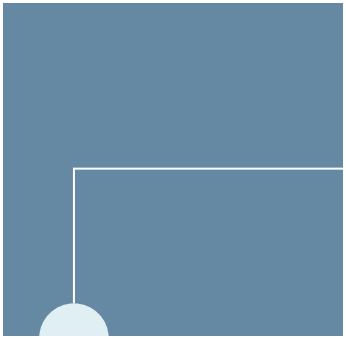
Flux requirements must be met for best solderability.

2 The temperature profile should be carefully characterized to ensure uniform temperature across the board and package.

Solder ball voiding may be affected by ramp rates and dwell times below and above liquids.

3 A nitrogen atmosphere is not required, but will make the process more robust. It can make a difference for marginally solderable PC board pads.

4 Full convection forced air furnaces work best, but IR, Convection/IR, or vapor phase can be used.



INDEX

E

F

G

I

J

L

M

O

P

Q

R

S

T

U

X

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