8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89960 Series

MB89965/P965A/F969A/ MB89PV960

■ DESCRIPTION

The MB89960 series is a single-chip microcontroller that utilizes the F²MC-8L core for low voltage and high speed performance. The microcontroller contains a range of peripheral functions including timers, a serial interface, I²C interface, A/D converter, and external interrupts. The internal I²C interface complies with the SM bus standard and supports an SM bus battery controller.

■ FEATURES

- **Range of package options**
- QFP and MQFP packages (0.8 mm pitch)
- LQFP package (0.5 mm and 0.65 mm pitch)

- **High speed operation at low voltage**
  Minimum instruction execution time = 0.4 μs (for a 10 MHz oscillation)

- **F²MC-8L CPU core**
  Instruction set optimized for controller applications
- Multiplication and division instructions
- 16-bit arithmetic operations
- Bit test branch instructions
- Bit manipulation instructions, etc.

- **Dual-clock control system**
- Main clock : 10 MHz max.
   (Four speed settings available, oscillation halts in sub-clock mode)
- Sub-clock : 32.768 kHz (Operation clock for sub-clock mode)

- **Four channels**
- 8/16-bit timer/counter (8-bit × 2 channels or 16-bit × 1 channel)
- 21-bit timebase timer
- Clock prescaler (15-bit)

- **Serial I/O**
  Selectable transfer format (MSB-first or LSB-first) supports communications with a wide range of devices.
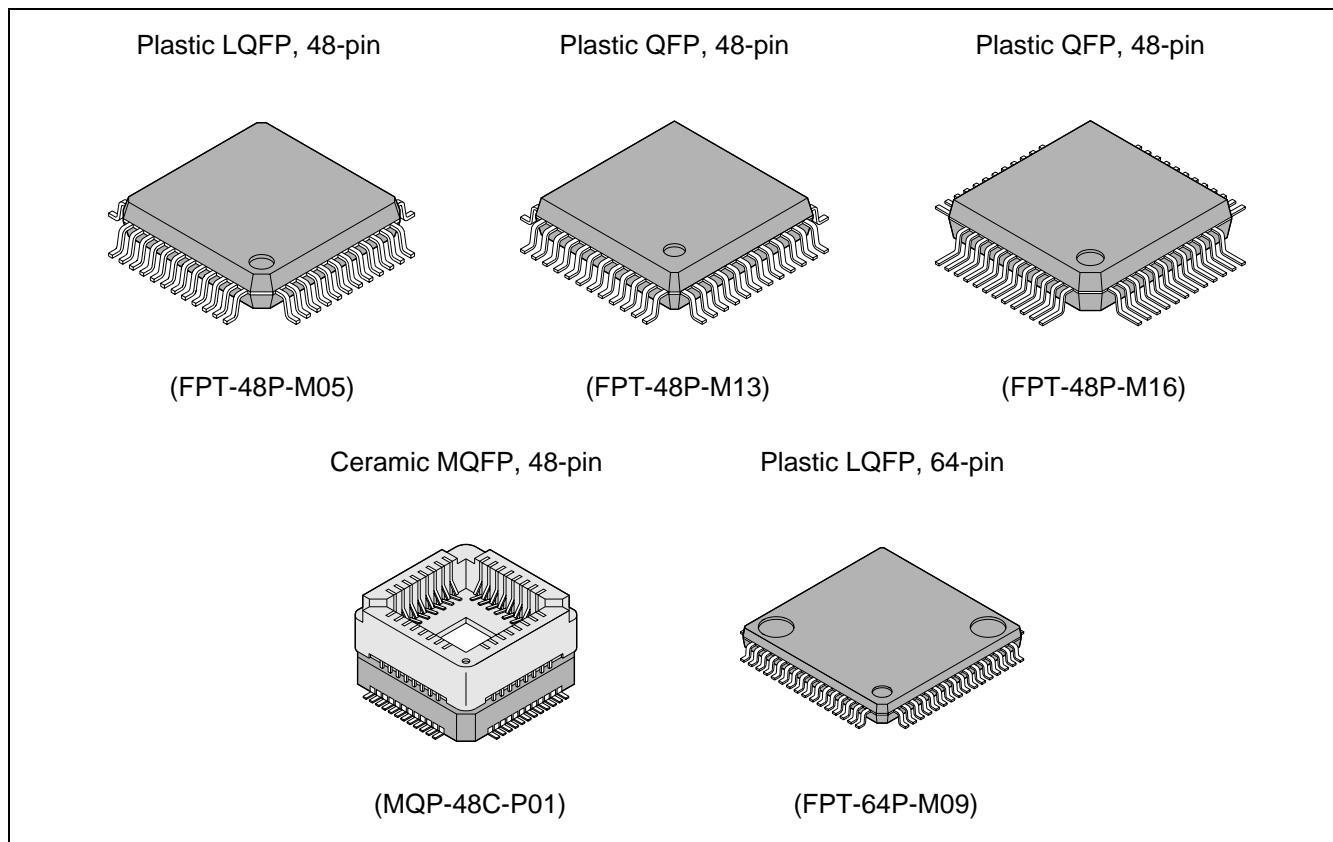
- **A/D converter**
  10-bit × 4 channels

- **External interrupts**
- External interrupt 1 (3 channels)
  Three independent interrupt inputs can be used to recover from low-power consumption modes (with edge-detection function)
- External interrupt 2 (1 channel with 8 inputs)
  Eight inputs can be used to recover from low-power consumption modes (with "L" level detection function)

- **Low-power consumption modes (standby modes)**
- Stop mode (As all oscillations halt in sub-clock mode, current consumption falls to almost zero.)
- Sleep mode (The CPU stops to reduce the current consumption to approximately 1/3 of normal.)
- Clock mode (All operation halts other than the clock prescaler resulting in very low power consumption.)

- **I²C interface***
- Supports Intel SM bus and Philips I²C bus standards.
- Uses a two-wire data transfer protocol.

- **Max. 35 I/O ports**
- Output-only ports (N-ch open drain)   : 6
- General-purpose I/O ports (CMOS)   : 21
- Output-only ports (CMOS)   : 8

* : I²C license
  The customer is licensed to use the Philips I²C patent when using this product in an I²C system that complies with the Philips I²C standard specifications.

■ PACKAGE

Plastic LQFP, 48-pin

(FPT-48P-M05)

Plastic QFP, 48-pin

(FPT-48P-M13)

Plastic QFP, 48-pin

(FPT-48P-M16)

Ceramic MQFP, 48-pin

(MQP-48C-P01)

Plastic LQFP, 64-pin

(FPT-64P-M09)

■ PRODUCT LINEUP

Part No. Prameter	MB89965	MB89P965A	MB89F969A	MB89PV960
Classification	Mass-produced products (mask ROM products)	One-time product	Flash product	Piggyback/ evaluation product for testing and development
ROM size	16 K × 8-bit (Internal mask ROM)		60 K × 8-bit	32 K × 8-bit (External ROM) *
RAM size	512 × 8-bit		1024 × 8-bit	
CPU functions	Number of instructions : 136 Instruction bit length : 8-bit Instruction length : 1 to 3 bytes Data bit length : 1-, 8-, 16bits Minimum execution time : 0.4 µs (at 10 MHz) Interrupt processing time : 3.6 µs (at 10 MHz)			
Peripheral functions — Ports	Output-only ports (N-ch open drain) : 6 (4 pins are shared with analog inputs) (2 pins are shared with resource I/O) Output-only ports (CMOS) : 8 General-purpose I/O ports (CMOS) : 21 (shared with resource I/O) Total 35 (max.)			
Peripheral functions — Timebase timer	21-bit Four interrupt intervals selectable 0.82 ms, 3.3 ms, 26.2 ms, or 419.4 ms (approx.) (for main clock)			
Peripheral functions — Watchdog timer	Reset trigger period : 419.4 ms (10 MHz main clock) 500 ms (32.768 MHz sub-clock)			
Peripheral functions — I²C interface	One channel. Supports Intel SM bus (version 1.0) and Philips I²C bus standards. Uses a 2-wire protocol for communications with other devices.			
	Included/Not included (Specified when ordering. See "Ordering Information" for details.)	Included		
Peripheral functions — 8/16-bit timer/ counter Timer	2 channel 8-bit timer/counter operation (independent operation clocks for timer 1 and timer 2) or 16-bit timer/counter operation (operation clock period : 0.8 µs to 204.8 µs) can execute an event counter operation and output a square wave using an external Clock. 1 or 16-bit timer/counter operation mode			
Peripheral functions — Serial I/O	8 bits LSB-first or MSB-first selectable Transfer clocks : External or three internal clocks (0.8 µs, 3.2 µs, 12.8 µs)			
Peripheral functions — External interrupt 1 (edge)	Selectable edge detection (rising, falling, or either edge) 3 independent channels These can also be used to recover from standby modes (edge detection is still available in stop mode) .			
Peripheral functions — External interrupt 2 (level)	1 channel with 8 inputs ("L" level interrupts, independent input enable) This can also be used to recover from standby modes (level detection is still available in stop mode) .			

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Part No. Prameter		MB89965	MB89P965A	MB89F969A	MB89PV960
Pe- riph- eral func- tions	A/D converter	4 channel × 10-bit resolution A/D conversion time : 15.2 μs (MB89965, MB89P965A, MB89F969A) 13.2 μs (MB89PV960) Continuous activation is available using the output from the 8/16-bit timer/counter or timebase timer. Reference voltage input (AVR)			
	Clock prescaler	15-bit Interrupt interval : 31.25 ms, 0.25 s, 0.50 s, 1.00 s (for a 32.768 kHz sub-clock)			
Low power consumption (standby modes)		Sleep mode, stop mode, and clock mode			
Process		CMOS			
Operating voltage		3.5 V to 5.5 V			

* : Use the MBM27C256A-20TVM as the external ROM (Operating voltage : 4.5 V to 5.5 V)

Note : Unless otherwise stated, clock periods and conversion times are for 10 MHz operation with the main clock operating at maximum speed.

■ PACKAGES AND CORRESPONDING PRODUCTS

Part No. Package	MB89965	MB89P965A	MB89F969A	MB89PV960
FPT-48P-M05	○	○	×	×
FPT-48P-M13	○	○	×	×
FPT-48P-M16	○	○	×	×
FPT-64P-M09	×	×	○	×
MQP-48C-P01	×	×	×	○

○ : Available
× : Not available

■ DIFFERENCES AMONG PRODUCTS

1. Memory Space

Please take note of the differences among products before testing and developing software for the MB89960 series.
• The RAM and ROM configurations differ among products.
• If the bottom stack address is set at the top RAM address, this will need to be relocated if changing to a different product.

2. Current Consumption
• In the case of the MB89PV960, add the current consumed by the EPROM which is connected to the top socket.
• When operated at low speed, one-time PROM and EPROM products will consume more current than mask ROM products. However, the current consumption in sleep/stop modes is the same.

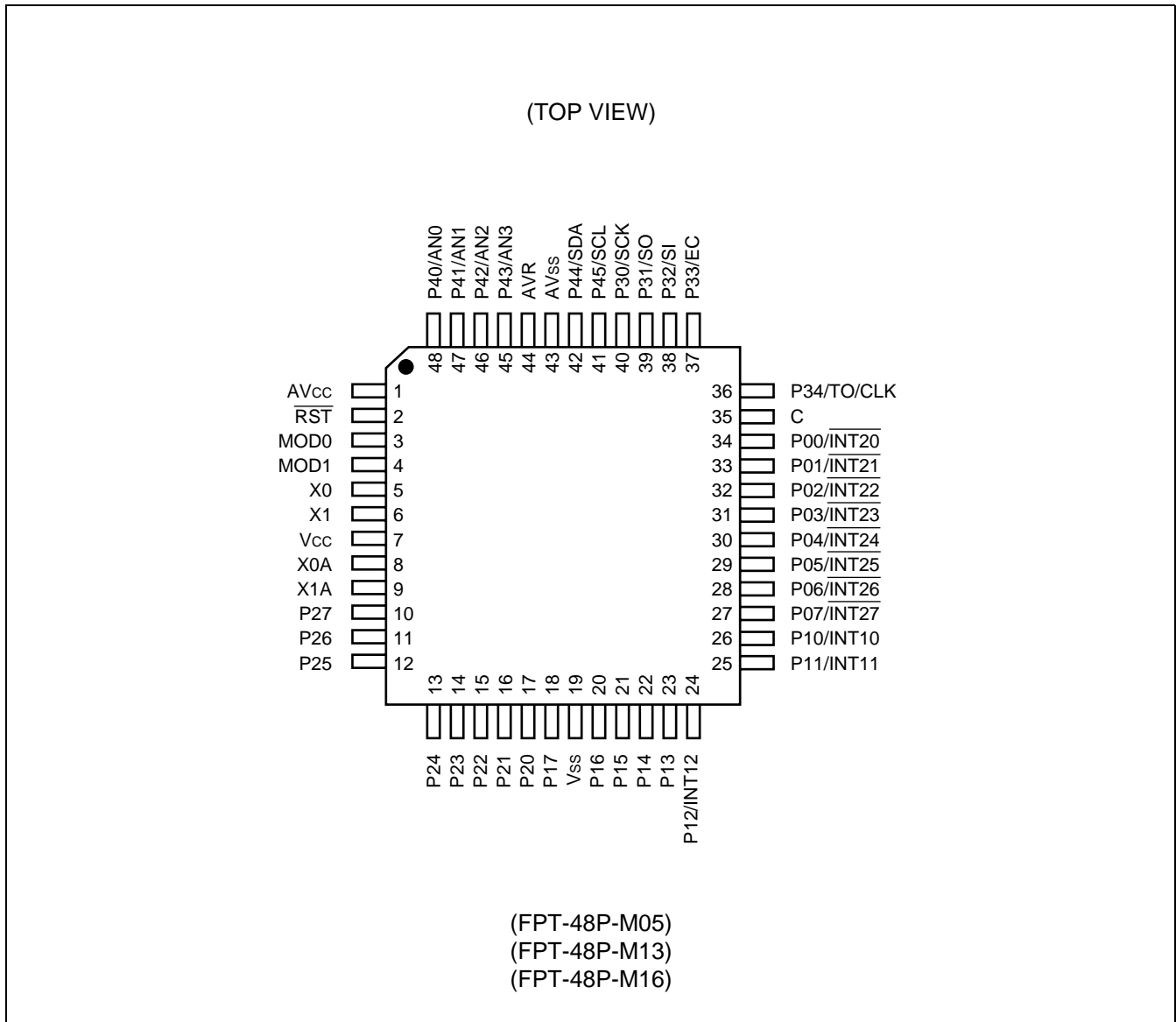### 3. Functional Differences Between MB89960 Series

	MB89965/P965A/F969A	MB89PV960
Power-on reset delay time	Regulator stabilization delay time, regulator recovery time, oscillation stabilization delay time	Oscillation stabilization delay time
External reset delay time in stop/sub-clock mode or external interrupt delay time in main stop mode	Regulator recovery time, oscillation stabilization delay time	Oscillation stabilization delay time
Port pin pull-up resistors	Software-selectable	Not available
A/D conversion time	38 instruction cycles	33 instruction cycles
I^2C noise elimination circuit	Always present regardless of ICCR : DMPB bit setting	Disabled if ICCR : DMPB bit = "1"

4. Mask Options

Functions that can be selected as options and the methods used to specify these options vary by the product. Before using mask options, check section " ■ Mask Options".
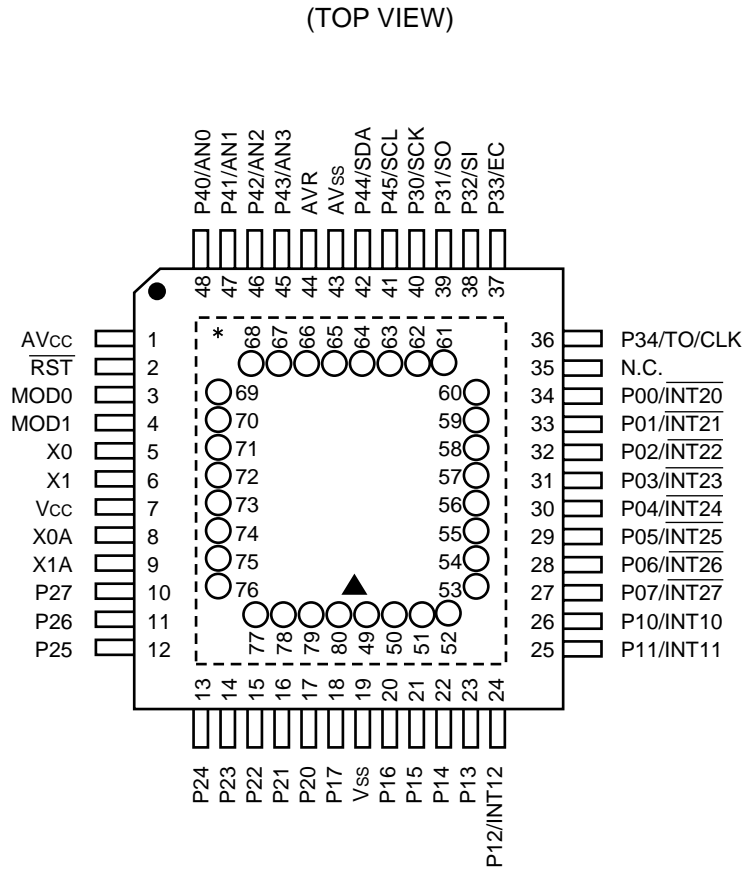
■ PIN ASSIGNMENT

(TOP VIEW)

Top pins (left to right, 48 to 37):
P40/AN0, P41/AN1, P42/AN2, P43/AN3, AVR, AVss, P44/SDA, P45/SCL, P30/SCK, P31/SO, P32/SI, P33/EC

Left pins (top to bottom, 1 to 12):
Pin	Signal
1	AVcc
2	RST
3	MOD0
4	MOD1
5	X0
6	X1
7	Vcc
8	X0A
9	X1A
10	P27
11	P26
12	P25

Right pins (top to bottom, 36 to 25):
Pin	Signal
36	P34/TO/CLK
35	C
34	P00/INT20
33	P01/INT21
32	P02/INT22
31	P03/INT23
30	P04/INT24
29	P05/INT25
28	P06/INT26
27	P07/INT27
26	P10/INT10
25	P11/INT11

Bottom pins (left to right, 13 to 24):
P24, P23, P22, P21, P20, P17, Vss, P16, P15, P14, P13, P12/INT12

(FPT-48P-M05)
(FPT-48P-M13)
(FPT-48P-M16)

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(TOP VIEW)

(MQP-48C-P01)

* : Pin assignment on package top (MB89PV960)

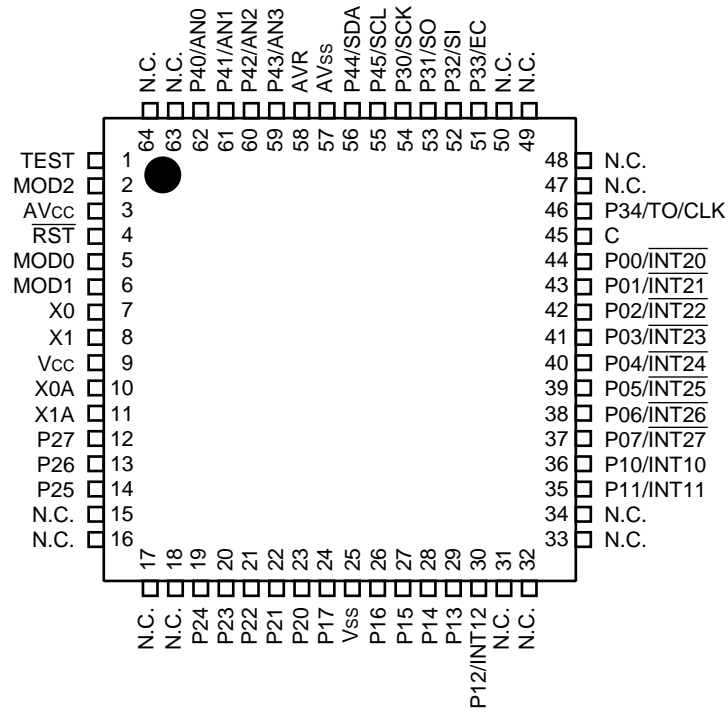| Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
49	V_{PP}	57	N.C.	65	O4	73	$\overline{OE}$
50	A12	58	A2	66	O5	74	N.C.
51	A7	59	A1	67	O6	75	A11
52	A6	60	A0	68	O7	76	A9
53	A5	61	O1	69	O8	77	A8
54	A4	62	O2	70	$\overline{CE}$	78	A13
55	A3	63	O3	71	A10	79	A14
56	N.C.	64	V_{SS}	72	N.C.	80	V_{CC}

N.C. : Internally connected. Do not use.

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(TOP VIEW)

(FPT-64P-M09)

■ PIN DESCRIPTIONS

Pin No.			Pin Name	Circuit Type	Function
MQFP-48*[3]	LQFP-48*[1] QFP-48*[2]	LQFP-64*[4]			
5	5	7	X0	A	Oscillator connection pins for the main clock oscillator (crystal oscillator or similar) . When using an external clock, input the clock signal to X0 and leave X1 open.
6	6	8	X1		
8	8	10	X0A	B	Oscillator connection pins for the sub-clock oscillator (crystal oscillator or similar) . When using an external clock (low speed : 32.768 kHz) , input the clock signal to X0A and leave X1A open.
9	9	11	X1A		
3	3	5	MOD0	C	Input pins for setting the memory access mode. Connect directly to Vss.
4	4	6	MOD1		
2	2	4	$\overline{\text{RST}}$	D	Reset I/O pin This is an N-ch open-drain output type with pull-up resistor and a hysteresis input type. The pin outputs "L" when an internal reset is present. Similarly, inputting "L" initializes the internal circuits.
27 to 34	27 to 34	37 to 44	P00/$\overline{\text{INT20}}$ to P07/$\overline{\text{INT27}}$	E	General-purpose I/O ports Also serves as the external interrupt 2 inputs (wakeup inputs) . The external interrupt 2 inputs are hysteresis inputs.
24 to 26	24 to 26	30, 35, 36	P10/INT10 to P12/INT12	E	General-purpose I/O ports Also serves as the external interrupt 1 inputs (wakeup inputs) . The external interrupt 1 inputs are hysteresis inputs.
18, 20 to 23	18, 20 to 23	24, 26 to 29	P13 to P17	E	General-purpose I/O ports
10 to 17	10 to 17	12 to 14 19 to 23	P20 to P27	G	General-purpose outoput-only ports
40	40	54	P30/SCK	F	General-purpose I/O port Also serves as the serial clock I/O. A hysteresis input.
39	39	53	P31/SO	F	General-purpose I/O port Also serves as the serial I/O data output. A hysteresis input.

*1 : FPT-48P-M05

*2 : FPT-48P-M16, FPT-48P-M13

*3 : MQP-48C-P01

*4 : FPT-64P-M09

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Pin No.			Pin Name	Circuit Type	Function
MQFP-48*3	LQFP-48*1 QFP-48*2	LQFP-64*4			
38	38	52	P32/SI	F	General-purpose I/O port Also serves as the serial I/O data input. A hysteresis input.
37	37	51	P33/EC	F	General-purpose I/O port Also serves as the external clock input for the 8/16-bit timer/counter. A hysteresis input.
36	36	46	P34/TO/ CLK	F	General-purpose I/O port Also serves as the overflow output for the 8/16-bit timer/counter and the CLK clock output. A hysteresis input.
—	35	45	C	—	Connect a 0.1 μF capacitor on the MB89965, MB89P965A, and MB89F969A.
45 to 48	45 to 48	59 to 62	P40/AN0 to P43/AN3	H	General-purpose Nch open-drain outputs. Also serves as the A/D converter analog inputs.
42	42	56	P44/SDA	I	General-purpose Nch open-drain output. Also serves as the I^2C interface data output.
41	41	55	P45/SCL	I	General-purpose Nch open-drain output. Also serves as the I^2C interface clock I/O.
7	7	9	V_{CC}	—	Power supply pin
19	19	25	V_{SS}	—	Power supply (GND) pin
1	1	3	AV_{CC}	—	A/D converter power supply pin Use this pin at the same voltage as V_{CC}.
44	44	58	AVR	—	A/D converter reference voltage input pin
43	43	57	AV_{SS}	—	A/D converter power supply pin Use this pin at the same voltage as V_{SS}.
35	—	15 to 18 31 to 34 47 to 50 63, 64	N.C.	—	These pins are not connected. Do not connect these on the MB89PV960.
—	—	1	TEST	C	TEST pin. Connect directly to V_{SS}. Only used on the MB89F969A. Treat as an N.C. pin on the MB89965.
—	—	2	MOD2	C	Memory access mode setting pin. Connect directly to V_{SS}. Only used on the MB89F969A. Treat as an N.C. pin on the MB89965.

*1 : FPT-48P-M05

*2 : FPT-48P-M16, FPT-48P-M13

*3 : MQP-48C-P01

*4 : FPT-64P-M09

• Pin Descriptions for External EPROM (MB89PV960 only)

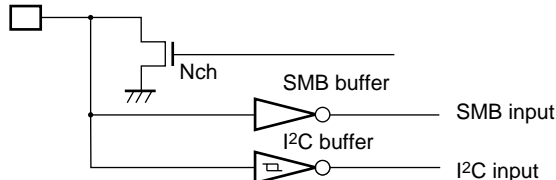| Pin No.	Pin Name	I/O	Function
49	Vpp	O	"H" level output pin
50 51 52 53 54 55	A12 A7 A6 A5 A4 A3	O	Address output pins
58 59 60	A2 A1 A0	O	Address output pins
61 62 63	O1 O2 O3	I	Data input pins
64	Vss	—	Power supply (GND) pin
65 66 67 68 69	O4 O5 O6 O7 O8	I	Data input pins
70	$\overline{\text{CE}}$	O	ROM chip enable pin Outputs "H" during standby mode.
71	A10	O	Address output pin
73	$\overline{\text{OE}}$	O	ROM output enable pin Always outputs "L".
75 76 77 78 79	A11 A9 A8 A13 A14	O	Address output pins
80	Vcc	—	EPROM power supply pin
56 57 72 74	N.C.	—	Internally connected pins Always leave open circuit.
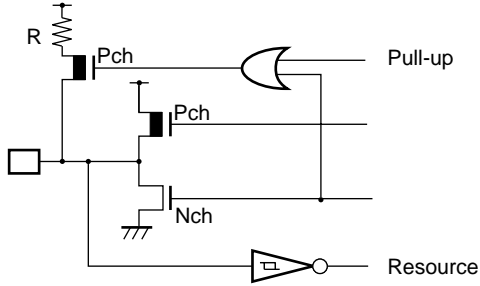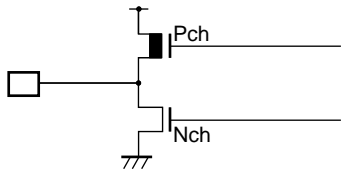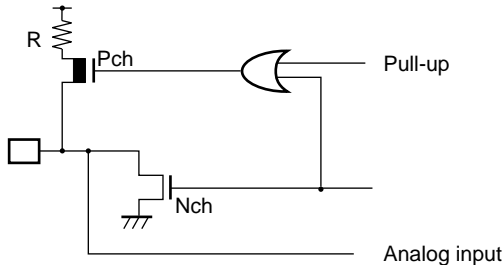
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	X1 X0 Nch Pch Pch Nch Main clock control signal	High speed clock (main clock oscillation) • Oscillation feedback resistor
B	X1A X0A Nch Pch Pch Nch Nch Sub-clock control signal	Low speed clock (sub-clock oscillation) • Oscillation feedback resistor
C		• CMOS input
D	R Pch Nch	• Output pull-up resistor (Pch) approx. 50 kΩ (at 5 V) • Hysteresis input
E	R Pch Pch Nch Pull-up Port Resource	• CMOS output • CMOS input • Selectable pull-up resistor approx. 50 kΩ (at 5 V)

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Type	Circuit	Remarks
F		• CMOS output • Hysteresis input • Selectable pull-up resistor approx. 50 kΩ (at 5 V)
G		• CMOS output
H		• Nch-open drain output • Analog input (A/D converter) • Selectable pull-up resistor • (The pull-up resistor cannot be used when used as an analog input.) approx. 50 kΩ (at 5 V)
I		• Nch open drain output • Selectable SMB or I^{2}C input buffer

■ HANDLING DEVICES

1. Do not exceed maximum rated voltage (to prevent latch-up)

Latch-up may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input or output pins other than medium- and high voltage pins or if the voltage applied between V_{CC} and V_{SS} higher the rating.
If latch-up occurs, the power supply current increases rapidly resulting in thermal damage to circuit elements. Therefore, ensure that maximum ratings are not exceeded in circuit operation.
Similarly, when turning the analog power supply on or off, ensure the analog power supply voltages (AV_{CC} and AVR) and analog input voltages do not exceed the digital power supply (V_{CC}).

2. Power supply voltage fluctuations

Rapid fluctuation of the voltage may cause the device to misoperate, even if the voltage remains within the allowed operating range.

The standard for power supply voltage stability is a peak-to-peak V_{CC} ripple voltage at the mains supply frequency (50 to 60 Hz) of 10% or less of V_{CC} and a transient voltage change rate of 0.1 V/ms or less such as when turning the power supply on or off.

3. Treatment of unused input pins

Leaving unused input pins unconnected can cause misoperation or permanent damage to the device due to latchup. Always pull-up or pull-down unused input pins using a 2 kΩ or larger resistor.

If some I/O pins are unused, either set as outputs and leave open circuit or set as inputs and treat in the same way as input pins.

4. Treatment of N.C. pins

Always leave N.C. (internally connected) pins open.

5. Treatment of power supply pins on microcontrollers with an A/D converter

Even if not using the A/D converter, connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$.

6. Precautions on using an external clock

An oscillation stabilization delay occurs after a power-on reset or when recovering from sub-clock or stop mode, even if an external clock is used.

■ PROGRAMMING SPECIFICATIONS FOR ONE-TIME PROM PRODUCTS

The MB89P965A has a "PROM mode" that enables the microcontroller to be programmed using a general-purpose ROM programmer via a special adaptor. Note, however, that electronic signature mode is not available.

### 1. ROM Programmer Adaptor and Recommended ROM Writers

Package Name	Adaptor Part No.	Recommended Programmer Manufacturer and Model
	Sun Hayato Co. Ltd.	Ando Denki Co. Ltd.
FPT-48P-M05	ROM2-48LQF-32DP-8LA	AF9708 (ver 1.44 or later) AF9709 (ver 1.44 or later)
FPT-48P-M13	ROM2-48QF2-32DP-8LA	
FPT-48P-M16	ROM2-48QF-32DP-8LA	

* Enquiries
  Sun Hayato Co. Ltd. : TEL   03-3986-0403
  Ando Denki Co. Ltd. : TEL   044-549-7300

2. PROM Mode Memory Map
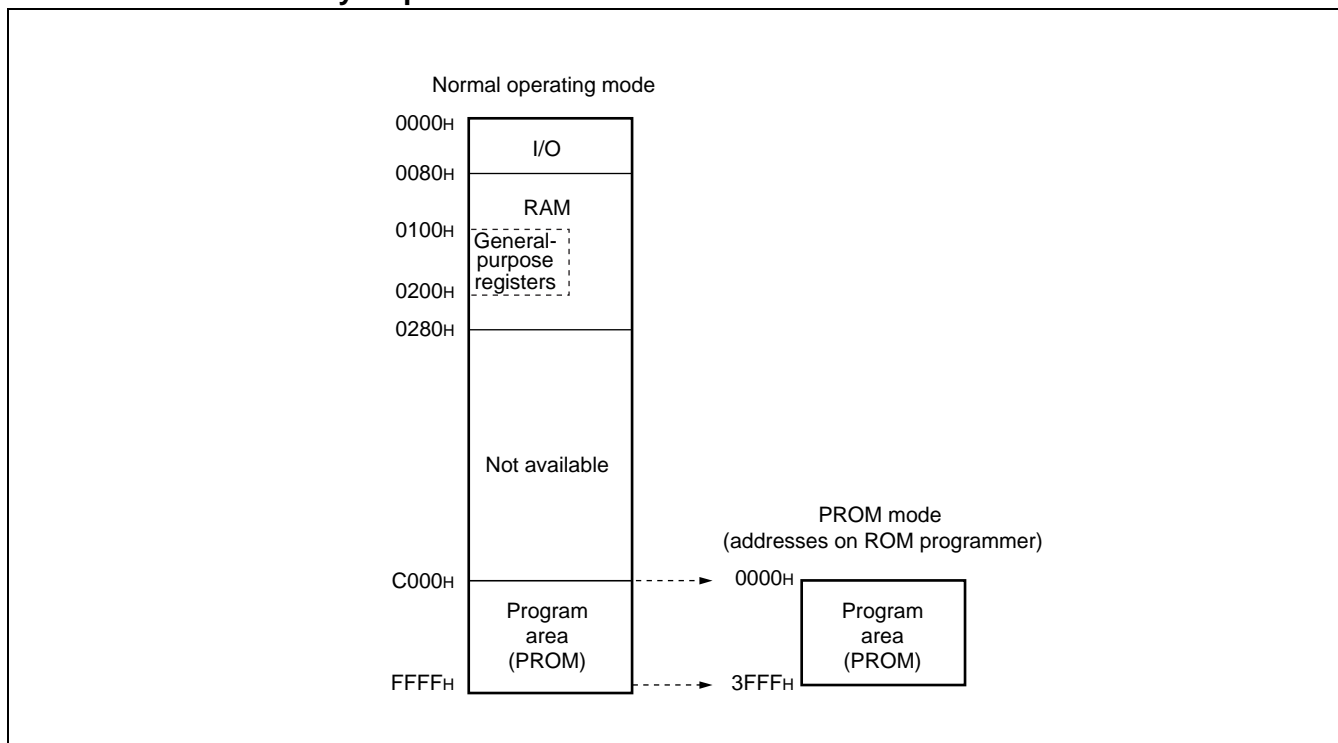
3. PROM Programming Procedure (When using an Ando EPROM programmer)

1) Set the EPROM programmer type code to 17209.

2) Load the program data into addresses 0000$_H$ to 3FFF$_H$ in the EPROM programmer.

3) Use the EPROM programmer to program to addresses C000$_H$ to FFFF$_H$.

4. Programming Yield

Due to the nature of OTPROM memory, a program test to all bits on a blank OTPROM microcontroller cannot be performed at Fujitsu. For this reason, a programming yield of 100% cannot be assured at all times.

■ PROGRAMMING AND ERASING FLASH MEMORY ON THE MB89F969A

1. Flash Memory

The flash memory is located between 1000_H and $FFFF_H$ in the CPU memory map and incorporates a flash memory interface circuit that allows read access and program access from the CPU to be performed in the same way as mask ROM. Programming and erasing flash memory is also performed via the flash memory interface circuit by executing instructions in the CPU. This enables the flash memory to be updated in place under the control of the CPU, providing an efficient method of updating program and data.

2. Flash Memory Features
• 60 K byte × 8-bit configuration (16 K + 8 K + 8 K + 28 K sectors)
• Automatic programming algorithm (Embedded algorithm* : Equivalent to MBM29LV200)
• Includes an erase pause and restart function
• Data polling and toggle bit for detection of program/erase completion
• Detection of program/erase completion via CPU interrupt
• Compatible with JEDEC-standard commands
• Sector Protection (sectors can be combined in any combination)
• No. of program/erase cycles : 10,000 (min.)

Embedded Algorithm is a trademark of Advanced Micro Devices.

3. Procedure for Programming and Erasing Flash Memory

Programming and reading flash memory cannot be performed at the same time. Accordingly, to program or erase flash memory, the program must first be copied from flash memory to RAM so that programming can be performed without program access from flash memory.

4. Flash Memory Register
• Control status register (FMCS)

	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
	$002E_H$	INTE	RDYINT	WE	RDY	Reserved	Reserved	—	Reserved	$000X00\text{-}0_B$
		R/W	R/W	R/W	R	R/W	R/W	—	R/W	

5. Sector Configuration

The table below shows the sector configuration of flash memory and lists the addresses of each sector for both during CPU access a flash memory programming.

• Sector configuration of flash memory

Flash Memory	CPU Address	Programmer Address
16 K bytes	$FFFF_H$ to $C000_H$	$1FFFF_H$ to $1C000_H$
8 K bytes	$BFFF_H$ to $A000_H$	$1BFFF_H$ to $1A000_H$
8 K bytes	$9FFF_H$ to 8000_H	$19FFF_H$ to 18000_H
28 K bytes	$7FFF_H$ to 1000_H	$17FFF_H$ to 11000_H

* : Programmer address
The programmer address is the address to be used instead of the CPU address when programming data from a parallel flash memory programmer. Use the programmer address on programming or erasing using a general-purpose parallel programmer.

6. ROM Programmer Adaptor and Recommended ROM Programmers

Package Name	Adaptor Part No.	Recommended Programmer Manufacturer and Model
	Sun Hayato Co. Ltd.	Ando Denki Co. Ltd.
FPT-64P-M09	FLASH-64QF2-32DP-8LF	AF9708 (ver 1.60 or later) AF9709 (ver 1.60 or later)

• Enquiries
  Sun Hayato Co. Ltd. : TEL   03-3986-0403
  Ando Denki Co. Ltd. : TEL   044-549-7300

MB89960 Series

■ PROGRAMMING A PIGGYBACK/EVALUATION EPROM

1. EPROM Type

MBM27C256A-20TVM

2. Programming Adaptor

Use the following programming adaptor (made by Sun Hayato Co. Ltd.) to program the EPROM using a ROM programmer.

• Programming adaptor

Package	Adaptor Socket Part No.
LCC-32 (Square)	ROM-32LC-28DP-S

Enquiries   Sun Hayato Co. Ltd. : TEL03-3986-0403

3. Memory Space
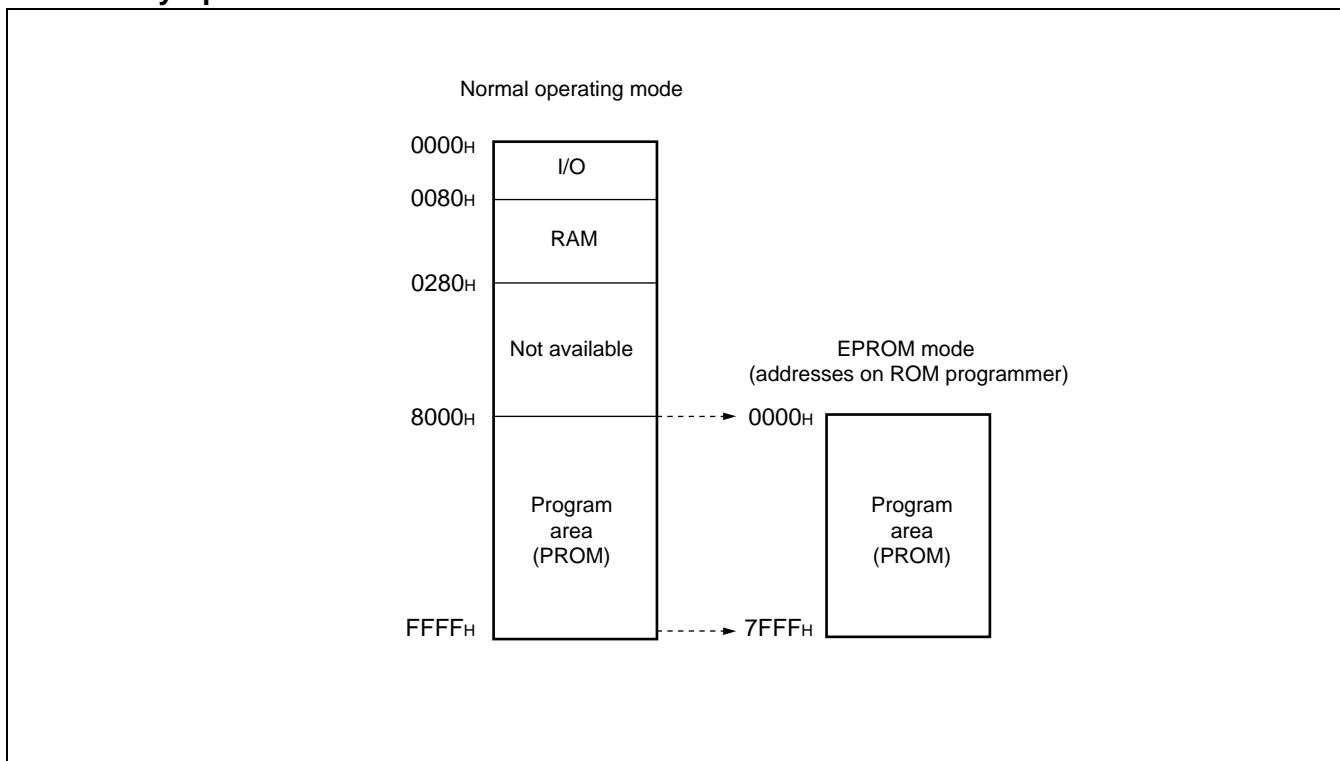
4. EPROM Programming Procedure

(1) Setup the EPROM programmer to the MBM27C256A.

(2) Load the program data into addresses 0000_H to $7FFF_H$ in the EPROM programmer.

(3) Use the ROM programmer to program to addresses 0000_H to $7FFF_H$.

■ BLOCK DIAGRAM

■ CPU CORE

1. Memory Space

(1) Structure of memory space
- **I/O area (address : 0000$_H$ to 007F$_H$)**
- Assign the control registers, data registers, and similar of the internal peripheral functions.
- As the I/O area is allocated as part of the memory space, it can be accessed in the same way as memory. Direct addressing also provides high speed access.

- **RAM area**
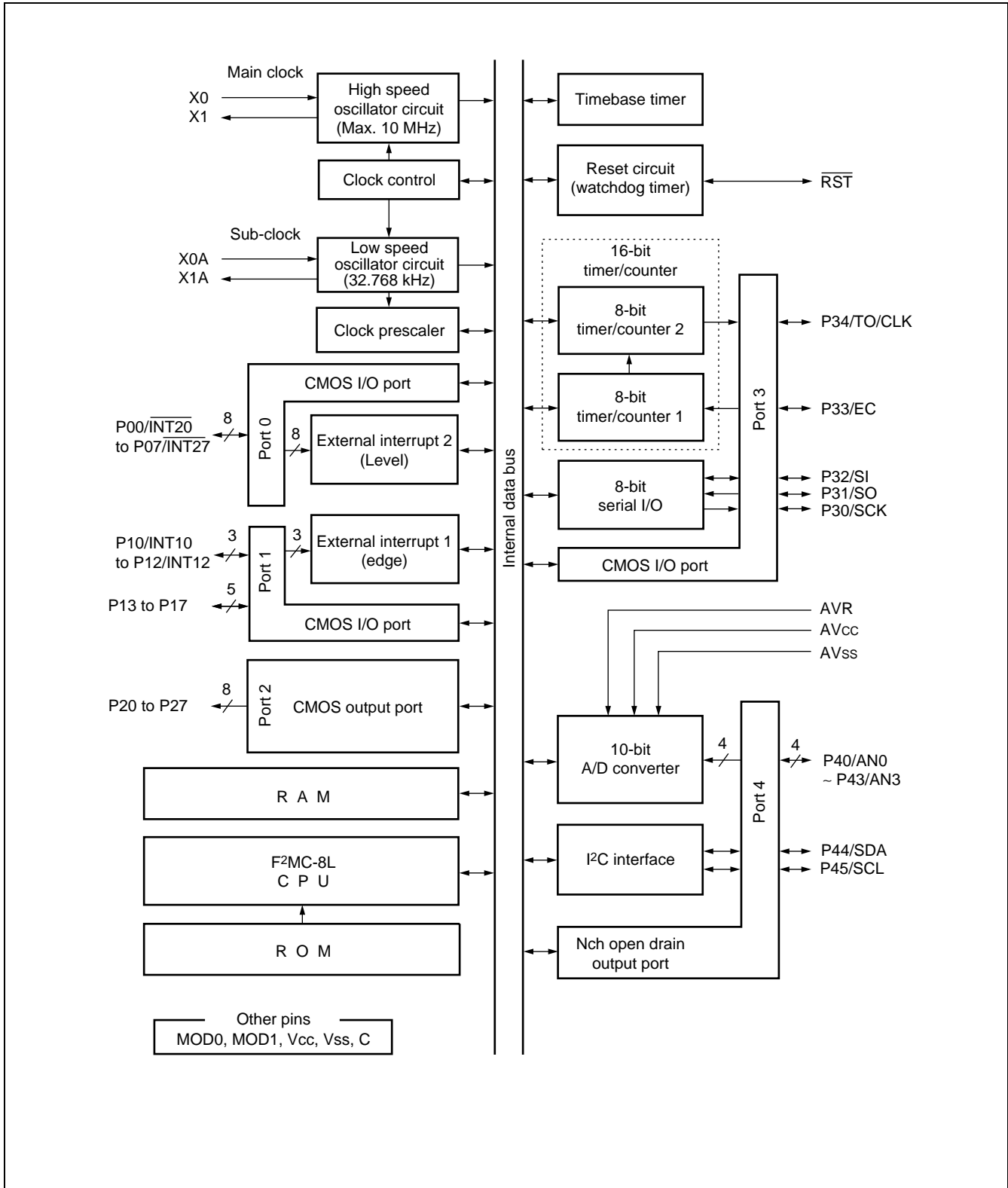- Static RAM is provided as an internal data area.
- The size of internal RAM differs between products.
- Addresses 80$_H$ to FF$_H$ provide high speed access using direct addressing.
- Addresses 100$_H$ to 1FF$_H$ are used as the general-purpose register area.
- The initial value of RAM after a reset is undefined.

- **ROM area**
- ROM memory is provided as the internal program area.
- The size of internal ROM differs between products.
- Addresses FFC0$_H$ to FFFF$_H$ are used for the vector table and similar.

(2) Memory map

Vector table
(Reset, interrupt, vector call instruction)

2. Registers

The MB89960 series provides two types of registers: dedicated registers in the CPU and general-purpose registers. The dedicated registers are as follows.

Program counter (PC)	:	A 16-bit register for indicating the instruction storage positions.
Accumulator (A)	:	A 16-bit register that provides temporary storage for arithmetic operations and similar. Instructions that operate on 8-bit data use the lower byte.
Temporary accumulator (T)	:	A 16-bit register used for arithmetic operations with the accumulator. Instructions that operate on 8-bit data use the lower byte.
Index register (IX)	:	A 16-bit register used for index modification.
Extra pointer (EP)	:	A 16-bit pointer used for indicating a memory address .
Stack pointer (SP)	:	A 16-bit register used for indicating a stack area.
Program status (PS)	:	A 16-bit register used to store a register pointer and condition code.

```
            16 bits                                          Initial value
    ┌──────────────────┐
    │        PC        │   : Program counter                   FFFDH
    └──────────────────┘
    ┌──────────────────┐
    │        A         │   : Accumulator                       Undefined
    └──────────────────┘
    ┌──────────────────┐
    │        T         │   : Temporary accumulator             Undefined
    └──────────────────┘
    ┌──────────────────┐
    │        IX        │   : Index register                    Undefined
    └──────────────────┘
    ┌──────────────────┐
    │        EP        │   : Extra pointer                     Undefined
    └──────────────────┘
    ┌──────────────────┐
    │        SP        │   : Stack pointer                     Undefined
    └──────────────────┘
    ┌────────┬─────────┐
    │   RP   │   CCR   │   : Program status            I flag = 0, IL1, IL0 = 11
    └────────┴─────────┘                               Other bits are undefined
           PS
```

The upper 8 bits of the PS contain the register bank pointer (RP) and the lower 8 bits contain the condition code register (CCR) . (See the diagram below.)

```
                        RP                                      CCR
      bit15 bit14 bit13 bit12 bit11 bit10 bit9 bit8  bit7 bit6 bit5 bit4 bit3 bit2 bit1 bit0  CCR Initial value
 PS │ R4 │ R3 │ R2 │ R1 │ R0 │ – │ – │ – │ H │ I │ IL1 │ IL0 │ N │ Z │ V │ C │   X011XXXXB

            Half carry flag ────────────────┘
            Interrupt enable flag ───────────────┘
            Interrupt level bits ──────────────────────┘
            Negative flag ───────────────────────────────────┘
            Zero flag ────────────────────────────────────────────┘
            Overflow flag ─────────────────────────────────────────────┘
            Carry flag ────────────────────────────────────────────────────┘

      X : Undefined
```

The RP contains the address of the currently used register bank. The conversion diagram below shows the relationship between the RP value and actual address.

Rules for converting of actual addresses of the general-purpose register area

Upper (RP)   Lower (op code)

"0" "0" "0" "0" "0" "0" "0" "1"   R4   R3   R2   R1   R0   b2   b1   b0

Actual address   A15 A14 A13 A12 A11 A10 A9   A8   A7   A6   A5   A4   A3   A2   A1   A0
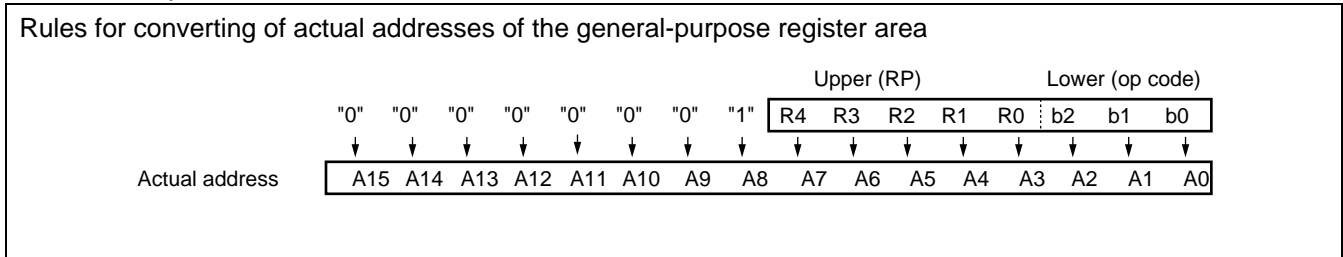
CCR contains bits that indicate the result of an arithmetic operation or information about transfer data and bits used to control CPU operation when an interrupt occurs.

H-flag : Set to "1" when a carry from bit 3 to bit 4 or a borrow from bit 4 to bit 3 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. This flag is for decimal adjustment instructions and should be ignored for operations other than addition and subtraction.

I-flag : Interrupts are enabled when this flag is set to "1" and disabled when the flag is set to "0". Cleared to "0" by a reset.

IL1, 0 : Indicates the level of interrupts currently allowed. The CPU only processes interrupts with a request level higher than the value indicated by these bits.

| IL1	IL0	Interrupt Level	Priority
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = No interrupt

N-flag : Set to "1" when the MSB of the result of an arithmetic operation is "1" and cleared to "0" when the MSB is "0".

Z-flag : Set to "1" when the result of an arithmetic operation is zero. Cleared to "0" otherwise

V-flag : Set to "1" when a 2's complement overflow occurs as the result of an arithmetic operation. Cleared to "0" if no 2's complement overflow occurs.

C-flag : Set to "1" when a carry from bit 7 or a borrow to bit 7 occurs as the result of an arithmetic operation. Cleared to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided :

General-purpose registers : 8-bit resisters for storing data

The general-purpose registers are 8-bit registers and are allocated in the register banks of the memory. Each bank contains 8 registers and all 32 banks can be used on MB89960 series microcontrollers.

The register bank pointer (RP) specifies the bank that is currently in use.

Register bank structure

Address = $0100_H + 8 \times (RP)$

R0
R1
R2
R3
R4
R5
R6
R7

32 banks

Memory area
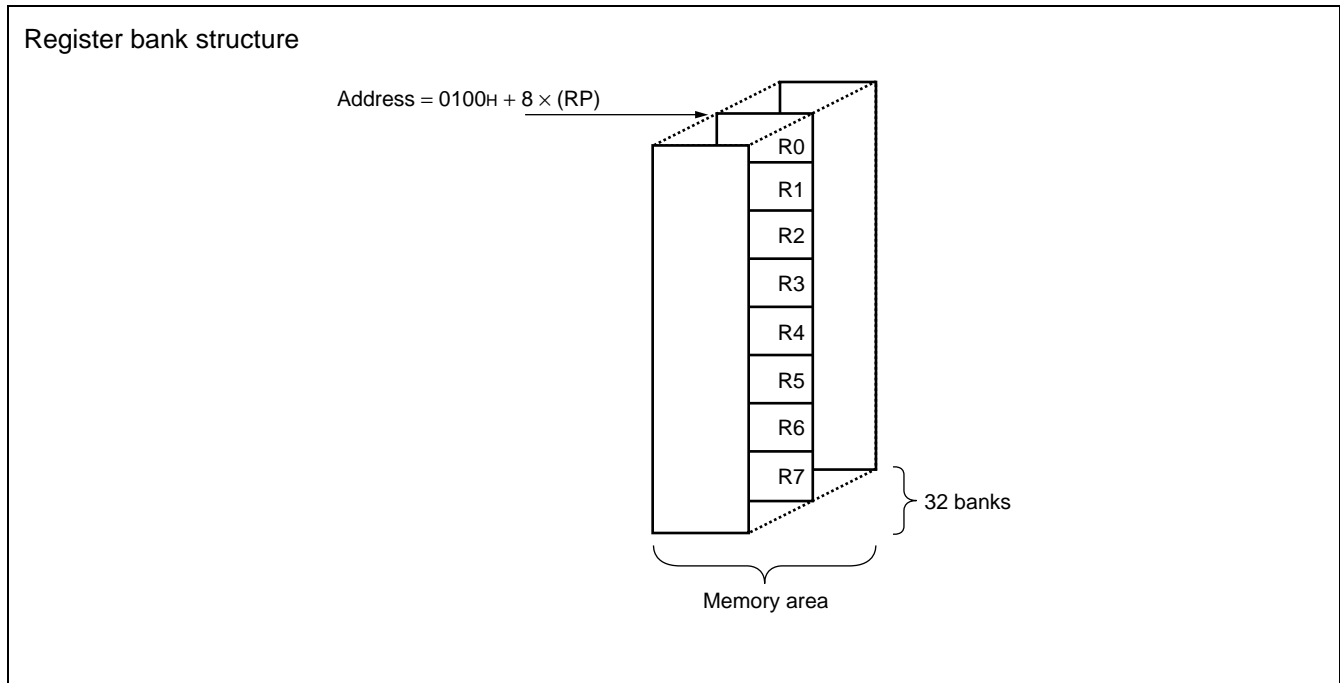
■ I/O MAP

Address	Abbreviation	Register Name	Read/Write	Initial Value
00H	PDR0	Port 0 data register	R/W	XXXXXXXX$_B$
01H	DDR0	Port 0 direction register	W	00000000$_B$
02H	PDR1	Port 1 data register	R/W	XXXXXXXX$_B$
03H	DDR1	Port 1 direction register	W	00000000$_B$
04H	PDR2	Port 2 data register	R/W	00000000$_B$
05H		(Unused area)		
06H				
07H	SYCC	System clock control register	R/W	X- -MM100$_B$
08H	STBC	Standby control register	R/W	00010- - -$_B$
09H	WDTC	Watchdog control register	R/W	0- - -XXXX$_B$
0AH	TBTC	Timebase timer control register	R/W	00- - -000$_B$
0BH	WPCR	Clock prescaler control register	R/W	00- - -000$_B$
0CH	PDR3	Port 3 data register	R/W	- - -XXXXX$_B$
0DH	DDR3	Port 3 direction register	R/W	- -000000$_B$
0EH	PDR4	Port 4 data register	R/W	- -111111$_B$
0FH		(Unused area)		
10H	IBSR	I²C bus status register	R	00000000$_B$
11H	IBCR	I²C bus control register	R/W	00011000$_B$
12H	ICCR	I²C clock control register	R/W	000XXXXX$_B$
13H	IADR	I²C address register	R/W	-XXXXXXX$_B$
14H	IDAR	I²C data register	R/W	XXXXXXXX$_B$
15H		(Unused area)		
16H				
17H				
18H	T2CR	Timer 2 control register	R/W	X0- -XXX0$_B$
19H	T1CR	Timer 1 control register	R/W	X000XXX0$_B$
1AH	T2DR	Timer 2 data register	R/W	XXXXXXXX$_B$
1BH	T1DR	Timer 1 data register	R/W	XXXXXXXX$_B$
1CH	SMR	Serial mode register	R/W	00000000$_B$
1DH	SDR	Serial data register	R/W	XXXXXXXX$_B$
1EH		(Unused area)		
1FH				
20H	ADC1	A/D control register 1	R/W	000000-0$_B$
21H	ADC2	A/D control register 2	R/W	-0000001$_B$
22H	ADDH	A/D data register H	R/W	- - - - - -XX$_B$

(Continued)

(Continued)

Address	Abbreviation	Register Name	Read/Write	Initial Value
23_H	ADDL	A/D data register L	R/W	$XXXXXXXX_B$
24_H	EIC1	External interrupt 1 control register 1	R/W	00000000_B
25_H	EIC2	External interrupt 1 control register 2	R/W	$----0000_B$
26_H to 27_H		(Unused area)		
28_H	PURR1	Pull-up resistor register 1 (MB89965, P965A, and F969A only)	R/W	11111111_B
29_H	PURR2	Pull-up resistor register 2 (MB89965, P965A, and F969A only)	R/W	11111111_B
$2A_H$	PURR3	Pull-up resistor register 3 (MB89965, P965A, nd F969A only)	R/W	$XXX11111_B$
$2B_H$	PURR4	Pull-up resistor register 4 (MB89965, P965A, and F969A only)	R/W	$XXXX1111_B$
$2C_H$ to 31_H		(Unused area)		
32_H	EIE2	External interrupt 2 control register	R/W	00000000_B
33_H	EIF2	External interrupt 2 flag register	R/W	$-------0_B$
34_H to $7B_H$		(Unused area)		
$7C_H$	ILR1	Interrupt level setting register 1	W	11111111_B
$7D_H$	ILR2	Interrupt level setting register 2	W	11111111_B
$7E_H$	ILR3	Interrupt level setting register 3	W	11111111_B
$7F_H$	ITR	Interrupt test register	Not available	$XXXXXX00_B$

• Read/write notation
R/W : Reading and writing available
R : Read-only
W : Write-only

• Initial value notation
0 : Initial value of bit is "0".
1 : Initial value of bit is "1".
X : Initial value of bit is undefined.
M : Initial value of bit is specified by mask option.
- : Bit is not used.

Note : Do not use the "unused areas".

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

$(AV_{SS} = V_{SS} = 0.0 \text{ V})$

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*
	AVR	$V_{SS} - 0.3$	$V_{SS} + 6.0$		
Input voltage	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	Pins other than P44 and P55
		$V_{SS} - 0.3$	$V_{SS} + 6.0$		Pins P44 and P45
Output voltage	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	Pins other than P44 and P55
		$V_{SS} - 0.3$	$V_{SS} + 6.0$		Pins P44 and P45
"L" level maximum output current	I_{OL}	—	15	mA	
"L" level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating ratio)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	40	mA	Average value (operating current × operating ratio)
"H" level maximum output current	I_{OH}	—	-15	mA	
"H" level average output current	I_{OHAV}	—	-4	mA	Average value (operating current × operating ratio)
"H" level total maximum output current	ΣI_{OH}	—	-50	mA	
"H" level total average output current	ΣI_{OHAV}	—	-20	mA	Average value (operating current × operating ratio)
Power consumption	P_D	—	300	mW	
		—	450		MB89F969A only
Operating temperature	T_A	-40	$+85$	°C	
Storage temperature	Tstg	-55	$+150$	°C	

* : Set AV_{CC} to the same potential as V_{CC}.
   Also ensure that AV_{CC} does not exceed V_{CC} at power on.


WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

$(AV_{SS} = V_{SS} = 0.0 \text{ V})$

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	3.5*	5.5*	V	Normal operation guaranteed range (MB89965/P965A/F969A)
		3.0	5.5	V	To maintain RAM state in stop mode (MB89965/P965A/F969A)
		2.7*	5.5*	V	Normal operation guaranteed range (MB89PV960)
		1.5	5.5	V	To maintain RAM state in stop mode (MB89PV960)
	AVR	3.5	AV_{CC}	V	
Operating temperature	T_A	−40	+85	°C	

* : Differs depending on the operating frequency and analog guaranteed range. See the figure below and "5. Electrical Characteristics for the A/D Converter".

Operating Voltage – Operating frequency
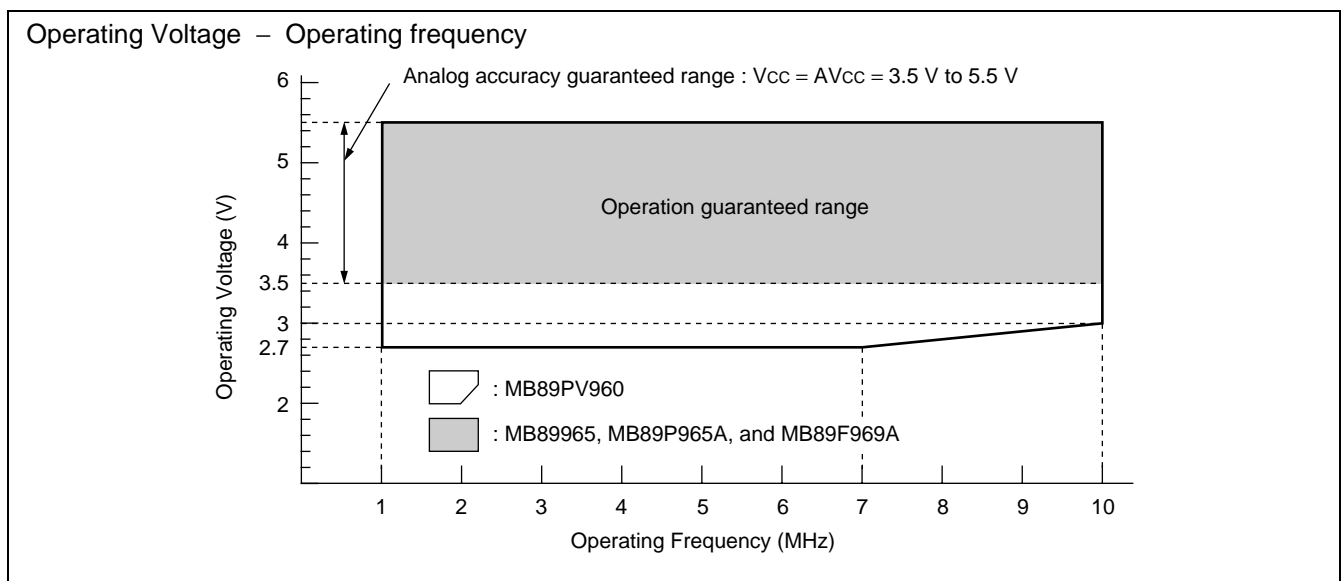
The figure above shows the frequency of the external oscillator when the instruction cycle setting is 4/F$_C$. As the operating voltage depends on the instruction cycle, change to the new instruction cycle value if using the gear function to change the operating speed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

$(AV_{CC} = V_{CC} = 5.0$ V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40$ °C to $+85$ °C$)$

Parameter	Sym-bol	Pin Name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P30 to P34	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IHS}	$\overline{RST}$, $\overline{INT20}$ to $\overline{INT27}$, INT10 to INT12, SI, SCK, EC, TEST	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IHM}	MOD0/1/2	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MOD pin input
	V_{IHSMB}	SCL, SDA	—	$V_{SS} + 1.4$	—	$V_{SS} + 5.5$	V	When SMB selected
	V_{IHI2C}			$0.7 V_{CC}$	—	$V_{SS} + 5.5$	V	When I²C selected
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P30 to P34	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	
	V_{ILS}	$\overline{RST}$, $\overline{INT20}$ to $\overline{INT27}$, INT10 to INT12, SI, SCK, EC, TEST	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	
	V_{ILM}	MOD0/1/2	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MOD pin input
	V_{ILSMB}	SCL, SDA	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.6$	V	When SMB selected
	V_{ILI2C}			$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	When I²C selected
Voltage applied to open drain output pins	V_D	P40 to P45	—	$V_{SS} - 0.3$	—	$V_{CC} + 0.3$	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P34	$I_{OH} = -2.0$ mA	4.0	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27, P30 to P34, P40 to P45, $\overline{RST}$	$I_{OL} = 4.0$ mA	—	—	0.4	V	

(Continued)

$(AV_{CC} = V_{CC} = 5.0$ V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40\ °C$ to $+85\ °C)$

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Input leak current	I_{LI}	P00 to P07, P10 to P17, P20 to P27, P30 to P34, P40 to P45	0 V $< V_I < V_{CC}$	-5	—	$+5$	µA	Without pull-up resistor option
		MOD0/1/2, TEST		-10	—	$+10$		
Open-drain output leak current	I_{LIOD}	P40 to P45	0 V $< V_I < V_{SS} + 5.5$ V	—	—	$+5$	µA	
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P30 to P34, P40 to P45, $\overline{RST}$	$V_I = 0.0$ V	25	50	100	Ω	With pull-up resistor option
Power supply current*1	I_{CC1}	V_{CC} (when using an external clock)	$F_{CH} = 10.0$ MHz t_{INST}*2 $= 0.4$ µs main run mode	—	10	20	mA	MB89PV960
				—	4	7		MB89965 MB89P965A
				—	5	8		MB89F969A
	I_{CC2}		$F_{CH} = 10.0$ MHz t_{INST}*2 $= 6.4$ µs main run mode	—	3	8	mA	MB89PV960
				—	1	3		MB89965 MB89P965A MB89F969A
	I_{CCS1}		$F_{CH} = 10.0$ MHz t_{INST}*2 $= 0.4$ µs main sleep mode	—	3	8	mA	MB89PV960
				—	2	4		MB89965 MB89P965A MB89F969A

(Continued)

(Continued)

$(AV_{CC} = V_{CC} = 5.0$ V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40$ °C to $+85$ °C$)$

Parameter	Sym-bol	Pin Name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current[1]	I_{CCS2}	V_{CC} (when using an external clock)	$F_{CH} = 10.0$ MHz t_{INST}[2] $= 6.4$ μs main sleep mode	—	1	3	mA	
	I_{CCL}		$F_{CH} = 32.768$ kHz sub run mode	—	70	150	μA	MB89PV960
				—	20	100	μA	MB89965
				—	0.3	1	mA	MB89P965A MB89F969A
	I_{CCLS}		$F_{CH} = 32.768$ kHz sub sleep mode	—	10	50	μA	
	I_{CCT}		$F_{CH} = 32.768$ kHz • clock mode, main stop mode	—	5	15	μA	
	I_{CCH}		$T_A = +25$ °C • sub stop mode	—	1	10	μA	MB89PV960
				—	5	10	μA	MB89965 MB89P965A MB89F969A
Input capacitance	C_{IN}	Except AV_{CC}, AV_{SS}, V_{CC}, and AV_{SS}	$f = 1$ MHz	—	10	—	pF	

*1 : The power supply current values are for an external clock.

*2 : See " (4) Instruction Cycle" in "4. AC Characteristics".

4. AC Characteristics

(1) Reset Timing

$(V_{CC} = 5.0 \text{ V}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40 \text{ °C to } +85 \text{ °C})$

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}*	—	ns	

* : t_{HCYL} is the period ($1/F_C$) of the oscillation input to X0.
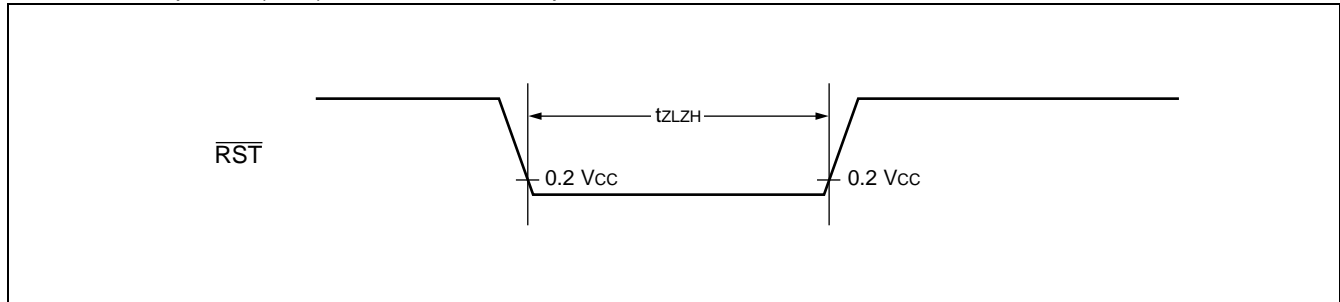
(2) Power-On Reset

$(AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40 \text{ °C to } +85 \text{ °C})$

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	0.5	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ns	For repeated operation

Note : Ensure that the power supply rising time is less than the selected oscillation stabilization delay time.
For example, if the main clock frequency $F_C = 10$ MHz and $2^{14}/F_C$ is selected as the oscillation stabilization delay time, the resulting oscillation stabilization delay time is 1.6 ms. As rapid changes in the power supply voltage may cause a power-on reset, if you need to change the power supply voltage while the device is operating, ensure that the power supply voltage changes smoothly.
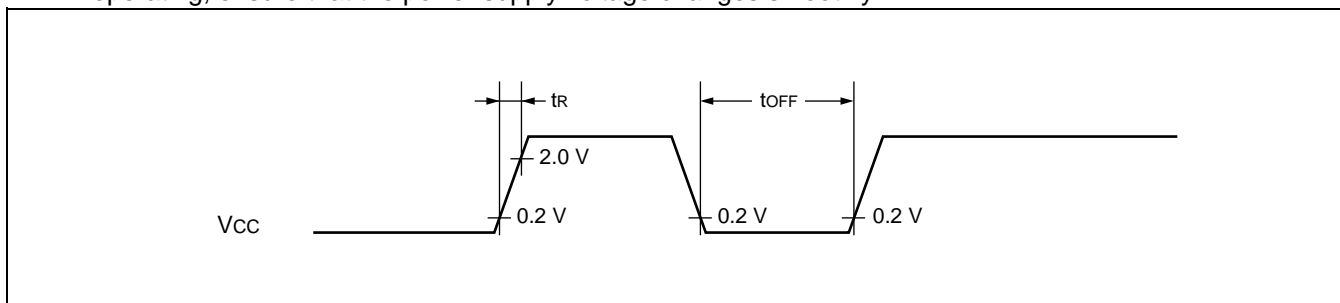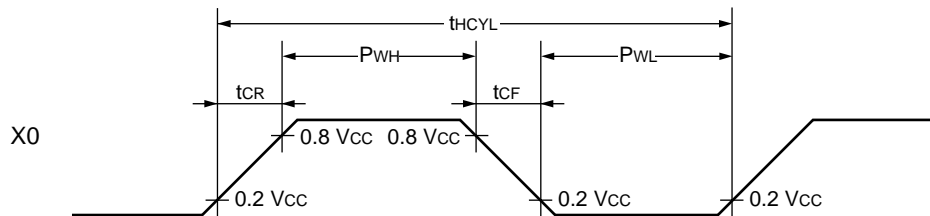
(3) Clock Timings

$(AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40 \text{ °C to } +85 \text{ °C})$

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	1	—	10	MHz	Main clock
	F_{CL}	X0A, X1A	—	32.768	—	kHz	Sub clock
Clock cycle time	t_{HCYL}	X0, X1	100	—	1000	ns	Main clock
	t_{LCYL}	X0A, X1A	—	30.5	—	μs	Sub clock
Input clock pulse width	P_{WH} P_{WL}	X0	20	—	—	ns	External clock
	P_{WHL} P_{WLL}	X0A	—	15.2	—	μs	External clock
Input clock rising/falling time	t_{CR} t_{CF}	X0	—	—	10	ns	External clock

• X0 and X1 clock timing and input conditions
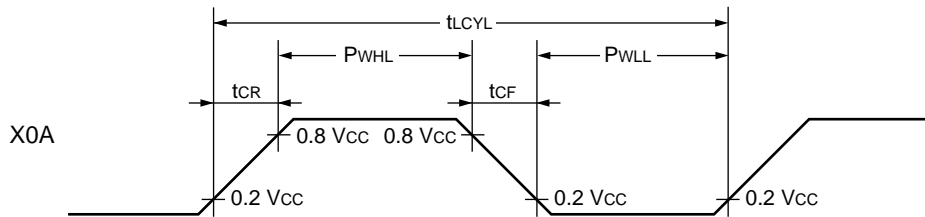

• Clock configurations

When using a crystal oscillator or ceramic oscillator
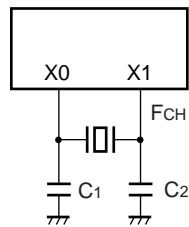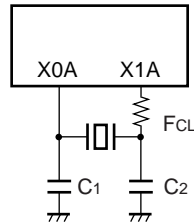
When using an external clock
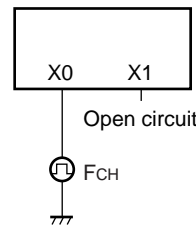
• X0A and X1A clock timing conditions
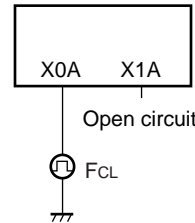

• Sub clock configuration

When using
a crystal oscillator
or ceramic oscillator

X0A   X1A

F_{CL}

C_1 C_2

When using
an external clock

X0A   X1A

Open circuit

F_{CL}

(4) Instruction Cycle

$(AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40 \text{ °C to } +85 \text{ °C})$

Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (Minimum instruction execution time)	t_{INST}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	$F_{CH} = 10$ MHz ($4/F_{CH}$) operation time $t_{INST} = 0.4$ µs
		$2/F_{CL}$		$F_{CL} = 32.768$ kHz operation time $t_{INST} = 61.036$ µs

(5) Serial I/O Timings

(Vcc = 5.0 V, AVss = Vss = 0.0 V, TA = −40 °C to +85 °C)

Parameter	Sym-bol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	tSCYC	SCK	Internal clock operation	2 tINST*	—	μs	
SCK ↓ → SO delay time	tSLOV	SCK, SO		−200	200	ns	
Valid SI → SCK ↑	tIVSH	SCK, SI		200	—	ns	
SCK ↑ → valid SI hold time	tSHIX	SCK, SI		200	—	ns	
Serial clock "H" pulse width	tSHSL	SCK	External clock operation	tINST*	—	μs	
Serial clock "L" pulse width	tSLSH	SCK		tINST*	—	μs	
SCK ↓ → SO delay time	tSLOV	SCK, SO		0	200	ns	
Valid SI → SCK	tIVSH	SCK, SI		200	—	μs	
SCK ↑ → valid SI hold time	tSHIX	SCK, SI		200	—	μs	

* : See " (4) Instruction cycle" for a definition of tINST.

• Internal shift clock mode
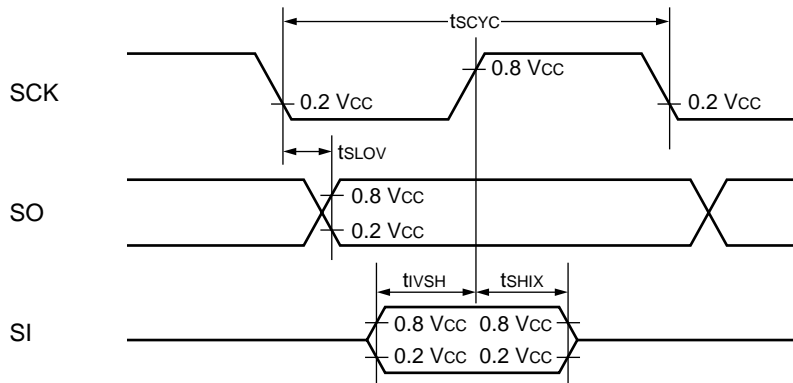
• External shift clock mode
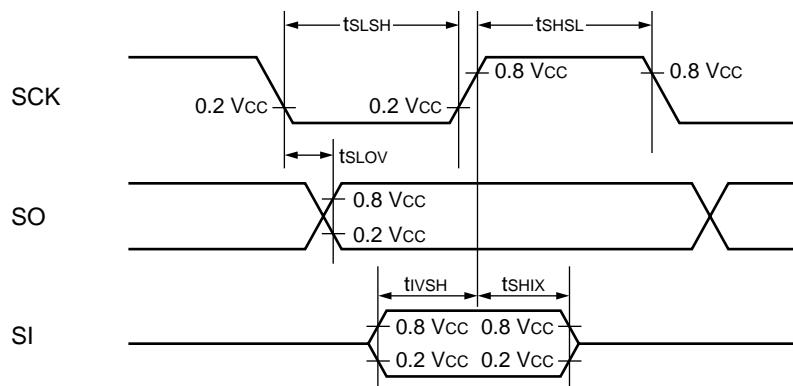
(6) Peripheral Input Timings

$(V_{CC} = 5.0 \text{ V}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40 \text{ °C to } +85 \text{ °C})$

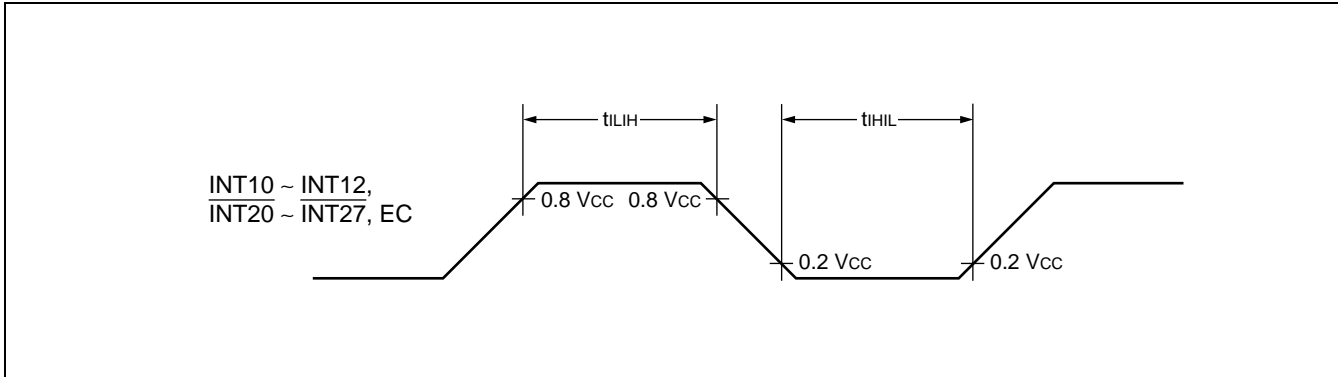| Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min.	Max.		
Peripheral input "H" pulse width	t_{ILIH}	INT10 to INT12, INT20 to INT27, EC	$2 t_{INST}$*	—	µs	
Peripheral input "L" pulse width	t_{IHIL}		$2 t_{INST}$*	—	µs	

* : See " (4) Instruction cycle" for a definition of t_{INST}.

(7) I²C Timings

$$(V_{CC} = 5.0 \text{ V}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40 \text{ °C to } +85 \text{ °C})$$

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Start condition output	t_{STA}	SCL SDA	$1/4t_{INST}\text{*1} \times m\text{*} \times n\text{*3} - 20$	$1/4t_{INST}\text{*1} \times m\text{*2} \times n\text{*3} + 20$	ns	Master mode
Stop condition output	t_{STO}	SCL SDA	$1/4t_{INST}\text{*1} \times (m\text{*2} \times n\text{*3} + 8) - 20$	$1/4t_{INST}\text{*1} \times (m\text{*2} \times n\text{*3} + 8) + 20$	ns	Master mode
Start condition detect	t_{STA}	SCL SDA	$1/4t_{INST}\text{*1} \times 6 + 40$	—	ns	
Stop condition detect	t_{STO}	SCL SDA	$1/4t_{INST}\text{*1} \times 6 + 40$	—	ns	
Restart condition output	t_{STASU}	SCL SDA	$1/4t_{INST}\text{*1} \times (m\text{*2} \times n\text{*3} + 8) - 20$	$1/4t_{INST}\text{*1} \times (m\text{*2} \times n\text{*3} + 8) + 20$	ns	Master mode
Restart condition detect	t_{STASU}	SCL SDA	$1/4t_{INST}\text{*1} \times 4 + 40$	—	ns	
SCL output "L" width	t_{LOW}	SCL	$1/4t_{INST}\text{*1} \times m\text{*2} \times n\text{*3} - 20$	$1/4t_{INST}\text{*1} \times m\text{*2} \times n\text{*3} + 20$	ns	Master mode
SCL output "H" width	t_{HIGH}	SCL	$1/4t_{INST}\text{*1} \times (m\text{*2} \times n\text{*3} + 8) - 20$	$1/4t_{INST}\text{*1} \times (m\text{*2} \times n\text{*3} + 8) + 20$	ns	Master mode
SDA output delay	t_{DO}	SDA	$1/4t_{INST}\text{*1} \times 4 - 20$	$1/4t_{INST}\text{*1} \times 4 + 20$	ns	
SDA output setup time after interrupt	t_{DOSU}	SDA	$1/4t_{INST}\text{*1} \times 4 - 20$	—	ns	
SCL input "L" pulse width	t_{LOW}	SCL	$1/4t_{INST}\text{*1} \times 6 + 40$	—	ns	
SCL input "H" pulse width	t_{HIGH}	SCL	$1/4t_{INST}\text{*1} \times 2 + 40$	—	ns	
SDA input setup time	t_{SU}	SDA	40	—	ns	
SDA hold time	t_{HO}	SDA	0	—	ns	

*1: See " (4) Instruction cycle" for a definition of t_{INST}.

*2: m is the value set in the ICCR : CS4 and CS3 bits (bits 4 to 3) .

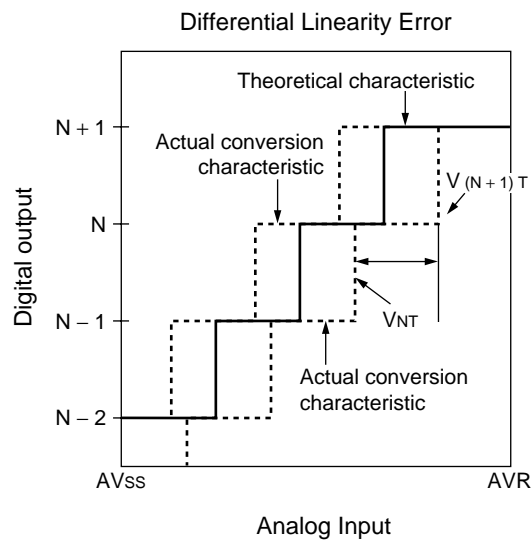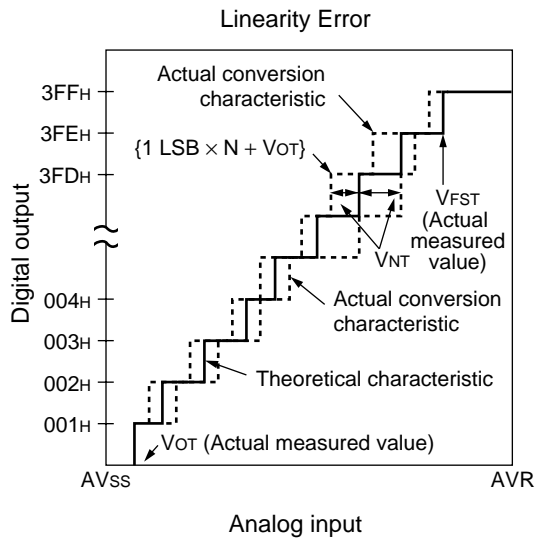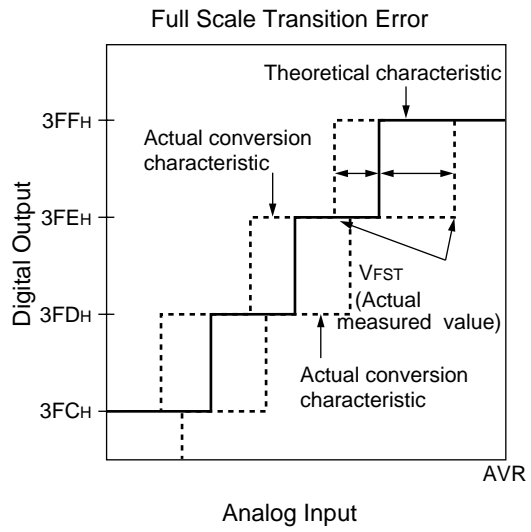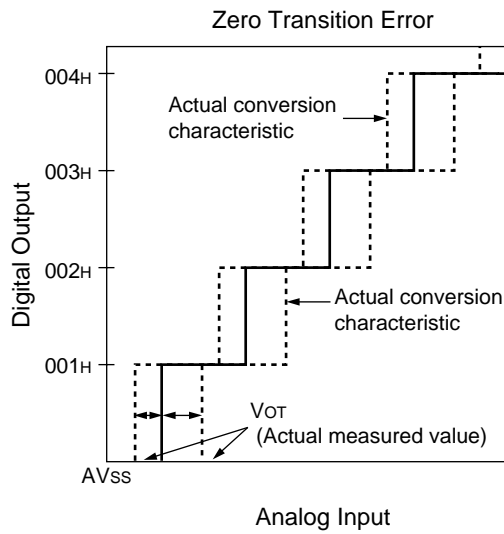*3: n is the value set in the ICCR : CS2 to CS0 bits (bits 2 to 0) .

- Data transmit (master/slave)

- Data receive (master/slave)
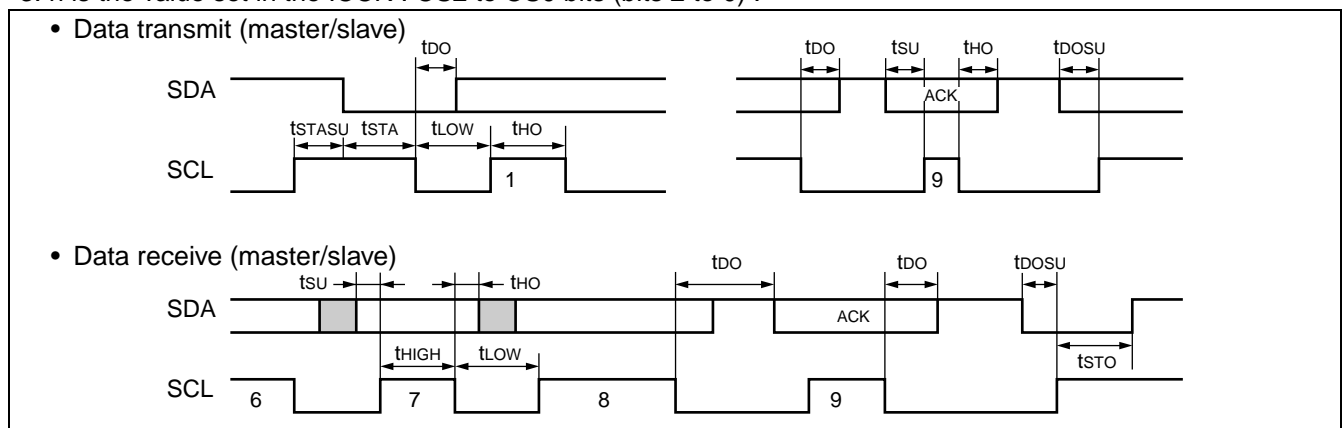
5. Electrical Characteristics for the A/D Converter

$(AV_{CC} = 3.5 \text{ V to } 5.5 \text{ V}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C})$

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—		—	—	—	10	bit	
Total error	—			−5.0	—	+5.0	LSB	
Non-linearity error				−2.5	—	+2.5	LSB	
Differential linearity error				−1.9	—	+1.9	LSB	
Zero transition voltage	V_{OT}	—	$AVR = A_{VCC}$	$AVR - 3.5$ LSB	$AVR + 0.5$ LSB	$AVR + 4.5$ LSB	mV	
Full-scale transition voltage	V_{FST}			$V_{CC} - 6.5$ LSB	$V_{CC} - 1.5$ LSB	$V_{CC} + 1.5$ LSB	mV	
Variation between channels	—			—	—	4	LSB	
A/D mode conversion time*2	—		—	—	60 t_{INST}*1	—	μs	MB89965 MB89P965A MB89F969A
				—	38 t_{INST}*1	—	μs	MB89PV960
A/D sampling time				—	16 t_{INST}*1	—	μs	
Analog input current	I_{AIN}	AN0 to AN3		—	—	10	μA	
Analog input voltage range	V_{AIN}			AV_{SS}	—	AVR	V	
Power supply current	I_A	A_{VCC}	A/D operation	—	1.5	3	mA	
	I_{AH}		$T_A = +25 \text{ }^\circ\text{C}$ A/D stop	—	1	5	μA	
Reference voltage	—	AVR	—	$AV_{SS} + 3.5$	—	AV_{CC}	V	
Reference voltage supply current	I_R		A/D operation	—	400	—	μA	
	I_{RH}		A/D stop	—	—	5	μA	

*1 : See " (4) Instruction cycle" for a definition of t_{INST}.

*2 : Includes sampling time.

6. A/D Converter Glossary

• Resolution

   The change in analog voltage that can be recognized by the A/D converter.

• Linearity error (unit : LSB)

   The deviation between the actual conversion characteristics and the line linking the zero transition point ("00 0000 0000$_B$" $\longleftrightarrow$ "00 0000 0001$_B$") and the full scale transition point ("11 1111 1110$_B$" $\longleftrightarrow$ "11 1111 1111$_B$") .

• Differential linearity error (unit : LSB)

   The variation from the ideal input voltage required to change the output code by 1 LSB.

• Total error (unit : LSB)

   The total error is the difference between the actual value and the theoretical value.

Theoretical I/O Characteristics

Total Error

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ (V)}$$

$$\text{Total error for digital output N} = \frac{V_{NT} - \{1 \text{ LSB} \times N + 0.5 \text{ LSB}\}}{1 \text{ LSB}}$$

Zero Transition Error

Digital Output

004H

003H

002H

001H

Actual conversion characteristic

Actual conversion characteristic

V_{OT} (Actual measured value)

AVss

Analog Input

Full Scale Transition Error

Digital Output

3FFH

3FEH

3FDH

3FCH

Theoretical characteristic

Actual conversion characteristic

V_{FST} (Actual measured value)

Actual conversion characteristic

AVR

Analog Input

Linearity Error

Digital output

3FFH
3FEH
3FDH

004H
003H
002H
001H

Actual conversion characteristic

$\{1\ LSB \times N + V_{OT}\}$

V_{FST} (Actual measured value)

V_{NT}

Actual conversion characteristic

Theoretical characteristic

V_{OT} (Actual measured value)

AVss   AVR

Analog input

Differential Linearity Error

Digital output

N + 1

N

N − 1

N − 2

Theoretical characteristic

Actual conversion characteristic

$V_{(N + 1)\ T}$

V_{NT}

Actual conversion characteristic

AVss   AVR

Analog Input

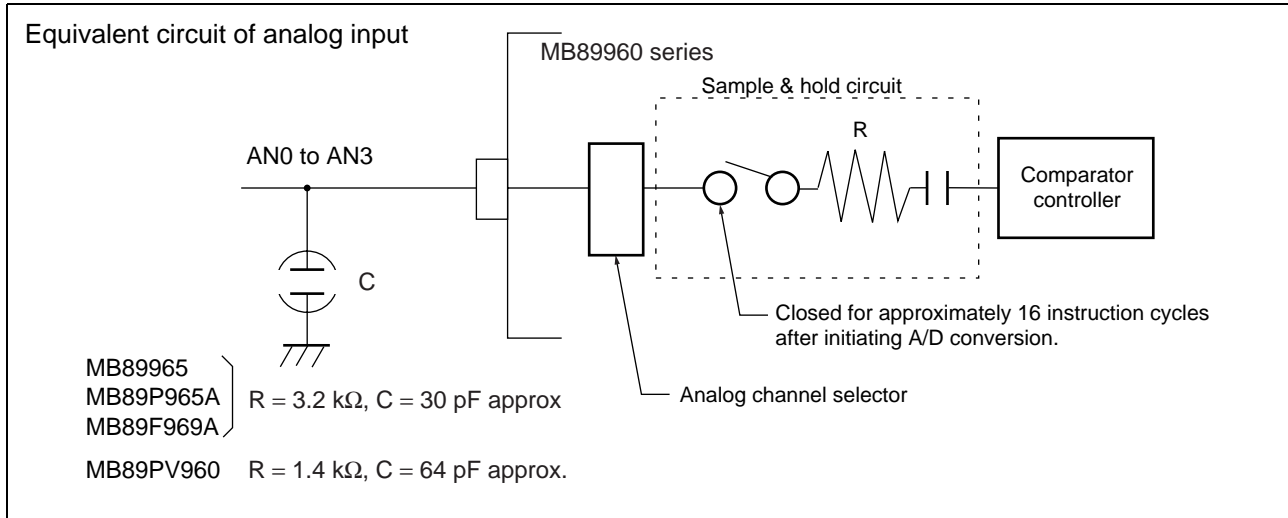$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ LSB \times N + V_{OT}\}}{1\ LSB}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N + 1)\ T} - V_{NT}}{1\ LSB} - 1$$

7. Notes for A/D Conversion

• Analog input pins and input impedance

The A/D converter incorporates a sample & hold circuit as shown below. When an A/D conversion starts, the voltage at the analog input pin is captured by the sample & hold capacitor for a period of 16 instruction cycles. Accordingly, if the output impedance of the external circuit connected to the analog input is high, the analog input voltage may not stabilize within the period of the analog input sampling time. Therefore, ensure that the output impedance of the external circuit is sufficiently low (10 kΩ or less) . If it is not possible to reduce the output impedance of the external circuit, connecting an external capacitor of approximately 0.1 μF is recommended.

Equivalent circuit of analog input

MB89960 series

Sample & hold circuit

R

AN0 to AN3

Comparator controller

C

Closed for approximately 16 instruction cycles after initiating A/D conversion.

MB89965
MB89P965A   R = 3.2 kΩ, C = 30 pF approx   Analog channel selector
MB89F969A

MB89PV960   R = 1.4 kΩ, C = 64 pF approx.

• Error

The relative error increases as |AVR − AV$_{SS}$| becomes smaller.

8.   **Electrical Characteristics of Flash Memory**
   • Programming and erasing characteristics

Parameter			Symbol	Pin Name	Condition	Value			Unit	Remarks
						Min.	Typ.	Max.		
Power supply current*1			I_{FWE}	V_{CC}	V_{CC} = 5.0 V	—	—	40	mA	
Sector erasing time	Fixed time per sector regardless of size	Successful completion time	—	—	—	—	1	15	s	
		Unsuccessful completion time				—	—	*2	—	
Programming time	per byte	Successful completion time	—	—	—	—	8	3600	µs	
		Unsuccessful completion time				—	650	3600	µs	

*1 : Automatic algorithm executing

*2 : If a fault occurs during sector erasing, detection via DQ_5 may not be available (DQ_5 = 1 may not occur) .
   Accordingly, a fault must be assumed after 15 s, even if DQ_5 does not go to "1".

■ MASK OPTIONS

NO	Part No.	MB89965	MB89P965A/MB89F969A	MB89PV960
	Specifying procedure	Specify when ordering mask	Not available	Not available
1	Initial value* selection for main clock oscillation stabilization delay time (F_{CH} = 10 MHz) • 01 : $2^{12}/F_{CH}$ (0.4 ms approx.) • 10 : $2^{16}/F_{CH}$ (6.6 ms approx.) • 11 : $2^{18}/F_{CH}$ (26.2 ms approx.)	Selectable	$2^{18}/F_{CH}$ (26.2 ms approx.)	$2^{18}/F_{CH}$ (26.2 ms approx.)

F_{CH} : Frequency of main clock oscillation

* : This specifies the initial value after a reset of the oscillation stabilization delay time setting bits in the system clock control register (SYCC : WT1, WT0)

■ ORDERING INFOMATION

Part Number	Package	Remarks
MB89965PFV1 MB89P965APFV1 MB89965CPFV1	Plastic LQFP, 48-pin (FPT-48P-M05)	The MB89965PFV1 does not have an I^{2}C function.
MB89965PFM MB89P965APFM MB89965CPFM	Plastic QFP, 48-pin (FPT-48P-M13)	The MB89965PFM does not have an I^{2}C function.
MB89965PF MB89P965APF MB89965CPF	Plastic QFP, 48-pin (FPT-48P-M16)	The MB89965PF does not have an I^{2}C function.
MB89F969APFM	Plastic LQFP, 64-pin (FPT-64P-M09)	
MB89PV960CF	Ceramic MQFP, 48-pin (MQP-48C-P01)	

■ **PACKAGE DIMENSIONS**

(These package dimensions are provisional. Please obtain the actual dimensions of the final product separately.)

Plastic LQFP, 48-pin
(FPT-48P-M05)

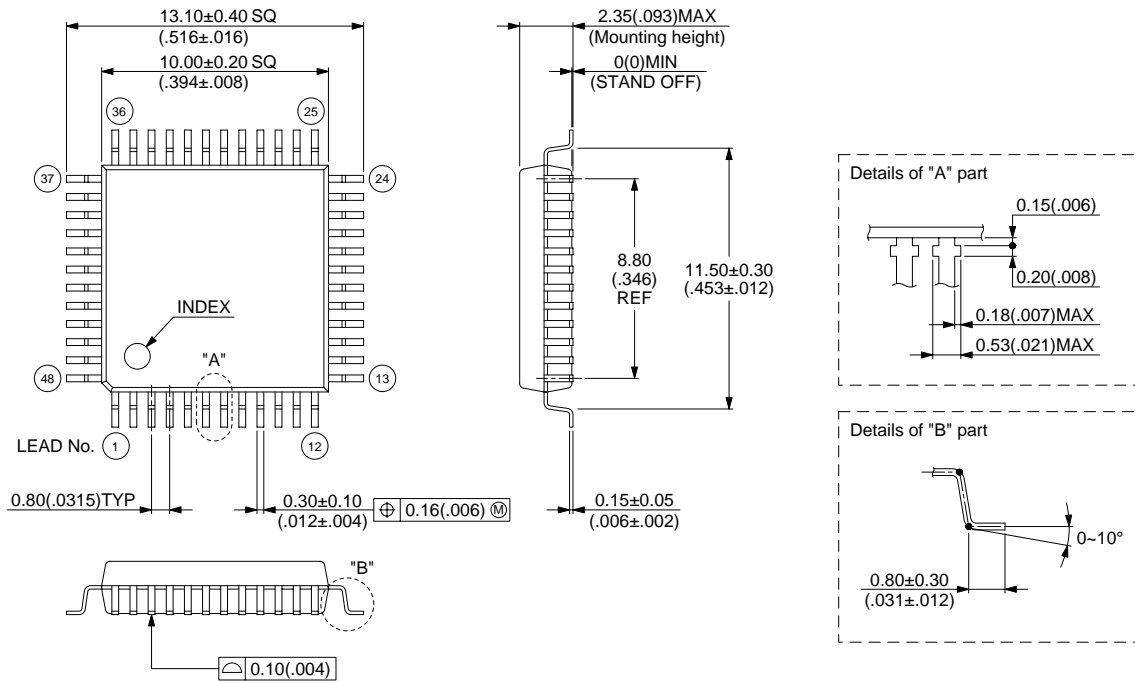Note : The pin width and thickness includes plating.

9.00±0.20(.354±.008)SQ

7.00±0.10(.276±.004)SQ

36   25

37   24

INDEX

48   13

LEAD No. 1   12

0.50(.020)

0.20±0.05
(.008±.002)   ⊕ 0.08(.003) Ⓜ

0.145±0.055
(.006±.002)

⌒ 0.08(.003)

"A"

Details of "A" part

1.50 $^{+0.20}_{-0.10}$ (Mounting height)
(.059 $^{+.008}_{-.004}$)

0°~8°

0.10±0.10
(.004±.004)
(Stand off)

0.50±0.20
(.020±.008)

0.60±0.15
(.024±.006)

0.25(.010)
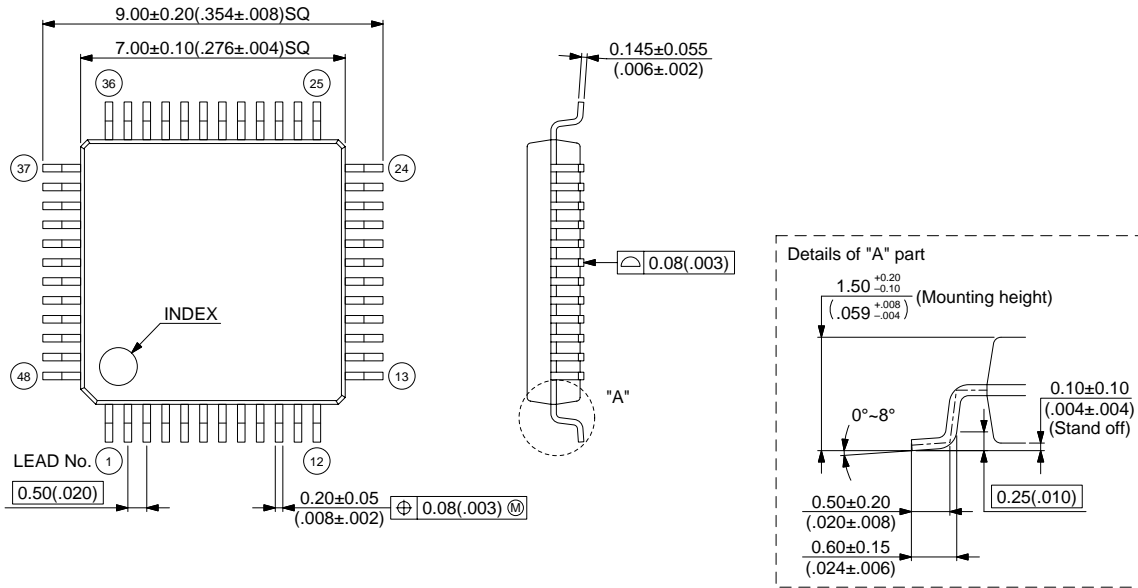
© 2000 FUJITSU LIMITED F48013S-c-4-8

Dimensions in mm (inches).

Plastic QFP, 48-pin
(FPT-48P-M13)

13.10±0.40 SQ
(.516±.016)

10.00±0.20 SQ
(.394±.008)

36   25

37   24

INDEX

"A"

48   13

LEAD No. 1   12

0.80(.0315)TYP   0.30±0.10   ⊕ 0.16(.006) Ⓜ
(.012±.004)

"B"

0.10(.004)

2.35(.093)MAX
(Mounting height)

0(0)MIN
(STAND OFF)

8.80   11.50±0.30
(.346)   (.453±.012)
REF

0.15±0.05
(.006±.002)

Details of "A" part

0.15(.006)

0.20(.008)

0.18(.007)MAX

0.53(.021)MAX

Details of "B" part

0~10°

0.80±0.30
(.031±.012)

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Dimensions in mm (inches).

Plastic QFP, 48-pin
(FPT-48P-M16)

17.20±0.40 SQ
(.677±.016)
12.00 $^{+0.30}_{-0.10}$ SQ
$\left(.472 ^{+.012}_{-.004}\right)$

36   25

37   24

INDEX

48   13

"A"

LEAD No. 1   12

0.80(.0315)TYP   0.30±0.06
(.012±.002)   ⊕ 0.16(.006) Ⓜ

"B"

⌂ 0.15(.006)

2.70(.106)MAX
(Mounting height)
0.05(.002)MIN
(STAND OFF)

8.80
(.346)
REF   13.60±0.40
(.535±.016)

0.15 $^{+0.05}_{-0.01}$
$\left(.006 ^{+.002}_{-.0004}\right)$

Details of "A" part
0.15(.006)
0.20(.008)
0.15(.006)MAX
0.50(.020)MAX

Details of "B" part
0~10°
1.80±0.30
(.071±.012)
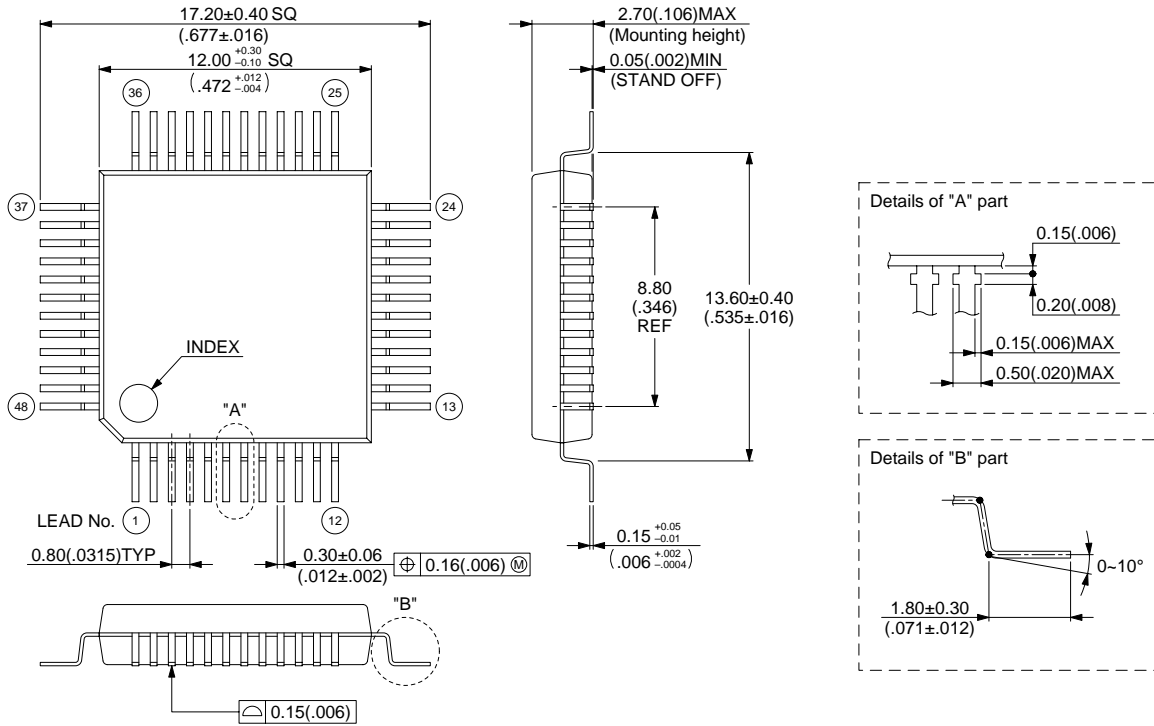
© 2000 FUJITSU LIMITED F48026S-1C-2

Dimensions in mm (inches).

Ceramic MQFP, 48-pin
(MQP-48C-P01)

17.20(.677)TYP

15.00±0.25
(.591±.010)

14.82±0.35
(.583±.014)

PIN No.1 INDEX

1.02±0.13
(.040±.005)

10.92 $^{+0.13}_{-0.0}$
$(.430 ^{+.005}_{-0})$

7.14(.281)
TYP

8.71(.343)
TYP

0.30(.012)TYP

PAD No.1 INDEX

4.50(.177)TYP

1.50(.059)TYP

8.80(.346)REF

1.00(.040)TYP

0.80±0.22
(.0315±.0087)

PIN No.1 INDEX

1.10 $^{+0.45}_{-0.25}$
$(.043 ^{+.018}_{-.010})$

0.40±0.08
(.016±.003)

0.60(.024)TYP

8.50(.335)MAX

0.15±0.05
(.006±.002)
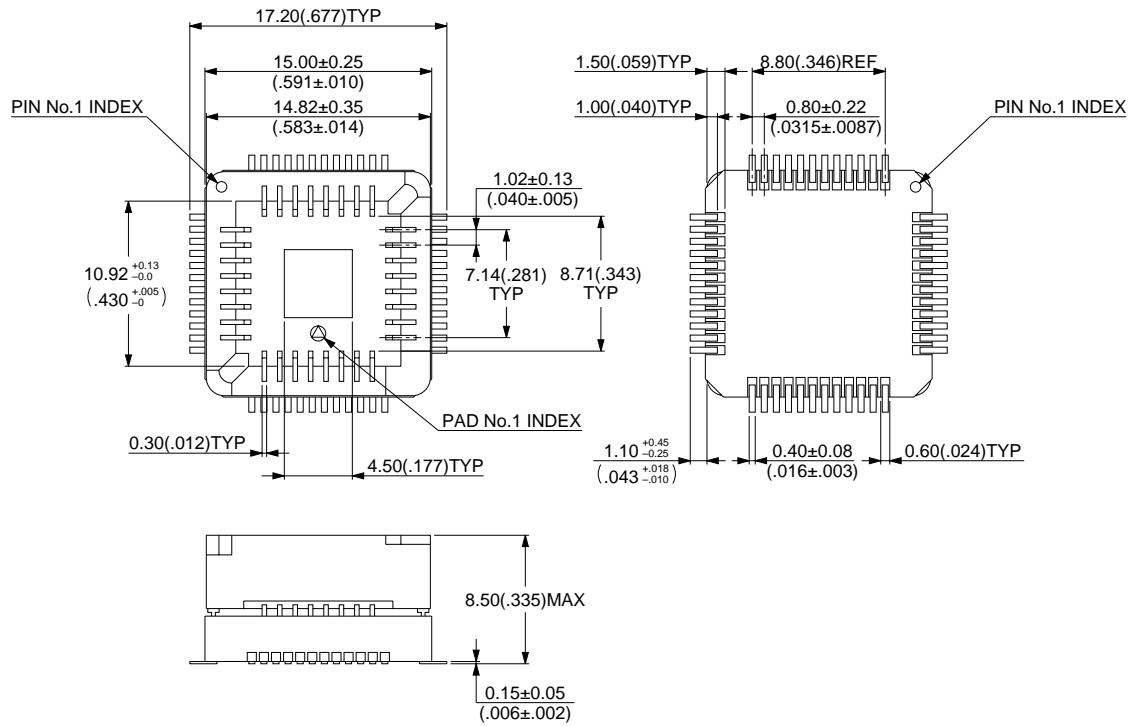
© 1994 FUJITSU LIMITED M48001SC-4-2

Dimensions in mm (inches).

Plastic LQFP, 64-pin
(FPT-64P-M09)

14.00±0.20(.551±.008)SQ

12.00±0.10(.472±.004)SQ

48

33

49

32

1 PIN INDEX

64

17

LEAD No. 1

16

0.65(.0256)TYP

0.30±0.10
(.012±.004)

⊕ 0.13(.005) Ⓜ

0.10(.004)

1.50 $^{+0.20}_{-0.10}$
(.059 $^{+.008}_{-.004}$) (Mounting height)

9.75
(.384)
REF

13.00
(.512)
NOM

"A"

0.127 $^{+0.05}_{-0.02}$
(.005 $^{+.002}_{-.001}$)

Details of "A" part

0.10±0.10
(.004±.004) (STAND OFF)

0.50±0.20
(.020±.008)

0 ～ 10°
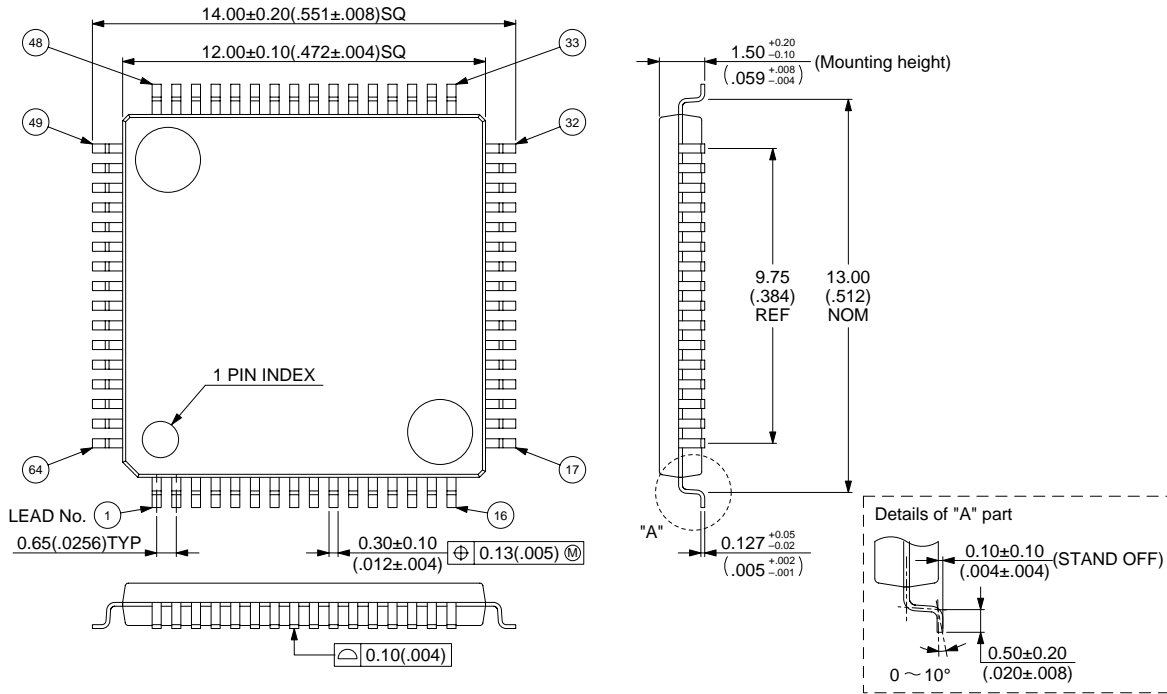
© 2000 FUJITSU LIMITED F64018S-1C-3

Dimensions in mm (inches).

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