

DESCRIPTION

The S3040 evaluation board provides a flexible platform for verifying the operation of AMCC OC-48 clock recovery units. This document provides information on the board contents and layout. It should be used in conjunction with the S3040 data sheet, which contains full technical details on the chips operation.

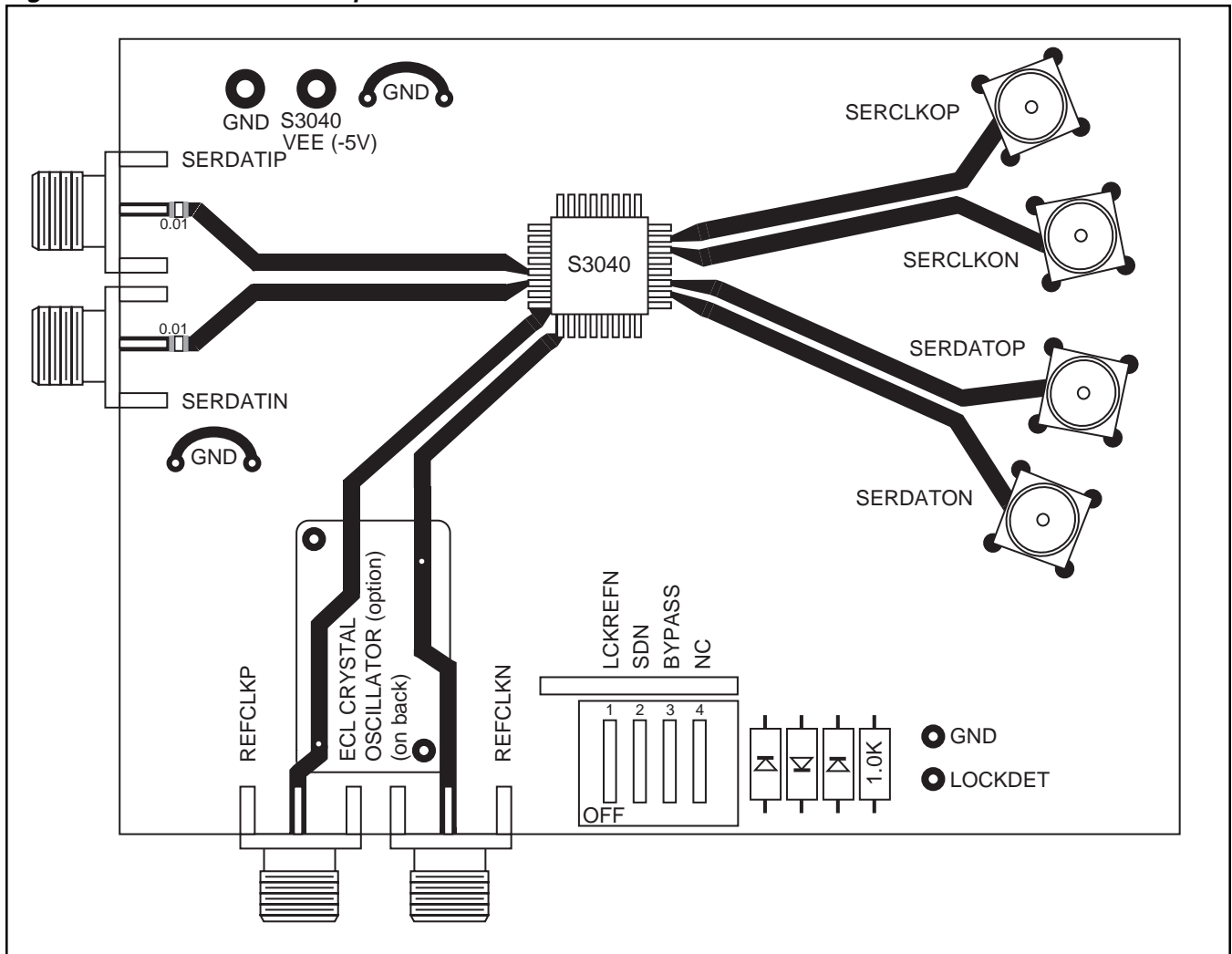
The S3040 evaluation board is factory configured with the S3040 device, and includes a test point to monitor the LOCKDET output. The board can be configured with either the on-board ECL crystal oscillator or with an external oscillator connected via the REFCLKP/N connectors.

ELECTRICAL CONNECTIONS

Power Connections

Terminal posts are provided at the top edge of the board allowing separate control of voltage levels for the S3040 itself. The serial input is terminated on the chip, and capacitive bypass to ground is provided on the board. For operation with standard test equipment, the board should be operated below ground, with the VEE supply at -5V DC.

Figure 1. Evaluation Board Top View



SET-UP FOR JITTER MEASUREMENT

Figure 2 depicts how the S3040 evaluation board can be connected for jitter measurements, and shows all of the DIP switch settings and power supply requirements. The connection from A to B will be used for the PK-PK jitter generation measurement on the Digital Sampling Oscilloscope (DSO). The connection from A to C will be used for the jitter transfer, jitter tolerance and jitter generation measurement on the transition analyzer.

Figure 2. Jitter Test Setup

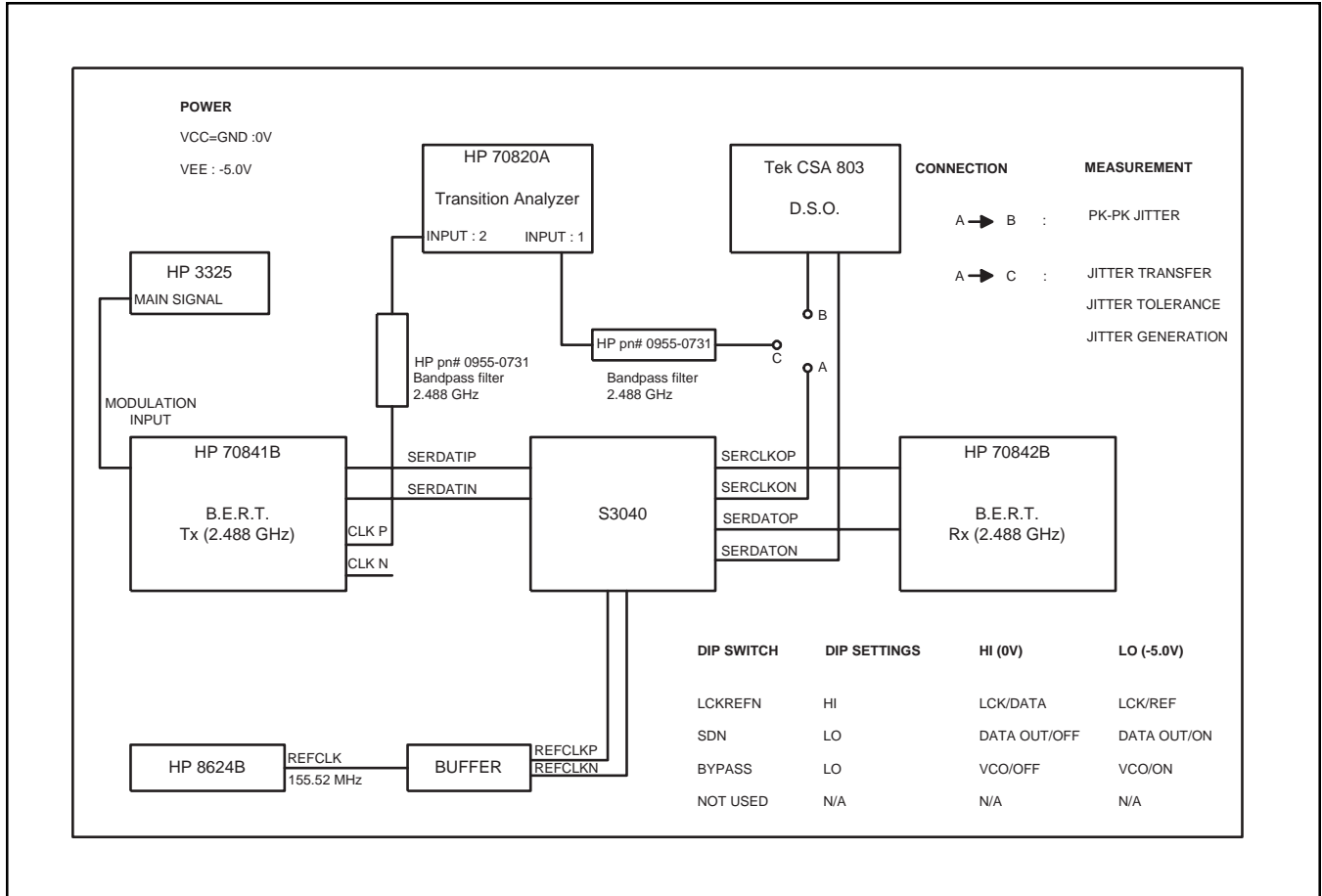


Table 1. Power Connections for DUT and Test Equipment Interface

Power Supply	Nominal Input Voltage	Type of Signal	CML Output Termination
DUT VCC DUT VEE	0V -5.0V	ECL	50 Ω to GND

SMA Connectors

SMA connectors are provided for the differential serial data input/output signals and output clock.

Serial Data In [SERDATIP/N] – PECL Differential inputs. Clock is recovered from the transition on these inputs.

Reference Clock [REFCLKP/N] – PECL Differential inputs. These inputs are used to establish the initial operating frequency of the clock recovery PLL and are also used as a standby clock in the absence of data. These inputs must be provided with a differential clock of 155.52 MHz.

Serial Data Out [SERDATOP/N] – CML outputs. This signal is the delayed version of the incoming data stream (SERDATI) updated on the falling edge of Serial Clock Out (SERCLKOP).

Serial Clock Output [SERCLKP/N] – CML outputs. This signal is phase aligned with Serial Data Out (SERDATOP).

Lock Detect [LOCKDET] – TTL output. Indicates that the Clock Recovery Unit (CRU) has locked onto the incoming data stream.

DIP Switches

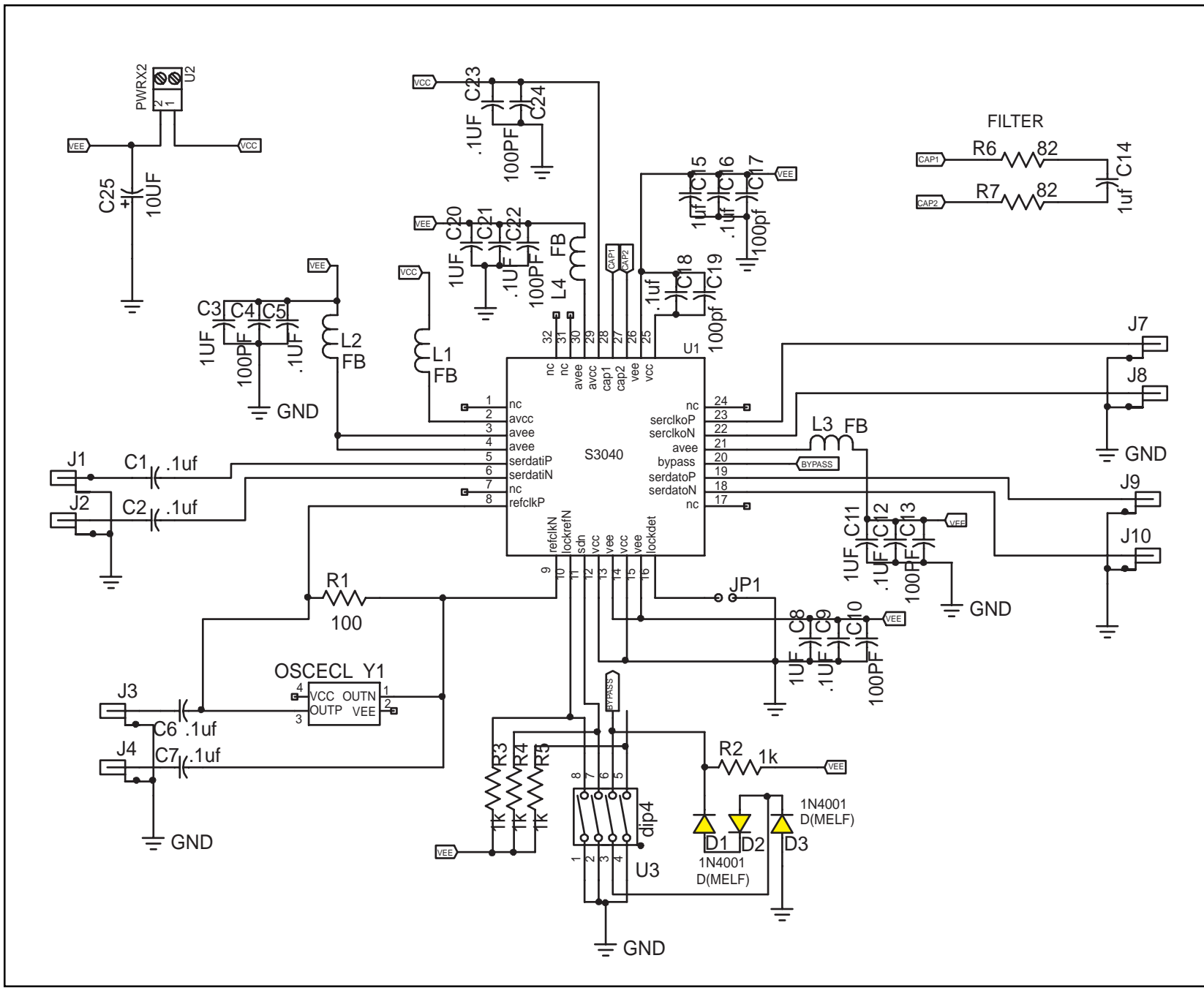
The evaluation board is equipped with a DIP switch to control the static control functions of the on-board device. For both arrays the OFF (open = “0”) condition of the DIP switch asserts a logic low on the assigned signal, and the ON (closed = “1”) condition asserts a logic high. Figure 2 shows the particular DIP switch settings that are needed for a particular test case.

Lock to Reference [LCKREFN] – Active Low. When active, the serial clock output will be forced to lock to the local reference clock input [REFCLK].

Signal Detect [SDN] – Active Low. Used to indicate a loss of received optical power.

Bypass Enable [BYPASS] – Active High. Used to bypass the VCO in the PLL.

Figure 3. EV3040 Evaluation Board Schematic



Ordering Information

PREFIX	DEVICE	PACKAGE
EV – Evaluation Board	3040	A – 32 TQFP

XX
Prefix

XXXX
Device

X
Package



Applied Micro Circuits Corporation • 6290 Sequence Dr., San Diego, CA 92121

Phone: (858) 450-9333 • (800) 755-2622 • Fax: (858) 450-9885

<http://www.amcc.com>

AMCC reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

AMCC does not assume any liability arising out of the application or use of any product or circuit described herein, neither does it convey any license under its patent rights nor the rights of others.

AMCC reserves the right to ship devices of higher grade in place of those of lower grade.

AMCC SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

AMCC is a registered trademark of Applied Micro Circuits Corporation.
Copyright © 1999 Applied Micro Circuits Corporation