10 /100Base-Tx/Fx Media Converter

Features

- A 10/100BASE-TX/ 100BASE-FX converter
- Built in a 10/100BASE-TX transceiver
- Built in a PHY for 100BASE-FX
- Built in a 2-port switch
  - Pass all packets without address and CRC check (optional)
  - Supports modified cut-through frame forwarding for low latency
  - Supports pure converter mode data forwarding for extreme low latency
  - Supports flow control for full and half duplex operation
  - Bandwidth control
  - Forward 1600 bytes packet for management
  - Optional forward fragments
- Built in 128Kb RAM for data buffer
- Supports auto MDI-MDIX function
- Supports link fault pass through function
- Supports far end fault function
- LED display for link/activity, full/half, 10/100
- Built in a watchdog timer to monitor internal switch error
- Supports EEPROM Configuration
- 0.25u CMOS technology
- Single 2.5V power supply
- 48-pin LQFP package

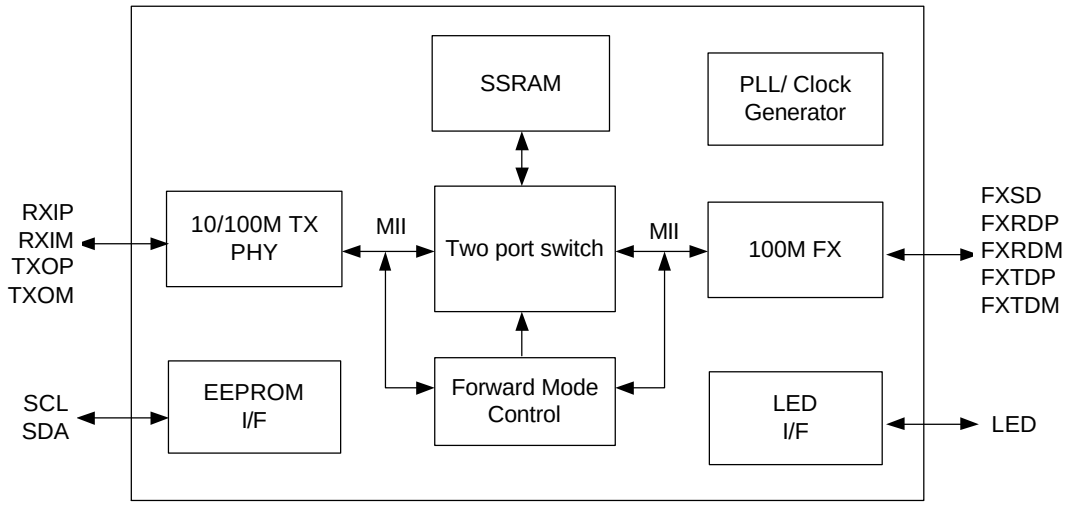
General Description

IP113A can be a 10/100BASE-TX to 100BASE-FX converter or a 100BASE-FX to 100BASE-FX repeater. It consists of a 2-port switch controller, a fast Ethernet transceiver and a PHY for 100BASE-FX. The transceivers in IP113A are designed in DSP approach with advance 0.25-um technology; this results in high noise immunity and robust performance.

IP113A not only supports store and forward mode, it also supports modified cut through mode and pure converter mode for low latency data forwarding. IP113A can transmit packet(s) up to 1600 bytes to meet requirement of extra long packets.

IP113A supports IEEE802.3x, collision base backpressure, and various LED functions, etc. These functions can be configured to fit the different requirements by feeding operation parameters via EEPROM interface or pull up/down resistors on specified pins.

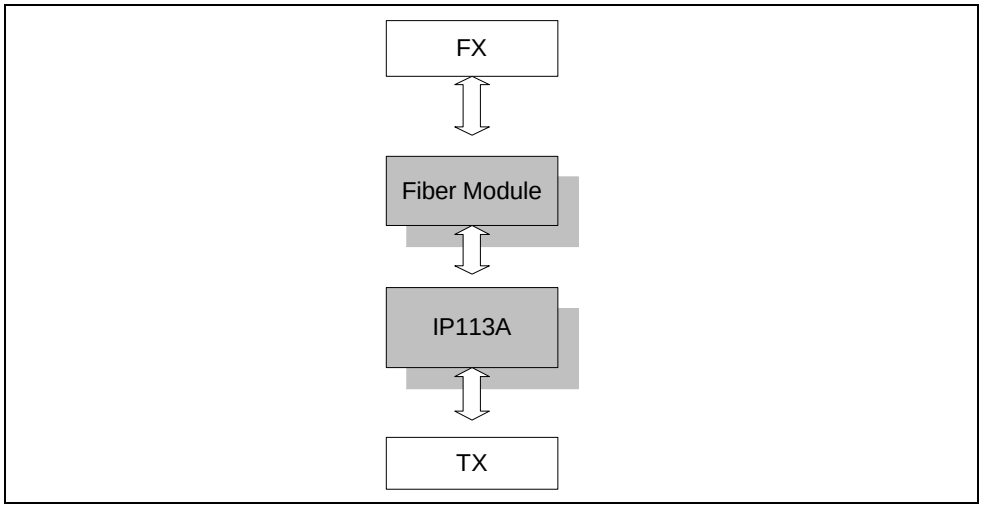
Block Diagram



Revision History

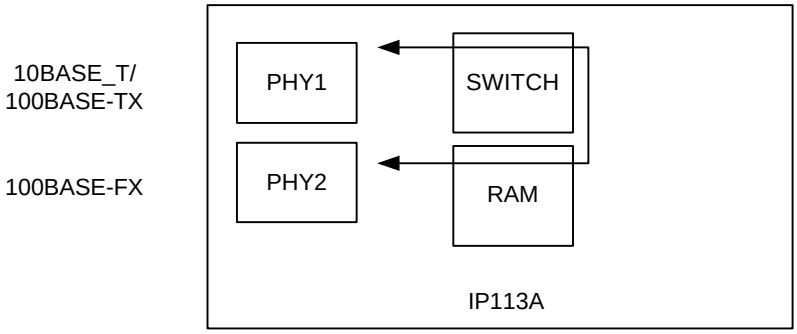
Revision #	Change Description
IP113A-DS-R01	Initial release.
IP113A-DS-R02	Remove Operation Junction Temperature
IP113A-DS-R03	TP port should be linked at 100M full duplex when working at this mode.

Application Diagram

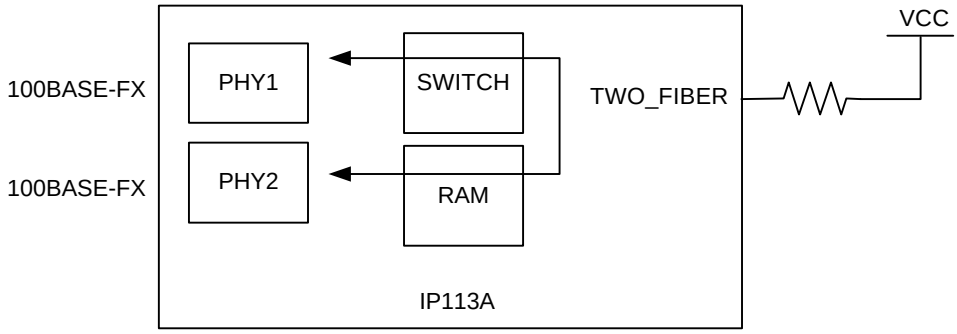


Applications

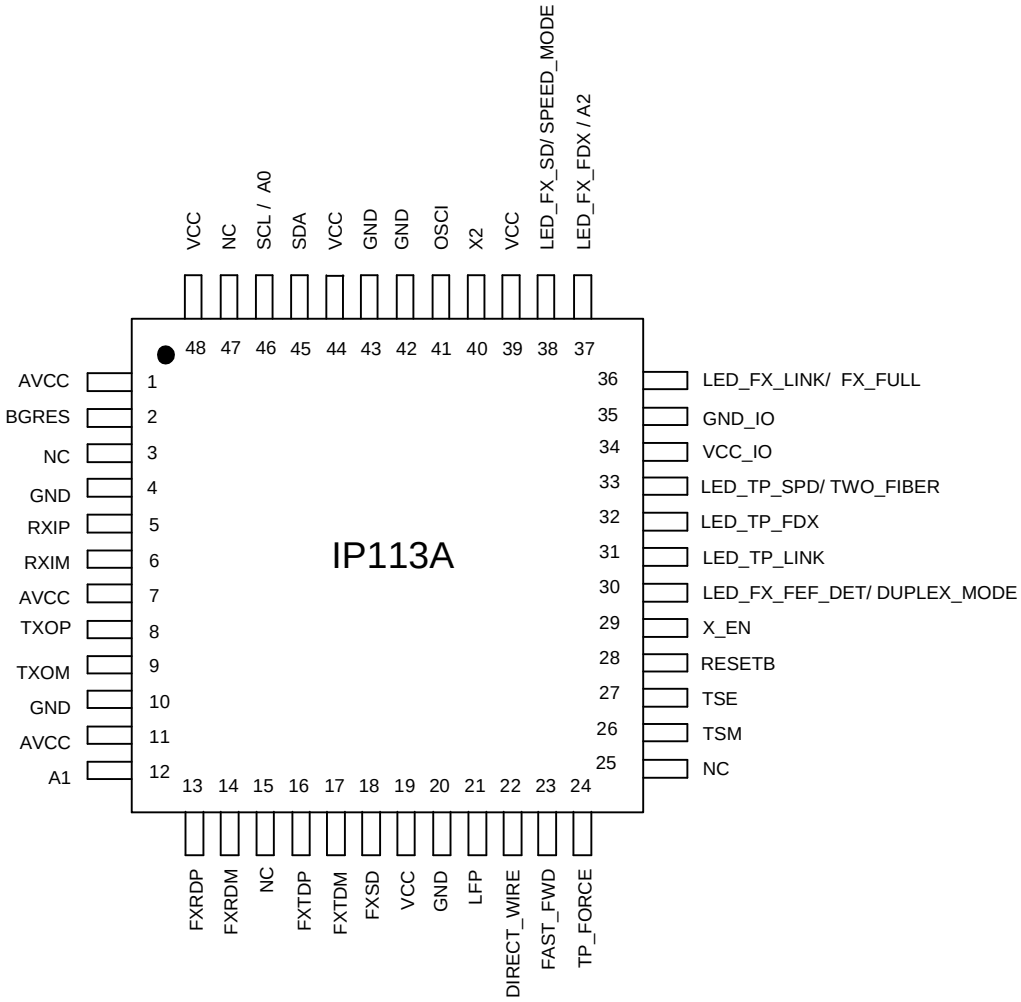
Un-managed converter



Fiber Repeater



PIN Diagram



1. PIN Description

Type	Description
I	Input pin
O	Output pin
IPL	Input pin with pull-hi resistor, pull-high resistance ˜ 160K?
IPH	Input pin with pull-low resistor, pull-low resistance ˜ 70K?

Pin no.	Label	Type	Description
Transceiver			
5, 6	RXIP, RXIM	I	**TP receive**
8, 9	TXOP, TXOM	O	**TP transmit**
2	BGRES	O	**Band gap resistor** It is connected to GND through a 6.19k (1%) resistor in application circuit.
18	FXSD	I	**100Base-FX signal detect** Fiber signal detect. It is an input signal from fiber MAU. Fiber signal detect is active if the voltage on FXSD is higher than the threshold voltage, which is 1.35v ±5% when VCC is equal to 2.5v.
13, 14	FXRDP, FXRDM	I	**Fiber receiver data pair**
16, 17	FXTDP, FXTDM	O	**Fiber transmit data pair**

1. PIN Description (continued)

Pin no.	Label	Type	Description
LED pins			
31	LED_TP_LINK	O	**TP port link LED** On: link ok, Off: link fail, Flash: link ok & activity (Flash: on for 20ms and off for 80ms)
33	LED_TP_SPD	O	**TP port speed LED** On: 100M, Off: 10M
32	LED_TP_FDX	O	**TP port full duplex LED** On: full, Off: half, Flash: half & collision happens (Flash: on for 20ms and off for 80ms)
36	LED_FX_LINK	O	**Fiber port link LED** On: link ok, Off: link fail, Flash: link ok & activity (Flash: on for 20ms and off for 80ms)
37	LED_FX_FDX	O	**Fiber port full duplex LED** On: full, Off: half, Flash: half & collision happens (Flash: on for 20ms and off for 80ms)
38	LED_FX_SD		**Fiber port signal detect** On: fiber signal detected, Off: fiber unplugged
30	LED_FX_FEF_DET	O	**Far end fault pattern received** For End Fault Patterns Receive LED On: 80ms, LED Off: 20ms For End Fault Pattern not Receive LED always Off

Note: The output of LED pin is logic low when the LED is on.

1. PIN Description (continued)

Pin no.	Label	Type	Description
MC operation mode			
29	X_EN	IPH	**IEEE 802.3X enable on TP port and fiber port** 1: enable (default), 0: disable
24	TP_FORCE	IPL	**Local TP port auto negotiation enable** 1: TP port supports auto-negotiation with limited capability defined in SPEED_MODE and DUPLEX_MODE. 0: TP port supports auto-negotiation with 10M/100M, full/ half capability (default) The default value may be updated by either programming EEPROM register 3.5 or MII register 20.13.
38	SPEED_MODE	IPH	**Local TP port speed** 1: TP port has the 100Mb speed ability 0: TP port has the 10Mb speed ability only It is valid only if TP_FORCE is enabled.
30	DUPLEX_MODE	IPH	**Local TP port duplex** 1: TP port has the Full duplex ability 0: TP port has the Half duplex ability only It is valid only if TP_FORCE is enabled.
36	FX_FULL	IPH	**Set the duplex of fiber port** 1: full duplex (default) 0: half duplex

1. PIN Description (continued)

Pin no.	Label	Type	Description
MC operation mode			
33	TWO_FIBER	IPL	**Two fiber ports** 1: IP113A supports two-fiber ports mode. Both port 1 and port 2 are fiber ports. RXIP and RXIM are used as FXRDP and FXRDM for the second fiber port. TXOP and TXOM are used as FXTDP and FXTDM for the second fiber port. A special requirement for the fiber MAU of port1 in this application is that the output of FXRDP and FXRDM should have no incoming signals when fiber wire is unplugged. For some fiber MAUs, there are amplified noisy signals on FXRDP and FXRDM when fiber is unplugged. These amplified noisy signals, which include coupled idle patterns from FXTDP and FXTDM will cause the LEDs of port1 malfunction Generally, a 3.3-V small form factor type fiber MAUs (e.g. Agilent HFBR-5903) can meet this special requirement, but 5-V duplex-SC and -ST type fiber MAUs cannot. Port2 is not limited by this special requirement. 0: IP113A supports one fiber port and one TP port. Port 1 is a TP port and port 2 is a fiber port.

1. PIN Description (continued)

<table>
<tr><th>Pin no.</th><th>Label</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">MC operation mode</td></tr>
<tr><td>21</td><td>LFP</td><td>IPL</td><td>Link fault pass through (LFP)
1: enable
Link status of one port is forwarded to the other port.
0: disable (default)</td></tr>
<tr><td>22,
23</td><td>DIRECT_WIRE,
FAST_FWD</td><td>IPL</td><td>
<table>
<tr><th>DIRECT_WIRE</th><th>FAST_FWD</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Store and forward switch mode (default)</td></tr>
<tr><td>0</td><td>1</td><td>Modified cut-through switch mode</td></tr>
<tr><td>1</td><td>0</td><td>Converter mode</td></tr>
<tr><td>1</td><td>1</td><td>Converter mode with auto-change-forward function</td></tr>
</table>
Store and forward switch mode:
IP113A will begin to transmit a frame right after the completion of receiving a frame.

Modified cut-through switch mode:
IP113A will begin to forward a frame after the first 64 bytes data received. TP port should be forced at 100M at this mode.

Converter mode:
Incoming frames are not buffered in IP113A to achieve the min latency. Both TP port and fiber port of IP113A should work at 100M full duplex in this mode. If TP port is linked at half duplex, the total length of UTP cable and fiber should be less than 60 meters to meet the requirement of CSMACD in IEEE802.3.

Converter mode with auto-change-forward function:
IP113A will change to forward mode if it detects the speed is different in TP port and FX port.

In converter mode, IP113A forwards IEEE802.3x pause frame directly. In the other modes, IP113A doesn't forward IEEE802.3x pause frame directly, it sends out pause frame when its internal buffer is full.</td></tr>
</table>

1. PIN Description (continued)

Pin no.	Label	Type	Description
EEPROM interface			
45, 46	SDA, SCL	IPH, O	**EEPROM interface**
37, 12, 46	A[2:0]	IPL	**PHY address** IP113A uses A[2:0] as EEPROM address to read EPROM.

Pin no.	Label	Type	Description
Misc.			
28	RESETB	I	**Reset** It is low active.
41, 40	OSCI, X2	I, O	**Crystal pins** OSCI and X2 are connected to a 25Mhz crystal. If a 25MHz oscillator is used, OSCI is connected to the oscillator's output and X2 should be left open.
26, 27	TSM, TSE	IPL	**Scan pins** These two pins should be left open or connected to ground for normal operation.

2. Functional Description

Data forwarding

IP113A supports three types of data forwarding mode, store & forward mode, modified cut-through mode and pure converter mode. It can forward a frame despite of its address and CRC error. IP113A begins to forward the received data only after it receives the frame completely. The latency depends on the packet length.

Modified cut-through mode

IP113A begins to forward the received data when it receives the first 64 bytes of the frame. The latency is about 512 bits time width. The maximum packet length can be up to1600 bytes in this mode. Please refer to the pin description of FAST_FWD for configuration information.

Pure converter mode

IP113A operates with the minimum latency in this mode. The transmission flow does not wait until entire frame is ready, but instead it forwards the received data immediately after the data being received. Both transceivers are interconnected via internal MII signals, therefore the internal switch engine and data buffer are not used. Both TP port and fiber port of IP113A should work at 100M full duplex in this mode. If TP port is linked at half duplex, the total length of UTP cable and fiber should be less than 60 meters to meet the requirement of CSMACD in IEEE802.3.The packet length is not limited at this mode. Please see pin description of DIRECT_WIRE for configuration information.

Fragment forwarding

IP113A forwards CRC error packets but it will filter fragments when it works in modified cut-through mode. IP113A forwards fragments if user turns on bit 3 of EEPROM register 2.

TP port force mode

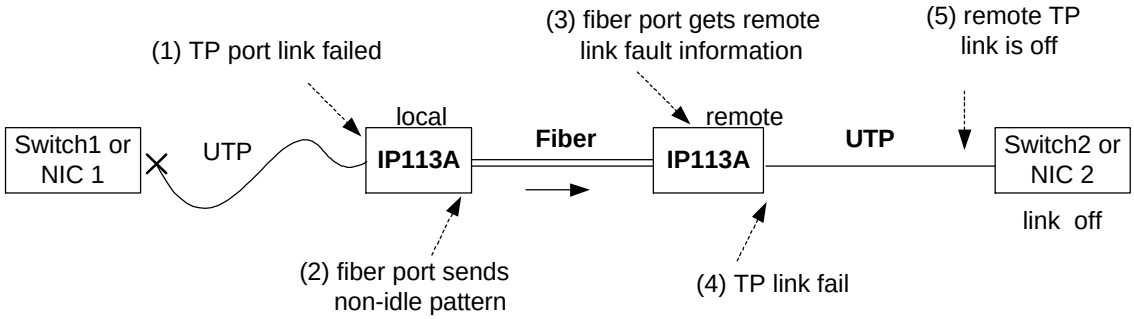
The TP port of IP113A can work at auto mode or force mode. The following table shows all of the combination of its TP port.

		Link partner's capability							
		AN on				AN off			
{TP_FORCE, SPEED_MODE, DUPLEX_MODE}	IP113A's link result / IP113A's capability	100F	100H	10F	10H	100F	100H	10F	10H
011	100/10M, Full/Half, AN on	100F	100H	10F	10H	100H	100H	10H	10H
010	100/10M, Half, AN on	X	100H	X	10H	100H	100H	10H	10H
001	10M, Full/Half, AN on	X	X	10F	10H	100H	100H	10H	10H
000	10M, Half, AN on	X	X	X	10H	100H	100H	10H	10H
111	100M, Full, AN on	100F	X	X	X	100F	100F	X	X
110	100M, Half, AN on	X	100H	X	X	100H	100H	X	X
101	10M, Full, AN on	X	X	10F	X	X	X	10F	10F
100	10M, Half, AN on	X	X	X	10H	X	X	10H	10H

Note:
AN on: with auto-negotiation capability
AN off: without auto-negotiation capability
100F: 100M full duplex
100H: 100M half duplex
10F: 10M full duplex
10H: 10M half duplex

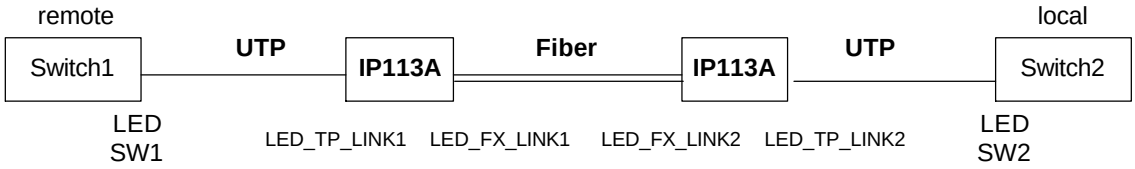
Link fault pass through

When link fault pass through function is enabled, link status on TX port will inform the FX port of the same device and vice versa. From the link fault pass through procedure illustrates in the figure below, if link fail happens on IP113A's TX port (1), the local FX port sends non-idle pattern to notice the remote FX port (2). The remote FX port then forces its TX port to link failed after receiving the non-idle pattern (4). In other words, this mechanism will alert the link fault status of local TX port to the remote converter's TX port, and the link status of the remote TX port will become off. Link status LED will also be off for both IP113A and its link partner.



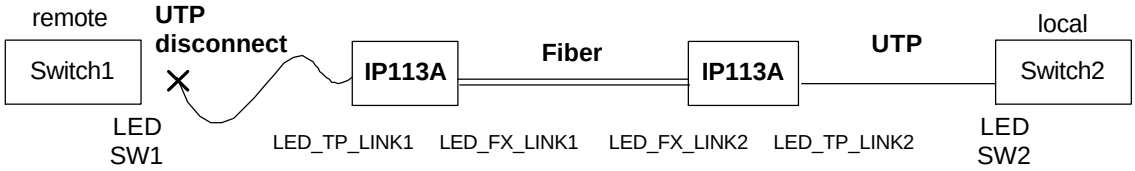
The procedure of link fault pass through

Normal case



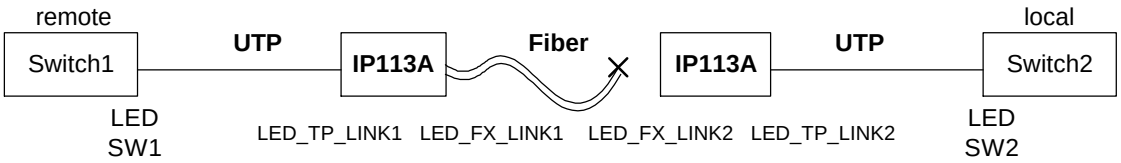
Link LED on SW1	LED_TP_LINK1	LED_FX_LINK1	LED_FX_LINK2	LED_TP_LINK2	Link LED on SW2
ON	ON	ON	ON	ON	ON

Remote TP port disconnected



Link LED on SW1	LED_TP_LINK1	LED_FX_LINK1	LED_FX_LINK2	LED_TP_LINK2	Link LED on SW2
Off	Off	Off	Off	Off	Off

FX port disconnected



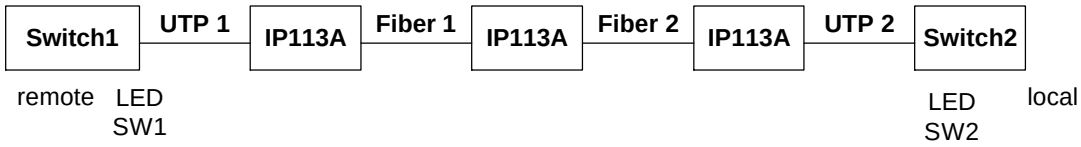
Link LED on SW1	LED_TP_LINK1	LED_FX_LINK1	LED_FX_LINK2	LED_TP_LINK2	Link LED on SW2
Off	Off	Off	Off	Off	Off

LED diagnostic functions for fault indication

LED_TP_LINK	LED_FX_LINK	LED_FX_SD	LED_FX_FEF_DET	Status
On	On	On	Off	Link ok
Flash	Flash	On	Off	Link ok & activity
Off	Off	On	Off	Remote TP link off
Off	Off	Off	Off	Fiber RX off, Fiber TX/ RX off
Off	Off	On	Flash	Fiber TX off

Note
Flash: flash, period 100 ms
Link fault pass through is enabled.

Link fault pass through in FX to FX application

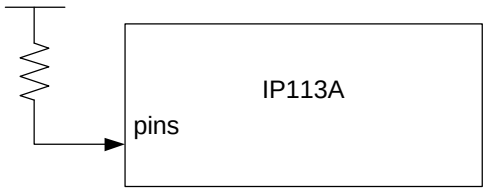


LED SW1 and LED SW2 are both off, if either UTP1, Fiber1, Fiber2 or UTP2 is broken and link fault pass through is enabled. That is, if link status is ok on switch port then all segments are guaranteed link good.

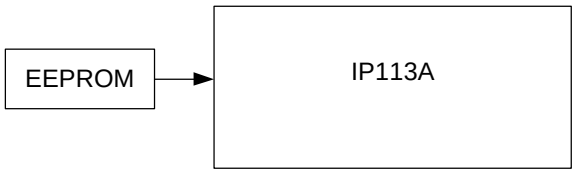
EEPROM – store the initial value

IP113A supports two ways to load initial value of MII registers. The procedure is illustrated as below.

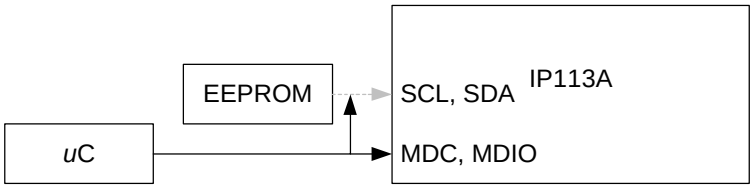
1. IP113A reads the default setting of MII register from pins



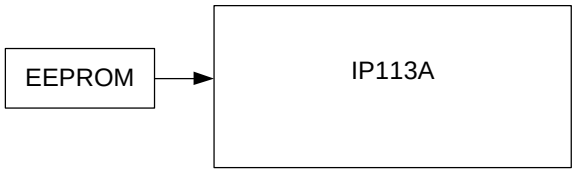
2. IP113A updates the default setting of MII by reading EEPROM. If there exists an EEPROM.



3. After reading EEPROM, IP113A is virtually isolated from the EEPROM. Micro-controller can program both MII register and EEPROM.

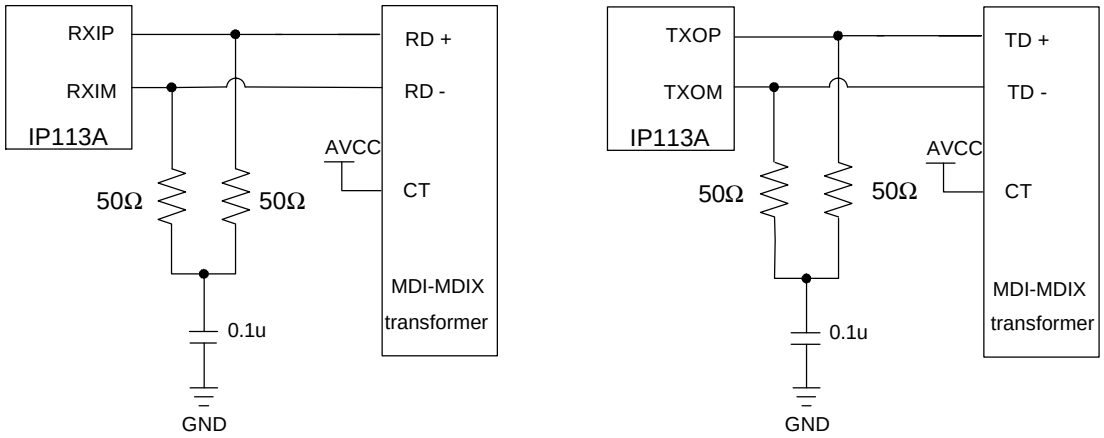


4. IP113A reloads the content of EEPROM to recover the value in MII registers programmed by Micro-controller after power on reset.



Auto MDI_MDIX

IP113A supports auto MDI-MDIX. It is always enabled. The following is its application circuit for auto MDI-MDIX.



IP113A's application circuit (auto MDI-MDIX on)

EEPROM registers

Type	Description
R/W	Read/Write
SC	Self-Clearing
RO	Read Only
Pin(1)	The default value is “1” and it depends on the setting of its corresponding pin.

Type	Description
RC	Read and Clear
LL	Latching Low
LH	Latching High
Pin(0)	The default value is “0” and it depends on the setting of its corresponding pin.

ROM	NAME	R/W	DESCRIPTION	DEFAULT
EEPROM enable register 0				
0[7:0]		--	**EEPROM enable register 0** This register should be filled with 55. IP113A will examine the specified pattern to confirm if there is a valid EEPROM.	55h

ROM	NAME	R/W	DESCRIPTION	DEFAULT
EEPROM enable register 1				
1[7:0]		--	**EEPROM enable register 1** This register should be filled with AA. IP113A will examine the specified pattern to confirm if there is a valid EEPROM. The initial setting is updated with the content of EEPROM only if the specified pattern 55AA is found.	AAh

EEPROM registers (continued)

ROM	NAME	R/W	DESCRIPTION	DEFAULT
Switch configuration register 1				
2.0	reserved	--	The default value must be adopted for normal operation.	0
2.1	direct_wire	--	Please see pin description of DIRECT_WIRE for more detail information.	Pin (0)
2.2	fast_fwd	--	Please see pin description of FAST_FWD for more detail information.	Pin (0)
2.3	mg_pass_fragment _en	--	Pass fragment packet (>7B and <64B) 1: pass fragment 0: not pass fragment	0
2.4	mg_col16_drop_en	--	Collision 16 times drop enable 1: drop 0: not drop	0
2.5	mg_col_backoff _en	--	Collision back-off enable 1: back after collision 0: not back off after collision	1
2.6	reserved	--	The default value must be adopted for normal operation.	0
2.7	p01_mg_backpress_en	--	TP port backpressure control enable for half duplex 1: backpressure enable 0: backpressure disable	1
3.0	reserved	--	The default value must be adopted for normal operation.	0
3.1	reserved	--	The default value must be adopted for normal operation.	0
3.2	reserved	--	The default value must be adopted for normal operation.	1
3.3	reserved	--	The default value must be adopted for normal operation.	1
3.4	mg_em_bist_en	--	SSRAM BIST enable (R/W by EEPROM only) 1: BIST enable 0: bypass BIST	1
3.5	tp_force	--	This pin overwrites the setting on pin 26 TP_FORCE.	Pin (0)
3.6	mg_receive_en	--	TP receive enable 1: TP port can receive packet 0: TP port drop all received packet	1
3.7	reserved	--	The default value must be adopted for normal operation.	0

ROM	NAME	R/W	DESCRIPTION	DEFAULT
Switch configuration register 2				
4[7:0]	p01_mg_port_page_no	--	TP port allocated memory pages The default is 120 pages with 64 bytes per page.	120d
5[7:0]	p02_mg_port_page_no	--	FX port allocated memory pages The default is 120 pages with 64 bytes per page.	120d

Note: p01_mg_port_page_no adds p02_mg_port_page_no must be equal to 240.

EEPROM registers (continued)

ROM	NAME	R/W	DESCRIPTION	DEFAULT
Local MC extended register				
6.0	reserved	--	The default value must be adopted for normal operation.	0
6.1	reserved	--	The default value must be adopted for normal operation.	0
6.2	p01_mg_auto_neg_en	--	TP port auto-negotiation enable 1: TP auto-negotiation enable 0: TP auto-negotiation disable	1
6.3	p01_mg_speed_mode	--	TP port speed selection 1: 100M, 0:10M	1
6.4	p01_mg_duplex_mode	--	TP port duplex mode selection 1: full duplex, 0:half duplex	1
6.5	p01_mg_flow_ctrl_en	--	TP port flow control selection 1: on, 0:off	1
6.6	reserved	--	The default value must be adopted for normal operation.	0
6.7	p02_mg_flow_ctrl_en	--	Fiber port flow control/backpressure enable 1: enable, 0: disable	Pin (1)
7.0	p02_mg_duplex_mode	--	Fiber port duplex mode (FX_FULL) 1: full duplex, 0:half duplex	1
7.1	reserved	--	The default value must be adopted for normal operation.	1
7.2	reserved	--	The default value must be adopted for normal operation.	0
7[4:3]	p01_mg_throttle_confg	--	TP port input Rate Control 2'b00: full speed 2'b01: 1/4 speed 2'b10: 2/4 speed 2'b11: 3/4 speed	00
7[6:5]	p01_mg_throttle_confg	--	TP port output Rate Control 2'b00: full speed 2'b01: 1/4 speed 2'b10: 2/4 speed 2'b11: 3/4 speed	00
7.7	mg_link_pass_en	--	Link Fault Pass through enable (LFP) 1: enable, 0: disable	1

3. Signal Requirements

Absolute Maximum Rating

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

Supply Voltage	–0.3V to Vcc+0.3V
Input Voltage	–0.3V to Vcc+0.3V
Output Voltage	–0.3V to Vcc+0.3V
Storage Temperature	-55°C to 125°C
Ambient Operating Temperature (Ta)	0°C to 70°C

DC Characteristic

Operating Conditions

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC	2.375	2.5	2.625	V	
Power Consumption			0.475		W	VCC=2.5v

Input Clock

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Frequency			25		MHz	
Frequency Tolerance		-100		+100	PPM	

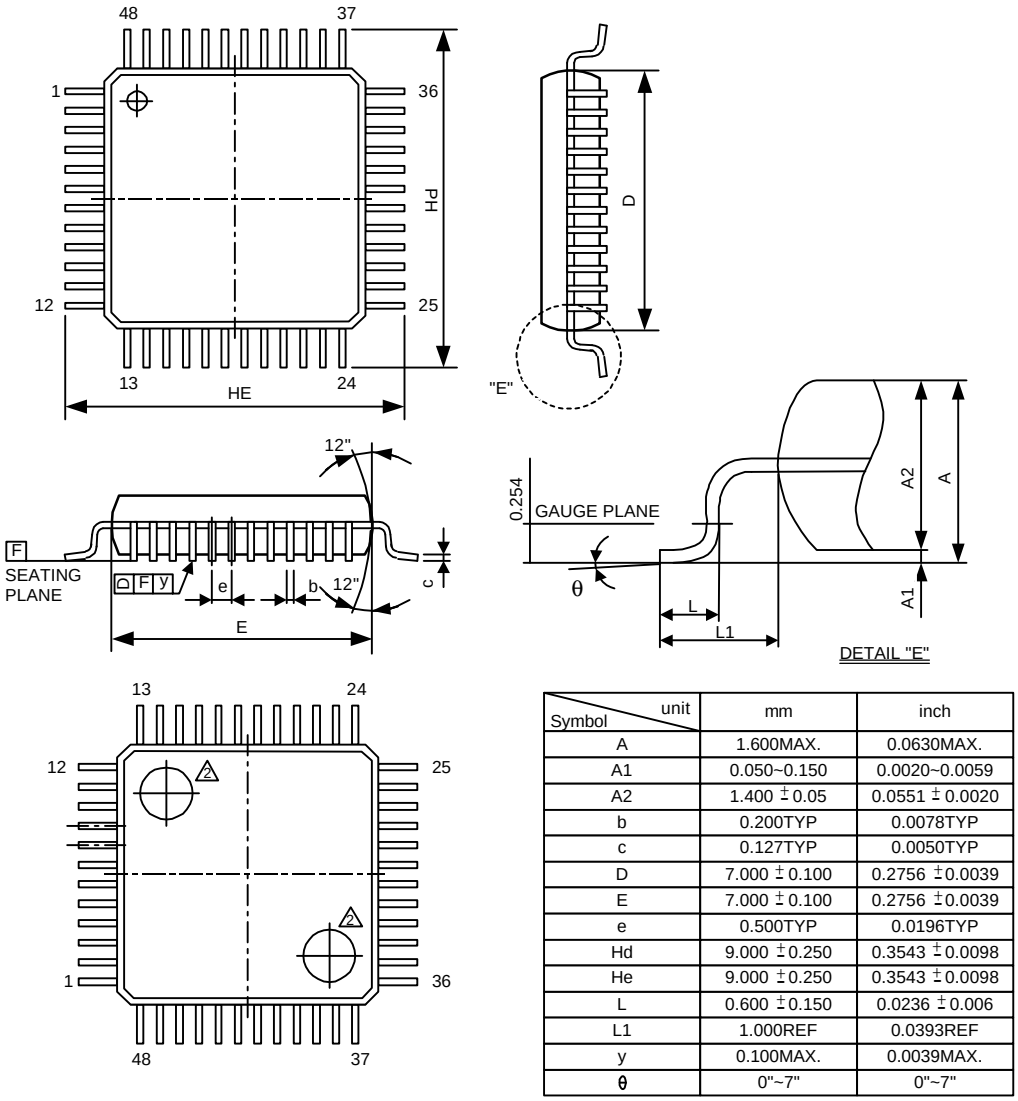
I/O Electrical Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOH=4mA
Output High Voltage	VOH	VCC_IO-0.4			V	IOL=4mA

4. Order Information

Part No.	Package	Notice
IP113A	48-PIN LQFP	-

5. Package Detail



Symbol \ unit	mm	inch
A	1.600MAX.	0.0630MAX.
A1	0.050~0.150	0.0020~0.0059
A2	1.400 ± 0.05	0.0551 ± 0.0020
b	0.200TYP	0.0078TYP
c	0.127TYP	0.0050TYP
D	7.000 ± 0.100	0.2756 ± 0.0039
E	7.000 ± 0.100	0.2756 ± 0.0039
e	0.500TYP	0.0196TYP
Hd	9.000 ± 0.250	0.3543 ± 0.0098
He	9.000 ± 0.250	0.3543 ± 0.0098
L	0.600 ± 0.150	0.0236 ± 0.006
L1	1.000REF	0.0393REF
y	0.100MAX.	0.0039MAX.
θ	0"~7"	0"~7"

Notes:
1. DIMENSION D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSION.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION / INTRUSION.
3. MAX. END FLASH IS 0.15MM.
4. MAX. DAMBAR PROTRUSION IS 0.13MM.
GENERAL APPEARANCE SPEC SHOULD BE BASED ON FINAL VISUAL INSPECTION SPEC.

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