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Integrated 10/100/1000 Gigabit Ethernet Transceiver

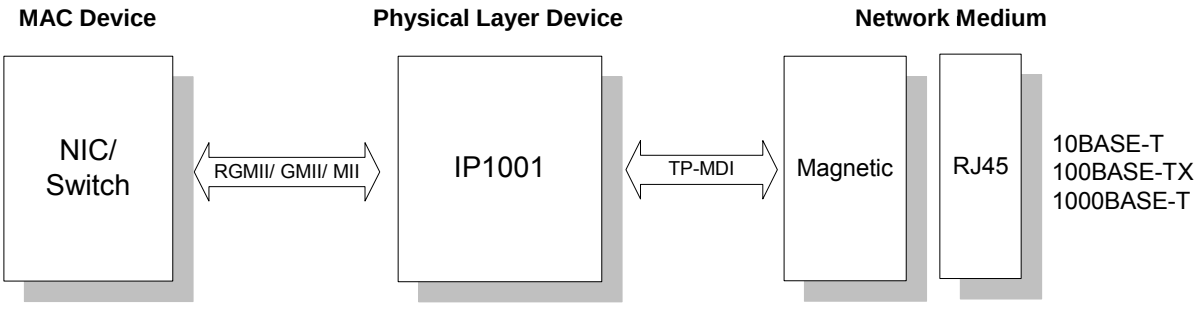
Features

- IEEE 802.3 compliant 1000BASE-T, 100BASE-TX, and 10BASE-T
- Support auto-negotiation
- Support timing programmable MII/ GMII/ RGMII (delay clock, and driving current etc.)
- Support 3 power saving modes
- Support software based Smart Cable Analyzer (SCA)
- Support auto MDI/MDIX (auto negotiation or force mode)
- Support auto polarity correction
- Supports programmable LED modes and LED driving current
- Supports speed down shift feature
- Built in synchronization FIFO to support jumbo frame size up to 10KB in giga mode (4KB in 10M/100M mode)
- Supports 2.1v and 1.2v built-in regulator control
- Provide a 125MHz free running clock
- Operating voltage 3.3v/ (2.5v option for RGMII)/ 1.8v/ 1.2v
- 64-pin QFN lead-free package
- Supports Lead Free package (Please refer to the Order Information)

General Description

IP1001 is an integrated physical layer device for 1000BASE-T, 100BASE-TX, and 10BASE-T applications. IP1001 supports MII, GMII and RGMII for different types of 10/100/1000Mb Media Access Controller (MAC). It supports Auto MDI/MDIX function to simplify the network installation and reduce the system maintenance cost. IP1001 supports speed down shift feature for a poor link quality to guarantee data transmission. Cable analysis function “SCA” is supported by programming MII registers of IP1001 through MDC/MDIO.

IP1001 supports 2 types of power saving modes; i.e., power down mode defined in IEEE802.3, and APS (auto power saving).



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Revision History

Revision #	Change Description
IP1001-DS-R01	Initial release.
IP1001-DS-R02	Assign pin number to power pins. Modify CAP pin description. Modify package dimension.
IP1001-DS-R03	Modify features description. Modify the pin desecration for X1. Change the part number to “IP1001 LF”. Modify the LED pins description. Modify the RGMII/GMII driving current. Modify the operating temperature range. Modify RGMII/GMII timing.
IP1001-DS-R04	Modify LED mode description of pin 55. Modify DC characteristics. Add thermal parameters.
IP1001-DS-R05	Correct an editing error found on Page 4.
IP1001-DS-R06	Modify Maximum voltage of AVDD to 2.2V on Page 42 DC. Characteristic.

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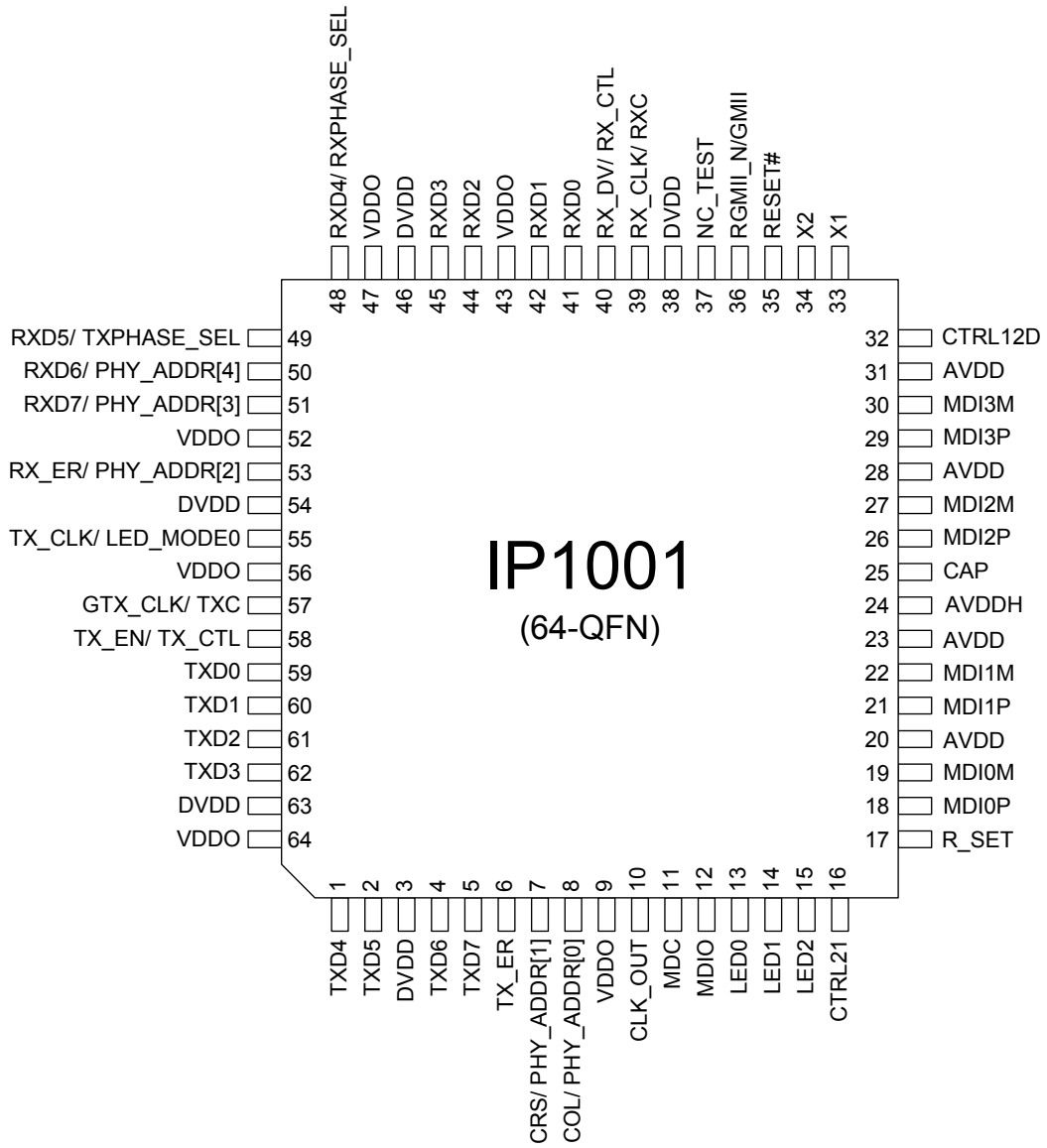
1 Pin diagram



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2 Pin description

Abbreviation

Abbreviation	Description
PWR	Power and Ground Pin
I	Schmitt trigger input
LI	The input is latched at the end of reset and used as a default value
O	Output
I/O	Schmitt trigger input/ Output
OD	Open drain output
IPH	Schmitt trigger input with 60 kohm internal pull high
IPL	Schmitt trigger input with 60 kohm internal pull low
IPECL	PECL input
OPECL	PECL output

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Pin description (continued)

Pin no.	Label	Type	Description
Configuration			
50,51,53,7,8	PHY_ADDR[4:0]	LI/O, IPH	PHY Address Configuration These pins are latched upon power-on reset to define the PHY address of IP1001. PHY_ADDR[1:0] are internally pulled high. PHY_ADDR[4:0] share the same pins with RXD6, RXD7, RX_ER, CRS and COL.
36	RGMII_N/GMII	IPL	GMII (MII)/ RGMII MAC Interface Mode Selection This pin is latched upon power-on reset to define the RGMII/GMII interface mode. 0: RGMII mode (default) 1: GMII/MII mode
48	RXPHASE_SEL	LI/O	RX_CLK Phase Selection This pin is latched upon power-on reset, and acts as the initial value of register16 [0] to adjust timing of RX_CLK. 0: No output delay is added on RX_CLK 1: An output delay is added on RX_CLK (with respect to RXD, about 2ns delay in 1000BASE-T, and about 4ns delay in 100BASE-TX and 10BASE-T). RXPHASE_SEL shares the same pin with RXD4.
49	TXPHASE_SEL	LI/O	GTX_CLK/TXC Phase Selection This pin is latched upon power-on reset, and acts as the initial value of register16 [1] to adjust timing of GTX_CLK/TXC. 0: No input delay is added on GTX_CLK/TXC 1: An input delay is added on GTX_CLK/TXC (with respect to TXD, about 2ns delay in 1000BASE-T, and about 4ns delay in 100BASE-TX and 10BASE-T). TXPHASE_SEL shares the same pin with RXD5.

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Pin description (continued)

<table>
<tr><th>Pin no.</th><th colspan="3">Label</th><th>Type</th><th>Description</th></tr>
<tr><td></td><td colspan="3">MAC Interface</td><td></td><td></td></tr>
<tr><td></td><td>GMII</td><td>RGMII</td><td>MII</td><td></td><td></td></tr>
<tr><td>57</td><td>GTX_CLK</td><td>TXC</td><td>--</td><td>I</td><td>GMII/RGMII Transmit Clock
<table>
<tr><th>I/F</th><th>MDI speed</th><th>Description</th></tr>
<tr><td rowspan="2">GMII Mode</td><td>Gigabit</td><td>125Mhz input.
IP1001 utilizes this clock to sample TXD[7:0], TX_ER and TX_EN at the rising edge.</td></tr>
<tr><td>10/100Mbps</td><td>Not used.</td></tr>
<tr><td rowspan="3">RGMII Mode</td><td>Gigabit</td><td>125Mhz input.
IP1001 utilizes this clock to sample TXD[3:0] and TX_CTL at both the rising edge and falling edge of GTX_CLK.</td></tr>
<tr><td>100Mbps</td><td>25Mhz input.
IP1001 utilizes this clock to sample TXD[3:0] and TX_CTL at both the rising edge and falling edge.</td></tr>
<tr><td>10Mbps</td><td>2.5Mhz input.
IP1001 utilizes this clock to sample TXD[3:0] and TX_CTL at both the rising edge and falling edge.</td></tr>
</table></td></tr>
<tr><td>55</td><td>--</td><td>--</td><td>TX_CLK</td><td>O</td><td>MII Transmit Clock
<table>
<tr><th>I/F</th><th>MDI speed</th><th>Description</th></tr>
<tr><td rowspan="3">GMII Mode</td><td>Gigabit</td><td>Not used.</td></tr>
<tr><td>100Mbps</td><td>25Mhz output.
IP1001 uses the clock to sample TX_EN, TX_ER, and TXD[3:0].</td></tr>
<tr><td>10Mbps</td><td>2.5Mhz output.
IP1001 uses the clock to sample TX_EN, TX_ER, and TXD[3:0].</td></tr>
<tr><td rowspan="3">RGMII Mode</td><td>Gigabit</td><td rowspan="3">Not used.
This pin should be left open for normal operation.</td></tr>
<tr><td>100Mbps</td></tr>
<tr><td>10Mbps</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>Pin no.</th><th colspan="3">Label</th><th>Type</th><th>Description</th></tr>
<tr><td></td><td colspan="3">MAC Interface</td><td></td><td></td></tr>
<tr><td></td><td>GMII</td><td>RGMII</td><td>MII</td><td></td><td></td></tr>
<tr><td>58</td><td>TX_EN</td><td>TX_CTL</td><td>TX_EN</td><td>I</td><td>GMII and MII Transmit Enable/ RGMII Transmit Control
<table>
<tr><th>I/F</th><th>MDI speed</th><th>Description</th></tr>
<tr><td>GMII Mode</td><td>Gigabit, 100Mbps, 10Mbps</td><td>Indicates the valid data is present on the data bus of TXD. Synchronous to the rising edge of GTX_CLK (Gigabit) or TXC_CLK (10/100M).</td></tr>
<tr><td>RGMII Mode</td><td>Gigabit, 100Mbps, 10Mbps</td><td>The TX_CTL indicates a signal like TX_EN at the rising edge of TXC. A signal like TX_ER is derived by the logical operation of latched “TX_EN” and the value at the falling edge of TXC.</td></tr>
</table></td></tr>
<tr><td>5,4,2,1</td><td>TXD[7:4]</td><td>--</td><td>--</td><td>I</td><td>GMII Transmit Data (high nibble)
Please see the pin description of pin 57.</td></tr>
<tr><td>62,61,60,59</td><td>TXD[3:0]</td><td>TXD[3:0]</td><td>TXD[3:0]</td><td>I</td><td>GMII/RGMII/MII Transmit Data
Please see the pin description of pin 57.</td></tr>
<tr><td>6</td><td>TX_ER</td><td>--</td><td>TX_ER</td><td>I</td><td>GMII and MII Transmit Error
<table>
<tr><th>I/F</th><th>MDI speed</th><th>Description</th></tr>
<tr><td rowspan="2">GMII Mode</td><td>Gigabit</td><td>A “high” state present on this pin indicates transmit data error or carrier extension. It is synchronous to GTX_CLK</td></tr>
<tr><td>100Mbps, 10Mbps</td><td>A “high” state present on this pin indicates transmit data error. It is synchronous to TX_CLK</td></tr>
<tr><td>RGMII Mode</td><td>Gigabit, 100Mbps, 10Mbps</td><td>Not used.</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>Pin no.</th><th colspan="3">Label</th><th>Type</th><th>Description</th></tr>
<tr><td></td><td colspan="3">MAC Interface</td><td></td><td></td></tr>
<tr><td></td><td>GMII</td><td>RGMII</td><td>MII</td><td></td><td></td></tr>
<tr><td>39</td><td>RX_CLK</td><td>RXC</td><td>RX_CLK</td><td>O</td><td>GMII/ RGMII Receive Clock.
<table>
<tr><th>I/F</th><th>MDI speed</th><th>Description</th></tr>
<tr><td rowspan="3">GMII Mode</td><td>Gigabit</td><td>125Mhz output.
IP1001 sends out RXD[7:0], RXDV and RX_ER at the rising edge of RX_CLK.</td></tr>
<tr><td>100Mbps</td><td>25Mhz output.
IP1001 sends out RXD[3:0], RXDV and RX_ER at the rising edge of RX_CLK.</td></tr>
<tr><td>10Mbps</td><td>2.5Mhz output.
IP1001 sends out RXD[3:0], RXDV and RX_ER at the rising edge of RX_CLK.</td></tr>
<tr><td rowspan="3">RGMII Mode</td><td>Gigabit</td><td>125Mhz output.
IP1001 sends out RXD[3:0] and RX_CTL at both the rising edge and falling edge of RXC.</td></tr>
<tr><td>100Mbps</td><td>25Mhz output.
IP1001 sends out RXD[3:0] and RX_CTL at both the rising edge and falling edge of RXC.</td></tr>
<tr><td>10Mbps</td><td>2.5Mhz output.
IP1001 sends out RXD[3:0] and RX_CTL at both the rising edge and falling edge of RXC.</td></tr>
</table></td></tr>
<tr><td>40</td><td>RX_DV</td><td>RX_CTL</td><td>RX_DV</td><td>O</td><td>GMII and MII Receive Enable/ RGMII Receive Control
<table>
<tr><th>I/F</th><th>MDI speed</th><th>Description</th></tr>
<tr><td>GMII Mode</td><td>Gigabit
100Mbps
10Mbps</td><td>RX_DV indicates the valid data is present on the data bus of RXD. Synchronous to the rising edge of RX_CLK.</td></tr>
<tr><td rowspan="3">RGMII Mode</td><td>Gigabit</td><td rowspan="3">RX_CTL indicates a signal like RX_DV at the rising edge of TXC. A signal like RX_ER is derived by the logical operation of latched RX_DV and the value at the falling edge of RX_CLK</td></tr>
<tr><td>100Mbps</td></tr>
<tr><td>10Mbps</td></tr>
</table></td></tr>
<tr><td>51,50,49,48</td><td>RXD[7:4]</td><td>--</td><td>--</td><td>O</td><td>GMII Receive Data (high nibble)
Please see the pin description of pin 39.
RXD[7:4] share the same pins with PHY_ADDR[3:4], TXPHASE_SEL, and RXPHASE_SEL.</td></tr>
</table>

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<table>
<tr><th>Pin no.</th><th colspan="3">Label</th><th>Type</th><th>Description</th></tr>
<tr><td></td><td colspan="3">MAC Interface</td><td rowspan="2"></td><td rowspan="2"></td></tr>
<tr><td></td><td>GMII</td><td>RGMII</td><td>MII</td></tr>
<tr><td>45,44,42,41</td><td>RXD[3:0]</td><td>RXD[3:0]</td><td>RXD[3:0]</td><td>O</td><td>GMII/RGMII/MII Receive Data
Please see the pin description of pin 39.</td></tr>
<tr><td>53</td><td>RX_ER</td><td>--</td><td>RX_ER</td><td>O</td><td>GMII and MII Receive Error

RX_ER shares the same pin with PHY_ADDR2.
<table>
<tr><th>I/F</th><th>MDI speed</th><th>Description</th></tr>
<tr><td rowspan="2">GMII Mode</td><td>Gigabit</td><td>A “high” state present on this pin indicates received data error or carrier extension. It is synchronous to RX_CLK</td></tr>
<tr><td>100Mbps, 10Mbps</td><td>A “high” state present on this pin indicates received data error. It is synchronous to RX_CLK</td></tr>
<tr><td>RGMII Mode</td><td>Gigabit, 100Mbps, 10Mbps</td><td>Not used.</td></tr>
</table></td></tr>
<tr><td>7</td><td>CRS</td><td>--</td><td>CRS</td><td>IPH/O</td><td>GMII/MII Carrier Sense
It asserts during either the transmission or the reception.
CRS shares the same pin with PHY_ADDR1.</td></tr>
<tr><td>8</td><td>COL</td><td>--</td><td>COL</td><td>IPH/O</td><td>GMII/MII Collision
If IP1001 operates in half mode, it asserts when both transmission and reception are running. If IP1001 works in full duplex mode, COL is always idle (logic low).
COL shares the same pin with PHY_ADDR0.</td></tr>
</table>

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Pin description (continued)

Pin no.	Label	Type	Description
LED Display			
55	LED_MODE0	LI/O	LED Mode Selection (MODE0~MODE3). LED_MODE[1:0] can provide 4 LED display modes, Mode0~ Mode3. LED_MODE1 is set by register16[15]. LED_MODE0 is defined by pin or by register16[14]. The pin state of LED_MODE0 is latched upon reset and set to register 16[14]. After power up, the designer can configure LED_MODE[1:0] register during the operation. Since LED_MODE1 is set to “0” upon reset, the designer can set pin 55 to select “00” or “01” display mode if the register 16[15:14] is unchanged.
15,14,13	LED2, LED1, LED0	IPH/O, LI/O	LED output pins 0,1,2

	Mode0	Mode1	Mode2	Mode3
LED_Mode1, LED_Mode0	00	01	10	11
LED0	10/100M Link/Act 0: link off 1: 10/100M link on Flash: TX or RX	Bi-color mode {LED0, LED1}= 10= 1G Link; 01=10/100M Link; 00= link off 11= link off	1G Link/Act 0: link off 1: Giga link on Flash: TX or RX	Bi-triple-color mode {LED0, LED1}= 10= 1G Link; 01= 100M Link 00= 10M Link; 11= link off
LED1	100M Link/Act 0: link off 1: 100M link on Flash: TX or RX		100M Link/Act 0: link off 1: 100M link on Flash: TX or RX	
LED2	1G Link/Act 0: link off 1: Giga link on Flash: TX or RX	Act 0: link off or idle 1: TX or RX	10M Link/Act 0: link off 1: 10M link on Flash: TX or RX	Link/ Act 0: link off 1: 10/100M/giga link on Flash: TX or RX

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Pin description (continued)

Pin no.	Label	Type	Description
Serial Management Interface			
11	MDC	I	Management Data Clock. MDC is the management data clock reference. A continuous clock is not expected. The maximum frequency supported is 12.5 MHz.
12	MDIO	I/O	Management Data Input Output. MDIO transfers management data in and out of the device synchronous to MDC. This pin should be connected to VDDO through a 5.1-kΩ pull up resistor.

Pin no.	Label	Type	Description
Medium Interface			
29,26,21,18, 30,27,22,19	MDI[3:0]P, MDI[3:0]M	I/O	Twisted- Pair Media Dependent Interface In 1000BASE-T mode, all 4 pairs are both input and output at the same time. In 100BASE-TX and 10BASE-T mode, MDI[0]P/M are used for transmit pair under MDI configuration, and is used for receive pair under MDIX configuration. MDI[1]P/M are used for receive pair under MDI configuration, and is used for transmit pair under MDIX configuration. MDI[2]P/M and MDI[3]P/M are unused in 100BASE-TX and 10BASE-T mode.

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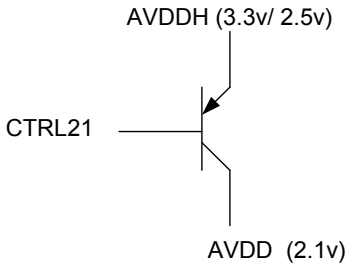
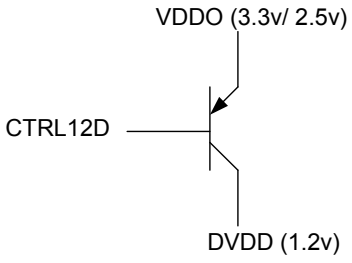
Pin description (continued)

Pin no.	Label	Type	Description
Miscellaneous			
16	CTRL21	O	Regulator Control. The internal linear regulator uses this pin to control an external PNP transistor to generate a 2.1v voltage source. IP1001 uses the AVDDH as a reference voltage, which can be 3.3v or 2.5v as shown in the following figure. The 2.1v power source is used for center tap of transformer and AVDD. The built in regulator works only if AVDD pins are connected to the collector of the external PNP as shown in the following figure. If AVDD pins are connected to an external power source instead of the collector of PNP, the function of CTRL21 doesn't work.  This pin can be left open if it is not used.
32	CTRL12D	O	Regulator Control. The internal linear regulator uses this pin to control an external PNP transistor to generate a 1.2v voltage source. IP1001 uses the VDDO as a reference voltage, which can be 3.3v or 2.5v as shown in the following figure. The 1.2v power source is used for DVDD. The built in regulator works only if DVDD pins are connected to the collector of the external PNP as shown in the following figure. If DVDD pins are connected an external power source instead of the collector of PNP, the function of CTRL12D doesn't work.  This pin can be left open if it is not used.

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Pin description (continued)

Pin no.	Label	Type	Description
Miscellaneous			
33	X1	I	Reference Clock. 25 MHz crystal reference or oscillator input. Connects to crystal to provide the 25MHz crystal input. If a 25MHz oscillator is used, connect X1 to the oscillator's output. The input voltage of this pin should not exceed 1.8V. A voltage divider formed by 2 resistors is recommended if the output voltage of oscillator is over 1.8V. Please refer to the Crystal Specifications in detail.
34	X2	O	Reference Clock. 25 MHz crystal reference.
35	RESET#	I	Hardware reset Active low. IP1001 enters reset state when this pin is pulled low.
37	NC_TEST	IPL	It is used for scan test only. It should be left open for normal operation.
10	CLK_OUT	O	125M clock output It is used by external MAC device. This signal is always active after reset.
25	CAP		Capacitor pin It should be connected to GND through an external 10uF capacitor. It is used to stabilize the internal analog power.
17	R_SET	I	Band gap Reference Add an external 6.19kΩ±1% resistor between this pin and GND. IP1001 utilizes this resistor to set the current source.

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Pin description (continued)

Pin no.	Label	Type	Description
Power pins			
3, 38, 46, 54, 63	DVDD		1.2v digital power
20, 23, 28,31,	AVDD		1.8v or 2.1v analog power AVDD can be fed with external 1.8v or 2.1v power. If there is no external 1.8v power source, AVDD can be connected the 2.1v power source generated by CTRL21. If an external 1.8v power is available, AVDD can be connected to 1.8v to reduce the power consumption. If there is no external 2.5v power source, the center tap of transformer can be connected the 2.1v power source generated by CTRL21. If an external 2.5v power is available, the center tap of transformer can be connected to it, consuming the extra power consumption.
9, 43, 47, 52, 56, 64	VDDO		3.3v/ 2.5v digial I/O power VDDO is connected to 3.3v if IP1001 works in MII or GMII mode. VDDO is connected to 2.5v if IP1001 works at RGMII mode.
24	AVDDH		3.3v/ 2.5v analog power AVDDH can be fed with 3.3v or 2.5v, using the same power source of VDDO. Although VDDO and AVDDH use the same power source, user has to place a bead between VDDO and AVDDH to prevent the noise of AVDDH noise.
--	GND		Exposed PAD (E-PAD) (Thermal PAD) is Analog and Digital ground.

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3 Functional Description

The IP1001 is an Ethernet transceiver for 1000BASE-T, 100BASE-TX, and 10BASE-T. It uses one pair of UTP wires to transmit data and uses another pair to receive data when working in 100BASE-TX or 10BASE-T. It uses four pairs of UTP wires to transmit and to receive data when working in 1000BASE-T.

It supports auto-negotiation, including next page exchanging, speed (1000M, 100M, 10M), duplex (full/ half) mode and master/slave resolution. This device also supports RGMII/ GMII/ MII to interface a MAC device.

Registers in the IP1001 can be accessed via the SMI (MDC/MDIO). Three LEDs shows the various statuses of the device. Pair skews in the cables are automatically adjusted. Wiring errors are automatically corrected via pair swapping (automatic MDI/MDIX) and polarity correction.

3.1 Medium Dependent Interface (MDI) for Twisted Pair Cable

The interface between IP1001 and CAT5 cable consists of four signal pairs, channel A, B, C and D, that are used for 1000BASE-T transmission/receiving. Each signal pair consists of two bi-directional pins that transmit and receive data stream at the same time.

When the IP1001 operates in 100BASE-TX or 10BASE-T mode, only channel A and B are used, one for transmission and the other for reception. IP1001 will handle the MDIX/MDI crossover issue of the twisted-pair wire automatically. Please refer to section 3.5 Auto MDI/MDIX Crossover for detail.

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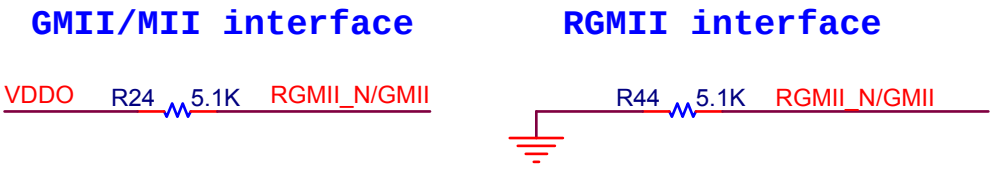
3.2 MAC Interface (RGMII/ GMII/ MII)

IP1001 supports RGMII and GMII/ MII interfaces. User can select the one of the interfaces by configure pin 36 and IP1001 will latch the setting at the end of hardware reset. If pin 36 is connected to GND through a resistor R44, RGMII is selected. If pin 36 is connected to VDDO through a resistor R24, GMII/ MII is selected.



If GMII mode is selected and IP1001 links in 1000BASE-T mode, GTX_CLK, TX_EN, TXD[7:0] and TX_ER are input signals and should be driven by an external MAC device, TX_CLK is driven low. RX_CLK, CRS, RX_DV, RXD[7:0], RX_ER and COL are output signals to an external MAC device.

In the 100BASE-TX (10BASE-T) modes, both TX_CLK and RX_CLK source 25 MHz (2.5 MHz) clock respectively. TX_EN, TXD[3:0] and TX_ER are input signal and should be driven by an external MAC device. RX_CLK, CRS, RX_DV, RXD[3:0], RX_ER and COL are output signals to an external MAC device. GTX_CLK and TXD[7:4] signals are ignored and RXD[7:4] drives low.

If RGMII mode is selected, TXC, TX_CTL and TXD[3:0] are input signals and should be driven by an external MAC device, TX_CLK is driven low. RXC, RX_CTL and RXD[3:0] are output signals to an external MAC device. RXC provides a 125 Mhz, 25 Mhz or 2.5 Mhz reference clock depending on the link speed is 1000M, 100M or 10M.

A timing adjustment on MAC interface is implemented in IP1001 by adding delay to the clock pins and changing driving capability on RX pins. User can add input delay to the GTX_CLK(TXC) by programming pin 49 TXPHASE_SEL or register 16.1 or add output delay to the RX_CLK(RXC) by programming pin 48 RXPHASE_SEL or register 16.0. The driving capability of RX signals can be configured by programming MII register 16[8:5]

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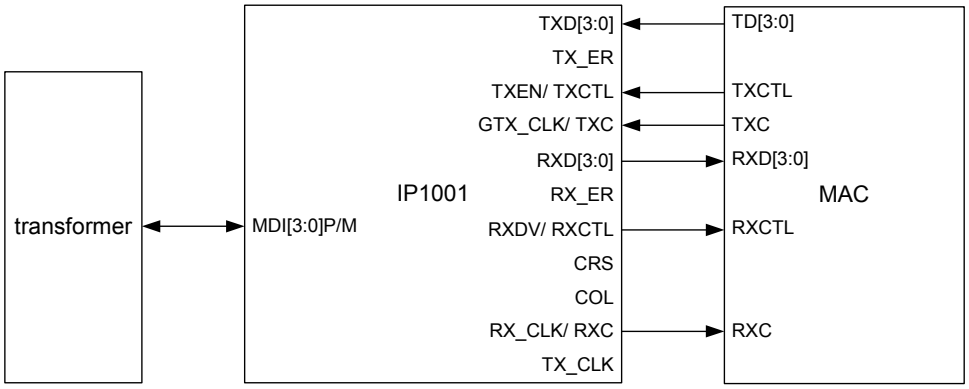
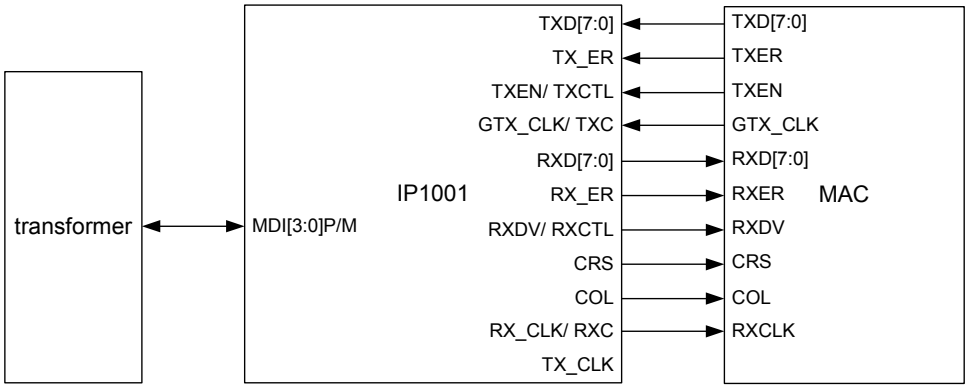
MII/GMII/RGMII selection and signal direction

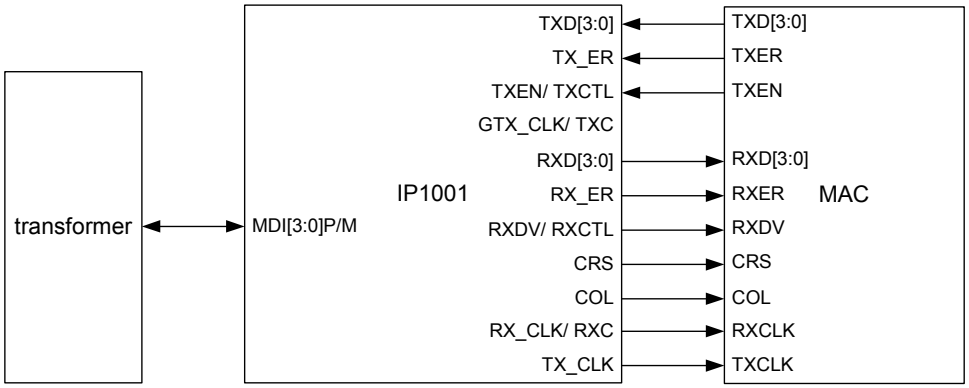
RGMII is active if pin 36 RGMII_N/GMII is pulled low.



GMII is active if pin 15 RGMII_N/GMII is pulled high and IP1001is linked at giga mode.



MII is active if pin 15 RGMII_N/GMII is pulled high and IP1001 islinked at 100M, or 10M.



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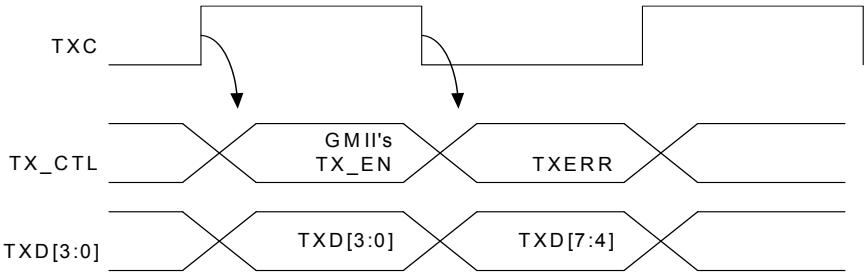
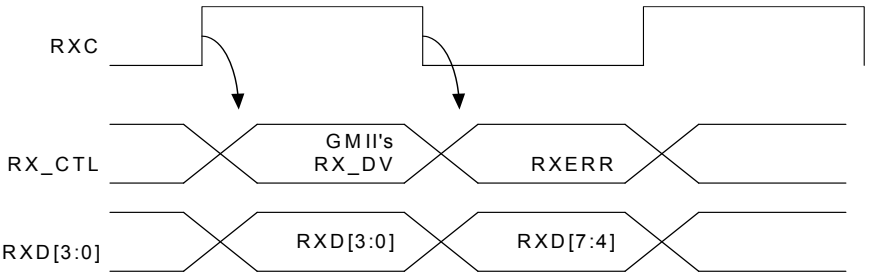
Waveform of RGMII and GMII (MII)

RGMII

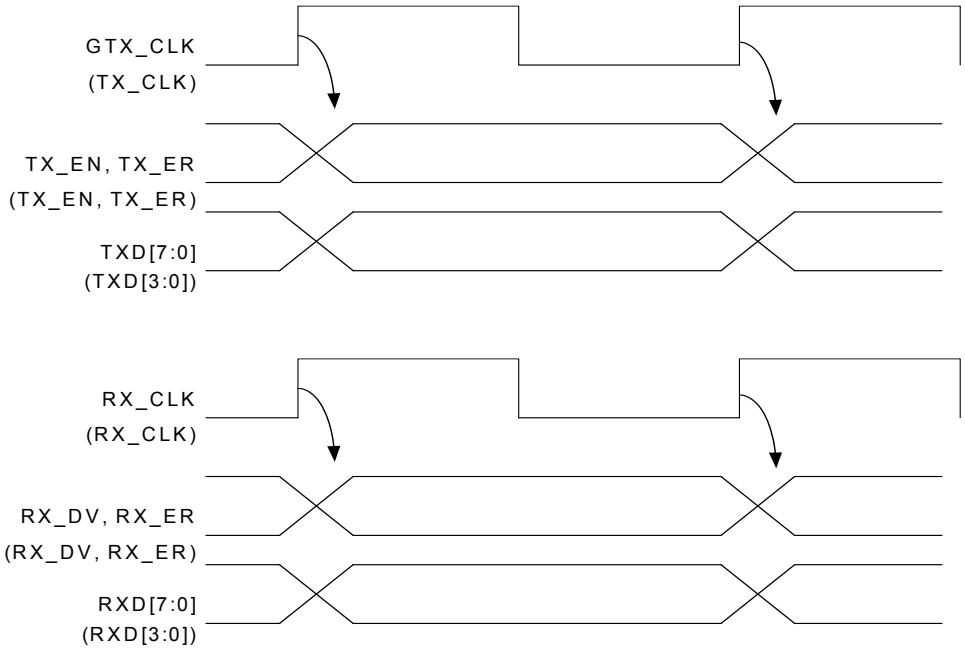


TXERR = GMII's TX_EN (XOR) GMII's TX_ER



RXERR = GMII's RX_DV (XOR) GMII's RX_ER

GMII (MII)



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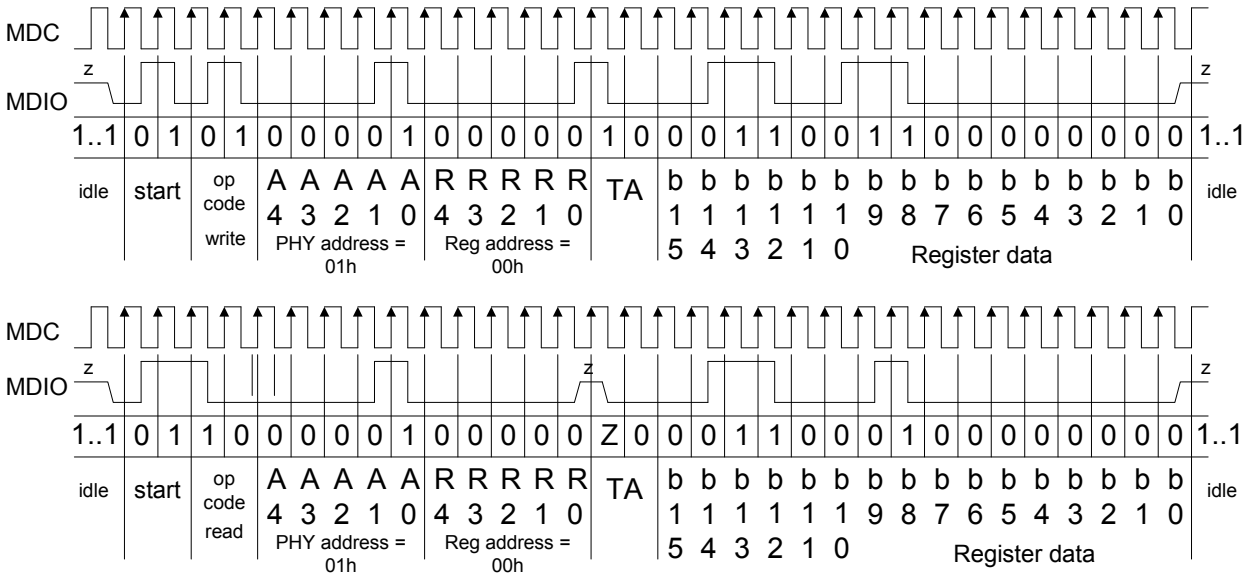
3.3 Serial Management Interface

The serial management interface consisting of two pins, MDC and MDIO, provides access to the MII registers of IP1001. MDC is a clock input and runs at a maximum rate of 12.5 MHz. MDIO is a bi-directional data pin that runs synchronously to MDC. The MDIO pin requires a 5.1-kΩ pull up resistor. To access MII register in IP1001, MDC should be at least one more cycle than MDIO. That is, a complete command consists of 32 bits MDIO data and at least 33 MDC clocks.

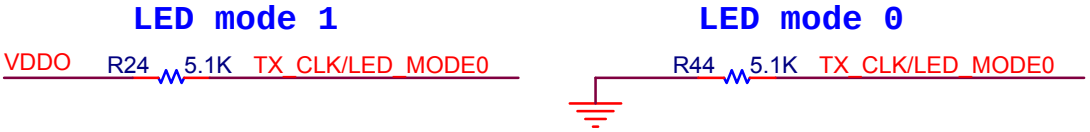
Frame format	<Idle><start><op code><PHY address><Registers address><turnaround><data><idle>
Read Operation	<Idle><01><10><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><Z0><b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1b_0><Idle>
Write Operation	<Idle><01><01><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><10><b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1b_0><Idle>



3.4 LED

IP1001 provides 3 LED pins, LED0~2, and four LED display modes, mode0~3. User can select one of four LED modes by configuring LED_MODE1 and LED_MODE0. LED_MODE1 and LED_MODE0 are defined in register 16[15:14]. Pin 55 LED_MODE0 defines the default value of register 16[14].
The functionality of the LED pins is shown in the table below. The driving capability of LED pins can be programmed by writing MII register 16[13].

LED mode setting



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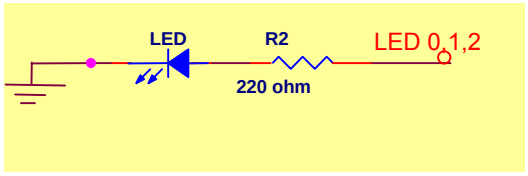
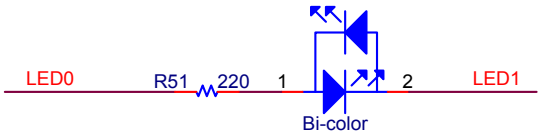
LED application circuit

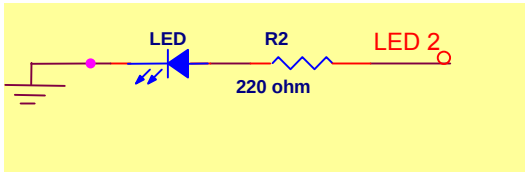
Mode 0 & mode 2



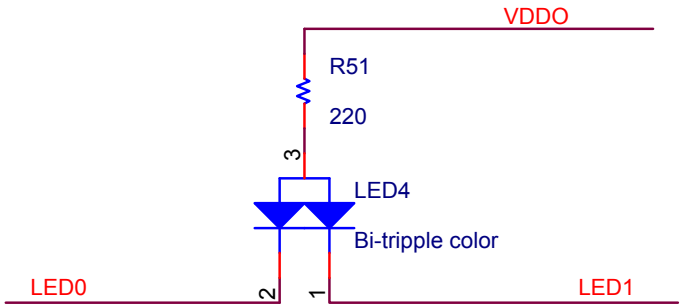
Mode 1



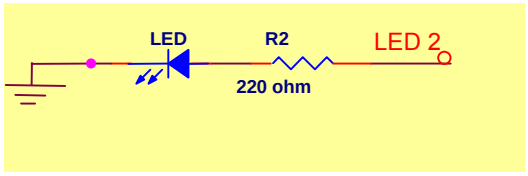
Bi-color LED configuration



Mode 3



Bi-tripple color LED configuration



	Mode0	Mode1	Mode2	Mode3
LED_MODE1, LED_MODE0	0,0	0,1	1,0	1,1
Pin 13 LED0	10/100M Link/Act	Bi-color mode {LED0, LED1}= 10= 1G Link; 01=10/100M Link; 00= link off 11= link off	1G Link/ Act	Bi-triple-color mode {LED0, LED1}= 10= 1G Link; 01= 100M Link 00= 10M Link; 11= link off
Pin 14 LED1	100M Link/Act		100M Link/ Act	
Pin 15 LED2	1G Link/Act	Act	10M Link/ Act	Link/ Act

Note:
Link: LED on
Act (activity): LED blinking (frequency is about 10Hz)

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3.5 Auto MDI/MDIX Crossover

The IP1001 implements auto-crossover function, that is, users don't have to care using a crossover or non-crossover cable. Its pin mapping in MDI and MDIX modes is shown in the following table. If IP1001 interoperates with a device that does not implement auto MDI/MDIX crossover, the IP1001 makes the necessary adjustment prior to performing auto-negotiation. If the IP1001 interoperates with a device that implements auto MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 section 40.4.4 determines which device performs the crossover.

When the IP1001 interoperates with a 10BASE_T PHY or a PHY that implements auto-negotiation, IP1001 decides the MDI/MDIX by the presence of link pulses. However, when interoperating with a 100BASE_TX PHY that does not implement auto-negotiation (i.e. link pulses are not present), IP1001 uses signal energy of receiving MLT3 signals to determine whether or not to crossover.

The auto MDI/MDIX function is turned on automatically after hardware reset and users can disable it by programming MII register 20.2. User can check if IP1001 is in MDI or MDIX type by reading MII register 17.11. Auto MDI/MDIX function is not affected by disabling auto-negotiation function.

Pin	MDI			MDIX		
	1000BASE-T	100BASE-TX	10BASE-T	1000BASE-T	100BASE-TX	10BASE-T
MDI[0]P/M	BI_DA+/-	TX+/-	TX+/-	BI_DB+/-	RX+/-	RX+/-
MDI[1]P/M	BI_DB+/-	RX+/-	RX+/-	BI_DA+/-	TX+/-	TX+/-
MDI[2]P/M	BI_DC+/-	Unused	Unused	BI_DD+/-	Unused	Unused
MDI[3]P/M	BI_DD+/-	Unused	Unused	BI_DC+/-	Unused	Unused

3.6 Polarity Correction

The IP1001 performs polarity correction without any manual setting. It corrects polarity errors on the receive pairs in 1000BASE-T and 10BASE-T modes automatically.

In 1000BASE-T mode, polarity correction is based on the sequence of idle symbols. In 10BASE-T mode, polarity correction is based on the detection the polarity of valid normal link pulse and idle pulse. In 100BASE-TX mode, the polarity does not matter.

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3.7 Auto-Negotiation

IP1001 will performs Auto-Negotiation automatically if one of the following conditions happened:
1) Power up reset, hardware reset, or software reset (by programming MII register 0.15).
2) Restart Auto-Negotiation (by programming MII register 0.9).
3) Transition from power down to power up (by programming MII register 0.11).
4) Link is down.

Once Auto-Negotiation is initiated, IP1001 sends out the appropriate base pages/ next pages to advertise its capability and negotiate with the link partner to determine speed, duplex, and master/slave. Note that IP1001 handles the base page/ next page exchanges automatically without user intervention. To link at giga mode, the link partner of IP1001 has to support Auto-Negotiation, too. Once IP1001 completes Auto-Negotiation it updates the statuses in registers 1, 5, 6, 10 and 17. The advertised abilities can be changed by writing registers 4 and 9. It is noted that a write access to register 4 or 9 has no effect once the IP1001 begins transmitting Fast Link Pulses (FLPs). This guarantees that the transmitted FLPs are consistent. Register 7 is treated in a similar way as registers 4 and 9 during additional next page exchanges.

If the link partner doesn't support Auto-Negotiation, IP1001 determines the link speed using parallel detection and the link result is either 10M half duplex or 100M half duplex. Please refer to IEEE 802.3 clause 28 and 40 for more detailed description of Auto-Negotiation.

Auto-Negotiation can be disabled by programming register 0.12. When Auto-Negotiation is disabled, the speed and duplex of IP1001 can be changed by programming registers 0.13, 0.6 and 0.8, respectively.

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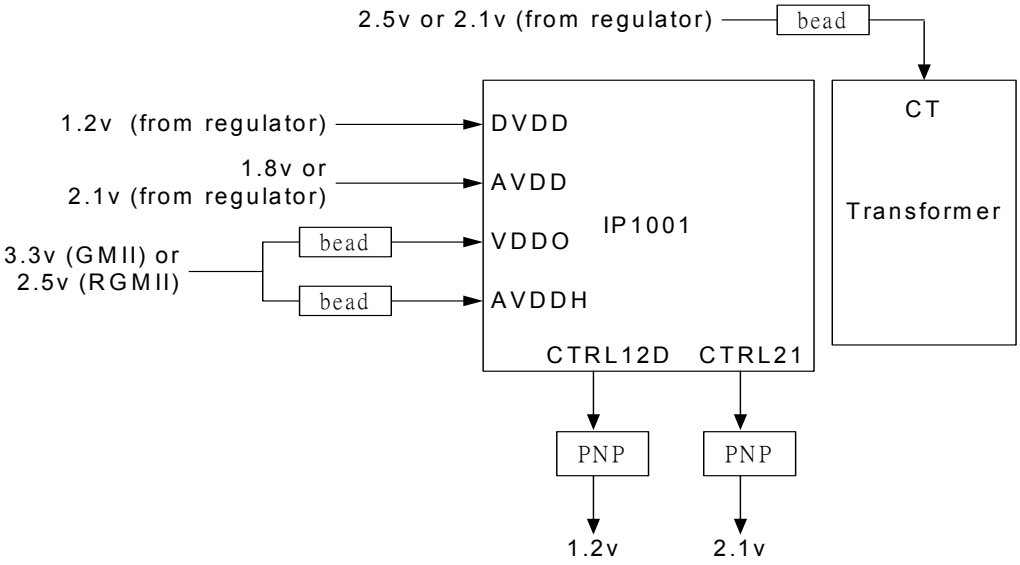
3.8 Smart speed

IP1001 supports smart speed function. If IP1001 can't link at Gigabit speed due to cable quality, the link speed is down shift to 100M automatically if smart speed option is turned on. If the function is turned off, IP1001 will link down if it can't link at giga mode due to cable quality. The function is default on and it can be enabled/disabled by programming MII register 16.11.

3.9 Power supply

IP1001 has 4 sets of power pins, DVDD, AVDD, VDDO and AVDDH. VDDO is connected to 3.3v or 2.5v depending on MAC interface is GMII or RGMII. AVDDH can use the same power source of VDDO, that is 3.3v or 2.5v, but it needs a bead to prevent VDDO noise. AVDD can be connected to 1.8v or 2.1v. If there is no external 1.8v power source, user can use the 2.1v power generated by the built in regulator (CTRL21). DVDD is connected to 1.2v. The center tap of transformer can be connected to 2.1v or 2.5v. If there is no external 2.5v power source, user can use the 2.1v power generated by the built in regulator control(CTRL21). The current limit of bead should be large enough to prevent the IR drop in power supply input.



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3.10 Digital Internal Function

The IP1001 integrates all necessary function blocks to achieve the communication ability over CAT5 unshielded twisted pair cables. These function blocks include analog blocks and digital blocks.

Analog function blocks includes analog to digital converter (ADC), digital to analog converter (DAC), active hybrid, and high-speed 1.25GHz transmitter/receiver. Digital function blocks include digital adaptive feed-forward equalizer (FFE), decision-feedback equalizer (DFE), echo canceller (EC), near-end-cross-talk canceller, baseline wander canceller, and digital phase lock-loop (DPLL). Some other encoding/decoding blocks are also necessary in the transmission/receiving data path.

3.11 IEEE802.3 1000BASE_T Test mode

IP1001 supports four test modes for 1000BASE_T defined in IEEE802.3 clause 40.6. User can force IP1001 to be in test mode to characterize its waveform, jitter, and distortion by programming MII register 9[15:13].

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4 Register Descriptions

Abbreviation description

Abbreviation	Description
SC	Self-Clear
LH	Latched High
LL	Latched Low
RO	Read Only
R/W	Read and Write
NA	Not Affected
HW Reset	Reset by RESET# pin
SW Reset	Reset by MII register 0 bit 15

PHY registers

The IP1001 supports a full set of PHY registers, which can be accessed through the MDC/MDIO interface.

Register	Description
Reg0	Control Register
Reg1	Status Register
Reg2	PHY Identifier Register
Reg3	PHY Identifier Register
Reg4	Auto-Negotiation advertise register
Reg5	Link Partner Ability Register
Reg6	Auto-Negotiation Expansion Register
Reg7	Auto-Negotiation Next Page Transmit Register
Reg8	Auto-Negotiation Link Partner Next Page Register
Reg9	1000BASE-T Control Register
Reg10	1000BASE-T Status Register
Reg11~14	Reserved. Do not access to these registers.
Reg15	Extended Status Register
Reg16	PHY Specific Control Register1
Reg17	PHY Link Status Register
Reg18~19	Reserved. Do not access to these registers.
Reg20	PHY Specific Control Register2
Reg21~31	Reserved

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4.1 Control Register (Reg0)

Bit	Name	Description			Type	HW Reset	SW Reset
0.5:0	Reserved				RO	Always 0	
0.6	Speed Selection (MSB)	0.6	0.13		R/W	1	NA
		1	1	Reserved			
		1	0	1000Mb/s			
		0	1	100Mb/s			
		0	0	10Mb/s			
0.7	Collision Test	1: Enable COL signal test 0: Disable COL signal test			R/W	0	0
0.8	Duplex Mode	1: Full duplex 0: Half duplex			R/W	1	NA
0.9	Restart Auto-NEG	1: Restart Auto-Negotiation Process 0: Normal operation			R/W SC	0	SC
0.10	Isolate	1: Isolate PHY from MII, GMII, or RGMII electrically 0: normal operation			R/W	0	0
0.11	Power Down	1: Power down 0: Normal operation			R/W	0	0
0.12	Auto-Negotiation Enable	1: Enable Auto-Negotiation Process 0: Disable Auto-Negotiation Process			R/W	1	NA
0.13	Speed Selection (LSB)	Please refer to bit 0.6 for detail information			R/W	0	NA
0.14	Loopback	1: Enable loop back mode 0: Disable loop back mode			R/W	0	0
0.15	Software Reset	1: PHY software reset 0: normal operation			R/W SC	0	0 (SC)

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4.2 Status Register (Reg1)

Bit	Name	Description	Type	HW Reset	SW Reset
1.0	Extended Capability	1: Support extended register capabilities 0: Support basic register set capabilities only	RO	1	1
1.1	Jabber Detect	1: Jabber condition detected 0: No jabber condition detected	RO LH	0	0
1.2	Link Status	1: Link is up 0: Link is down	RO LL	0	0
1.3	Auto-Negotiation Ability	1: PHY is able to perform Auto-Negotiation 0: PHY is not able to perform Auto-Negotiation	RO	1	1
1.4	Remote Fault	1: Remote fault condition detected 0: No remote fault condition detected	RO LH	0	0
1.5	Auto-Negotiation Complete	1: Auto-Negotiation process completed 0: Auto-Negotiation process not completed	RO	0	0
1.6	MF Preamble Suppression	1: PHY accepts management frames with preamble suppressed. 0: PHY does not accept management frames with preamble suppressed.	RO	Reserved 1	
1.7	Reserved	Ignore when read	RO	Reserved 0	
1.8	Extended Status	1: There is extended status information in Register 15 0: No extended status information in Register 15	RO	Reserved 1	
1.9	100BASE-T2 Half Duplex	1: PHY able to perform half duplex 100BASE-T2 0: PHY not able to perform half duplex 100BASE-T2	RO	Reserved 0	
1.10	100BASE-T2 Full Duplex	1: PHY able to perform full duplex 100BASE-T2 0: PHY not able to perform full duplex 100BASE-T2	RO	Reserved 0	
1.11	10Mb/s Half Duplex	1: PHY able to operate at 10 Mb/s in half duplex mode 0: PHY not able to operate at 10 Mb/s in half duplex mode	RO	1	1
1.12	10 Mb/s Full Duplex	1: PHY able to operate at 10Mb/s in full duplex mode 0: PHY not able to operate at 10Mb/s in full duplex mode	RO	1	1
1.13	100BASE-X Half Duplex	1: PHY able to perform half duplex 100BASE-X 0: PHY not able to perform half duplex 100BASE-X	RO	1	1
1.14	100BASE-X Full Duplex	1: PHY able to perform full duplex 100BASE-X 0: PHY not able to perform full duplex 100BASE-X	RO	1	1
1.15	100BASE-T4	1: PHY able to perform 100BASE-T4 0: PHY not able to perform 100BASE-T4	RO	Reserved 0	

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4.3 PHY Identifier Register (Reg2)

Bit	Name	Description	Type	HW Reset	SW Reset
2[15:0]	Organizationally Unique Identifier Bit [3:18]	0000_0010_0100_0011 Note: ICplus's OUI is 0x0090C3	RO	Always 0x0243	

4.4 PHY Identifier Register (Reg3)

Bit	Name	Description	Type	HW Reset	SW Reset
3[3:0]	Revision Number	0000	RO	Always 0000	
3[9:4]	Manufacturer's Model Number	011001	RO	Always 011001	
3[15:10]	Organizationally Unique Identifier Bit [19:24]	000011	RO	Always 000011	

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4.5 Advertisement Register (Reg4)

Bit	Name	Description	Type	HW Reset	SW Reset
4[4:0]	Selector Filed	Only CSMA/CD <00001> is specified. No other protocols are supported.	RO	00001	00001
4.5	10BASE-T Half Duplex	1 = 10Base-T full duplex is supported 0 = 10Base-T full duplex not supported	R/W	1	1
4.6	10BASE-T Full Duplex	1 = 10Base-T half duplex is supported 0 = 10Base-T half duplex not supported	R/W	1	1
4.7	100BASE-TX Half Duplex	1 = 100Base-TX half duplex is supported 0 = 100Base-TX half duplex not supported	R/W	1	1
4.8	100BASE-TX Full Duplex	1 = 100Base-TX full duplex is supported 0 = 100Base-TX full duplex not supported	R/W	1	1
4.9	100BASE-T4	1 = 100Base-T4 is supported 0 = 100Base-T4 not supported	RO	Reserved 0	
4.10	PAUSE	1 = flow control is supported 0 = flow control is not supported	R/W	0	
4.11	Asymmetric Pause	1 = asymmetric flow control is supported 0 = asymmetric flow control is not supported	R/W	0	
4.12	Reserved	Ignore when read	R/W	0	0
4.13	Remote Fault	1 = Advertise remote fault detection capability 0 = Not advertise remote fault detection capability	R/W	0	
4.14	Reserved	Ignore when read	RO	Reserved 0	
4.15	Next Page	1 = Next pages are supported 0 = Next pages are not supported	R/W	1	

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4.6 Link Partner's Ability Register (Base Page) (Reg5)

Bit	Name	Description	Type	HW Reset	SW Reset
5[4:0]	Selector Field		RO	0	0
5.5	10BASE-T Half Duplex	1 = 10Base-T is supported by link partner 0 = 10Base-T not supported by link partner	RO	0	0
5.6	10BASE-T Full Duplex	1 = 10Base-T full duplex is supported by link partner 0 = 10Base-T full duplex not supported by link partner	RO	0	0
5.7	100BASE-TX Half Duplex	1 = 100Base-TX is supported by link partner 0 = 100Base-TX not supported by link partner	RO	0	0
5.8	100BASE-TX Full Duplex	1 = 100Base-TX full duplex is supported by link partner 0 = 100Base-TX full duplex not supported by link partner	RO	0	0
5.9	100BASE-T4	1 = 100Base-T4 is supported by link partner 0 = 100Base-T4 not supported by link partner	RO	0	0
5.10	PAUSE	1 = flow control is supported by Link partner 0 = flow control is not supported by Link partner	RO	0	0
5.11	Asymmetric Pause	1 = asymmetric flow control is supported by Link partner 0 = asymmetric flow control is NOT supported by Link partner	RO	0	0
5.12	Reserved		RO	0	0

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Bit	Name	Description	Type	HW Reset	SW Reset
5.13	Remote Fault	1 = link partner is indicating a remote fault 0 = link partner does not indicate a remote fault. It is Received Code Word Bit 13.	RO	0	0
5.14	Acknowledge	1 = link partner acknowledges reception of local node's capability 0 = no acknowledgement It is Received Code Word Bit 14.	RO	0	0
5.15	Next Page	1 = Next pages are supported by link partner 0 = Next pages are not supported by link partner. It is Received Code Word Bit 15.	RO	0	0

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4.7 Auto-Negotiation Expansion Register (Reg6)

Bit	Name	Description	Type	HW Reset	SW Reset
6.0	Link Partner Auto-Negotiation Able	1: Link partner supports Auto-Negotiation 0: Link partner does not support Auto-Negotiation	RO	0	0
6.1	Page Received	1: A new page has been received 0: A new page has not been received	RO LH	0	0
6.2	Local Next Page Able	1: Local device supports Next Page 0: Local device does not support Next Page	RO	1	0
6.3	Link Partner Next Page Able	1: Link Partner supports Next Page 0: Link Partner does not support Next Page	RO	0	0
6.4	Parallel Detection Fault	1: A fault has been detected via Parallel Detection function 0: A fault has not been detected via Parallel Detection function	RO	0	0
6.15:5	Reserved	Ignore when read	RO	Reserve 0	

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4.8 Auto-Negotiation Next Page Transmit Register (Reg7)

Bit	Name	Description	Type	HW Reset	SW Reset
7[10:0]	Message/Unformatted Field	Transmit Code Word Bit 10:0	R/W	0x001	0x001
7.11	Toggle	Transmit Code Word Bit 11	RO	0	0
7.12	Acknowledge 2	Transmit Code Word Bit 12	R/W	0	0
7.13	Message Page	Transmit Code Word Bit 13	R/W	1	1
7.14	Reserved	Transmit Code Word Bit 14	RO	Reserved 0	
7.15	Next Page	Transmit Code Word Bit 15	R/W	0	0

4.9 Auto-Negotiation Link Partner Next Page Register (Reg8)

Bit	Name	Description	Type	HW Reset	SW Reset
8[10:0]	Message/Unformatted Field	Received Code Word Bit 10:0	RO	0x000	0x000
8.11	Toggle	Received Code Word Bit 11	RO	0	0
8.12	Acknowledge 2	Received Code Word Bit 12	RO	0	0
8.13	Message Page	Received Code Word Bit 13	RO	0	0
8.14	Acknowledge	Received Code Word Bit 14	RO	0	0
8.15	Next Page	Received Code Word Bit 15	RO	0	0

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4.10 1000BASE-T Control Register (Reg9)

Bit	Name	Description	Type	HW Reset	SW Reset
9[7:0]	Reserved	Ignore when read	R/W	Reserved to 0x00	
9.8	1000BASE-T Half Duplex	1: Advertise 1000BASE-T half duplex capable 0: Not advertise	R/W	1	0
9.9	1000BASE-T Full Duplex	1: Advertise 1000BASE-T full duplex capable 0: Not advertise	R/W	1	0
9.10	Port Type	1: Prefer multi-port device (MASTER) 0: Prefer single-port device (SLAVE)	R/W	1	0
9.11	Configuration Value	1: Manual configure as MASTER 0: Manual configure as SLAVE It is valid only if bit 9.12 is set to 1.	R/W	0	0
9.12	Manual Configuration Enable	1: Manual Configuration Enabled 0: Manual Configuration Disabled	R/W	0	0
9[15:13]	Test mode	1000BASE_T test mode defined in IEEE802.3 clause 40.6.	R/W	000	000

9[15:13]	Mode
000	Normal Mode
001	Test Mode 1 - Transmit waveform test
010	Test Mode 2 - Transmit Jitter test in MASTER mode
011	Test Mode 3 - Transmit Jitter test in SLAVE mode
100	Test Mode 4 - Transmit distortion test
Others	Reserved

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4.11 1000BASE-T Status Register (Reg10)

Bit	Name	Description	Type	HW Reset	SW Reset
10[7:0]	Idle Error Count		RO	0x00	0x00
10.8	Reserved	Ignore when read	RO	Reserved to 0	
10.9	Reserved	Ignore when read	RO	Reserved to 0	
10.10	Link Partner's 1000BASE-T Half Duplex Capability	1: Link Partner is capable of 1000BASE-T half duplex 0: Link Partner is not capable of 1000BASE-T half duplex	RO	0	0
10.11	Link Partner's 1000BASE-T Full Duplex Capability	1: Link Partner is capable of 1000BASE-T full duplex 0: Link Partner is not capable of 1000BASE-T full duplex	RO	0	0
10.12	Remote Receiver Status	1: Remote Receiver OK 0: Remote Receiver Not OK	RO	0	0
10.13	Local Receiver Status	1: Local Receiver OK 0: Local Receiver Not OK	RO	0	0
10.14	MASTER/SLAVE Configuration Resolution	1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE	RO	0	0
10.15	MASTER/SLAVE Configuration Fault	1: MASTER/SLAVE configuration fault detected 0: No MASTER/SLAVE configuration fault detected	RO LH SC	0	0

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4.12 Extended Status Register (Reg15)

Bit	Name	Description	Type	HW Reset	SW Reset
15[11:0]	Reserved	Ignore when read	RO	0x000	0x000
15.12	1000BASE-T Half Duplex	1: be able to perform half duplex 1000BASE-T 0: not able to perform half duplex 1000BASE-T	RO	1	1
15.13	1000BASE-T Full Duplex	1: be able to perform full duplex 1000BASE-T 0: not able to perform full duplex 1000BASE-T	RO	1	1
15.14	1000BASE-X Half Duplex	1: be able to perform half duplex 1000BASE-X 0: not able to perform half duplex 1000BASE-X	RO	0	0
15.15	1000BASE-X Full Duplex	1: be able to perform full duplex 1000BASE-X 0: not able to perform full duplex 1000BASE-X	RO	0	0

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4.13 PHY Specific Control & Status Register (Reg16)

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th><th>Type</th><th>HW Reset</th><th>SW Reset</th></tr>
<tr><td>16.0</td><td>RXPHASE_SEL</td><td>This bit is used to adjust RX clock phase at GMII/ RGMII interface
0: No intentional delay is added on RX_CLK
1: An intentional delay is added on RX_CLK (about 2ns delay in 1000BASE-T, and about 4ns delay in 100BASE-TX and 10BASE-T).
(Pin 48 sets the default value of this bit)</td><td>RW</td><td>Pin 48</td><td>NA</td></tr>
<tr><td>16.1</td><td>TXPHASE_SEL</td><td>This bit is used to adjust TX clock phase at GMII/ RGMII interface
0: No intentional delay is added on GTX_CLK/ TXC
1: An intentional delay is added on GTX_CLK/ TXC
(about 2ns delay in 1000BASE-T, and about 4ns delay in 100BASE-TX and 10BASE-T)
Pin 49 sets the default value of this bit.</td><td>RW</td><td>Pin 49</td><td>NA</td></tr>
<tr><td>16.2</td><td>Repeater Mode</td><td>1 = Enable repeater mode
0 = Disable repeater mode</td><td>RW</td><td>0</td><td>NA</td></tr>
<tr><td>16[4:3]</td><td>Reserved</td><td></td><td></td><td>01</td><td>NA</td></tr>
<tr><td>16[6:5]</td><td>RXCLK_DRIVE[1:0]</td><td>These 2 bits are used to adjust driving current of RX_CLK.
<table>
<tr><td>I/F</td><td>2’b00</td><td>2’b01</td><td>2’b10</td><td>2’b11</td></tr>
<tr><td>MII</td><td>2mA</td><td>4mA</td><td>8mA</td><td>2mA</td></tr>
<tr><td>GMII/ RGMII (10/100)</td><td>2mA</td><td>4mA</td><td>8mA</td><td>2mA</td></tr>
<tr><td>GMII/ RGMII (1000)</td><td>4mA</td><td>8mA</td><td>12mA</td><td>2mA</td></tr>
</table></td><td>RW</td><td>10</td><td>NA</td></tr>
<tr><td>16[8:7]</td><td>RXD_DRIVE[1:0]</td><td>These 2 bits are used to adjust driving current of RXD[7:0], RX_ER, and RX_DV.

The driving current of RXD[3:0] and RX_DV
<table>
<tr><td>I/F</td><td>2’b00</td><td>2’b01</td><td>2’b10</td><td>2’b11</td></tr>
<tr><td>MII</td><td>2mA</td><td>4mA</td><td>8mA</td><td>2mA</td></tr>
<tr><td>GMII/ RGMII (10/100)</td><td>2mA</td><td>4mA</td><td>8mA</td><td>2mA</td></tr>
<tr><td>GMII/ RGMII (1000)</td><td>4mA</td><td>8mA</td><td>12mA</td><td>2mA</td></tr>
</table>

The driving current of RXD[7:4] and RX_ER
<table>
<tr><td>I/F</td><td>2’b00</td><td>2’b01</td><td>2’b10</td><td>2’b11</td></tr>
<tr><td>MII</td><td>2mA</td><td>4mA</td><td>8mA</td><td>2mA</td></tr>
<tr><td>GMII (10/100)</td><td>2mA</td><td>4mA</td><td>8mA</td><td>2mA</td></tr>
<tr><td>GMII (1000)</td><td>4mA</td><td>8mA</td><td>12mA</td><td>2mA</td></tr>
<tr><td>RGMII (10/100)</td><td>2mA</td><td>2mA</td><td>2mA</td><td>2mA</td></tr>
<tr><td>RGMII (1000)</td><td>4mA</td><td>2mA</td><td>12mA</td><td>2mA</td></tr>
</table></td><td>RW</td><td>10</td><td>NA</td></tr>
<tr><td>16.9</td><td>Jabber</td><td>1 = Enable Jabber</td><td>RW</td><td>1</td><td>NA</td></tr>
</table>

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Bit	Name	Description	Type	HW Reset	SW Reset
		0 = Disable Jabber			
16.10	Heart beat	1 = Enable Heart beat 0 = Disable Heart beat	RW	0	NA
16.11	Smart Speed	1 = Downshift to 100Mbps when 1000Mbps link fails 0 = No Downshift	RW	1	NA
16.12	Reserved	The default value (1) should be adopted for normal operation.		1	NA
16.13	LED_DRIVE	This bit is used to adjust LED driving current 1'b0: 4mA; 1'b1: 8mA	RW	0	NA
16[15:14]	LED_MODE[1:0]	These 2 bits are used to select LED displaying mode (Pin 55 sets the default value of bit14)	RW	0 Pin55	NA

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4.14 PHY Link Status Register (Reg17)

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th><th>Type</th><th>HW Reset</th><th>SW Reset</th></tr>
<tr><td>17[8:0]</td><td>Reserved</td><td></td><td>RO</td><td>0</td><td></td></tr>
<tr><td>17.9</td><td>Jabber Detected</td><td>0: 10Base Jabber not detected
1: 10Base Jabber detected</td><td>RO</td><td>0</td><td></td></tr>
<tr><td>17.10</td><td>APS_Sleep</td><td>0: Normal Operation
1: APS sleep mode is entered</td><td>RO</td><td>0</td><td></td></tr>
<tr><td>17.11</td><td>MDI/MDIX</td><td>0: MDI
1: MDIX
<table>
<tr><td></td><td colspan="3">MDI</td><td colspan="3">MDIX</td></tr>
<tr><td></td><td>1G</td><td>100M</td><td>10M</td><td>1G</td><td>100M</td><td>10M</td></tr>
<tr><td>MDI0</td><td>A</td><td>TX</td><td>TX</td><td>B</td><td>RX</td><td>RX</td></tr>
<tr><td>MDI1</td><td>B</td><td>RX</td><td>RX</td><td>A</td><td>TX</td><td>TX</td></tr>
<tr><td>MDI2</td><td>C</td><td>--</td><td>--</td><td>D</td><td>--</td><td>--</td></tr>
<tr><td>MDI3</td><td>D</td><td>--</td><td>--</td><td>C</td><td>--</td><td>--</td></tr>
</table></td><td>RO</td><td>0</td><td></td></tr>
<tr><td>17.12</td><td>Link_Duplex</td><td>0: link at half duplex
1: link at full duplex
It is valid only if bit 15 is 1.</td><td>RO</td><td>0</td><td></td></tr>
<tr><td>17[14:13]</td><td>Link_Speed[1:0]</td><td>2’b00: link at 10Base-T
2’b01: link at 100Base-TX
2’b10: link at 1000Base-T
2’b11: Reserved
It is valid only if bit 15 is 1.</td><td>RO</td><td>0</td><td></td></tr>
<tr><td>17.15</td><td>Link_Status</td><td>1: link up
0: link down</td><td>RO</td><td>0</td><td></td></tr>
</table>

Register 18~19 are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

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4.15 PHY Specific Control Register2 (Reg20)

Bit	Name	Description	Type	HW Reset	SW Reset
20[1:0]	SR_V/ SR_FAST	Sew rate control parameters	RW	11	NA
20.2	Auto-crossover Enable	1: Enable auto MDI/MDIX 0: Disable auto MDI/MDIX	RW	1	NA
20[5:3]	Reserved	The default value should be adopted for normal operation.	R/W	101	NA
20.6	Speed10to100enable	Detect the link partner's speed change from 10BASE-T to 100BASE-TX by detecting MLT3 signals 1: Enable 0: Disable	RW	1	NA
20[8: 7]	FIFO_Depth	FIFO depth latency 00: latency = 2 01: latency = 3 10: latency = 4 11: latency = 5	RW	10	NA
20.9	MDIX Enable	When disable auto-crossover 0: MDI 1: MDIX	RW	0	0
20.10	Reserved	The default value should be adopted for normal operation.	R/W	1	NA
20.11	APS_ON	This bit is used to activate auto power saving (APS) mode 0: Disable APS 1: Enable APS	RW	1	NA
20[15:12]	Reserved	The default value should be adopted for normal operation.	R/W	0000	NA

Register 21~31 are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

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5 Electrical Characteristics

5.1 Absolute Maximum Rating

Stresses exceed those values listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

Supply Voltage	–0.3V to 4.0V
Input Voltage	–0.3V to 5.0V
Output Voltage	–0.3V to 5.0V
Storage Temperature	-65°C to 150°C
Ambient Operating Temperature (Ta)	-10°C to 70°C

5.2 DC. Characteristic

Symbol	Conditions	Minimum	Typical	Maximum	Note
DVDD	Digital core supply voltage		1.2V		
AVDD	Analog core supply voltage	1.7V	1.8V	2.2V	
VDDO	I/O pad supply voltage	3.0V	3.3V	3.6V	GMII/MII
VDDO	I/O pad supply voltage	1.88V	2.5V	2.75V	RGMII
AVDDH	Analog supply voltage	3.0V	3.3V	3.6V	GMII/MII
AVDDH	Analog supply voltage	2.4V	2.5V	2.75V	RGMII
VCT	Transformer center tap voltage	2.1V	2.5V	2.75V	
TA	Operating Temperature	-10°C		70°C	

Input Clock

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Frequency			25		MHz	
Frequency Tolerance		-50		+50	PPM	

I/O Electrical Characteristics

Symbol	Specific Name	Condition	Min	Max
V_{IH}	Input High Vol.		0.5*Vcc	Vcc+0.5V
V_{IL}	Input Low Vol.		-0.5V	0.3*Vcc
V_{OH}	Output High Vol.		0.9*Vcc	Vcc
V_{OL}	Output Low Vol.			0.1*Vcc
I_{OZ}	Tri-state Leakage	Vout=Vcc or GND		
I_{IN}	Input Current	Vin=Vcc or GND		
Icc	Average Operating Supply Current	Iout=0mA		

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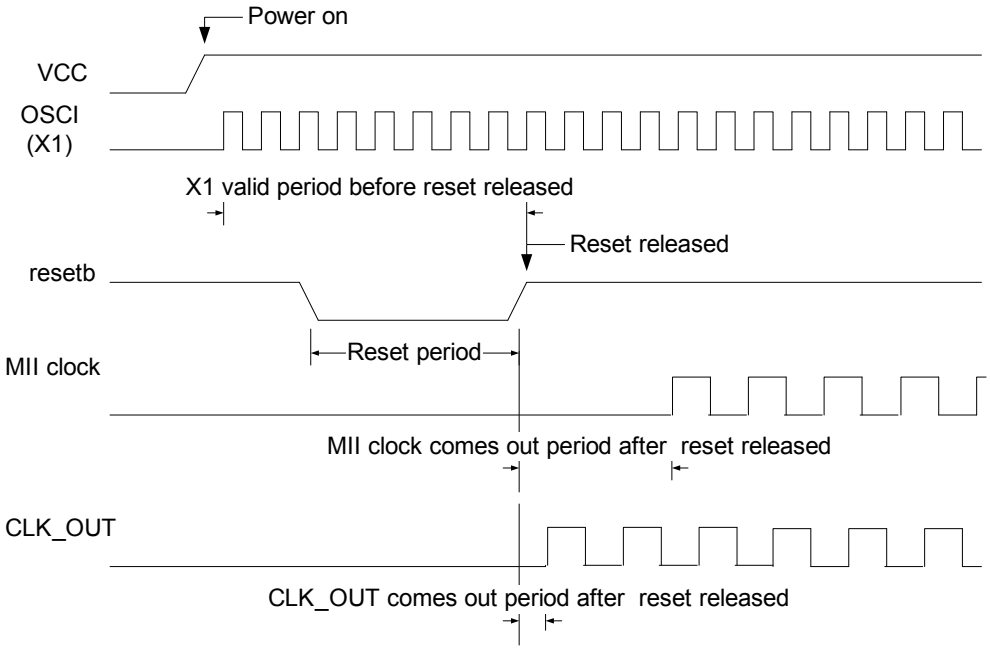
5.3 AC Timing

5.3.1 Reset Timing

Description	Min.	Typ.	Max.	Unit
X1 valid period before reset released	10	-	-	ms
Reset period	10	-	-	ms
MII/GMII/RGMII clock out after reset released	-	1	-	µs
CLK_OUT clock out after reset released	0	-	20	ns



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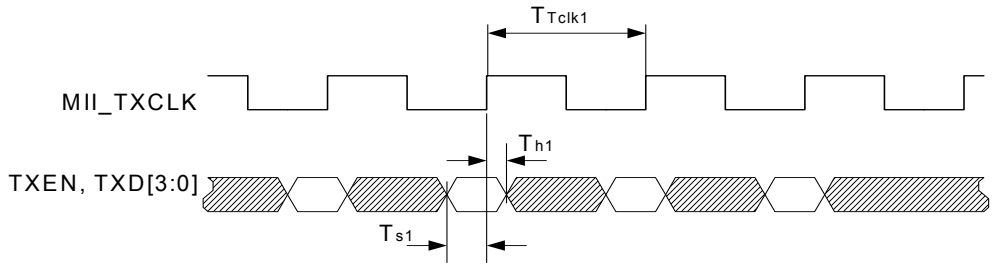
5.3.2 MII Timing

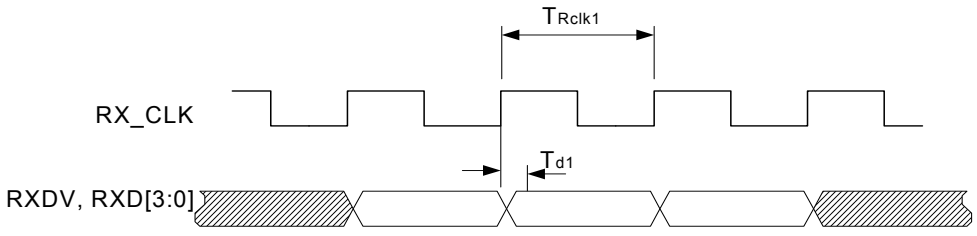
a. Transmit Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Tclk1}	Period of transmit clock in 100M mode	-	40	-	ns
T_{Tclk1}	Period of transmit clock in 10M mode	-	400	-	ns
T_{s1}	TXEN, TXD to TX_CLK setup time (TXPHASE_SEL=0, no clock delay added)	-0.65			ns
	TXEN, TXD to TX_CLK setup time (TXPHASE_SEL=1, clock delay added)	3.35			ns
T_{h1}	TXEN, TXD to TX_CLK hold time (TXPHASE_SEL=0, no clock delay added)	0.2			ns
	TXEN, TXD to TX_CLK hold time (TXPHASE_SEL=1, clock delay added)	4.2			ns



b. Receive Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Rclk1}	Period of receive clock in 100M mode	-	40	-	ns
T_{Rclk1}	Period of receive clock in 10M mode	-	400	-	ns
T_{d1}	MII_RXCLK rising edge to RXDV, RXD (RXPHASE_SEL=0, no clock delay added)	-0.4	0	0.4	ns
	MII_RXCLK rising edge to RXDV, RXD (RXPHASE_SEL=1, clock delay added)	3.6	4	4.4	ns



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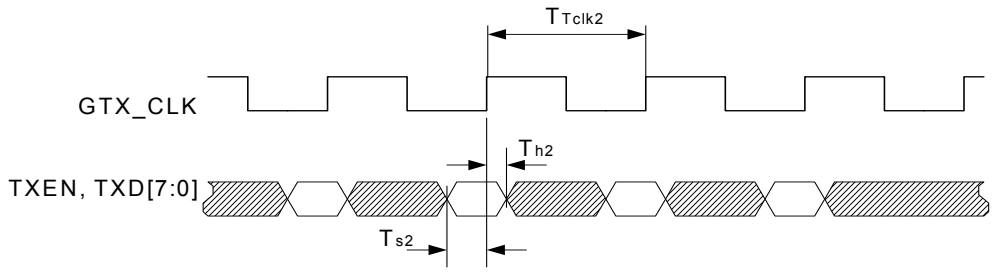
5.3.3 GMII Timing

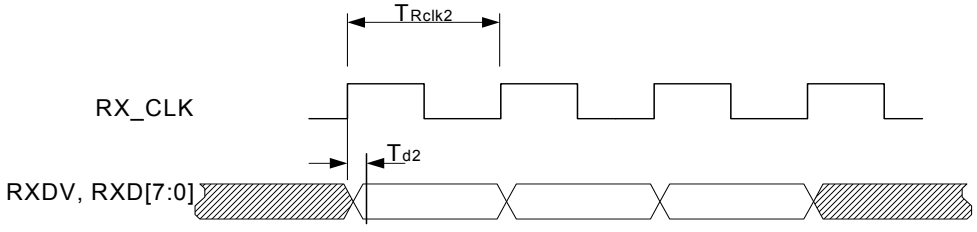
c. Transmit Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TXCLK}	Period of transmit clock	-	8	-	ns
T_{s2}	TXEN, TXD to GTX_CLK setup time (TXPHASE_SEL=0, no clock delay added)	-0.65			ns
	TXEN, TXD to GTX_CLK setup time (TXPHASE_SEL=1, clock delay added)	3.35			ns
T_{h2}	TXEN, TXD to GTX_CLK hold time (TXPHASE_SEL=0, no clock delay added)	0.2			ns
	TXEN, TXD to GTX_CLK hold time (TXPHASE_SEL=1, clock delay added)	4.2			ns



d. Receive Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Rclk2}	Period of receive clock	-	8	-	ns
T_{d2}	RX_CLK rising edge to RXDV, RXD (RXPHASE_SEL=0, no clock delay added)			0.4	ns
	RX_CLK rising edge to RXDV, RXD (RXPHASE_SEL=1, clock delay added)			4.4	ns



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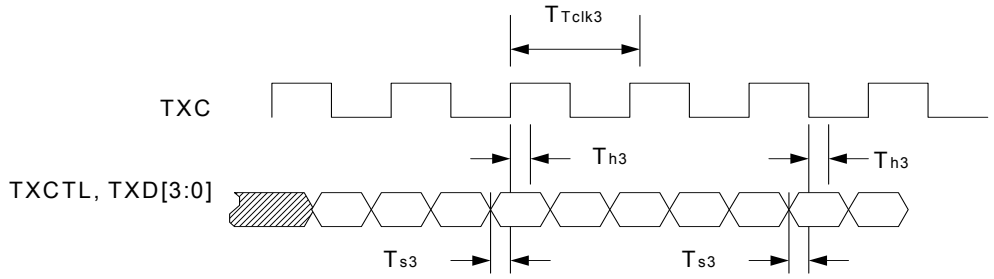
5.3.4 RGMII Timing

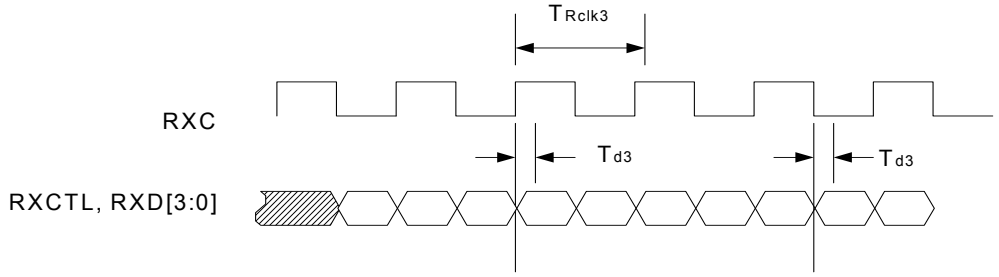
e. Transmit Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Tclk3}	Period of transmit clock in giga mode	-	8	-	ns
T_{Tclk3}	Period of transmit clock in 100M mode	-	40	-	ns
T_{Tclk3}	Period of transmit clock in 10M mode	-	400	-	ns
T_{s3}	TXEN, TXD to TXC setup time (TXPHASE_SEL=0, no clock delay added)	-0.65			ns
	TXEN, TXD to TXC setup time (TXPHASE_SEL=1, clock delay added)	1.35			ns
T_{h3}	TXEN, TXD to TXC hold time (TXPHASE_SEL=0, no clock delay added)	0.2			ns
	TXEN, TXD to TXC hold time (TXPHASE_SEL=1, clock delay added)	2.2			ns



f. Receive Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Rclk3}	Period of receive clock in giga mode	-	8	-	ns
T_{Rclk3}	Period of receive clock in 100M mode	-	40	-	ns
T_{Rclk3}	Period of receive clock in 10M mode	-	400	-	ns
T_{d3}	RXC edge to RXCTL, RXD (RXPHASE_SEL=0, no clock delay added)			0.4	ns
	RXC edge to RXCTL, RXD (RXPHASE_SEL=1, clock delay added)			2.4	ns



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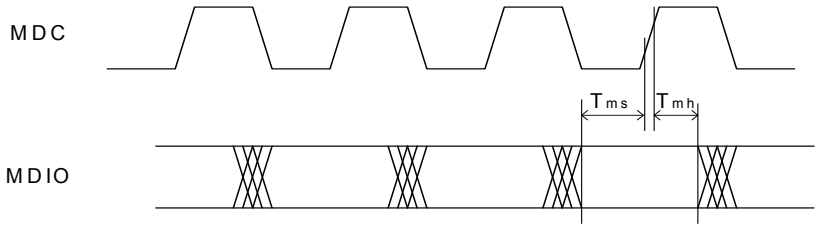
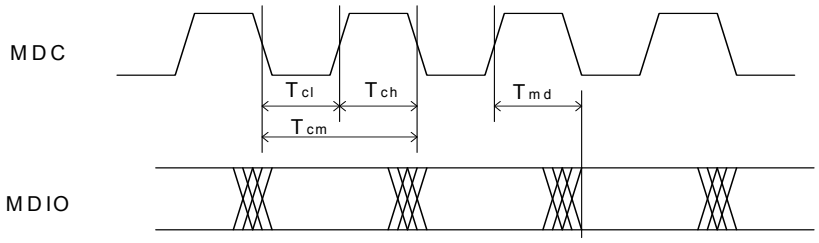
5.3.5 SMI Timing

a. MDC/MDIO Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDC0 High Time	40	-	-	ns
T_{cl}	MDC0 Low Time	40	-	-	ns
T_{cm}	MDC0 period	80	-	-	ns
T_{md}	MDIO0 output delay	-	-	5	ns
T_{mh}	MDIO0 setup time	10	-	-	ns
T_{ms}	MDIO0 hold time	10	-	-	ns



Write Cycle



Read Cycle

5.4 Thermal Data

Theta Ja	Theta Jc	Conditions	Units
24.5	11.1	4 Layer PCB; air flow@ 0m/sec	°C/ W
68.6	14.2	2 Layer PCB; air flow@ 0m/sec	°C/ W

6 Order Information

Part No.	Package	Notice
IP1001 LF	64-PIN QFN	Lead free

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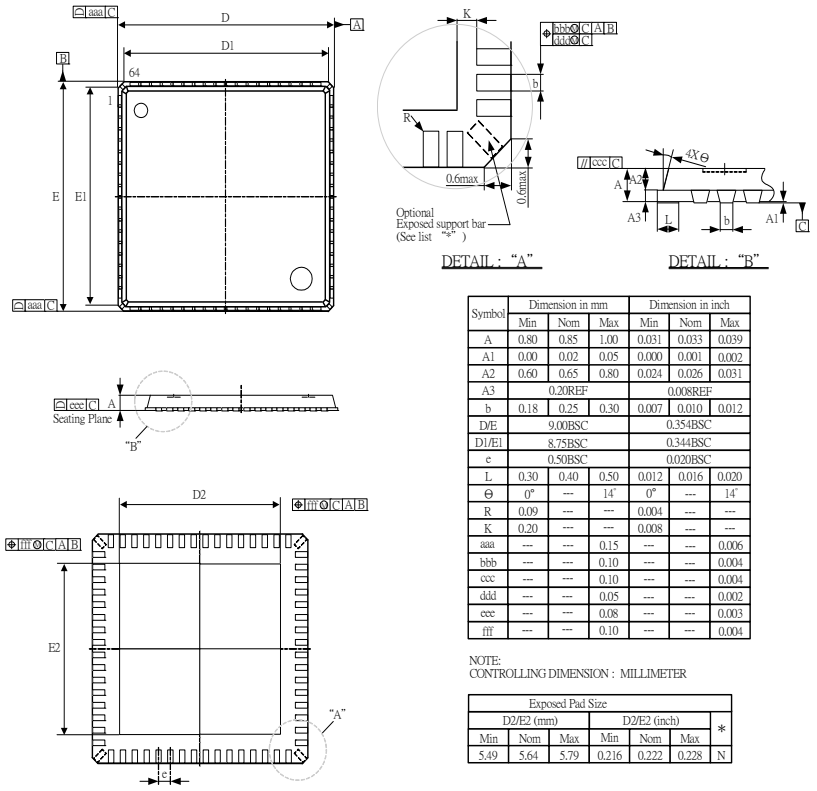
7 Package Detail

64 QFN Outline Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.80	0.024	0.026	0.031
A3	0.20REF			0.008REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	9.00BSC			0.354BSC		
D1/E1	8.75BSC			0.344BSC		
e	0.50BSC			0.020BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
Θ	0°	---	14°	0°	---	14°
R	0.09	---	---	0.004	---	---
K	0.20	---	---	0.008	---	---
aaa	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004

NOTE:
CONTROLLING DIMENSION : MILLIMETER

Exposed Pad Size						
D2/E2 (mm)			D2/E2 (inch)			*
Min	Nom	Max	Min	Nom	Max	
5.49	5.64	5.79	0.216	0.222	0.228	N

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