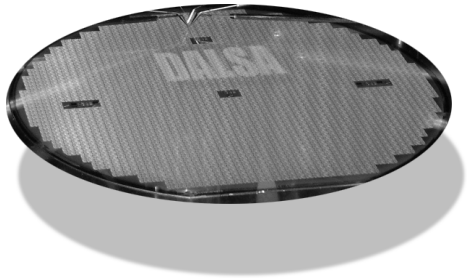
C08C 0.8µm 5V CMOS Process

DALSA Semiconductor's proven ability to transfer and develop customized processes is unmatched in the industry

C08C Overview

- 0.8µm 5V CMOS process, compatible with most 0.8µm CMOS processes in the industry.
- Twin-tub, P or N type epi or bulk substrates
- Single or double poly
- Two or three layer metal process



Features

- Propagation delay: Tpd = 200ps
- High value (10kΩ/sq.) and low TCR poly resistor options
- Fully transportable to C08E and C08G high voltage processes
- ProToDuction™ option for low-cost prototyping
- BSIM3v3.22 models available in Hspice and Spectre
- Comprehensive mixed signal Cadence Foundry Design Kit (FDK) available

Applications

- All 5V digital, analog or mixed signal circuits

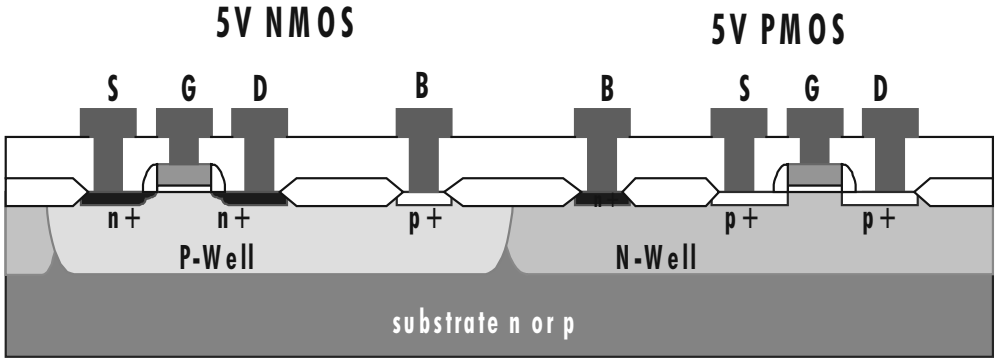
Layout Rules

Layer	Width (µm)	Space (µm)
Poly 1	0.8	0.9
Poly2	1.0	1.2
Contact	0.9x0.9	0.8
Metal 1	1.1	1.0
Via	1.0x1.0	1.0x1.0
Metal 2	1.2	1.1
Via 2	2.0x2.0	2.0
Metal 3	3.0	2.4

Mixed Signal Capabilities

- 5V double poly capacitor (1.05fF/µm²)
- High value poly resistor option (10kΩ/sq)
- 5V 0.8µm cmos
- Polysilicon fuses
- Digital gate count 1.8K gates/mm²

Simplified Cross-Section of 5V CMOS



DALSA SEMICONDUCTOR

26-Sep-02
03-70-00146-00
www.dalsasemi.com

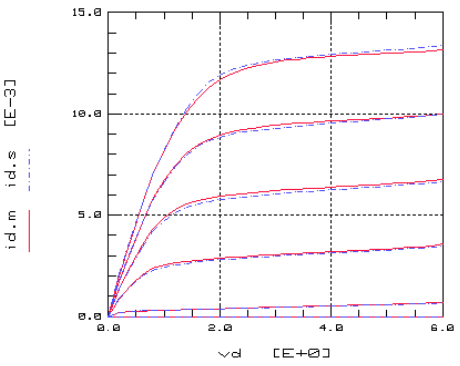
C08C 0.8µm 5V CMOS Process

Electrical Parameters of Representative Transistors

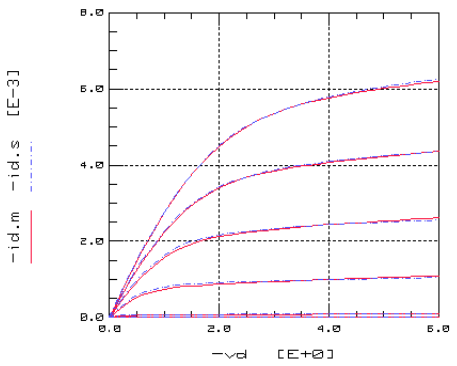
Parameter	5V NMOS	5V PMOS
W x L (µm)	50 x 0.8	50 x 0.8
VT (V)	0.65	-0.65
Ids (mA)	19	9
Bvdss (V)	12	12
Isub (µA/µm)	0.85	-
RON (Ω)	86	256

Resistor Type	Sheet Res Ω/sq
Poly 1	50 ± 25
Poly 2	37 ± 15
Low TCR	325 ± 100
HiRes	10K ± 3K

Example NMOS Output Curve (L=0.8µm, W=32µm)



Example PMOS Output Curve (L=0.8µm, W=32µm)



For More Information

DALSA Semiconductor

18 Blvd de l'aéroport
Bromont
Quebec Canada
J2L 1S7

Tel : +01 800 718 9701
Fax : +01 450 534 3201
e-mail: sales@dalsasemi.com
www.dalsasemi.com

26-Sep-02
03-70-00146-00
www.dalsasemi.com